DIGITAL ELECTRONICS VIVA AND INTERVIEW QUESTIONS

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Q-1 **What is DIGITAL GATE?**

Ans Digital gates are basically electronic components which are used for switching and manipulating binary data

Q-2 **What do u mean by universal gate?**

Ans The universal gates are those gate from which we can make any gate by using them. The universal gates are- NAND & NOR

Q-3 **What is truth table?**

Ans Truth table is a table from which we can get o/p of different gates

Q-4 **What is different between Ex-or & Ex-nor gate?**

Ans The basic difference between this two gate is that Ex-or gate gives o/p when both the i/p is different & Ex-nor gate give o/p when both i/p same.

Q-5 **What is D'morgans theorem**?

Ans D'morgans theorem is theorems through which we can easily manipulate and reduce the given equation.

Q-6 **Writes D'morgans theorem equations.**

Ans

1. (A+B)'=A'B'
2. A'B'= (A+B)'

Q-7 **Solve following example by using D'morgans theorem.**

Ans (ABC)'=A'+B'+C'

Q-8 **Solve following example by using D'morgans theorem. (A+B+C)'**

Ans (A+B+C)'=A'B'C'

Q-9 **Solve following example by using D'morgans theorem. (ABC)' (AB)'**

Ans (ABC)' (AB)'= (A'+B'+C') (A'+B')

Q-10 **Who invent the D'morgans theorem?**

Ans The law is named after Augustus De Morgan (1806–1871)

Q-11 **De Morgan theorem is used for what?**

Ans This theorem is useful for solving the different bullion expressions.

Q-12 **For what De Morgan theorem is used?**

Ans De Morgan theorem may be thought of in terms of breaking a long bar symbol.

Q-13 **What is use of half adder?**

Ans It is used for adding 2 bit data

Q-14 **In Half adder how many inputs are used?**

Ans Two

Q-15 **In o/p of Half adder what we gate?**

Ans SUM, CARRY

Q-16 **In Half adder SUM=?**

Ans SUM= A (+) B.

Q-17 **In half adder Carry=?**

Ans AB

Q-18 **How many AND gate required to make a Half adder?**

Ans 1 one

Q-19 **In Half adder how many types of gates are required?**

Ans Two types NAND & Ex-or

Q-20 **What is difference between the half and full adder?**
Ans In half adder only 2bits can be use but in full adder we can use 3 bit data.
Q-21 **What is difference between half adder and half subs tractor?**
Ans The only difference is in carry & borrows expression.
Q-22 **What is use of Full adder?**
Ans Full adder is used for adding three bit data.
Q-23 **In full adder how many inputs are used?**
Ans Three
Q-24 **In o/p of full adder what we gate?**
Ans SUM & Carry
Q-25 **In full adder SUM=?**
Ans SUM= A (+) B (+) C.
Q-26 **In full adder Carry=?**
Ans Carry=AB+BC+AC
Q-27 **How many half adders required to make a full adder?**
Ans 2 Half Adder
Q-28 **In full adder how many types of gates are required?**
Ans Three types 1. And, 2.Ex-or, 3.or
Q-29 **What is use of half Subs tractor?**
Ans It is used for subs tract 2 bit data.
Q-30 **In Half Subs tractor how many inputs are used?**
Ans Two
Q-31 **In o/p of Half Subs tractor what we gate?**
Ans Difference & Borrow
Q-32 **In Half Subs tractor Difference=?**
Ans Difference= A (+) B. Borrow=A'B'
Q-33 **How many AND gate required to make a Half Subs tractor?**
Ans One
Q-34 **In Half Subs tractor how many types of gates are required?**
Ans Two ANAD & Ex-or
Q-35 **What is difference between full & half substractor?**
Ans In half substractor we can subtract only 2 bit data but in full substractor we can subtract 3 bit data.
Q-36 **What is difference between half adder and half substractor?**
Ans The only difference is in carry & borrows expression.
Q-37 **If input of half substractor is 11 then output is?**
Ans Difference= 0, borrow=0.
Q-38 **What is use of Full Subs tractor?**
Ans Full substractor is used for differentiate three bit data.
Q-39 **In Full Subs tractor how many inputs are used?**
Ans Three
Q-40 **In output of Full Subs tractor what we gate?**

Ans Difference & borrow

Q-41 **In Full Subs tractor Difference=?**

Ans Difference= A (+) B (+) C. Borrow= A'B+A'C+BC?

Q-42 **How many NAND gate required to make a Full Subs tractor?**

Ans Nine

Q-43 **In Full Subs tractor how many Half Subs tractor are required?**

Ans Two

Q-44 **How many half substractor are required to construct a full adder?**

Ans Two half substractor are required to construct a full adder.

Q-45 **What is difference between full & half substractor?**

Ans In half substractor we can subtract only 2 bit data but in full substractor we can subtract 3 bit data.

Q-46 **What is magnitude comparator?**

Ans A digital comparator or magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number. Comparators are used in a central processing units (CPU) and microcontrollers. Examples of digital comparator include the CMOS 4063 and 4585 and the TTL 7485 and 74682-'89.The analog equivalent of digital comparator is the voltage comparator. Many microcontrollers have analog comparators on some of their inputs that can be read or trigger an interrupt.

Q-47 **What is most significant bit?**

Ans In computing, the most significant bit (msb, also called the high-order bit) is the bit position in a binary number having the greatest value. The msb is sometimes referred to as the left-most bit on big-endian architectures, due to the convention in positional notation of writing more significant digits further to the left.

Q-48 **Explain operation of AND gate?**

Ans The AND gate is a digital logic gate that implements logical conjunction - it behaves according to the truth table to the right. A HIGH output (1) results only if both the inputs to the AND gate are HIGH (1). If neither or only one input to the AND gate is HIGH, a LOW output results. In another sense, the function of AND effectively finds the minimum between two binary digits, just as the OR function finds the maximum.

Q-49 **What is equality?**

Ans The binary numbers A and B will be equal if all the pairs of significant digits of both numbers are equal, i.e., A3 = B3, A2 = B2, A1 = B1 and A0 = B0

Q-50 **What is inequality?**

Ans In order to manually determine the greater of two binary numbers, we inspect the relative magnitudes of pairs of significant digits, starting from the most significant bit, gradually proceeding towards lower significant bits until an inequality is found. When an inequality is found, if the corresponding bit of A is 1 and that of B is 0 then we conclude that A>B.

Q-51 **Explain magnitude comparator 7485 IC**

Ans The 74F85 is a 4-bit magnitude comparator that can be expanded t almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A0–A3) and (B0–B3) where A3 and B3 are the most significant bits.

Q-52 **What is 8-input Magnitude Comparator?**

Ans Magnitude Comparator. This Magnitude Comparator can be used perform comparisons of two 8-bit binary or BCD words. The output provides both a P equals Q function or P greater than Q function. A Magnitude Comparator would be considered standard logic or glue logic when a discrete IC is used. However, because of the internal complexity, a Magnitude Comparator would also be considered an MSI Function [Medium Scale Integration].

Q-53 **What is IC?**

Ans In electronics, an integrated circuit (also known as IC, chip, or microchip) is a miniaturized electronic circuit (consisting mainly of semiconductor devices, as well as passive components) that has been manufactured in the surface of a thin substrate of semiconductor material. Integrated circuits are used in almost all electronic equipment in use today and have revolutionized the world of electronics. Computers, cellular phones, and other digital appliances are now inextricable parts of the structure of modern societies, made possible by the low cost of production of integrated circuits.

Q-54 **Tell about advancement in integrated circuits?**

Ans Among the most advanced integrated circuits are the microprocessors or 'cores', which control everything from computers and cellular phones to digital microwave ovens. Digital memory chips and ASICs are examples of other families of integrated circuits that are important to the modern information society. While the cost of designing and developing a complex integrated circuit is quite high, when spread across typically millions of production units the individual IC cost is minimized. The performance of ICs is high because the small size allows short traces which in turn allows low power logic (such as CMOS) to be used at fast switching speeds.

Q-55 **What is flip-flop?**

Ans Flip-flop is a 1 bit storing element.

Q-56 **How many types of flip-flop are used?**

Ans 4 types of flip –flop, S-R, J-K, D, T

Q-57 **What is disadvantage of SR flip-flop?**

Ans When both the input is one then it gives invalid output.

Q-58 **What is disadvantage of JK flip-flop?**

Ans Race around condition.

Q-59 **To remove race around condition what we use?**

Ans Master slave Flip-flop.

Q-60 **What is race around condition?**

Ans When pulse width is more than signal width then for signal change of pulse width many no of times signal changes its state that is called race around condition.

Q-61 **What are the characteristic equation for T flip-flop?**

Ans $Q = TQ' + QT'$

Q-62 **Which Gates are used in SR flip flops to a JK flip-flop?**

Ans NAND Gates

Q-63 **D flip-flop is used for?**

Ans Providing delay.

Q-64 **What is full form of T flip-flop?**

Ans Toggle flip-flop

Q-65 **What is counter?**

Ans In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal.

Q-66 **Give types of counter?**

Ans There are two types of counters (1) Up counters, which increase (increment) in value (2) Down counters, which decrease (decrement) in value.

Q-67 **What are the implements of counter?**

Ans In electronics, counters can be implemented quite easily using register-type circuits such as the flip-flop, and a wide variety of designs exist, e.g.:

1. Asynchronous (ripple) counter – changing state bits are used as clocks to subsequent state flip-flops
2. Synchronous counter – all state bits change under control of a single clock
3. Decade counter – counts through ten states per stage
4. Up–down counter – counts both up and down, under command of a control input
5. Ring counter – formed by a shift register with feedback connection in a ring
6. Johnson counter – a twisted ring counter
7. Cascaded counter

Q-68 **Explain Asynchronous (ripple) counter?**

Ans An asynchronous (ripple) counter is a single K-type flip-flop, with its J (data) input fed from its own inverted output. This circuit can store one bit, and hence can count from zero to one before it overflows (starts over from 0). This counter will increment once for every clock cycle and takes two clock cycles to overflow, so every cycle it will alternate between a transition from 0 to 1 and a transition from 1 to 0. Notice that this creates a new clock with a 50percent duty cycle at exactly half the frequency of the input clock. If this output is then used as the clock signal for a similarly arranged D flip-flop (remembering to invert the output to the input), you will get another 1 bit counter that counts half as fast. Putting them together yields a two bit counter.

Q-69 **Explain Johnson counter?**

Ans A Johnson counter (or switch tail ring counter, twisted-ring counter, walking-ring counter, or Moebius counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage.[2][3][4] A pattern of bits equal in length to twice the length of the shift register thus circulates indefinitely. These counters find specialist applications, including those similar to the decade counter, digital to analog conversion, etc. it can be established by D flip flop and JK flip flop.

Q-70 **Explain Decade counter?**

Ans A decade counter is one that counts in decimal digits, rather than binary. A decade counter may have each digit binary encoded (that is, it may count in binary-coded decimal, as the 7490 integrated circuit did) or other binary encodings (such as the binary encoding of the 7490 integrated circuit). Alternatively, it may have a fully decoded or one-hot output code in which each output goes high in turn; the 4017 is such a circuit. The latter type of circuit finds applications in multiplexers and demultiplexer, or wherever a scanning type of behaviour is useful. Similar counters with different numbers of outputs are also common.

Q-71 **What is synchronous counters?**

Ans In synchronous counters, the clock inputs of all the flip-flops are connected together and are triggered by the input pulses. Thus, all the flip-flops change state simultaneously (in parallel). The circuit below is a 3-bit synchronous counter. The J and K inputs of FF0 are connected to HIGH. FF1 has its J and K inputs connected to the output of FF0, and

the J and K inputs of FF2 are connected to the output of an AND gate that is fed by the outputs of FF0 and FF1.

Q-72 Give types of ring counters?

Ans There are two types of ring counters:

1. A straight ring counter or Over beck counter connects the output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring. For example, in a 4-register one-hot counter, with initial register values of 1000, the repeating pattern is: 1000, 0100, 0010, 0001, 1000.... Note that one of the registers must be pre-loaded with a 1 (or 0) in order to operate properly.
2. A twisted ring counter (also called Johnson counter or Moebius counter) connects the complement of the output of the last shift register to its input and circulates a stream of ones followed by zeros around the ring. For example, in a 4-register counter, with initial register values of 0000, the repeating pattern is: 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, and 0000.

Q-73 What is one hot counter?

Ans In digital circuits, one-hot refers to a group of bits among which the legal combinations of values are only those with a single high (1) bit and all the others low (0). For example, the output of a decoder is usually a one-hot code, and sometimes the state of a state machine is represented by a one-hot code. A similar implementation in which all bits are (1) except one (0) is sometimes called one-cold

Q-74 What is counter?

Ans A counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal.

Q-75 What is the types of counter?

Ans In practice, there are two types of counters:

1. Up counters, which increase (increment) in value
2. Down counters, which decrease (decrement) in value

Q-76 What is the basic type of counter made by flip-flop or resistor?

Ans

1. Asynchronous (ripple) counter – changing state bits are used as clocks to subsequent state flip-flops
2. Synchronous counter – all state bits change under control of a single clock
3. Decade counter – counts through ten states per stage
4. Up–down counter – counts both up and down, under command of a control input
5. Ring counter – formed by a shift register with feedback connection in a ring
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Q-77 What is asynchronous counter?

Ans An asynchronous (ripple) counter is a single K-type flip-flop, with its J (data) input fed from its own inverted output. This circuit can store one bit, and hence can count from zero to one before it overflows (starts over from 0). This counter will increment once for every clock cycle and takes two clock cycles to overflow, so every cycle it will alternate between a transition from 0 to 1 and a transition from 1 to 0. Notice that this creates a new clock with a 50percent duty cycle at exactly half the frequency of the input clock. If this output is then used as the clock signal for a similarly arranged D flip-flop (remembering to invert the output to the input), you will get another 1 bit counter that counts half as fast

Q-78 What is Synchronous counter?

Ans A simple way of implementing the logic for each bit of an ascending counter (which is what is depicted in the image to the right) is for each bit to toggle when all of the less significant bits are at a logic high state. For example, bit 1 toggles when bit 0 is logic high; bit 2 toggles when both bit 1 and bit 0 are logic high; bit 3 toggles when bit 2, bit 1 and bit 0 are all high; and so on. Synchronous counters can also be implemented with hardware finite state machines, which are more complex but allow for smoother, more stable transitions.

Q-79 **What is the ring counter?**

Ans A ring counter is a shift register (a cascade connection of flip-flops) with the output of the last one connected to the input of the first, that is, in a ring. Typically a pattern consisting of a single 1 bit is circulated, so the state repeats every N clock cycles if N flip-flops are used. It can be used as a cycle counter of N states.

Q-80 **What is the Johnson counter?**

Ans A Johnson counter (or switch tail ring counter, twisted-ring counter, walking-ring counter, or Moebius counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage. A pattern of bits equal in length to twice the length of the shift register thus circulates indefinitely. These counters find specialist applications, including those similar to the decade counter, digital to analog conversion, etc. it can be established by D flip flop and JK flip flop

Q-81 **What is the decade counter?**

Ans A decade counter is one that counts in decimal digits, rather than binary. A decade counter may have each digit binary encoded (that is, it may count in binary-coded decimal, as the 7490 integrated circuit did) or other binary encodings (such as the bi-unary encoding of the 7490 integrated circuit). Alternatively, it may have a fully decoded or one-hot output code in which each output goes high in turn; the 4017 is such a circuit. The latter type of circuit finds applications in multiplexers and demultiplexers, or wherever a scanning type of behaviour is useful. Similar counters with different numbers of outputs are also common. The decade counter is also known as a mod-counter.

Q-82 **What do you mean by up down counter?**

Ans A counter that can change state in either direction, under the control of an up–down selector input, is known as an up–down counter. When the selector is in the up state, the counter increments its value; when the selector is in the down state, the counter decrements the count Machine cycle- the time taken by data/ opcode / operand from memory/ peripheral devices to acknowledge the external hardware. it takes 1to 6 T-state.

Q-83 **What is decade counter?**

Ans A decade counter is a binary counter that is designed to count to 10(decimal), or 1010(binary). An ordinary four stage counter can be easily modified to a decade counter by adding a NAND gate as shown in figure 325. Notice that FF2 and FF4 provide the inputs to the NAND gate. The NAND gate outputs are connected to the CLR input of each of the FFs.

Q-84 **How many stages are required for a decade counter?**

Ans Four

Q-85 **Which AND gate causes FF3 to reset?**

Ans Three.

Q-86 **What causes the specified condition to shift position?**

Ans The input or clock pulse.

Q-87 **If the specified state is OFF, how many FFs may be off at one time?**

Ans One

Q-88 **What is the shift resistor?**

Ans Shift resistor is a device which is used for storing and processing the bit in series or parallel.

Q-89 **Types of shift resistor?**

Ans Serial-in/serial-out shift register (FIFO or LIFO)
Serial-in/parallel-out shift register
Parallel-in/parallel-out shift register
Parallel-in/serial-out shift register

Q-90 **In SISO resistor how many input cycles are required?**

Ans It required n+1 clock pulse for input & n clock pulse for output.

Q-91 **In PISO resistor how many input cycles are required?**

Ans It required 1 clock pulse for input & n clock pulse for output

Q-92 **In PIPO resistor how many input cycles are required?**

Ans It required 1 clock pulse for input & 0 clock pulse for output

Q-93 **In SIPO resistor how many input cycles are required?**

Ans It required n+1 clock pulse for input & 0 clock pulse for output

Q-94 **What do you mean by clock enable?**

Ans When the Clock Enable input is High, the enabled load and shift actions take place on the next active Clock transition. When Clock Enable is Low, the register contents are unaffected by the Clock. Connections: Clock Enable is optional. Use this input when you need to disable the clock temporarily. If you do not use the Clock Enable input, the Clock is always enabled.

Q-95 **What is the clock?**

Ans Clock is a trigger. By Appling the clock the information proceeds.

Q-96 **What is the Universal gates?**

Ans The universal gates are the gate by help of which we can make other all gates.

Q-97 **Types of universal gate?**

Ans There are two universal gates:-

1. NAND
2. NOR

Q-98 **What is Setup Time?**

Ans Minimum time Period during which data must be stable before the clock makes a valid transition. E.g. for a positive edge triggered flip-flop having a setup time of 2ns so input data should be Stable for 2ns before the clock makes a valid transaction from zero to one

Q-99 **What is Hold Time?**

Ans Minimum time period during which data must be stable after the clock has made a valid transition. E.g. for a posedge triggered flip-flop, with a hold time of 1 ns. Input Data (i.e. R and S in the case of RS flip-flop) should be stable for at least 1 ns after clock has made transition from 0 to 1

Hold time is the amount of time after the clock edge that same input signal has to be held before changing it to make sure it is sensed properly at the clock edge. Whenever there are setup and hold time violations in any flip-flop, it enters a state where its output is unpredictable: this state is known as metastable state (quasi stable state); at the end of

metastable state, the flip-flop settles down to either (1) or (0). This whole process is known as metastability

Q-100 What is difference between latch and flip-flop?

Ans The main difference between latch and FF is that latches are level sensitive while FF is edge sensitive. They both require the use of clock signal and are used in sequential logic. For a latch, the output tracks the input when the clock signal is high, so as long as the clock is logic 1, the output can change if the input also changes. FF on the other hand, will store the input only when there is a rising/falling edge of the clock. Latch is sensitive to glitches on enable pin, whereas flip-flop is immune to glitches. Latches take fewer gates (also less power) to implement than flip-flops. Latches are faster than flip-flops

Q-101 Given only two XOR gates one must function as buffer and another as inverter?

Ans Tie one of XOR gates input to 1 it will act as inverter.
Tie one of XOR gates input to 0 it will act as buffer.

Q-102 Difference between Mealy and Moore state machine?

Ans

1. Mealy and Moore models are the basic models of state machines. A state machine which uses only Entry Actions, so that its output depends on the state, is called a Moore model. A state machine which uses only Input Actions, so that the output depends on the state and also on inputs, is called a Mealy model. The models selected will influence a design but there are no general indications as to which model is better. Choice of a model depends on the application, execution means (for instance, hardware systems are usually best realized as Moore models) and personal preferences of a designer or programmer
2. Mealy machine has outputs that depend on the state and input (thus, the FSM has the output written on edges) Moore machine has outputs that depend on state only (thus, the FSM has the output written in the state itself.

Q-103 What are the Advantage and Disadvantage of Mealy and Moore state machine?

Ans Advantage and Disadvantage

In Mealy as the output variable is a function both input and state, changes of state of the state variables will be delayed with respect to changes of signal level in the input variables, there are possibilities of glitches appearing in the output variables. Moore overcomes glitches as output dependent on only states and not the input signal level. All of the concepts can be applied to Moore-model state machines because any Moore state machine can be implemented as a Mealy state machine, although the converse is not true.

Moore machine: the outputs are properties of states themselves, which means that you get the output after the machine reaches a particular state, or to get some output your machine has to be taken to a state which provides you the output. The outputs are held until you go to some other state Mealy machine: Mealy machines give you outputs instantly, that is immediately upon receiving input, but the output is not held after that clock cycle.

Q-104 Difference between one hot and binary encoding?

Ans Common classifications used to describe the state encoding of an FSM are Binary (or highly encoded) and One hot. A binary-encoded FSM design only requires as many flip-flops as are needed to uniquely encode the number of states in the state machine. The actual number of flip-flops required is equal to the ceiling of the log-base-2 of the number of states in the FSM.A one hot FSM design requires a flip-flop for each state in the design and only one flip-flop (the flip-flop representing the current or hot state) is set at a time in a one hot FSM design. For a state machine with 9- 16 states, a binary

FSM only requires 4 flip-flops while a one hot FSM requires a flip-flop for each state in the design FPGA vendors frequently recommend using a one hot state encoding style because flip-flops are plentiful in an FPGA and the combinational logic required to implement a one hot FSM design is typically smaller than most binary encoding styles. Since FPGA performance is typically related to the combinational logic size of the FPGA design, one hot FSMs typically run faster than a binary encoded FSM with larger combinational logic blocks

Q-105 How to achieve 180 degree exact phase shift?

Ans Never tell using inverter

1. DCM an inbuilt resource in most of FPGA can be configured to get 180 degree phase shift.
2. b) BUFGDS that is differential signalling buffers which are also inbuilt resource of most of FPGA can be used.

Q-106 What is significance of RAS and CAS in SDRAM?

Ans SDRAM receives its address command in two address words. It uses a multiplex scheme to save input pins. The first address word is latched into the DRAM chip with the row address strobe (RAS). Following the RAS command is the column address strobe (CAS) for latching the second address word. Shortly after the RAS and CAS strobes, the stored data is valid for reading.

Q-107 Tell some of applications of buffer?

Ans

1. They are used to introduce small delays.
2. They are used to eliminate cross talk caused due to inter electrode capacitance due to close routing.
3. They are used to support high fan-out.

Q-108 Give two ways of converting a two input NAND gate to an inverter?

Ans

1. Short the 2 inputs of the NAND gate and apply the single input to it.
2. Connect the output to one of the input and the other to the input signal.

Q-109 Why is most interrupts active low?

Ans This answers why most signals are active low if you consider the transistor level of a module, active low means the capacitor in the output terminal gets charged or discharged based on low to high and high to low transition respectively. When it goes from high to low it depends on the pull down resistor that pulls it down and it is relatively easy for the output capacitance to discharge rather than charging. Hence people prefer using active low signals.

Q-110 Differences between D-Latch and D flip-flop?

Ans D-latch is level sensitive whereas flip-flop is edge sensitive. Flip-flops are made up of latches.

Q-111 What is a multiplexer?

Ans It is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. (2^n =>n). Where n is selection line.

Q-112 What is difference between RAM and FIFO?

Ans FIFO does not have address lines Ram is used for storage purpose whereas FIFO is used for synchronization purpose i.e. when two peripherals are working in different clock domains then we will go for FIFO.

Q-113 What are multi-cycle paths?

Ans Multi-cycle paths are paths between registers that take more than one clock cycle to become stable.

Q-114 **What is false path?**

Ans By timing all the paths in the circuit the timing analyser can determine all the critical paths in the circuit. However, the circuit may have false paths, which are the paths in the circuit which are never exercised during normal circuit operation for any set of inputs.

Q-115 **Difference between Synchronous and Asynchronous reset?**

Ans Synchronous reset logic will synthesize to smaller flip-flops, particularly if the reset is gated with the logic generating the dinput. But in such a case, the combinational logic gate count grows, so the overall gate count savings may not be that significant. The clock works as a filter for small reset glitches; however, if these glitches occur near the active clock edge, the Flip-flop could go metastable. In some designs, the reset must be generated by a set of internal conditions. A synchronous reset is recommended for these types of designs because it will filter the logic equation glitches between clocks.

Disadvantages of synchronous reset:

Problem with synchronous resets is that the synthesis tool cannot easily distinguish the reset signal from any other data signal. Synchronous resets may need a pulse stretcher to guarantee a reset pulse width wide enough to ensure reset is present during an active edge of the clock. if you have a gated clock to save power, the clock may be disabled coincident with the assertion of reset. Only an asynchronous reset will work in this situation, as the reset might be removed prior to the resumption of the clock. Designs that are pushing the limit for data path timing, cannot afford to have added gates and additional net delays in the data path due to logic inserted to handle synchronous resets.

Asynchronous reset:

The biggest problem with asynchronous resets is the reset release, also called reset removal. Using an asynchronous reset, the designer is guaranteed not to have the reset added to the data path. Another advantage favouring asynchronous resets is that the circuit can be reset with or without a clock present.

Disadvantages of asynchronous reset: ensure that the release of the reset can occur within one clock period. If the release of the reset occurred on or near a clock edge such that the flip-flops went metastable.

Q-116 **What is slack?**

Ans Slack is the amount of time you have that is measured from when an event actually happens and when it must happen. The term actually happens can also be taken as being a predicted time for when the event will actually happen. When something must happen can also be called a deadline so another definition of slack would be the time from when something actually happens (call this Tact) until the deadline (call this Tdead).

Slack = Tdead - Tact.

Negative slack implies that the actually happen time is later than the deadline time. .in other words it's too late and a timing violation. .you have a timing problem that needs some attention.

Q-117 **Difference between heap and stack?**

Ans The Stack is more or less responsible for keeping track of execution in our code (or what's been 'called'). The Heap is more or less responsible for keeping track of our objects. Think of the Stack as a series of boxes stacked one on top of the next. We keep track of what's going on in our application by stacking another box on top every time we call a method (called a Frame). We can only use what's in the top box on the stack. When we're done with the top box (the method is done executing) we throw it away and proceed to use the stuff in the previous box on the top of the stack. The Heap is similar

except that its purpose is to hold information (not keep track of execution most of the time) so anything in our Heap can be accessed at any time. With the Heap, there are no constraints as to what can be accessed like in the stack. The Heap is like the heap of clean laundry on our bed that we have not taken the time to put away yet - we can grab what we need quickly. The Stack is like the stack of shoe boxes in the closet where we have to take off the top one to get to the one underneath it.

Q-118 **What is Difference between write back and write through cache?**

Ans A caching method in which modifications to data in the cache aren't copied to the cache source until absolutely necessary. Write-back caching is available on many microprocessors, including all Intel processors since the 80486. With these microprocessors, data modifications to data stored in the L1 cache aren't copied to main memory until absolutely necessary. In contrast, a write-through cache performs all write operations in parallel data is written to main memory and the L1 cache simultaneously. Write-back caching yields somewhat better performance than write-through caching because it reduces the number of write operations to main memory. With this performance improvement comes a slight risk that data may be lost if the system crashes. A write-back cache is also called a copy-back cache.

Q-119 **What is skew, what are problems associated with it and how to minimize it?**

Ans In circuit design, clock skew is a phenomenon in synchronous circuits in which the clock signal (sent from the clock circuit) arrives at different components at different times. This is typically due to two causes. The first is a material flaw, which causes a signal to travel faster or slower than expected. The second is distance: if the signal has to travel the entire length of a circuit, it will likely (depending on the circuit's size) arrive at different parts of the circuit at different times. Clock skew can cause harm in two ways. Suppose that a logic path travels through combinational logic from a source flip-flop to a destination flip-flop. If the destination flip-flop receives the clock tick later than the source flip-flop, and if the logic path delay is short enough, then the data signal might arrive at the destination flip-flop before the clock tick, destroying there the previous data that should have been clocked through. This is called a hold violation because the previous data is not held long enough at the destination flip-flop to be properly clocked through. If the destination flip-flop receives the clock tick earlier than the source flip-flop, then the data signal has that much less time to reach the destination flip-flop before the next clock tick. If it fails to do so, a setup violation occurs, so-called because the new data was not set up and stable before the next clock tick arrived. A hold violation is more serious than a setup violation because it cannot be fixed by increasing the clock period. Clock skew, if done right, can also benefit a circuit. It can be intentionally introduced to decrease the clock period at which the circuit will operate correctly, and/or to increase the setup or hold safety margins. The optimal set of clock delays is determined by a linear program, in which a setup and a hold constraint appear for each logic path. In this linear program, zero clocks skew is merely a feasible point. Clock skew can be minimized by proper routing of clock signal (clock distribution tree) or putting variable delay buffer so that all clock inputs arrive at the same time

Q-120 **Difference between Synchronous, Asynchronous & I synchronous communication?**

Ans Sending data encoded into your signal requires that the sender and receiver are both using the same encoding/decoding method, and know where to look in the signal to find data. Asynchronous systems do not send separate information to indicate the encoding or clocking information. The receiver must decide the clocking of the signal on its own. This means that the receiver must decide where to look in the signal stream to find ones and zeroes, and decide for itself where each individual bit stops and starts. This

information is not in the data in the signal sent from transmitting unit. Synchronous systems negotiate the connection at the data-link level before communication begins. Basic synchronous systems will synchronize two clocks before transmission, and reset their numeric counters for errors etc. More advanced systems may negotiate things like error correction and compression. Time-dependent. It refers to processes where data must be delivered within certain time constraints. For example, Multimedia stream require an isochronous transport mechanism to ensure that data is delivered as fast as it is displayed and to ensure that the audio is synchronized with the video.

Q-121 **What is glitch?**

Ans The flip-flop is clocked at every clock cycle and the data path is controlled by an enable. When the enable is Low, the multiplexer feeds the output of the register back on itself. When the enable is High, new data is fed to the flip-flop and the register changes its state