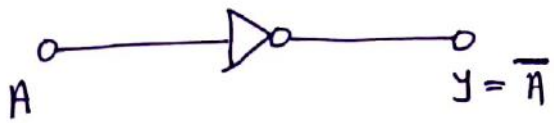
NOT Gate 54

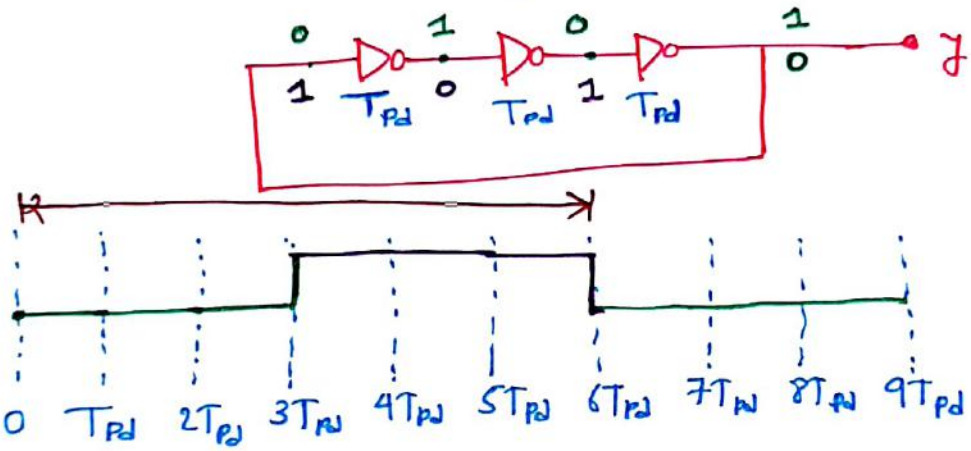


- o/p will be Invert of Input.

X	Y
0	1
1	0

- Applications of NOT gate.

1) Not gate as ring Oscillator.

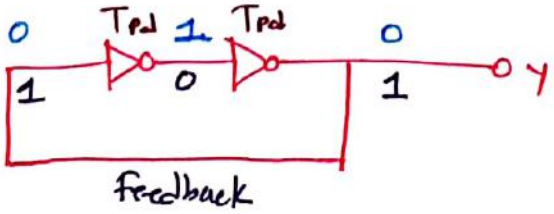


- Connect odd numbers of NOT gates.
- There Propagation delay T_{Pd} of each NOT gate.

- $T = 6T_{Pd} = 2nT_{Pd}$
- $f = 1/T = 1/2nT_{Pd}$

2) Not gate as a Buffer

3) Not gate as Bistable Multivibrator



- Connect even numbers of NOT gates.
- There is propagation delay of T_{Pd} for each NOT gate.

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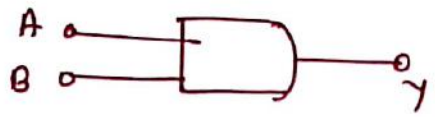
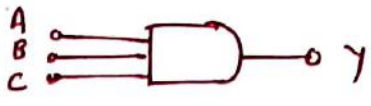
AND Gate 55



$Y = A.B$

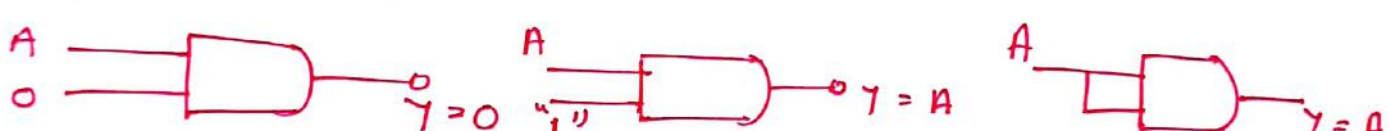


$Y = A.B.C$

- If all Ip's are "1" then only O/p is "1", else O/p is "0".

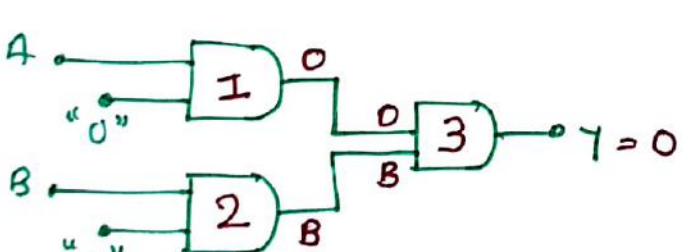
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

- Properties of AND



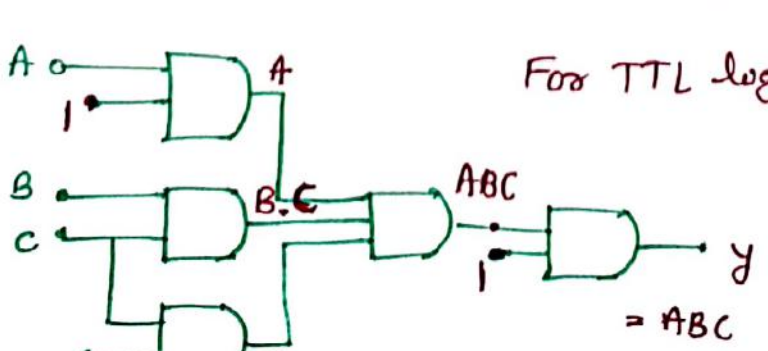
- Examples

1]



2]

3]



For TTL logic find y.

For TTL, Not connected terminals at Ip has active high "1" Input.

OR Gate 56

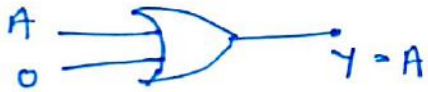
$Y = A + B$

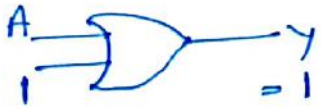
$Y = A + B + C$

- In OR gate, If any Input is "1" then O/p is "1". else O/p is "0".

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

- Properties of OR gate.

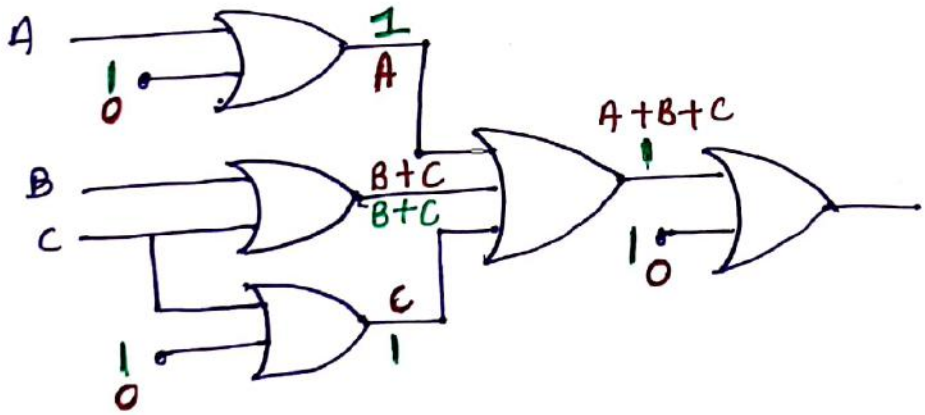




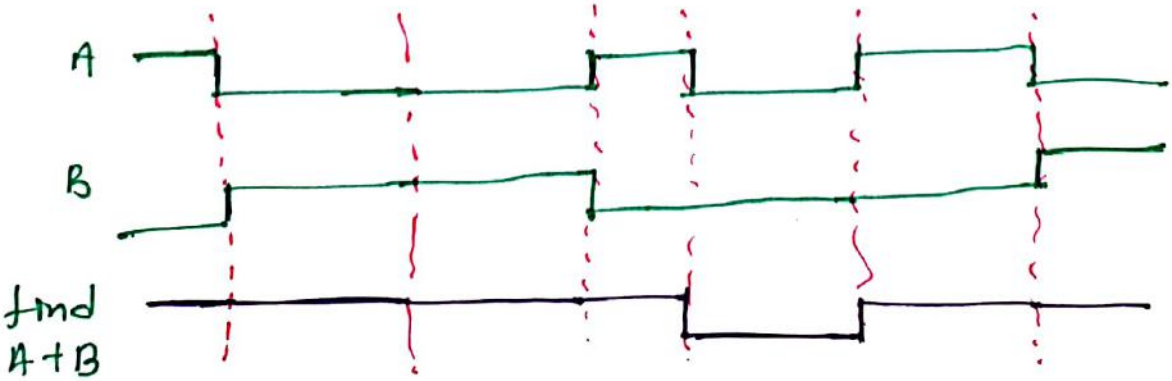
- Examples

Find output For TTL & ECL logic.

For TTL, NC = "1"
For ECL, NC = "0"



Y = 1 (TTL logic)
= A+B+C (ECL logic)



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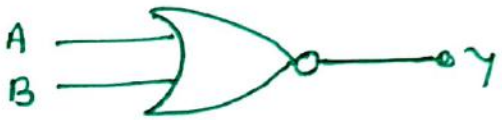
NAND and NOR gate. 57

$Y = \overline{A.B}$



$Y = \overline{A+B}$

- NAND and NOR gate are universal gates.
- In NAND gate, If any Input is "0" then o/p will be "1", else o/p will be "0".

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

- In NOR gate, If any Input is "1" then o/p will be "0", else o/p will be "1".

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

XOR and XNOR gate.

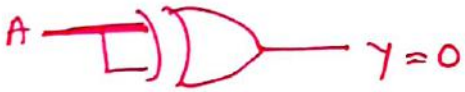
$Y = A \oplus B$

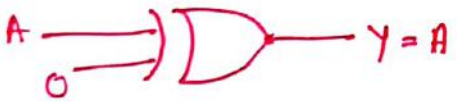
$= A\bar{B} + \bar{A}B$

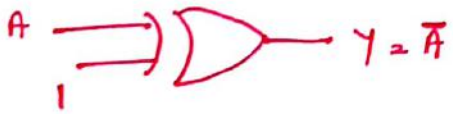
- If no of "1" at Input is odd then Output is "1", else Output is "0".

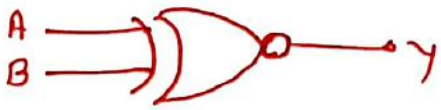
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

- Properties of XOR









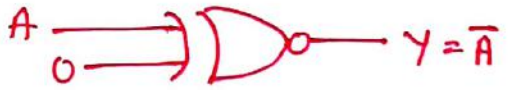
$Y = A \odot B$

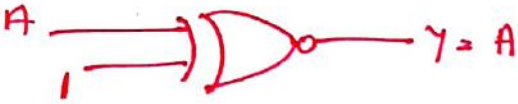
$= AB + \bar{A}\bar{B}$

- If no of "1" at Input is even, then output is "1", else output is "0".

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

- Properties of XNOR.





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Examples based on XOR and XNOR gates.

1) 

what is the equivalent gate of given Circuit ?

$Y = A \oplus \overline{B}$

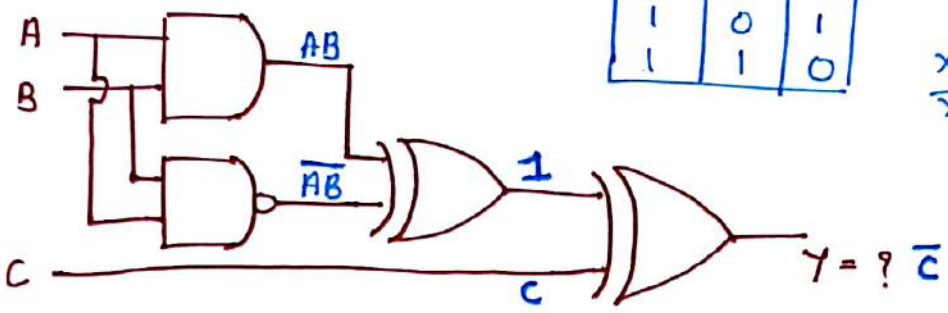
$= A\overline{B} + \overline{A}\overline{B}$

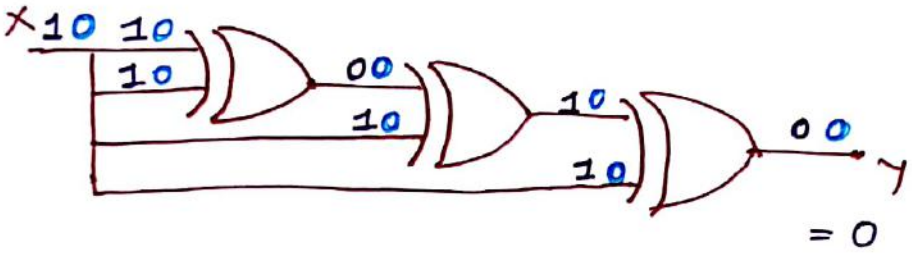
$\boxed{Y = A\overline{B} + \overline{A}\overline{B}} = A \odot B$

→ For $A \oplus B$

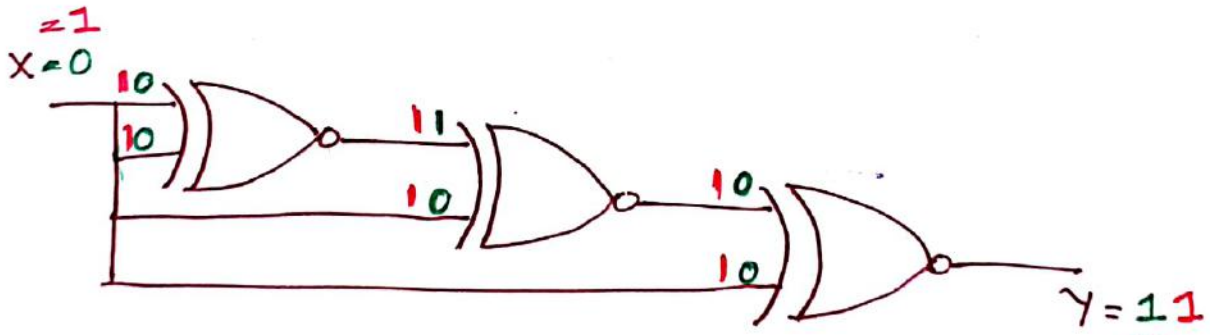
$= A\overline{B} + \overline{A}B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

2) 

3) 

X	Y
0	0
1	0



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

X	Y
0	1
1	1

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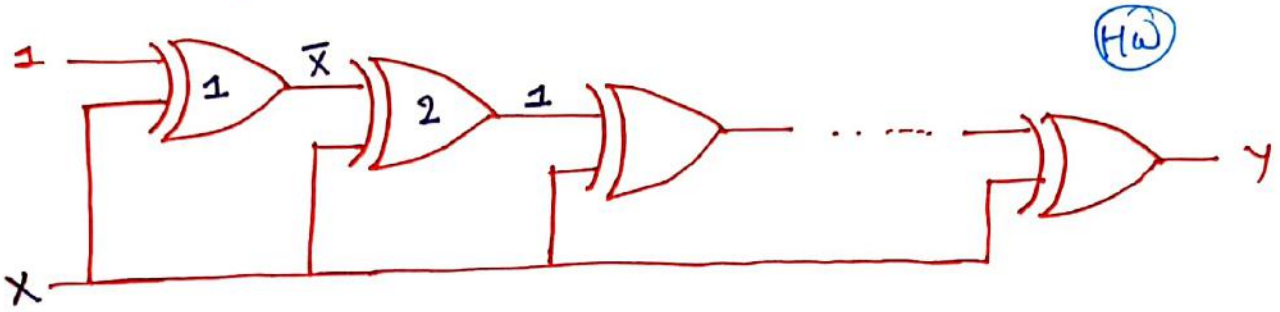
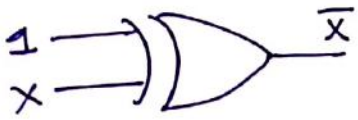
Examples on XOR and XNOR gate

1] If the Input to digital Circuit Consisting of Cascade of 20 XOR gates given. Then the output Y is



(HW)

a] 0 **b] 1** c] $\bar{x}$ d] X



X	Y	P
0	0	0
0	1	1
1	0	1
1	1	0

Output of gate [1, 3, 5, ..., 19]
$= \bar{X}$
Output of gate [2, 4, 6, ..., 20]
$= 1$

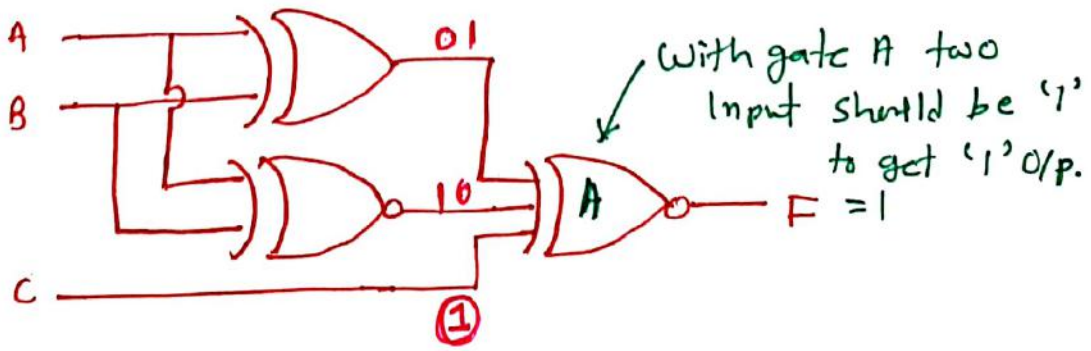
2] For the Output F to be 1 in the logic Circuit shown, The Input Combination may be

a] A = 1, B = 1, C = 0

b] A = 1, B = 0, C = 0

c] A = 0, B = 1, C = 0

d] A = 0, B = 0, **C = 1**



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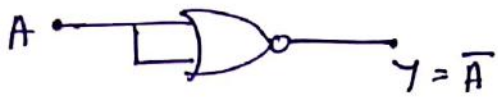
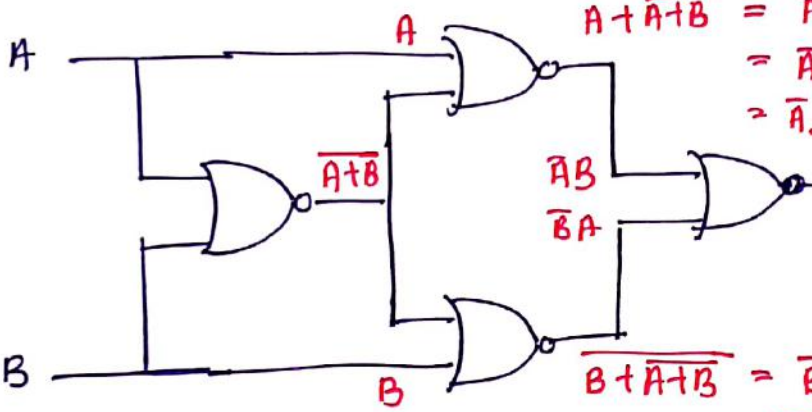
NOR gate as universal gate 61

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

- NOT gate by NOR gate.



- XOR gate by NOR gate.



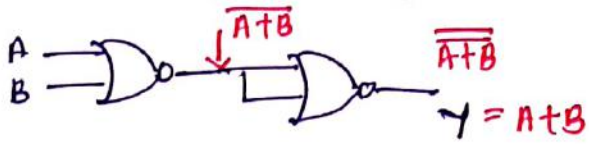
$\overline{A+\overline{A+B}} = \overline{A}.(\overline{\overline{A+B}})$
$= \overline{A}.(A+B)$
$= \overline{A}.A + \overline{A}B = \overline{A}B$

$\overline{B+\overline{A+B}} = \overline{B}.(\overline{\overline{A+B}})$
$= \overline{B}.(A+B)$
$= \overline{B}A + B\overline{B}$
$= \overline{B}A$

$Y = \overline{\overline{A}B + \overline{B}A}$

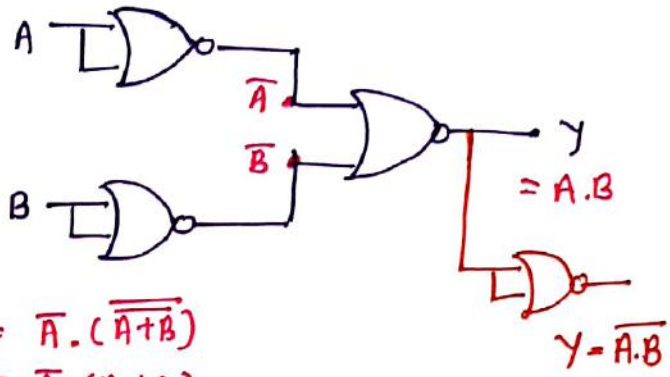
$Y' = \overline{A}B + \overline{B}A$

- OR gate by NOR gate.



- NOR gate as AND gate.

$Y = \overline{\overline{A}+\overline{B}} = \overline{\overline{A}}.\overline{\overline{B}} = A.B$



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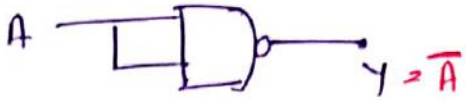
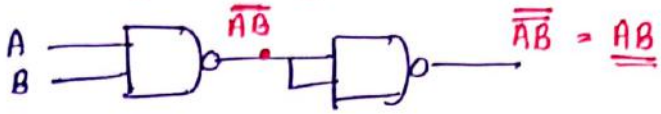
NAND gate as universal gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

- NOT gate by NAND gate.

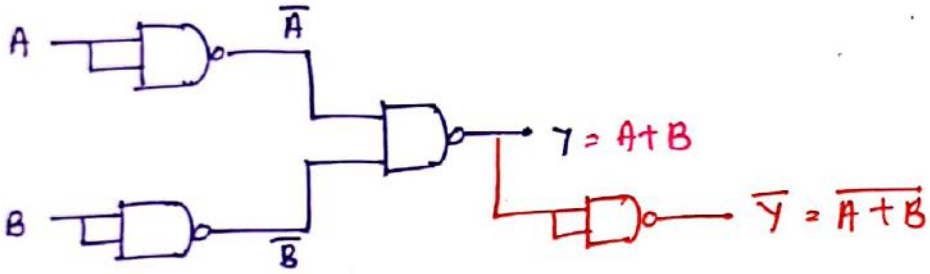


- AND gate by NAND gate.

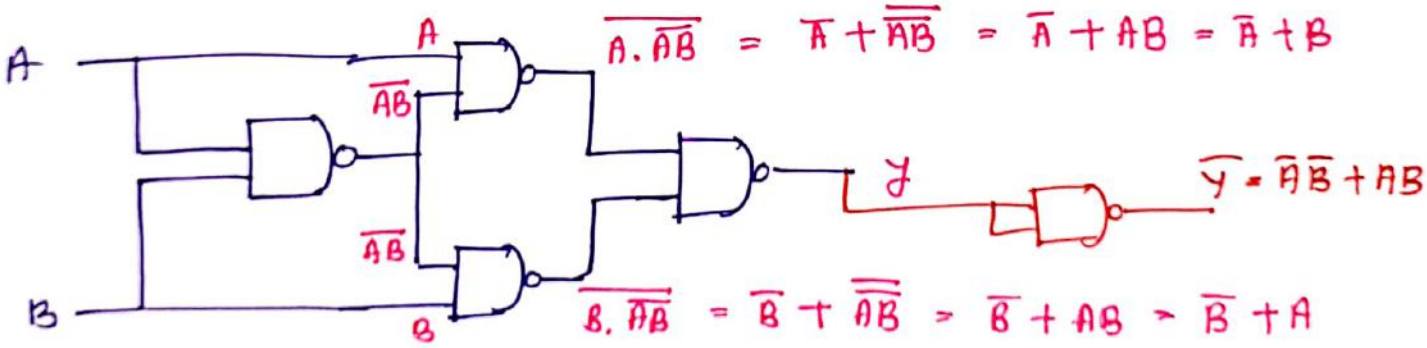


- OR gate by NAND.

$Y = \overline{\overline{A}.\overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$



- XOR gate by NAND gate.



$$J = \overline{(\overline{A}+B).(\overline{B}+A)} = \overline{(\overline{A}\overline{B} + \overline{A}A + B\overline{B} + BA)} = \overline{\overline{A}\overline{B} + AB}$$

($\overline{A}A$ and $B\overline{B}$ are both 0)

$$= A\overline{B} + \overline{A}B$$

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Minimum two Input NAND gates for Multi Input AND and Multi Input NAND gate. 63

- $2(n-1)$ [two I/p NAND to Implement n Input AND]
- $2n-3$ [two I/p NAND to Implement n Input NAND]

1] How many two Input NAND req.ed to Implement 4 I/p AND gate.

$= 2(n-1)$
$= 2(4-1)$
$= 6$ (NAND gates (with 2 I/p))

2] If we have 4 Input NAND gate, then how many 2 I/p NAND gates are req.ed to Implement it.

$= 2n-3$
$= 2\times4-3$
$= 5$ (2 I/p NAND gates).

3] Find two Input NAND gate for given boolean function.

A] $F = A.B.C.\overline{D}$ ← (we need 1 NAND gate for $\overline{D}$).

- For 4 Input AND gate, 2 Input NAND gates
  $= 2(n-1)$
  $= 2(4-1) = 6$
- Total 2 I/p NAND gate = $6+1 = 7$

B] $F = \overline{\overline{A}.B.\overline{C}}$

(So for $\overline{A}$ & $\overline{C}$ we need two 2 I/p NAND gates).

- For three I/p NAND gate, 2 Input NAND gates
  $= 2n-3$
  $= 2\times3-3$
  $= 3$
- So total 2 I/p NAND gate = $3+2 = 5$

HW Identify min. two Input NAND gates.

A] $F_1 = AB\overline{C}$
B] $F_2 = \overline{A.B}.\overline{C}$
C] $F_3 = \overline{\overline{A}.\overline{B}}$

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Minimum Number of 2 Input NAND gate for logical expression

1] The minimum number of 2 input NAND gates req.d to implement the function

$$F = (\bar{a} + \bar{b})(c + b)$$

64

1] 3 2] 4 3] 5 4] 6

$F = (\bar{a} + \bar{b})(c + b)$

[As per De Morgan's theorem $\bar{a} + \bar{b} = \overline{a.b}$]

$= \overline{(a.b)}(c + b)$

[Let $A = \overline{a.b}$] [1 NAND for A]

$= A(c + b)$

$= \overline{\overline{A.C + A.b}}$ [4 NAND gates].

$= \overline{\overline{A.C} \cdot \overline{A.b}}$

2] Minimum 2 input NAND gates req.d to implement the boolean function. [Note: w, x, y & z is available]

$f = w\bar{x}y\bar{z}$

1] 4 2] 5 3] 6 4] 7

$f = w\overline{(\bar{x})}\,y\overline{(\bar{z})}$

[two NAND gates req.d for $\bar{x}$ & $\bar{z}$]

- For four Vp AND gate, How many 2 ip NAND gate

$= 2(n-1)$

$= 2(4-1)$

$= 6$

- total NAND gate's $= 6 + 2 = 8$

3] Find min. two Vp NAND gates for given expression

$F = \overline{(A.B.C)}\,D$ (3 NAND gate).

- total NAND gates $= 3 + 5 = 8$.

$= 8 - 3 = 5$

- For Four Vp NAND, How many two Vp NAND $= 2n - 3$

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Minimum Number of NAND gates For given boolean eqn.

1) The minimum number of NAND gates req.ed to implement $A + A\bar{B} + A\bar{B}C$ is equal to

a) 0 b) 1 c) 4 d) 7

$$Y = A + A\bar{B} + A\bar{B}C$$

$$= A[1 + \bar{B} + \bar{B}C]$$

$[1 + A = 1]$

$$\boxed{Y = A}$$

2) Find Minimum NAND gates for

$$Y = AB + CD.$$

$$Y = \overline{\overline{AB + CD}}$$

[As per De Morgen's theorem $\overline{AB+CD} = \overline{AB} \cdot \overline{CD}$]

$$= \overline{\overline{AB} \cdot \overline{CD}}$$

[Here there is a need of three NAND gates].

3) Find Minimum number 2 Ip NAND gate req.ed for

$$Y = AB + BC + CA$$

$$Y = \overline{\overline{AB + BC + CA}}$$

[As per De Morgan's theorem, $\overline{AB + BC + CA} = \overline{AB} \cdot \overline{BC} \cdot \overline{CA}$]

$$= \overline{\overline{AB} \cdot \overline{BC} \cdot \overline{CA}}$$

↑ ↑ ↑ — [For $\overline{AB}$, $\overline{BC}$ & $\overline{CA}$ we need three NAND gates]

- For three termina NAND, How many two terminal NAND req.ed

$$= 2n - 3$$
$$= 2 \times 3 - 3$$
$$= 3$$

→ total = 3 + 3 = 6

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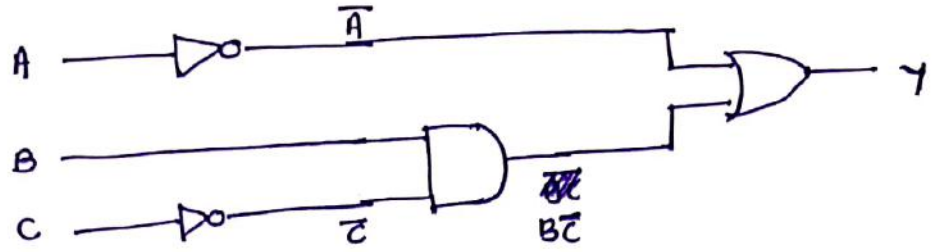
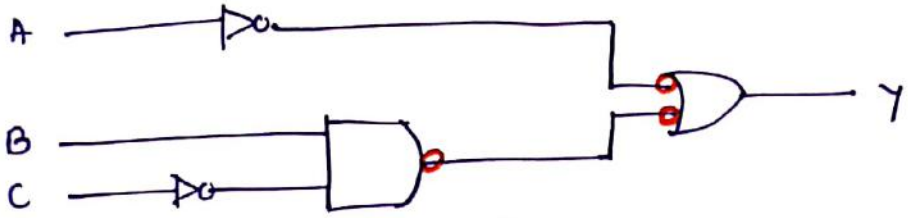
Boolean expression to NAND gate Implementation

1) $Y = \overline{A} + B\overline{C}$

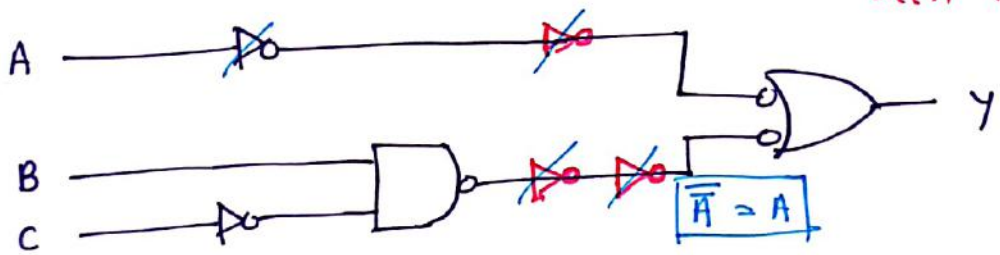
Step-1 Implement given Boolean expression interms of basic gates by AOI [AND, OR & NOT gates].



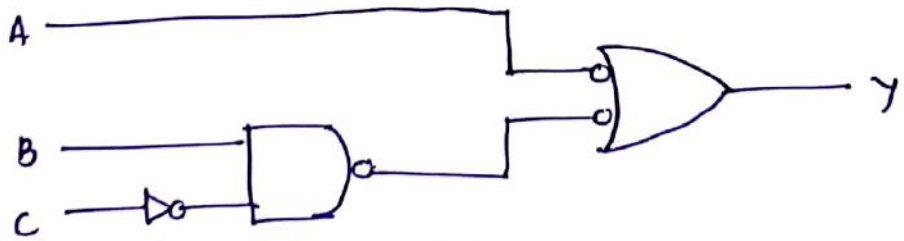
Step-2 Apply bubble to o/p of AND gate to i/p of OR gate.



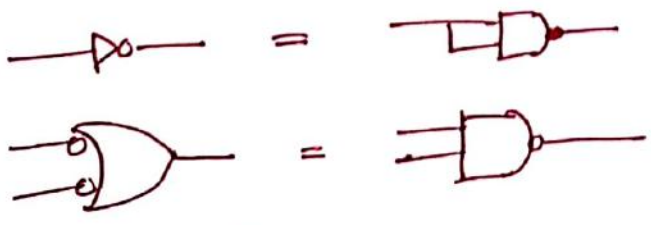
Step-3 Apply Not gate at places where bubbles have been inserted.



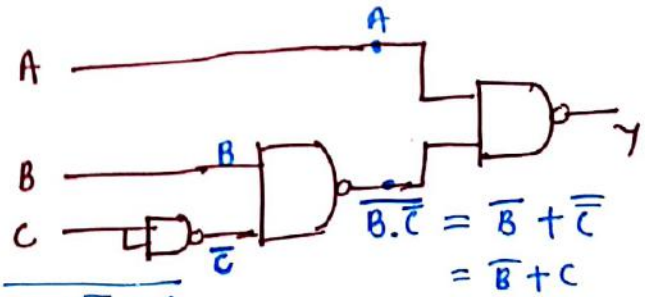
Step-4 Look out for double Inversions & cancel extra Not gates.



Step-5 place NAND equivalent



$\overline{A} + \overline{B} = \overline{A.B}$



$Y = \overline{A.(\overline{B}+C)}$

$= \overline{A} + \overline{(\overline{B}+C)}$

$= \overline{A} + \overline{\overline{B}}.\overline{C} = \overline{A} + B\overline{C}$

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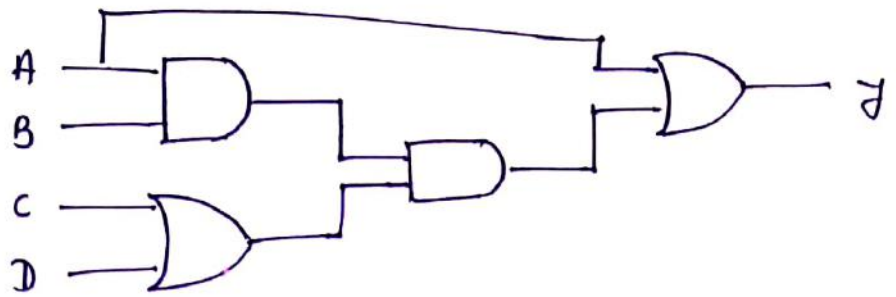
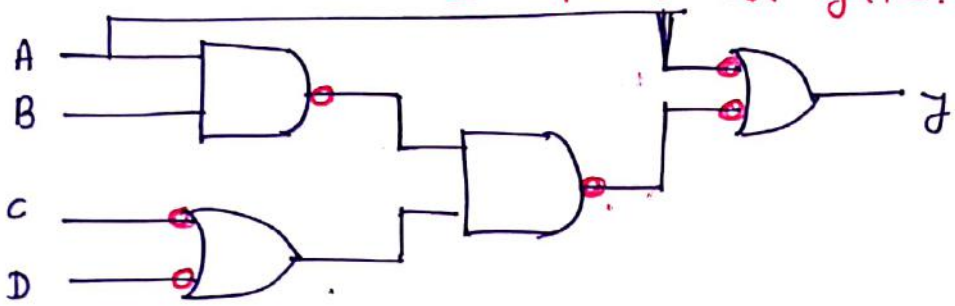
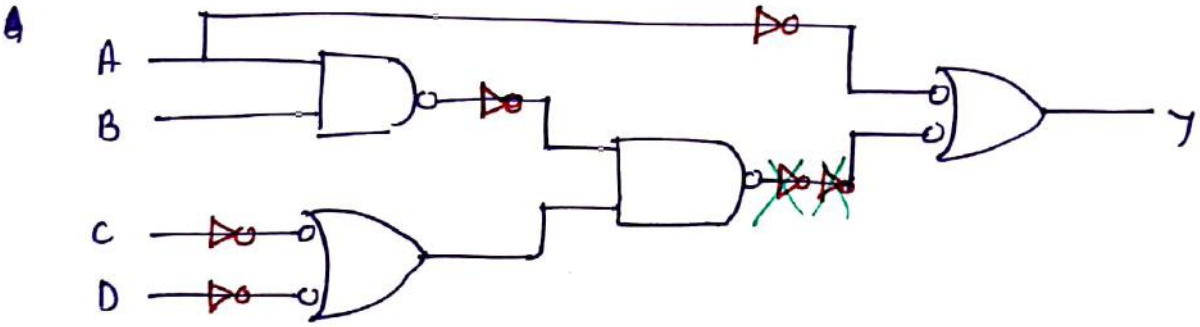
AOI to NAND Implementation



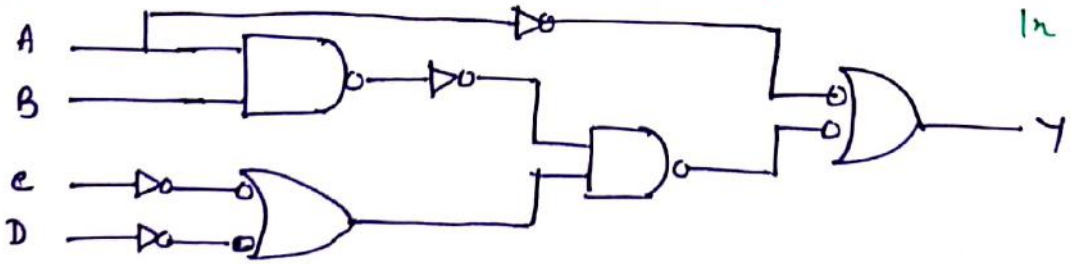
Step-1 Apply Bubble @ o/p of AND gate
@ Yp of OR gate.



Step-2 Apply NOT gates in place of bubbles we applied.

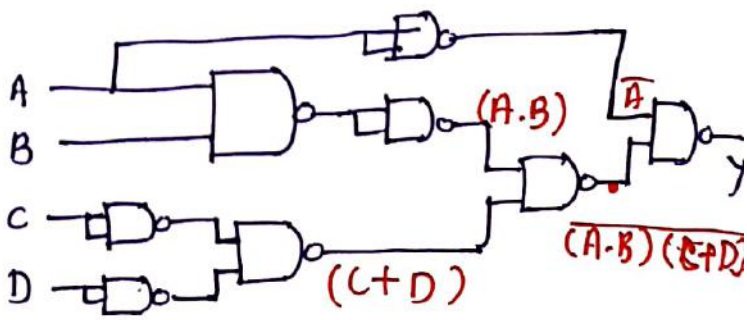


Step-3 look out for double NOT get cancel two NOT gates in series.



Step-4 place NAND equivalent

$$\overline{A} + \overline{B} = \overline{A \cdot B}$$



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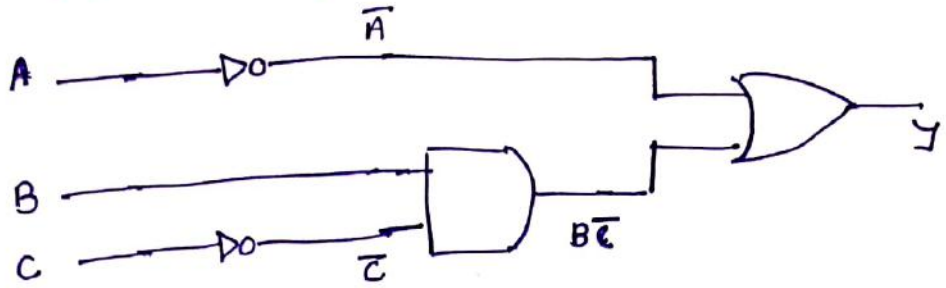
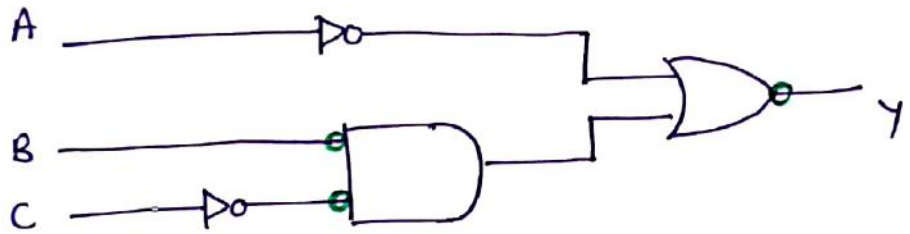
Boolean expression to NOR gate Implementation

If $Y = \overline{A} + B\overline{C}$

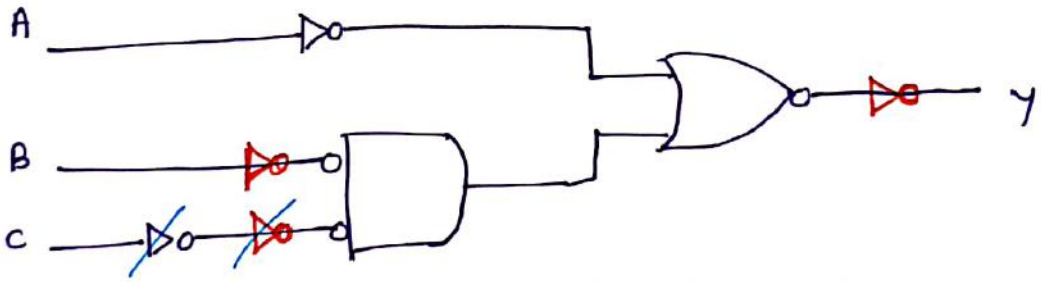
Step-1 Implement given boolean expression in terms of AOI [AND, OR & Inverter (NOT)] Implementation



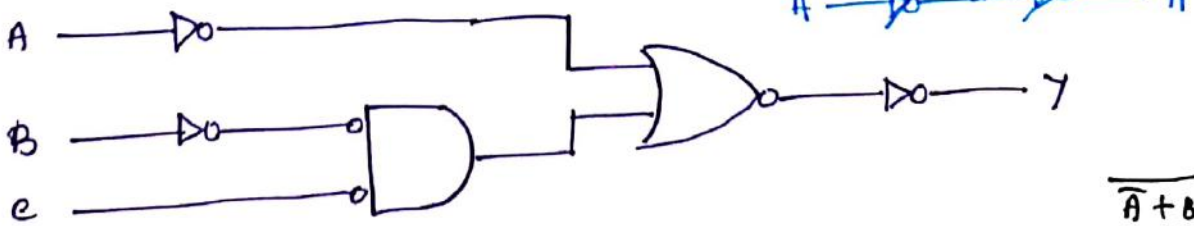
Step-2 Apply bubble at o/p of OR gate and at Yp of AND gate.



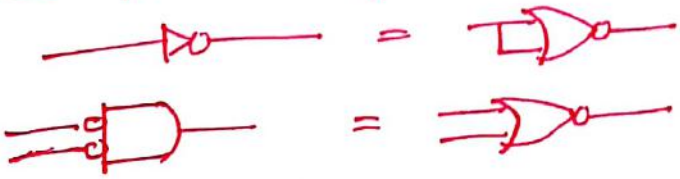
Step-3 Apply NOT gate in place of Bubble we have applied.



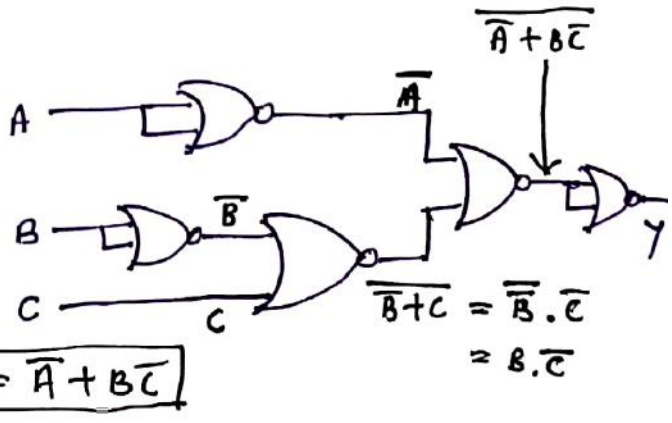
Step-4 Cancel NOT gates Connected in series.



Step-5 place NOR gate equivalent



$\overline{A}.\overline{B} = \overline{A+B}$



$Y = \overline{A} + B\overline{C}$

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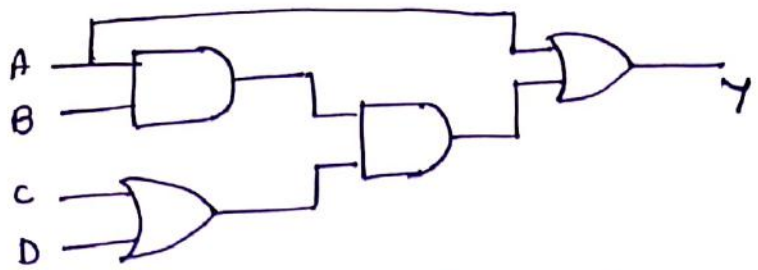
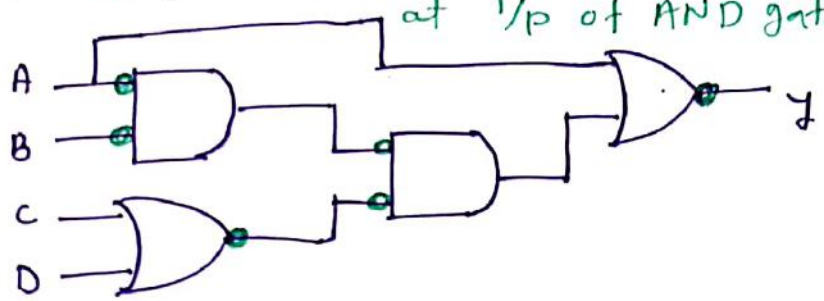
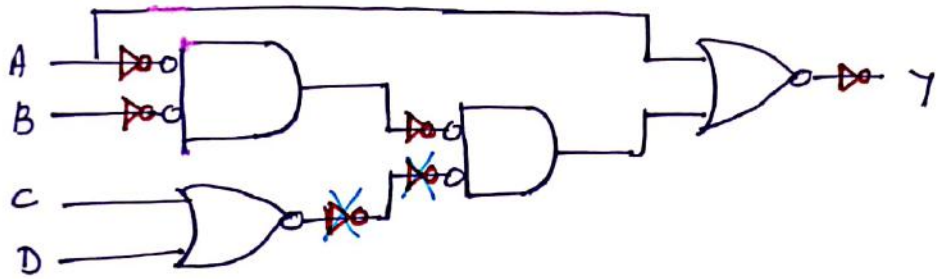
AOI to NOR Implementation



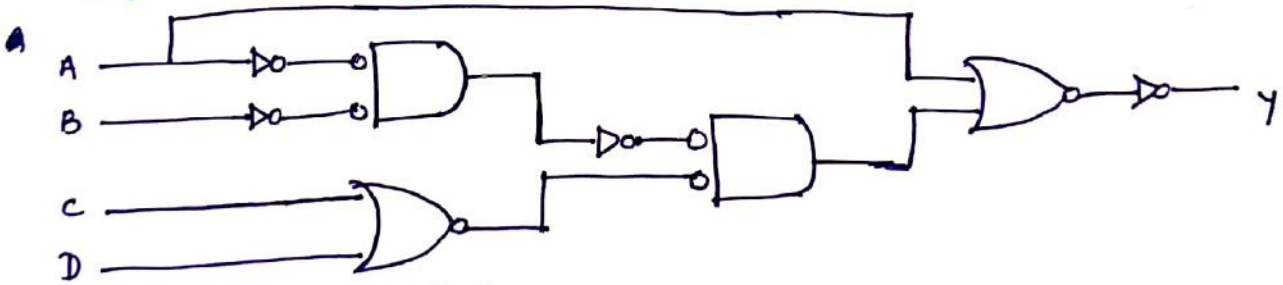
Step-1 Apply Bubble at o/p of OR gate and at i/p of AND gate.



Step-2 Apply NOT gates in place of bubble we applied.

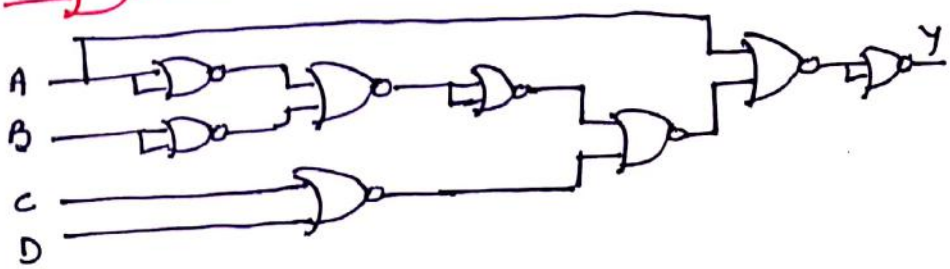


Step-3 Cancel two NOT gates connected in series.



Step-4 place NOR equivalent

$\overline{A}.\overline{B} = \overline{A+B}$



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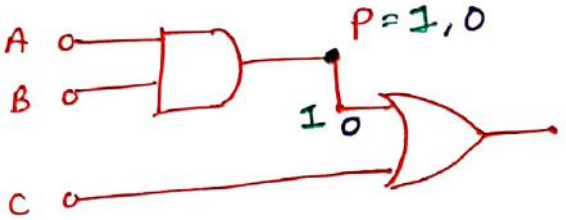
Stuck at 1 and Stuck at 0 Fault in logic Circuit

"Stuck at 1" ÷ O/p at given point will stay '1'. No matter what is the Circuit Connection

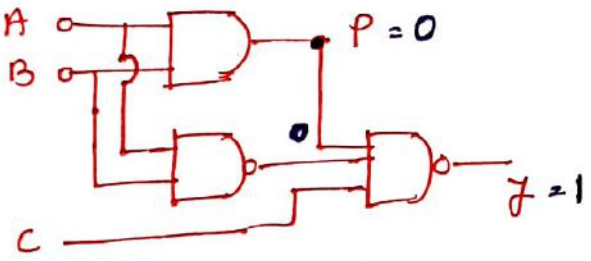
"Stuck at 0" ÷ O/p at given point will stay '0'. No matter what is the Circuit Connection.

Ex-1



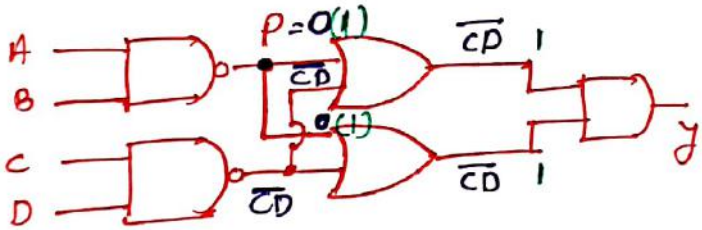
If point P is stuck at (0) 1, the output will be 1.

Ex-2



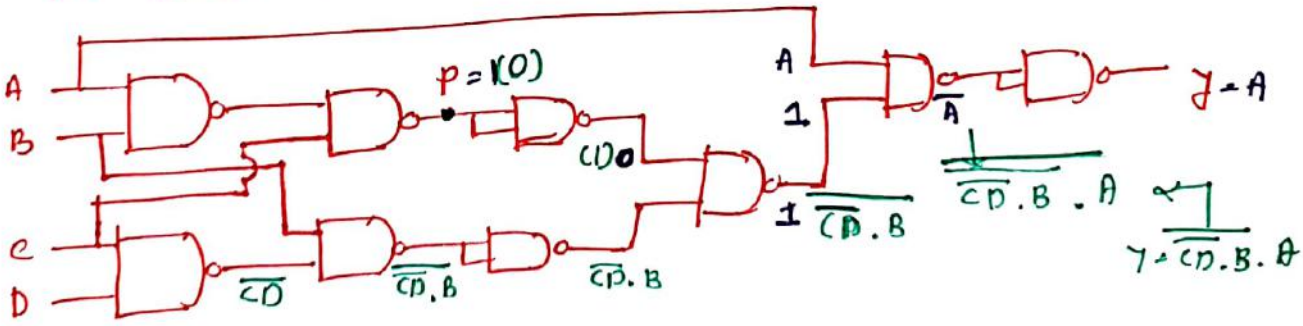
If point P is Stuck at 0, the O/p will be 1

Ex-3



If point P is Stuck at (1) 0, the O/p will be $\overline{CD}$

Ex-4



If poin P is Stuck at 1 then output y = ____

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