RAM [Random Access Memory]

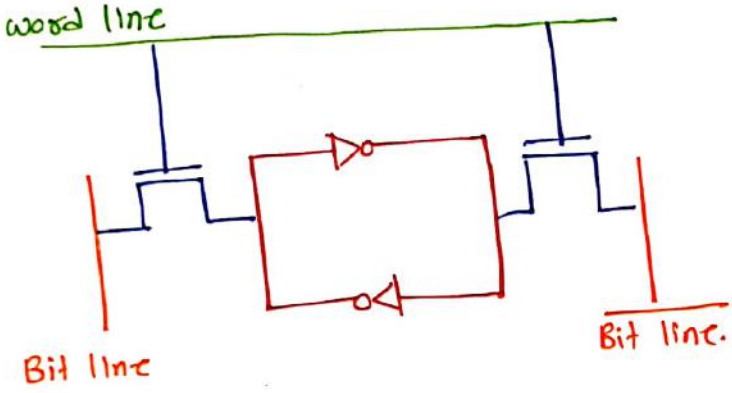
→ It is Voletile memory.

→ So, If power is OFF, then data of RAM will get erased.

SRAM

→ Stelfic RAM

→ It is made up of Flip Flop.



[Read/write]

→ Faster

→ No need of periodic refesh.

→ high cost

→ structure density is higher

→ It needs more power

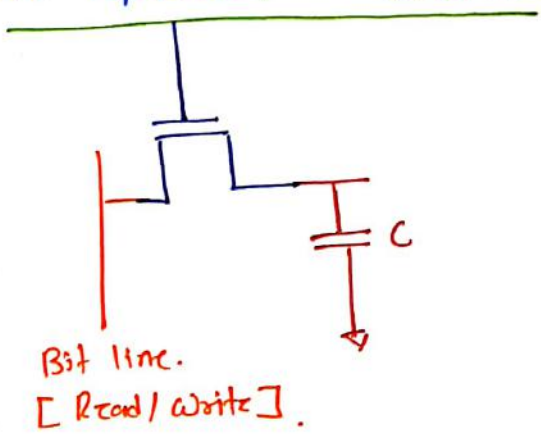
→ It generates more heat

→ It is used in CPU cache

DRAM

→ Dynamic RAM.

→ It is made up of Transister and capacitor.



[Read/write].

→ Slower.

→ It needs periodic refresh of capacitor.

→ low cost.

→ Structure density is lower.

→ It needs less power.

→ It generates less heat.

→ It is used in main memory of computer.

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ROM [Read Only Memory]

→ It is non Voletile memory.

→ So, when Power is OFF, Content of memery will stay Stored.

ROM structure.

= Decoder + Programmble OR gates.

= AND gates (fixed) + Programmble OR gates.

ROM size.

$= 2^x \times y$

Where, x = Number of Vp

y = Number of O/p.

→ E.g. If Vp = 8, O/p = 4 then what is the size of ROM

x = 8, y = 4

Size = $2^x \times y$

$= 2^8 \times 4 = 1024$ bits

$= (1024/8)$ bytes

= 128 bytes.

ROM Classitiations

PROM
- Programmble ROM
- Initially It is empty
- Then we Can program it Once
- Data Can not be erased here.

- EPROM
- Erasable PROM
- By UV rays we Can erase data.
- After that we Can reprogram this memory.

- EEPROM
- Electrically EPROM
- we Can erase data Electrically many times.
- Efficiency of memory will decay with respect to erase.
- Erase happens bit by bit.

- Flash memory
- Speed of erase is faster then EEPROM.
- Data erase is done block by block.

- Mask ROM
- It is PROM only.
- It is Programmed by chip manifacturer.
- this ROM is masked OFF during photolithography.

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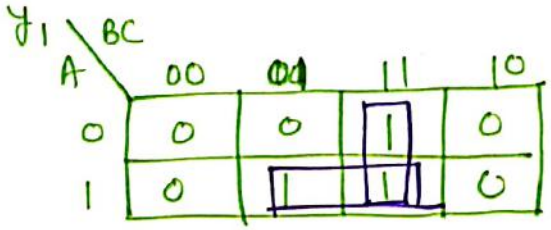
PLA - Programmable Logic Array

→ It is fixed architecture logic device with programmable AND gates and programmble OR gates.

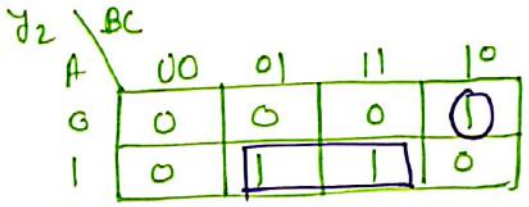
- Steps to program PLA

Step-1 Find boolean function from truth table.

A	B	C	y_1	y_2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	1
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1



$y_1 = AC + BC$

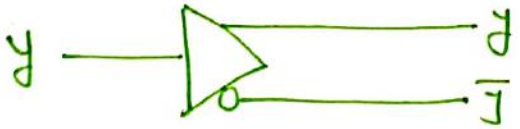


$y_2 = AC + \bar{A}B\bar{C}$

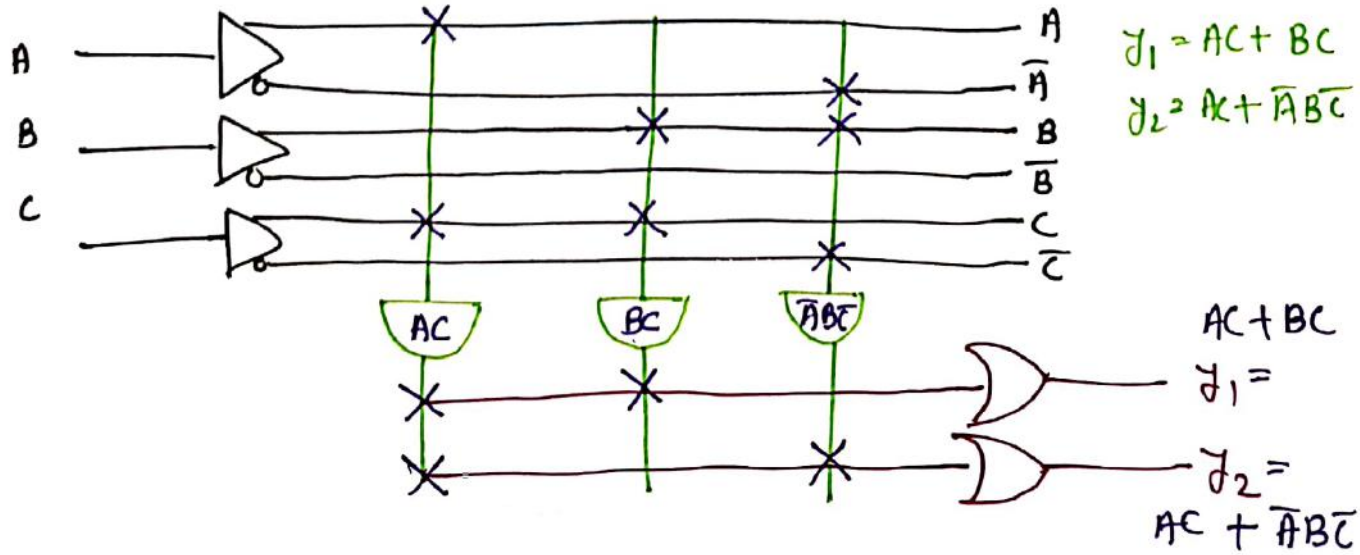
Step-2 Identify no of Input buttons.

- we have three input variables. So, we need

No of Input buttons = 3



Step-3 Implimentation of boolean function in PLA



$y_1 = AC + BC$

$y_2 = AC + \bar{A}B\bar{C}$

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PAL - Programmable Array Logic

→ It is most commonly used PLD.

→ It has programmable AND gates and fixed OR gates.

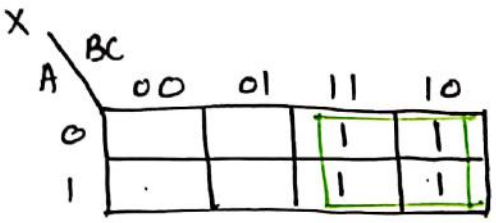
It provides simple structure

It has issues regarding flexibity.

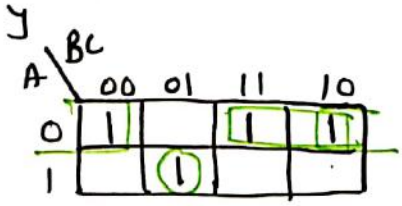
$X = \Sigma_m(2,3,6,7)$

$Y = \Sigma_m(0,2,3,5)$

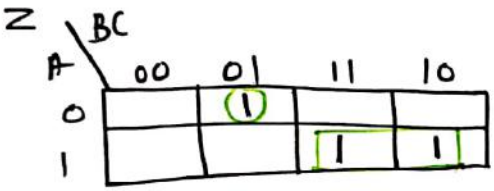
$Z = \Sigma_m(1,6,7)$



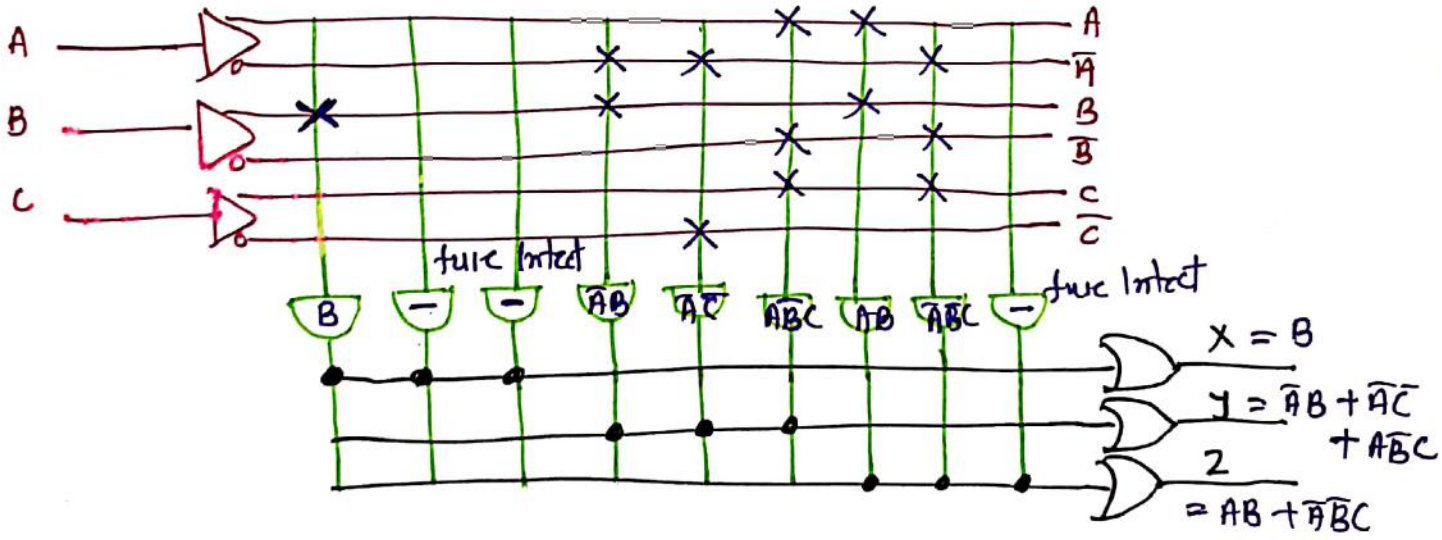
$X = B$



$Y = \bar{A}B + \bar{A}\bar{C} + A\bar{B}C$



$Z = AB + \bar{A}\bar{B}C$



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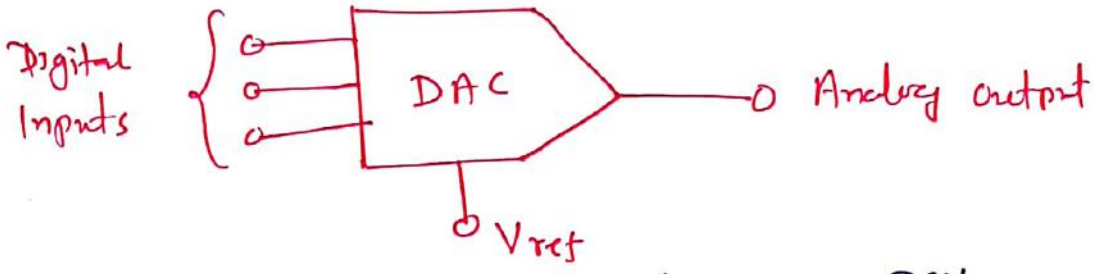
Binary Weighted Digital to Analog Converter [DAC]



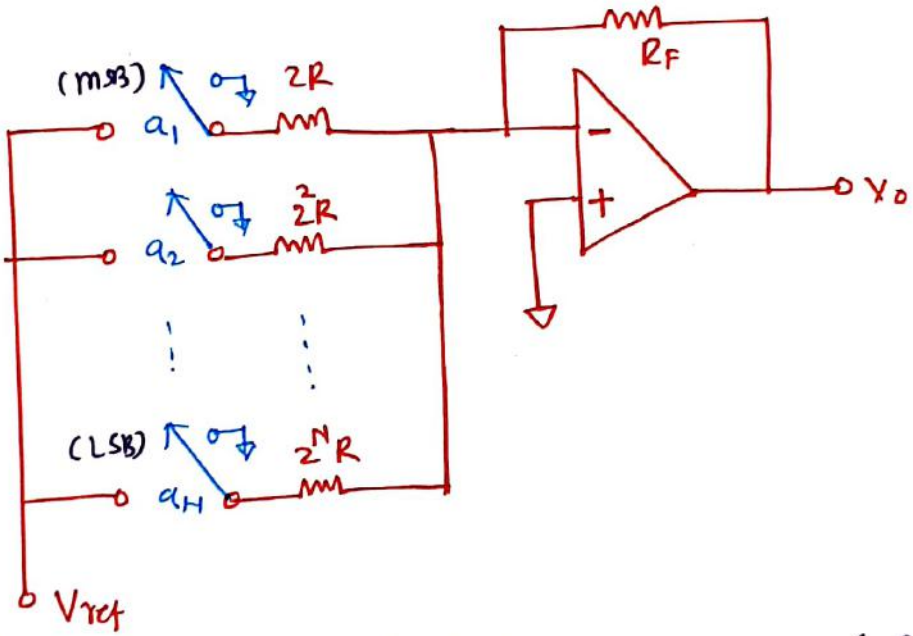
→ Resolution [Step Size] = $\frac{V_{ref}}{2^n} = \frac{FSV}{2^n - 1}$

where, n = number of bits.

→ IF gain is K with DAC.

→ Resolution [Step size] = $\frac{kV_{ref}}{2^n} = K\frac{FSV}{2^n-1}$

→ Full Scale Voltage FSV = $V_{ref}\left(\frac{2^n-1}{2^n}\right)$



→ $V_o = \left(-\frac{R_f}{2R}\right)a_1 V_{ref} + \left(-\frac{R_f}{2^2R}\right)a_2 V_{ref} + \ldots + \left(\frac{-R_f}{2^N R}\right)a_N V_{ref}$

$= \left(-\frac{R_f}{R}\right)V_{ref}\left[\frac{a_1}{2} + \frac{a_2}{4} + \ldots + \frac{a_N}{2^N}\right]$

→ For 3 bits O/p eqn.

$V_o = \left(-\frac{R_f}{R}\right)V_{ref}\left[\frac{a_1}{2} + \frac{a_2}{4} + \frac{a_3}{8}\right] = V_{ref}\left(\frac{a_1}{2} + \frac{a_2}{4} + \frac{a_3}{8}\right)$

→ $a_1a_2a_3 = 110$, then

$V_o = \left(-\frac{R_f}{R}\right)V_{ref}\left[\frac{1}{2} + \frac{1}{4} + \frac{0}{8}\right] = \left(-\frac{R_f}{R}\right)V_{ref}\left(\frac{6}{8}\right)$

Example of Binary weighted Digital to Analog Converter DAC

Find the V_{max} & V_{min} for 11111 Input with binary weighted DAC. $V_{ref} = 10$ V, $R_F = R = 1$ KΩ, Resistance tolerance 2%. Also Find Resolution, Full Scale Voltage.

→ $V_o = -V_{ref}\left(\frac{R_F}{R}\right)\left(\frac{a_1}{2} + \frac{a_2}{4} + \frac{a_3}{8} + \frac{a_4}{16} + \frac{a_5}{32}\right)$

$= -10\left(\frac{1}{1}\right)\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32}\right)$

$= -10\left(\frac{16+8+4+2+1}{32}\right)$

$= -10\left(\frac{31}{32}\right) = -9.6875$ Volt.

→ For V_{max}, $R_F = 1.02$ KΩ, $R = 0.98$ KΩ, $a_1a_2a_3a_4a_5 = 11111$

$V_{o_{max}} = -10\left(\frac{1.02}{0.98}\right)\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32}\right)$

$= -10.0829$ Volt

→ For V_{min}, $R_F = 0.98$ KΩ, $R = 1.02$ KΩ, $a_1a_2a_3a_4a_5 = 11111$

$V_{o\,min} = -10\left(\frac{0.98}{1.02}\right)\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32}\right)$

$= -9.30759$ Volt

→ Resolution $= k\frac{V_{ref}}{2^n} = \left(\frac{R_F}{R}\right)\frac{10}{2^5}$

$= \frac{10}{25} = 0.3125$ Volt

→ $FSV = V_{ref}\frac{(2^n - 1)}{2^n}$

$= 10\left(\frac{2^5 - 1}{2^5}\right)$

$= 10\left(\frac{31}{32}\right) = 9.6875$ Volt

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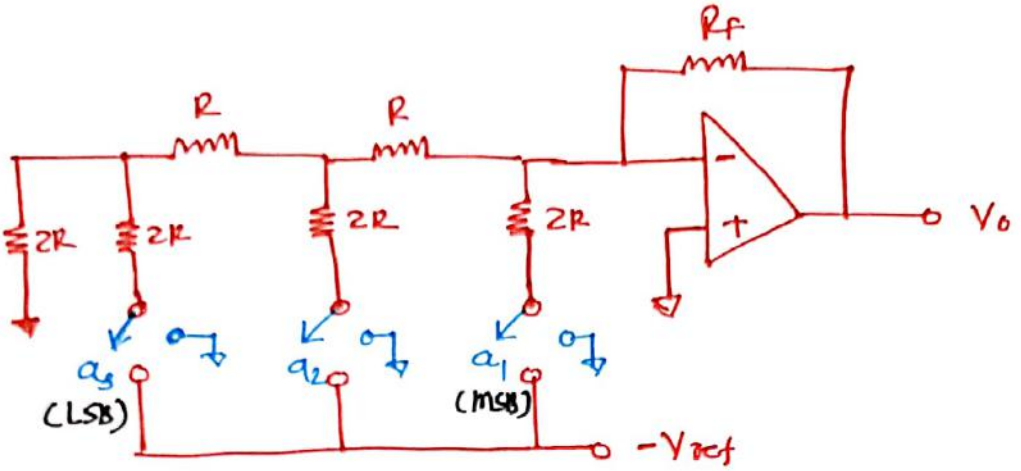
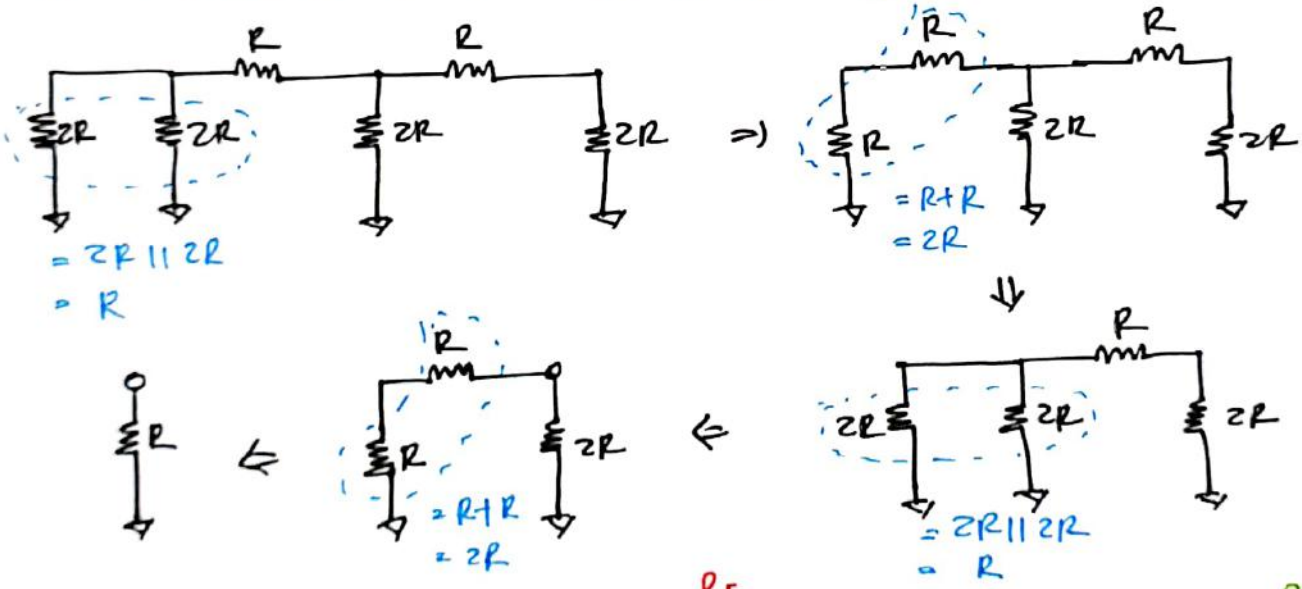
R-2R Ladder Digital to Analog Converter DAC [Voltage Switched]



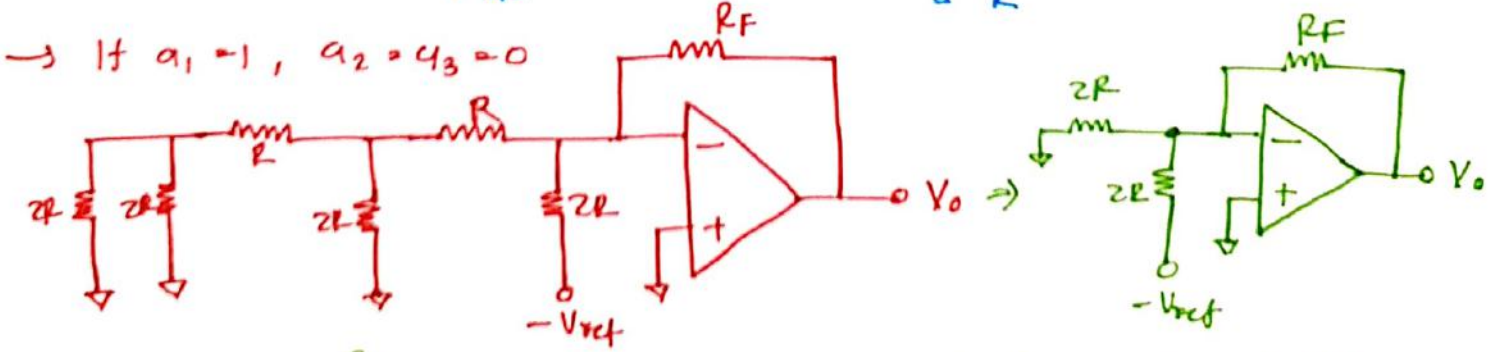
1] It uses only two values of resistor. Hence easy and accurate fabrication can be done.

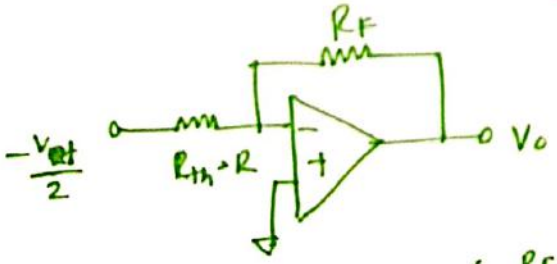
2] It is easy to scale with respect to number of bits.

3] Impedance of Network is R, regardless of number of bits.



→ If $a_1 = 1$, $a_2 = a_3 = 0$





→ $V_{th} = -V_{ref}\dfrac{(2R)}{2R+2R}$

$$\boxed{V_{th} = -\frac{V_{ref}}{2}}$$

→ $R_{th} = 2R \,||\, 2R = R$

$$V_o = \left(-\frac{R_f}{R}\right)\left(-\frac{V_{ref}}{2}\right) = \boxed{\left(\frac{R_f}{R}\right)\left(\frac{V_{ref}}{2}\right)}$$

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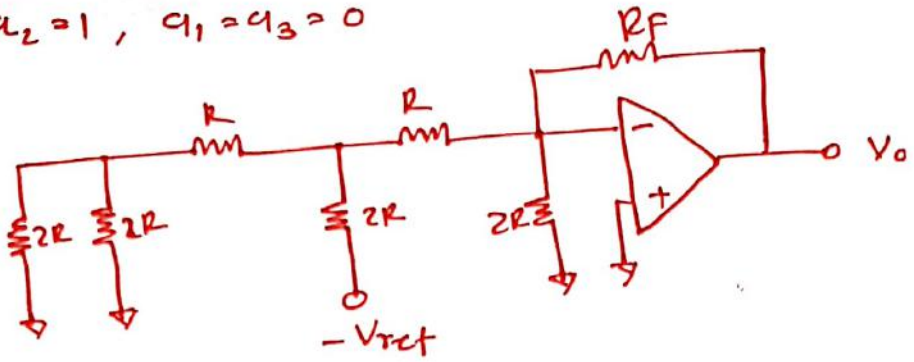
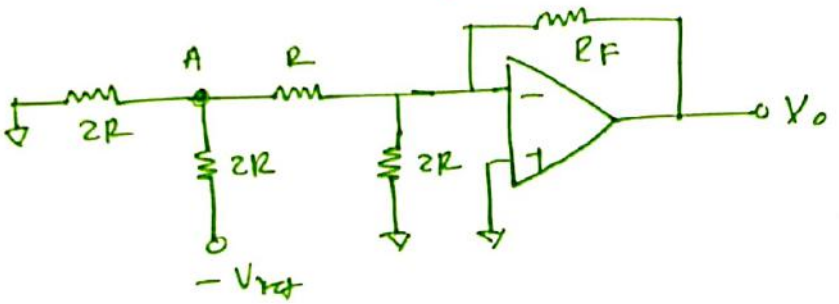
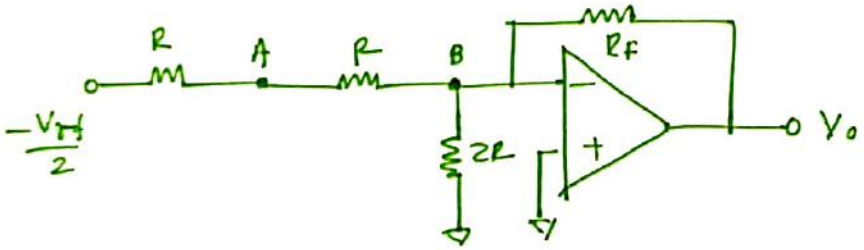
→ $a_2 = 1$, $a_1 = a_3 = 0$

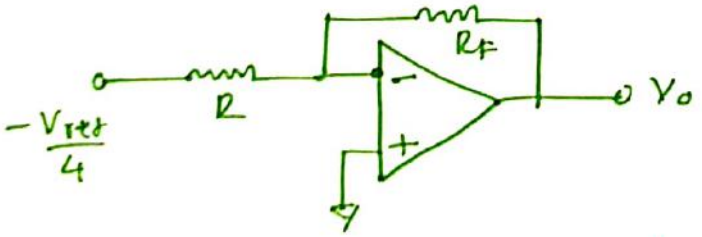




- at A, $V_{th} = \frac{-V_{ref}(2R)}{2R+2R} = -\frac{V_{ref}}{2}$, $R_{th} = 2R \,||\, 2R = R$



- at B, $V_{th} = \frac{\left(-\frac{V_{ref}}{2}\right)(2R)}{2R+2R} = -\frac{V_{ref}}{4}$, $R_{th} = 2R \,||\, 2R = R$



$$V_o = \left(-\frac{R_F}{R}\right)\left(-\frac{V_{ref}}{4}\right) = \left(\frac{R_F}{R}\right)\left(\frac{V_{ref}}{4}\right)$$

→ $a_3 = 1$, $a_1 = a_2 = 0$, $V_o = \left(\frac{R_F}{R}\right)\left(\frac{V_{ref}}{8}\right)$

→ $$V_o = \left(\frac{R_F}{R}\right) V_{ref}\left(\frac{a_1}{2} + \frac{a_2}{4} + \frac{a_3}{8}\right) = V_{ref}\left(\frac{a_1}{2} + \frac{a_2}{4} + \frac{a_3}{8}\right)$$

Digital data			Analog
a_1	a_2	a_3	V_o
0	0	0	0
0	0	1	$V_{ref}/8$
0	1	0	$2V_{ref}/8$
0	1	1	$3V_{ref}/8$
1	0	0	$4V_{ref}/8$
1	0	1	$5V_{ref}/8$
1	1	0	$6V_{ref}/8$
1	1	1	$7V_{ref}/8$

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Example on R-2R Ladder Digital to Analog Converter.

In R-2R DAC, Find the full scale output Voltage if $R_F = 2K\Omega$ and $R = 1K\Omega$. Also Find the output Voltage when the Input is 10110. Assume $V_{ref} = 5V$. Also Find resolution & FSR.

- $-V_0 = -V_{ref}\left(\frac{R_F}{R}\right)\left(\frac{a_1}{2} + \frac{a_2}{4} + \frac{a_3}{8} + \frac{a_4}{16} + \frac{a_5}{32}\right)$

- For Full scale output, $a_1a_2a_3a_4a_5 = 11111$

$$V_0 = -5\left(\frac{2}{1}\right)\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32}\right)$$

$$= -10\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32}\right)$$

$$= -10\left(\frac{16+8+4+2+1}{32}\right)$$

$$= -10\left(\frac{31}{32}\right) = -9.6875 \text{ Volt}$$

- For Input $a_1a_2a_3a_4a_5 = 10110$

$$V_0 = -5\left(\frac{2}{1}\right)\left(\frac{1}{2} + \frac{1}{8} + \frac{1}{16}\right)$$

$$= -10\left(\frac{8+2+1}{16}\right)$$

$$= -10\left(\frac{11}{16}\right) = -6.875 \text{ Volt}$$

- Resolution (Step Size) $= K\,\frac{V_{ref}}{2^n}$

$$= \left(\frac{R_F}{R}\right)\left(\frac{V_{ref}}{2^n}\right)$$

$$= \left(\frac{2}{1}\right)\left(\frac{5}{2^5}\right) = \frac{10}{32} = 0.3125 \text{ Volt}$$

- Full scale Range $= V_{ref}\left(\frac{R_F}{R}\right)\frac{(2^n-1)}{2^n}$

$$= 5\left(\frac{2}{1}\right)\frac{(2^5-1)}{2^5}$$

$$= 10\left(\frac{31}{32}\right)$$

$$= 9.6875 \text{ Volt.}$$

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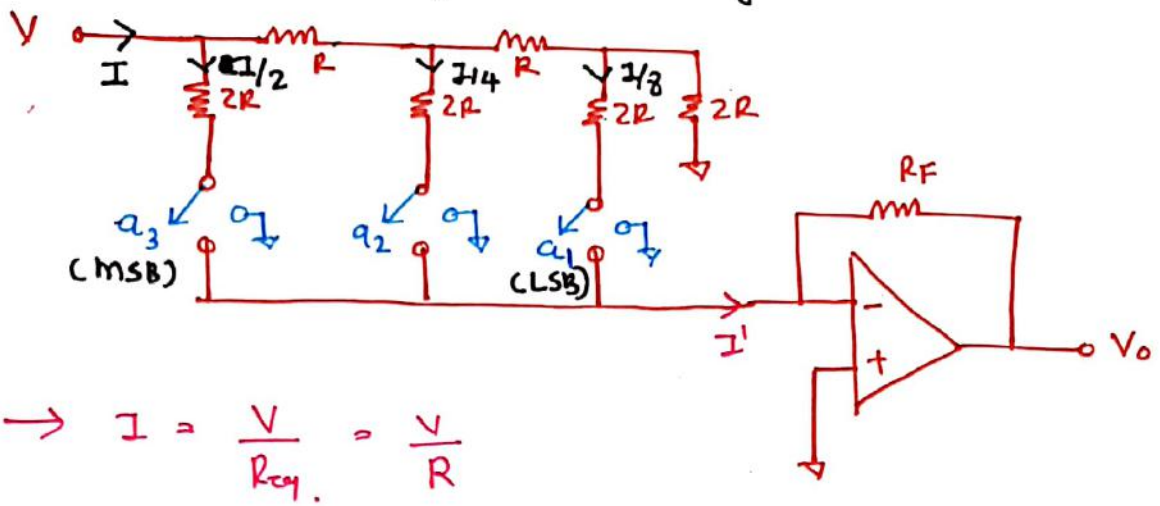
R-2R Ladder Digital to Analog Converter DAC [Current Switched]



$$\rightarrow I = \frac{V}{R_{eq.}} = \frac{V}{R}$$

$$\rightarrow V_o = -I' R_F$$

$$= -\left[a_3\left(\frac{I}{2}\right) + a_2\left(\frac{I}{4}\right) + a_1\left(\frac{I}{8}\right) \right] R_F$$

$$= -\left[\frac{a_3}{2} + \frac{a_2}{4} + \frac{a_1}{8} \right] I R_F$$

$$\boxed{V_o = -\left[\frac{a_3}{2} + \frac{a_2}{4} + \frac{a_1}{8} \right] V\left(\frac{R_F}{R}\right)}$$

$$\rightarrow V_o = -V\left(\frac{R_F}{R}\right)\left[\frac{a_1}{2} + \frac{a_2}{4} + \frac{a_3}{8} \right]$$ [Voltage Switched type].

$R = 1\ k\Omega$, $R_F = 1\ k\Omega$, $a_3\, a_2\, a_1 = 110$, $V_o = ?$

$$V_o = -\left[\frac{a_3}{2} + \frac{a_2}{4} + \frac{a_1}{8} \right] V\left(\frac{R_F}{R}\right)$$

$$= -\left[\frac{1}{2} + \frac{1}{4} \right] V\left(\frac{1}{1}\right)$$

$$= \boxed{-\frac{3}{4} V}$$

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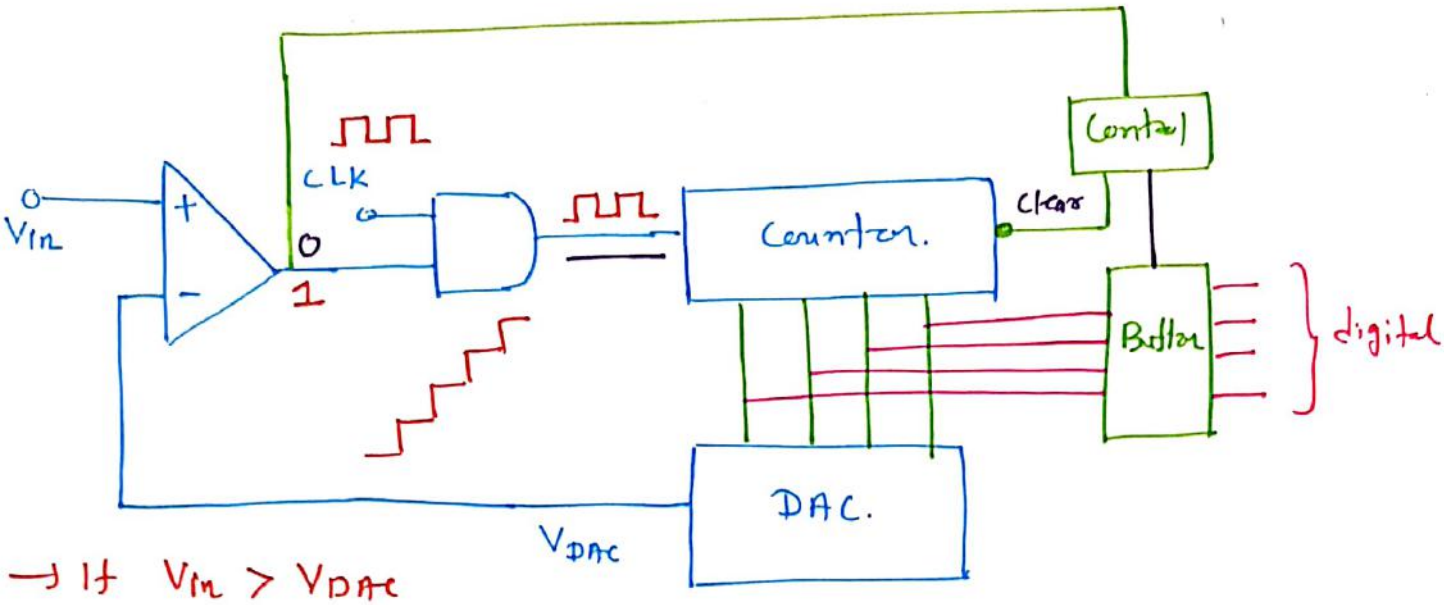
Counter Type ADC

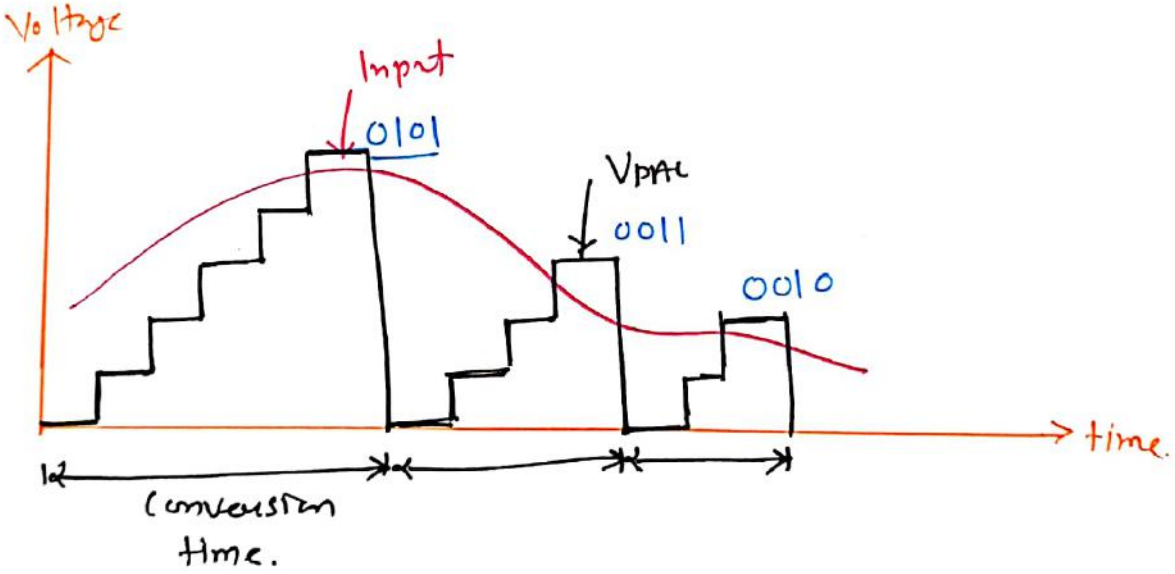


→ If $V_{in} > V_{DAC}$
Comparator o/p = 1

→ If $V_{DAC} > V_{in}$
Comparator o/p = 0

$T_{c(max)} = (2^N - 1)\, T_{CLK}$

N = number of bits



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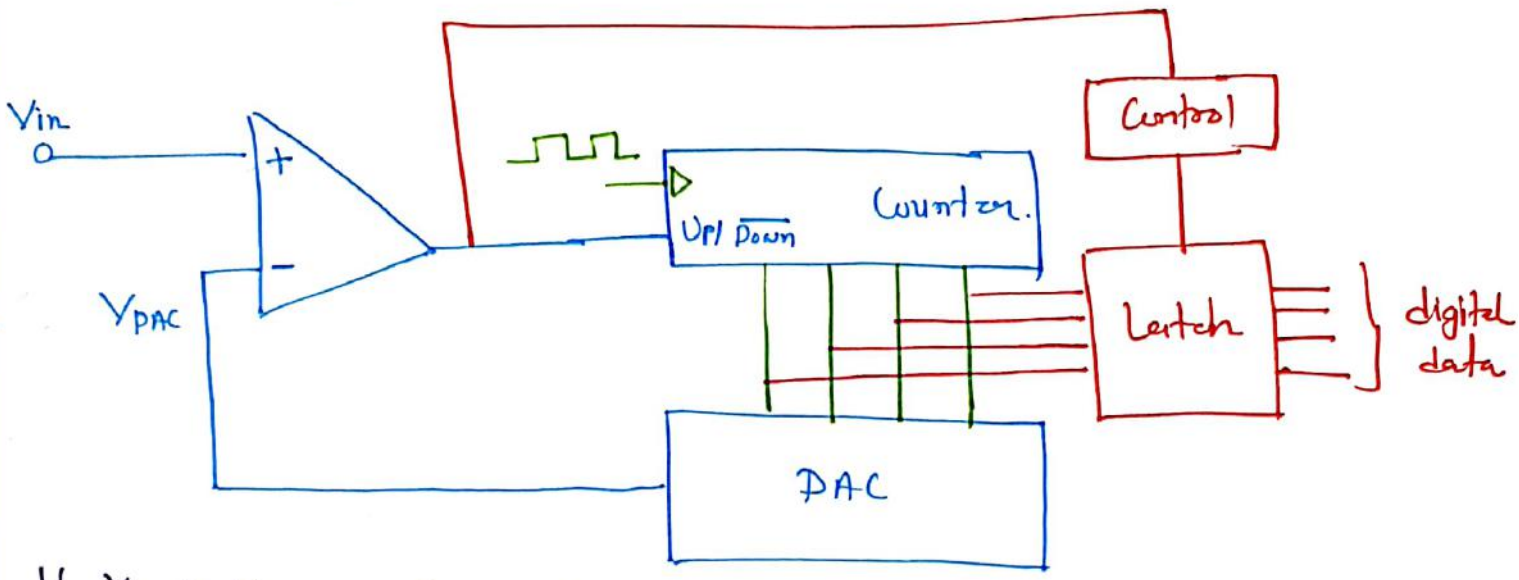
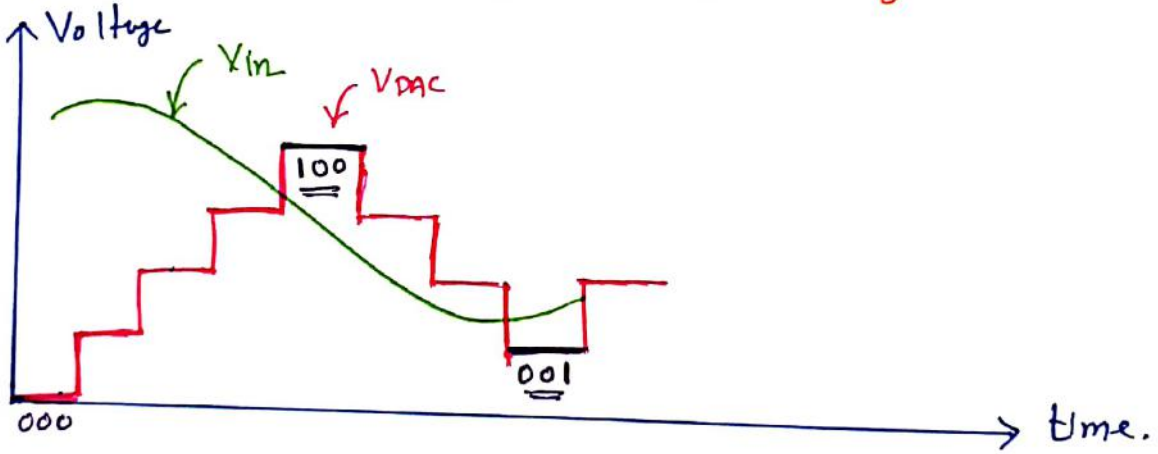
Tracking Type ADC



If $V_{in} > V_{DAC}$, Comparator o/p = +Ve (logic 1), Counter = up

If $V_{DAC} < V_{in}$, Comparator o/p = −Ve (Logic 0), Counter = Down

During transition from 0 to 1 and 1 to 0 at o/p of comparator, control circuit provides Latch digital o/p.



- Highest conversion time $T_{c(max)} = (2^N - 1)\, T_{CLK}$.
- Sampling time $T_s = T_c + T_d$

  ↑ It is due to Acquisition time and component delay.
- For uniform sampling $T_s = T_{c(max)}$
- Sampling freq $f_s = \frac{1}{T_s}$.
- As per Nyquist sampling theorm

$$f_s \geq 2 f_m \Rightarrow f_m \leq f_s/2 \Rightarrow \boxed{f_m \leq \frac{1}{2T_s}}$$

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✱ Examples on ADC.

1] Consider following ADC

(a) Successive Approximation type ADC

(b) Dual slope ADC

(c) flash ADC.

Find Max. conversion time for above ADC. with 8 bits.

→ N = 8 bits.

a] $T_{max} = N\,T_{CLK}$
$= 8\,T_{CLK}$

b] $T_{max} = 2^{N+1}\,T_{CLK}$
$= 2^{8+1}\,T_{CLK}$
$= 512\,T_{CLK}$

c] $T_{max} = T_{CLK}$
$= T_{CLK}$

2] No of comparators in 4 bits Flash ADC is 15

$= 2^N - 1$
$= 2^4 - 1$
$= 15$

3] A 12 bit ADC is operating with clock of 1μsec clock period & total conversion time is seen to be 14 μsec. The ADC must be

(a) Flash ADC
(b) Counter type
(c) Successive Approximation type ✓
(d) Dual Slope

[Note take Circuit delay = 2μsec]

→ Flash ADC $T_{max} = T_{CLK} = 1\mu sec + 2\mu sec = 3\mu sec$

→ Counter ADC $T_{max} = (2^N - 1)\,T_{CLK} = (2^{12} - 1)\,1\mu sec + 2\mu sec$
$= 4095 + 2 = 4097\,\mu sec$

→ Successive App. ADC $T_{max} = N\,T_{CLK}$
$= 12 \times 1\mu sec + 2\mu sec = 14\,\mu sec.$

→ Dual Slope ADC $T_{max} = 2^{N+1}\,T_{CLK} = 2^{13}\,T_{CLK} + 2\mu sec = 8194\,\mu sec$

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4] The resolution of 4 bits ADC is 0.5 Volt. For Analog Voltage 6.6 Volt, The digital o/p will be. ____

a] 1011 b] 1101 c] 1100 d] 1110

→ Δ = 0.5 Volt

→ V = 6.6 Volt

→ No of Steps = $\frac{V}{\Delta} = \frac{6.6}{0.5} = 13.2 = 13$

→ Digital data = 1101

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