Project Name: Build a Virtual CPU Emulator

Week 08: Performance Optimization

Objective:

To optimize the virtual CPU emulator for improved performance by identifying and addressing bottlenecks, optimizing critical code paths, and enhancing the assembler for efficient instruction encoding.

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1. Profile the Emulator to Identify Bottlenecks

Profiling allows us to pinpoint areas of inefficiency in the emulator's execution.

1.1 Performance Analysis:

- Use profiling tools (e.g., `cProfile`, `py-spy`) to monitor execution time and memory usage.
- Identify bottlenecks in instruction decoding, memory access, and pipeline stages.

1.2 Test Scenarios:

- Analyze performance under different workloads:
    - Linear execution.
    - Branching-heavy programs.
    - Interrupt and subroutine-intensive scenarios.

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2. Optimize Critical Code Paths

Improving the most frequently executed code paths ensures faster overall performance.

2.1 Instruction Fetch and Decode:

- Optimize opcode lookup using hash maps or lookup tables.
- Refactor instruction parsing for faster decoding.

2.2 Pipeline Efficiency:

- Reduce overhead between pipeline stages for smoother data flow.

- Improve hazard detection and stalling mechanisms to minimize delays.

2.3 Memory Access Optimization:

- Implement caching for frequently accessed memory regions.
- Restructure memory layouts to improve spatial and temporal locality.

2.4 Stack and Interrupt Handling:

- Optimize stack operations for CALL/RET instructions.
- Simplify the logic for saving and restoring CPU state in ISR (Interrupt Service Routine).

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3. Enhance the Assembler for Better Instruction Encoding

An optimized assembler generates compact and efficient machine code, boosting execution speed.

3.1 Instruction Format Optimization:

- Use shorter encoding formats for common instructions.
- Redesign operand encoding for smaller and faster instructions.

3.2 Instruction Bundling:

- Group compatible instructions to prevent pipeline hazards.
- Align instruction sequences for better branch prediction performance.
