North South University

Department of Electrical & Computer Engineering

Project: 20 bit Single Cycle CPU

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R-type Format:

OPCode 2 bits (18-19)	**RD** 4 bits (14-17)	**RS** 4 bits (10-13)	**RT** 4 bits (6-9)	**Shamt** 3 bits (3-5)	**Function** 3 bits (0-2)

I-type Format:

OPCode 2 bits (18-19)	**RD** 4 bits (14-17)	**RS** 4 bits (10-13)	**Address/Immediate** 7 bits (3-9)	**Function** 3 bits (0-2)

J-type Format:

OPCode 2 bits (18-19)	**Jump** 18 bits (0-17)

Table: 1: MIPS INSTRUCTION DIAGRAM:

Instruction	**Type**	**Instruction Code(Bin)**
ADD	R-type	00 0000 0001 0010 XXX 000
SUB	R-type	00 0011 0100 0101 XXX 001
AND	R-type	00 0100 0101 0110 XXX 010
AND	R-type	00 0111 1000 1001 XXX 011
OR	R-type	00 1010 1011 1100 XXX 100
NOR	R-type	00 0011 0100 0101 XXX 100
SLL	R-type	00 0100 0101 XXXX 010 101
SRL	R-type	00 0101 0110 XXXX 011 110
SLT	R-type	00 0011 0100 0101 XXX 111
LW	I-type	01 1001 0001 0001011 000
SW	I-type	01 0001 0001 0001001 001
BEQ	I-type	01 0010 0011 0000101 010
BNE	I-type	01 0011 0010 1000110 011
J	J-type	10 XXXXXXXXXXXXXXXXX

Table: 2: OPCODE TABLE:

Instruction Type	Opcode
R-type	00
I-type	01
J-type	10

Table: 3: Control Unit Table:

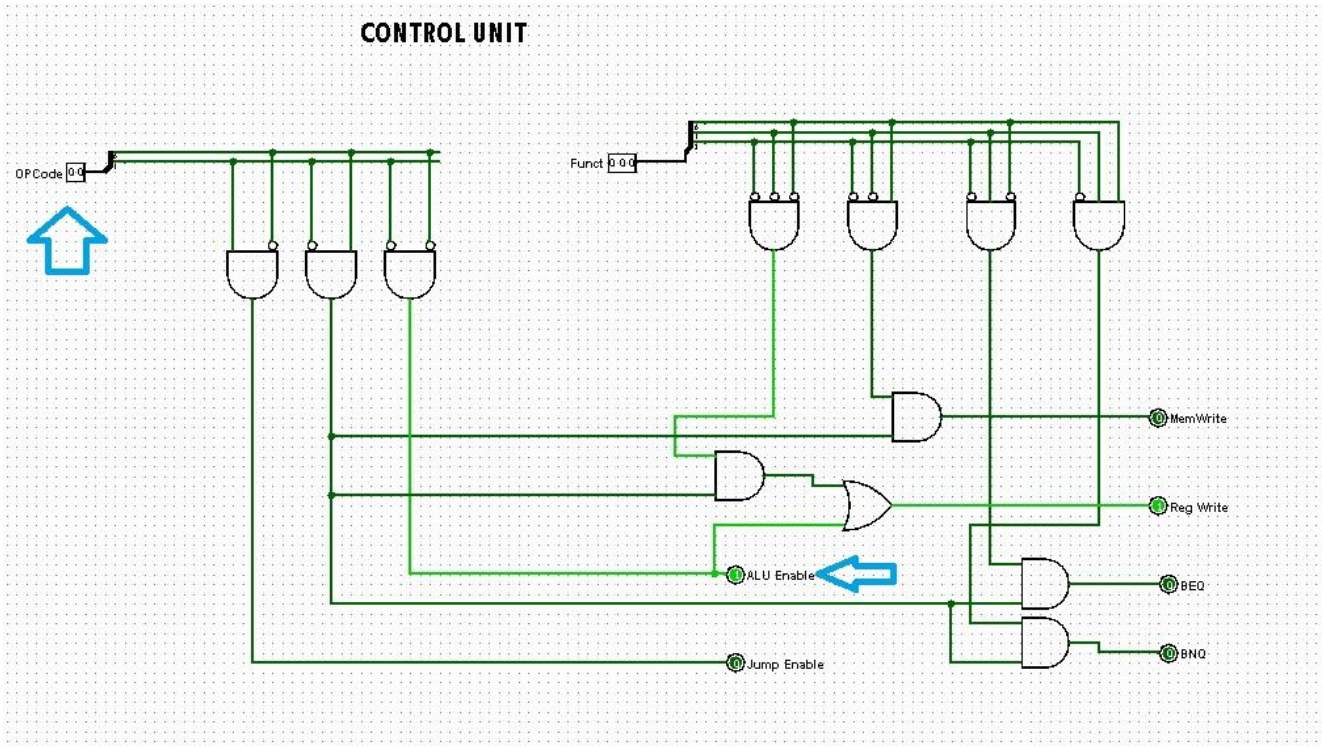
Instruction	Opcode	ALU Enable	Function Code
ADD	00	01	XXX
SUB	00	01	XXX
AND	00	01	XXX
AND	00	01	XXX
OR	00	01	XXX
NOR	00	01	XXX
SLL	00	01	XXX
SRL	00	01	XXX
SLT	00	01	XXX
LW	01	XX	000
SW	01	XX	001
BEQ	01	XX	010
BNE	01	XX	011
J	10	XX	XXX

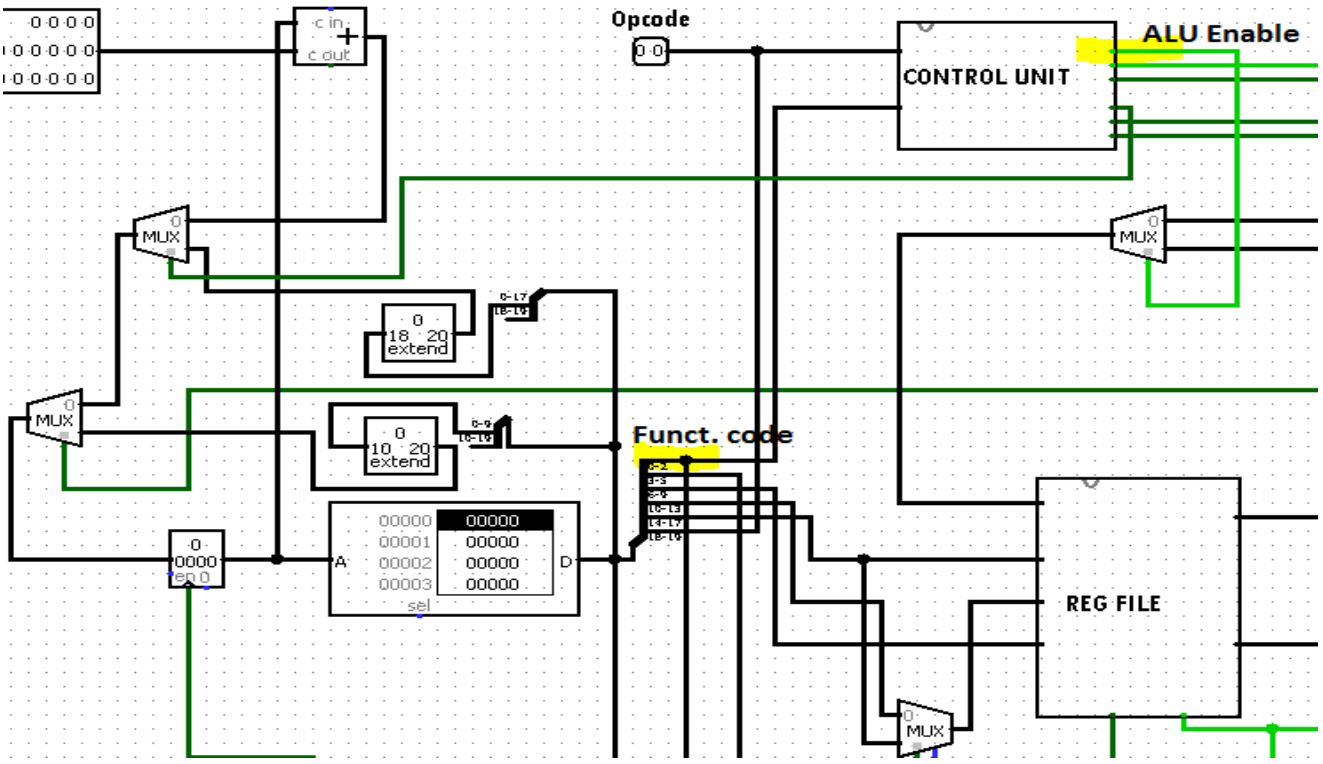
Table: 4: ALU Table:

Instruction	ALU OPCode
ADD	000
SUB	001
AND	010
OR	011
NOR	100
SLL	101
SRL	110
SLT	111

How it works:

For R-type instruction: At first when the control unit receives the OPCode as '00' it recognizes the instruction as an R-type instruction and sets the 'ALU Enable' key as '1' for executing the further ALU operation(s). In ALU there are specific function defined (stated at Table: 4). Those functions can be achieved using instruction of bit no. 0, 1 & 3 which is actually the function codes defined for each operation.

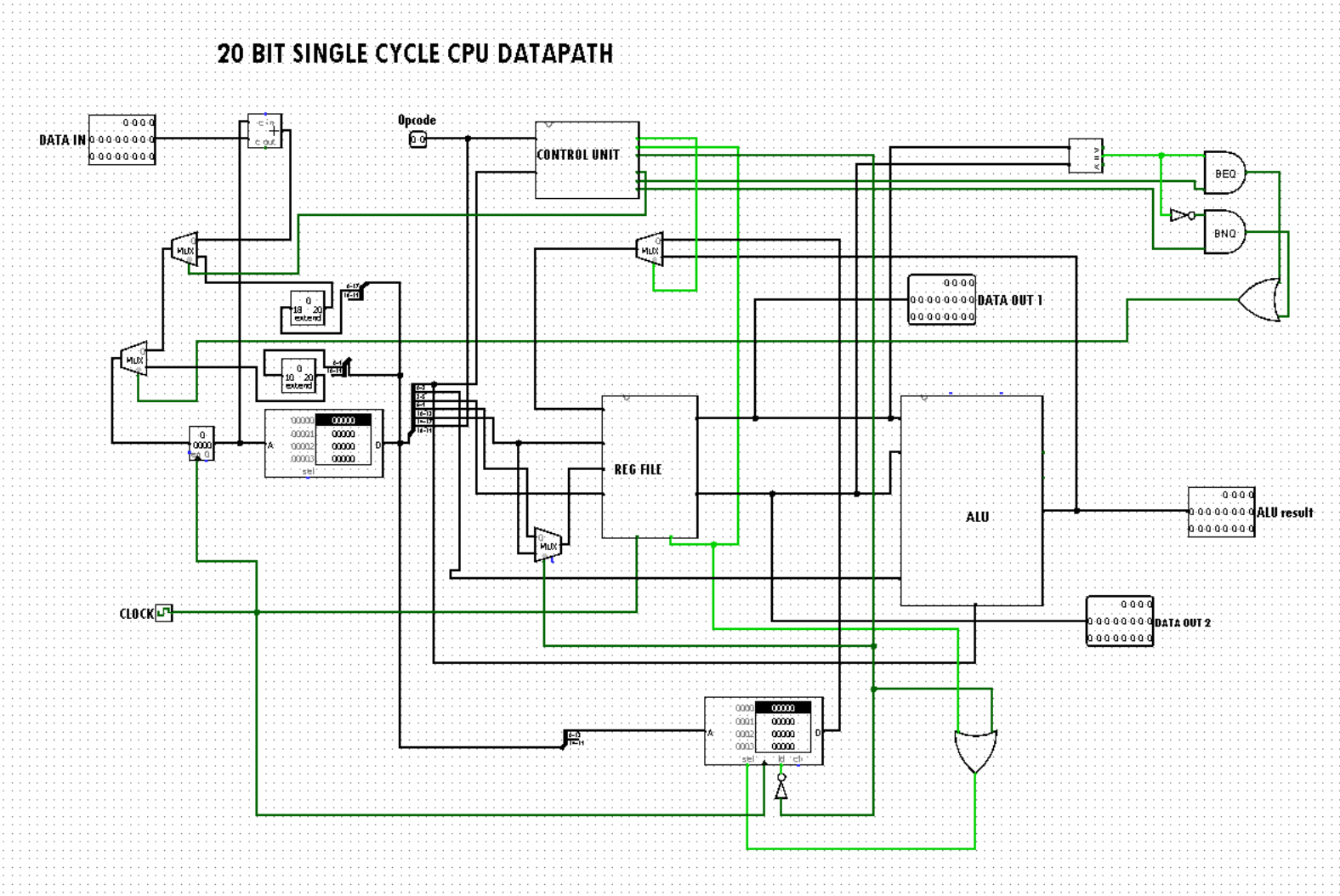


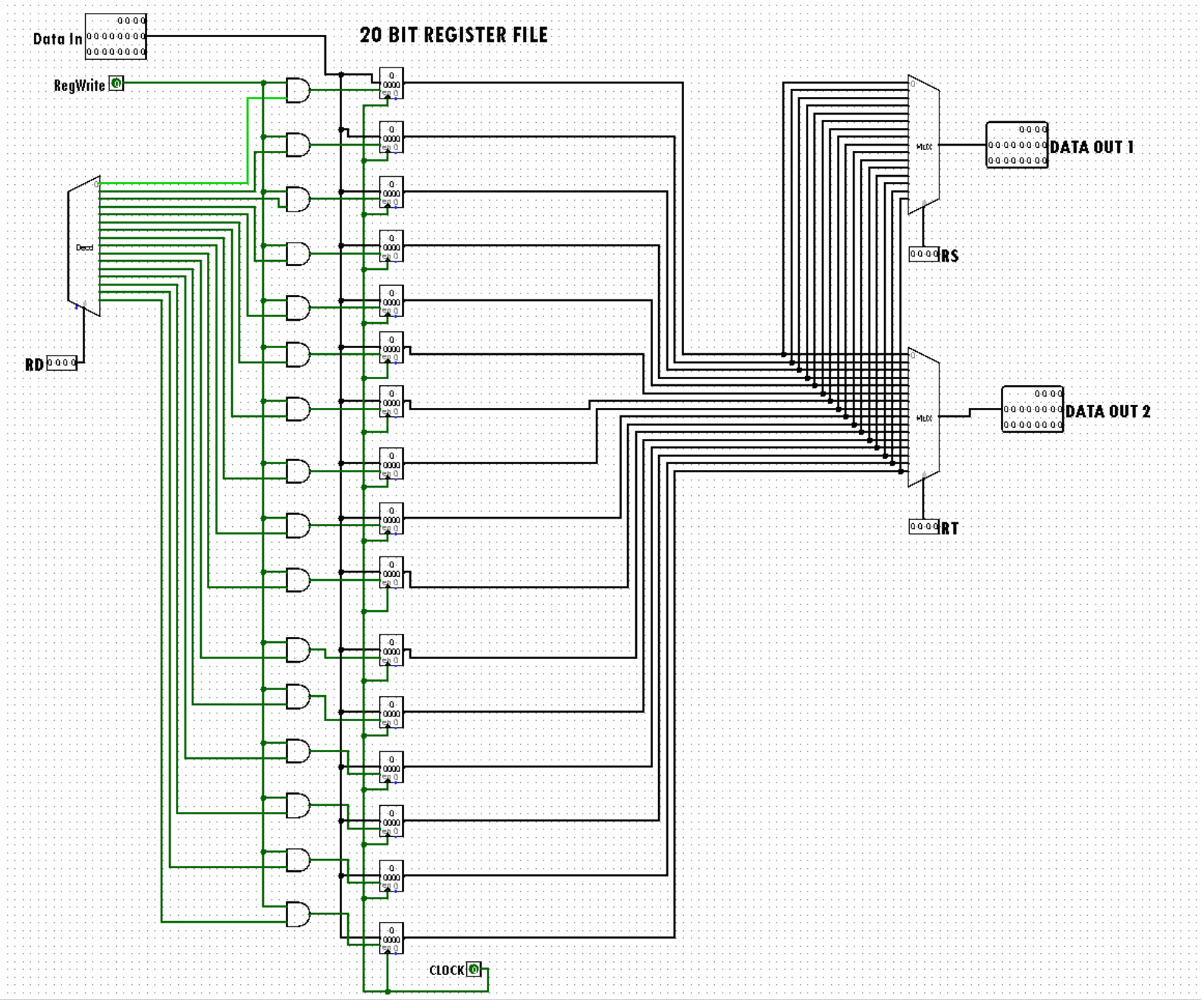


For I-type instruction: When the control unit receives the Opcode as '01' it recognizes it as an I-type instruction. Then it looks for further instruction code(s). As like R-type instruction in the control unit we have pre-defined the function codes (stated at table: 3) to carry out 4 I-type operation. The control unit sends signals for LW, SW, BEQ or BNE operations. The RegWrite & MemWrite signals are used here for executing LW and SW operation accordingly.

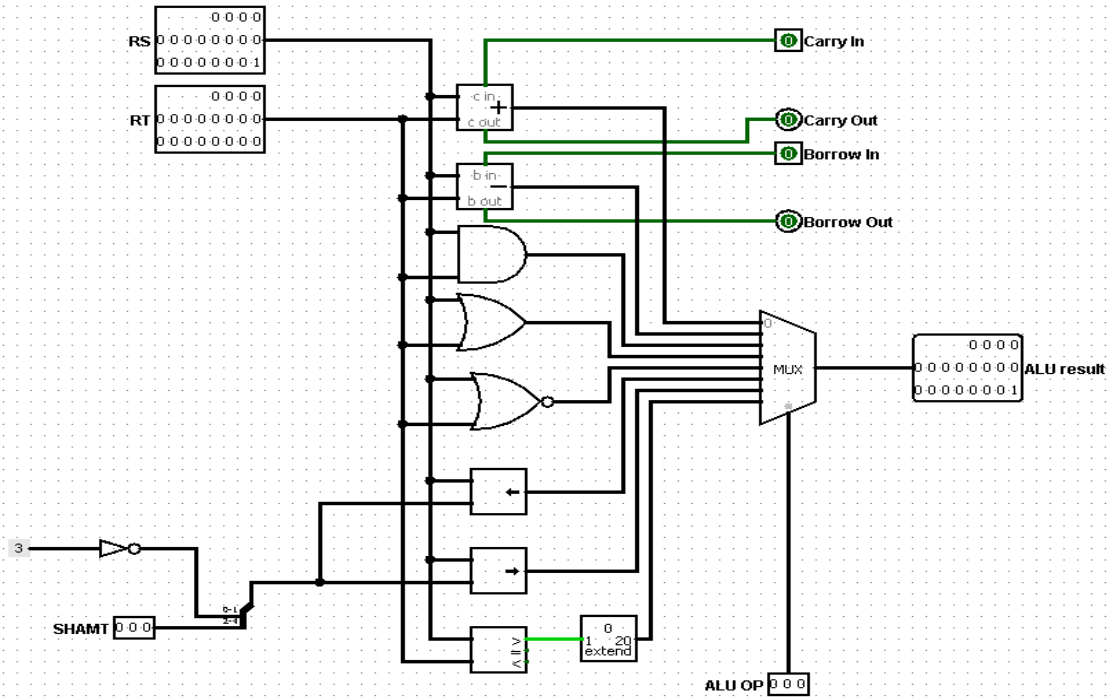
For J-type instruction: Here when the control unit gets opcode as '10' it recognized the operation as J-type operation and jumps as per the given address.

Screenshots:




20 BIT REGISTER FILE
Data In
RegWrite
Decd
RD
MUX
DATA OUT 1
RS
MUX
DATA OUT 2
RT
CLOCK

ARITHMATIC LOGIC UNIT



CONTROL UNIT