Design of Input/Output Buffer

ECE-611 (Memory Design and Test)
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INFORMATION TECHNOLOGY
DELHI

Problem Statement

- Scan chain on inputs, BIST mux, T bypass, input capacitance <15fF.
- Hold time: -ve at FF/1.32/-40 for all bits
- Setup time : To be within 500 ps at SS/1.08/125 for all bits.
- Implement a scan chain with 32 flip flops + 1 at the end.
- Sc_en signal controls if the data would be passed sequentially or loaded parallely.
- Mask Bit decides if we have to perform the ‘write’ or not.
- Test Mode has to be created to pass Test Data. Odd | Even pins.
- T_by-pass mode to check the functionality of any combinational logic at the output of the memory latch.
- Ensure the D-FF at the end (farthest from the clock) doesn’t contain a hold violation.

Challenges

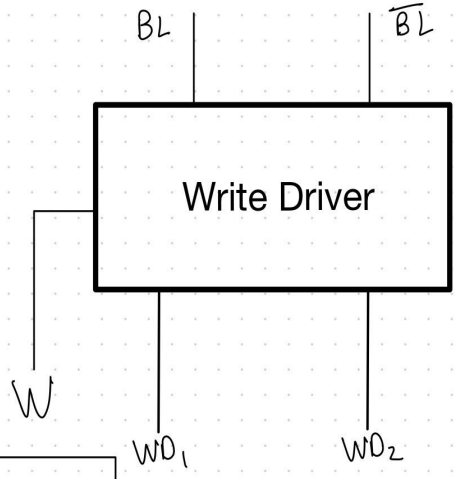
- How to use the masking-bit in a combinational logic with the data-bit, and how the output of this logic is to be used.
- Multiple MUX and Flip-Flop styles possible.
- Understanding BIST Mux, Bypass mode in memory and scan chain functionalities
- Understanding of Negative Hold Time
- Making Layout with minimal area, cleaning DRCs and LVS

WORKING

MASKING

W = 1

⇒ We are writing in the memory



BL is on Q

$\overline{BL}$ is on $\overline{Q}$

If D = = 1 :

we want to write 1 at Q

∴ Discharge $\overline{BL}$ to 0.

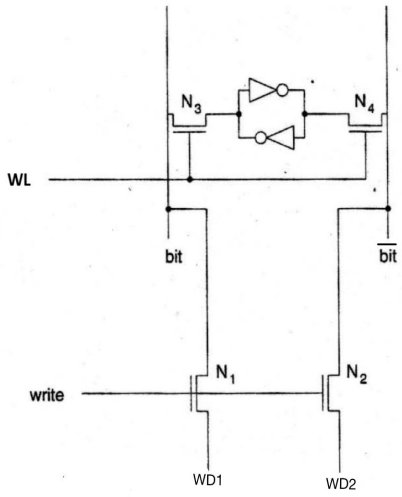
If D = = 0 :

we want to write 0 at Q . ∴ Discharge BL to 0.

M	D	WD_1	WD_2
0	0	1	0
0	1	0	1
1	0	1	1
1	1	1	1

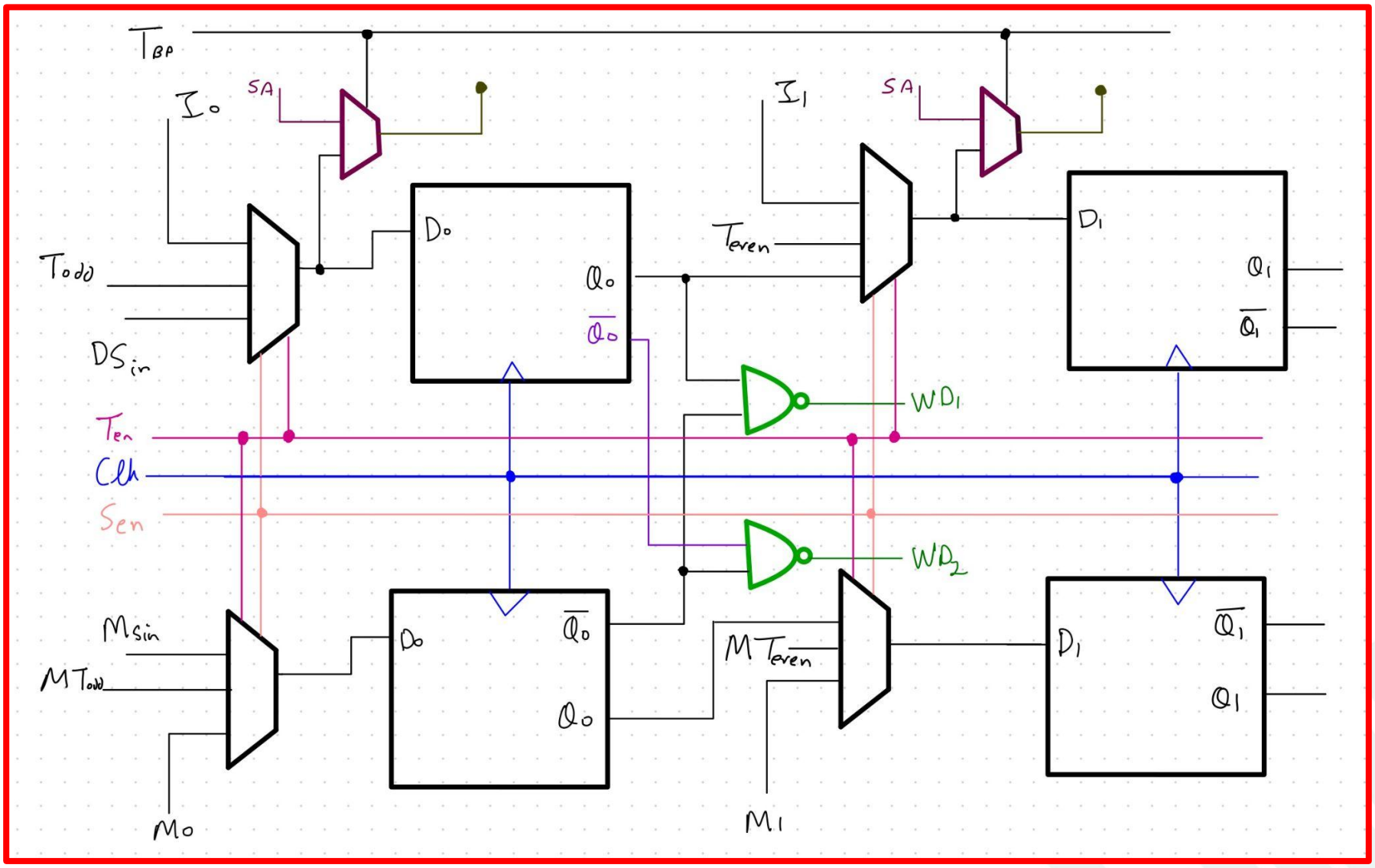
$$WD_1 = \overline{D\,\overline{M}}$$

$$WD_2 = \overline{\overline{D}\,\overline{M}}$$

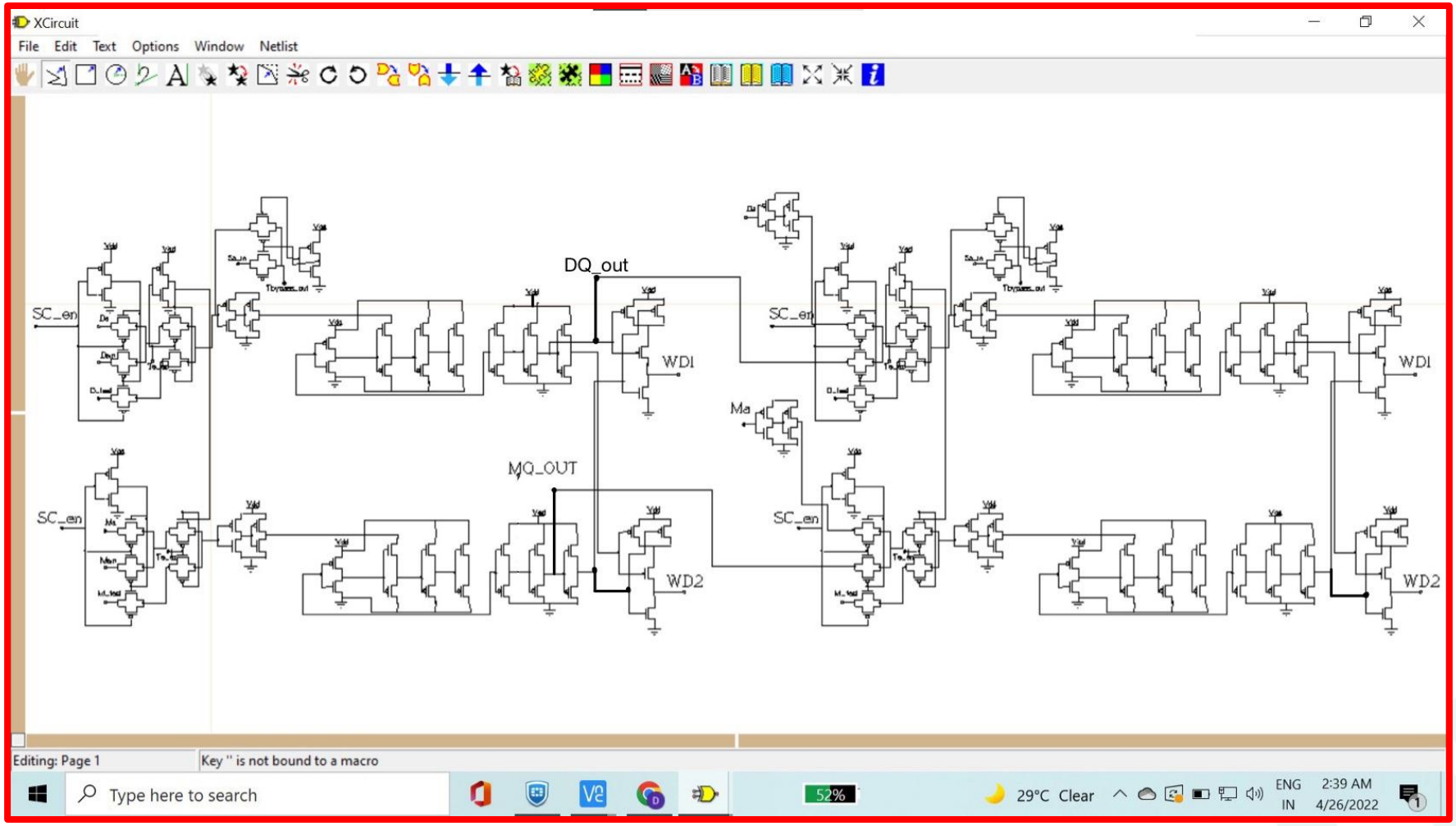


DESIGN SCHEMATIC

OVERVIEW

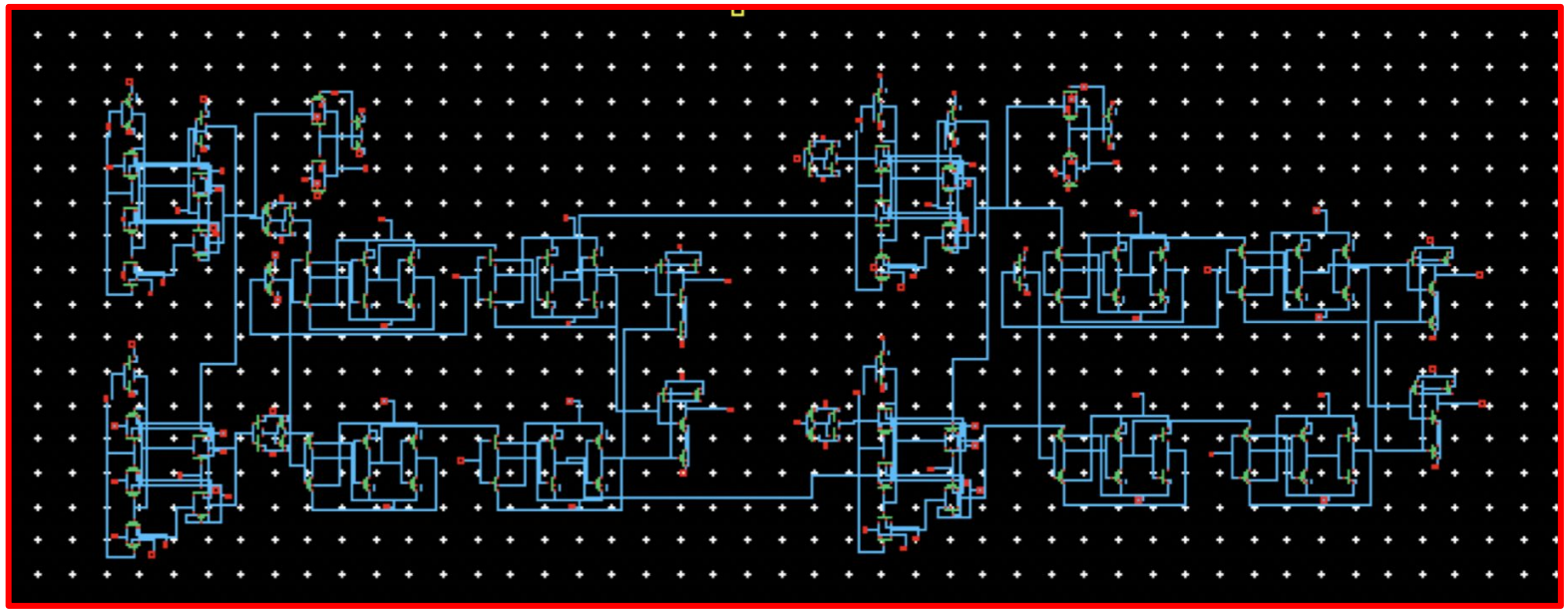

TBP
I0
SA
I1
SA
Todd
Teven
DS in
D0
Q0
Q0
D1
Q1
Q1
Ten
Clk
Sen
WD1
WD2
Msin
MTodd
M0
D0
Q0
Q0
MTeven
M1
D1
Q1
Q1

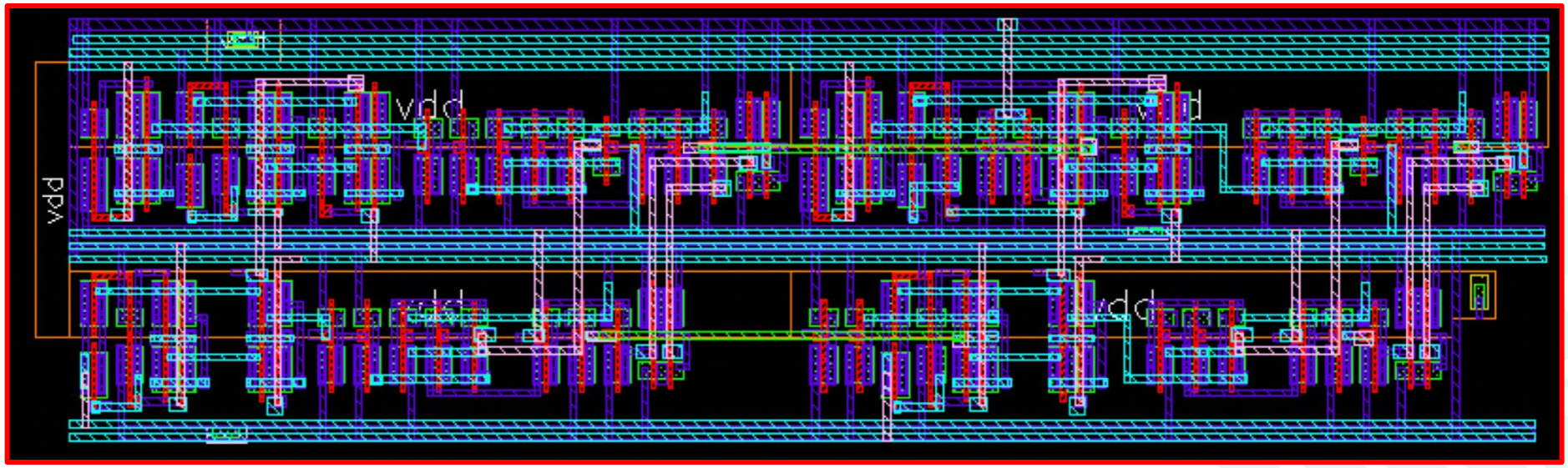
X- CIRCUIT

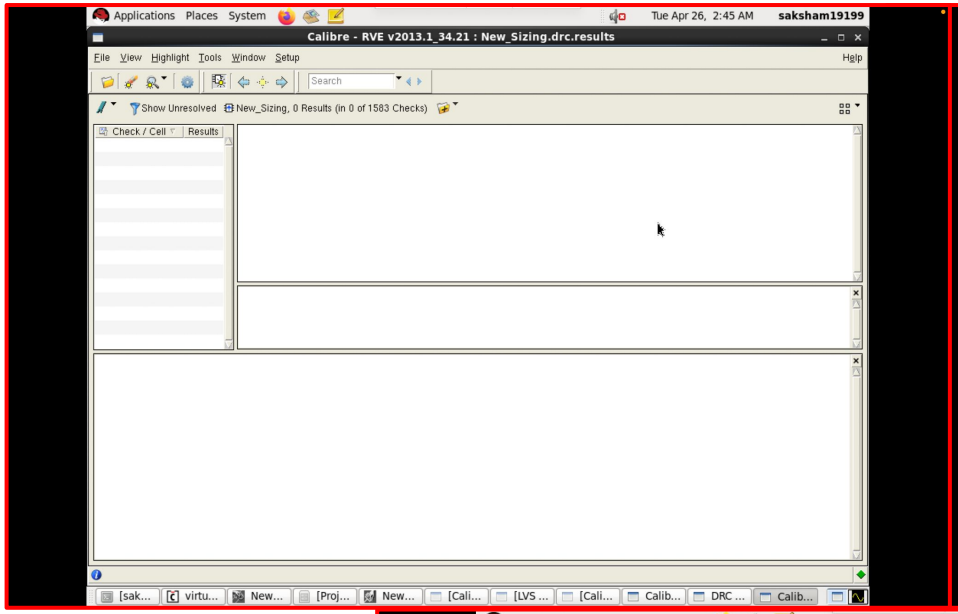


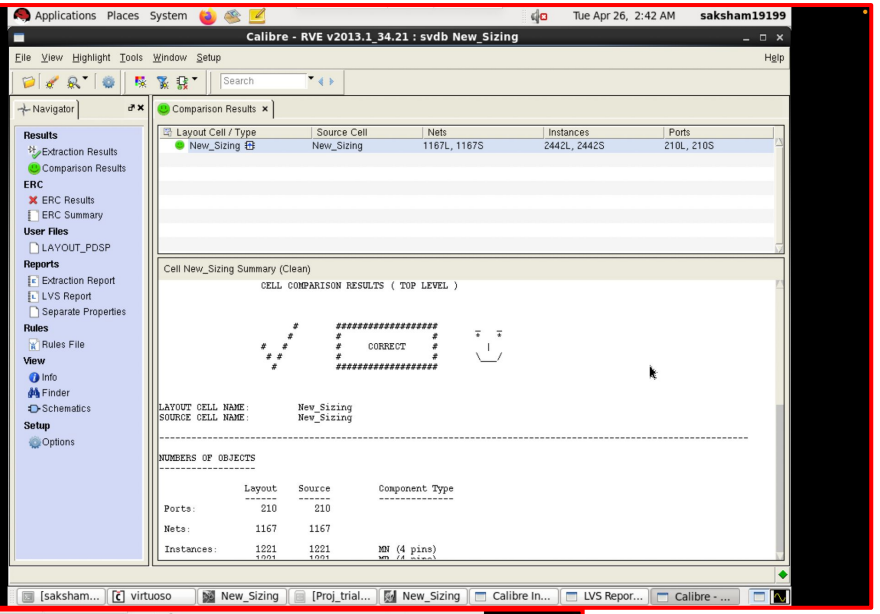
TG (Pmos, Nmos): 0.675, 0.675
NAND(Pmos, Nmos): 0.27, 1.35
Inverter(Pmos, Nmos): 0.27, 0.135
Flip Flop(Pmos, Nmos): 0.27, 0.54

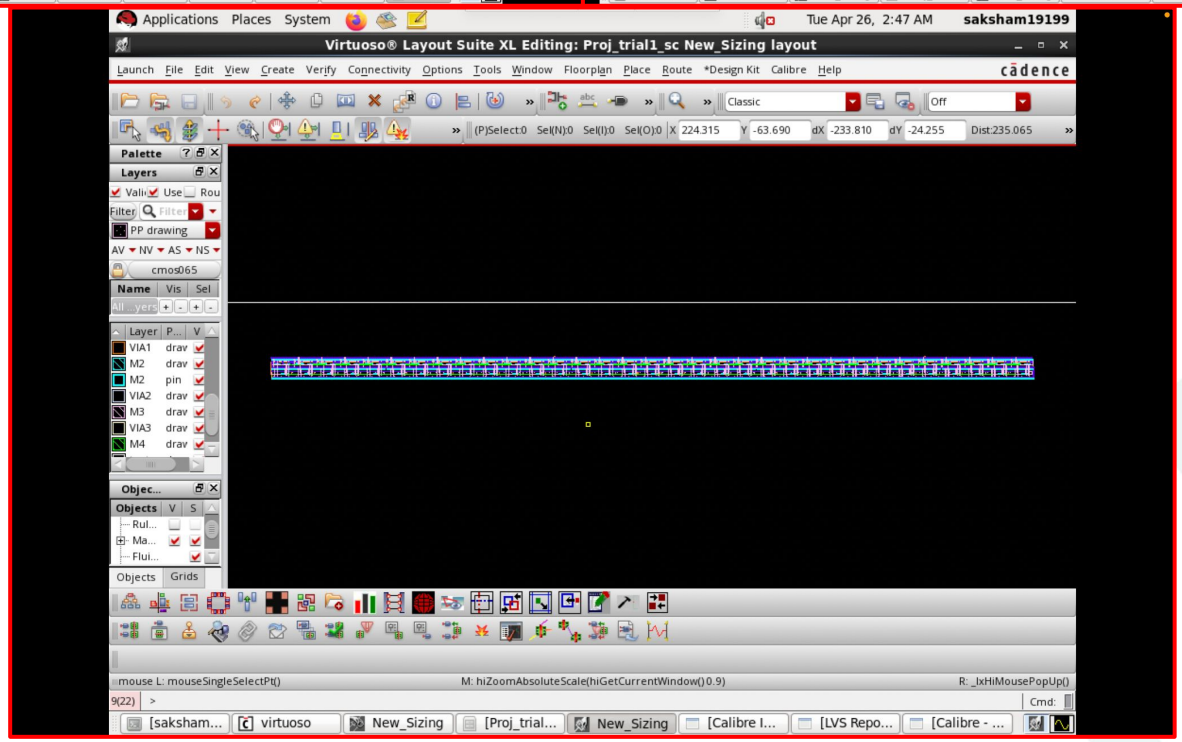
Virtuoso Layout and Schematic (2 Cells)



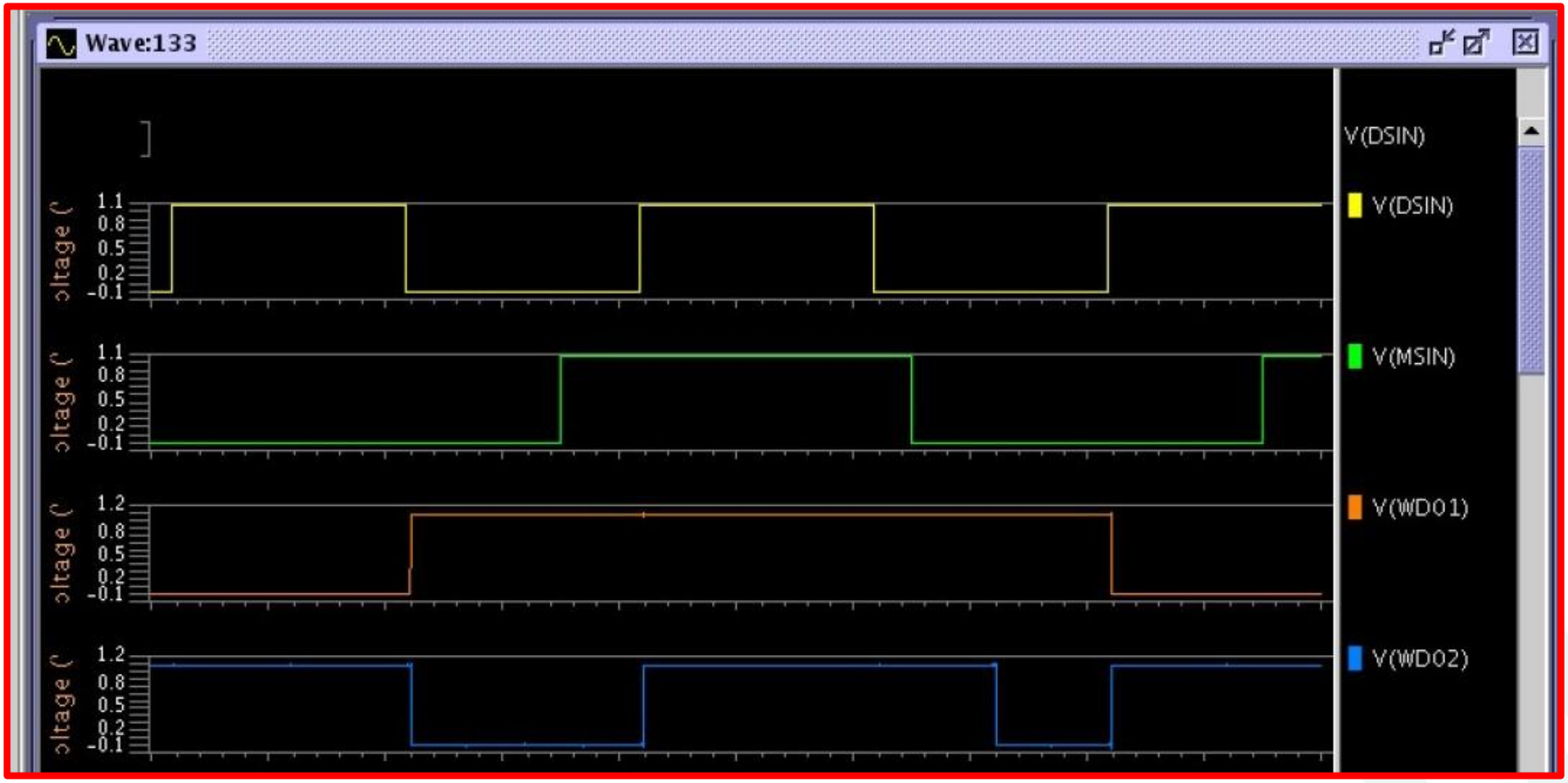



Applications Places System
Tue Apr 26, 2:45 AM saksham19199
Calibre - RVE v2013.1_34.21 : New_Sizing.drc.results
File View Highlight Tools Window Setup Help
Show Unresolved New_Sizing, 0 Results (in 0 of 1583 Checks)
Check / Cell Results

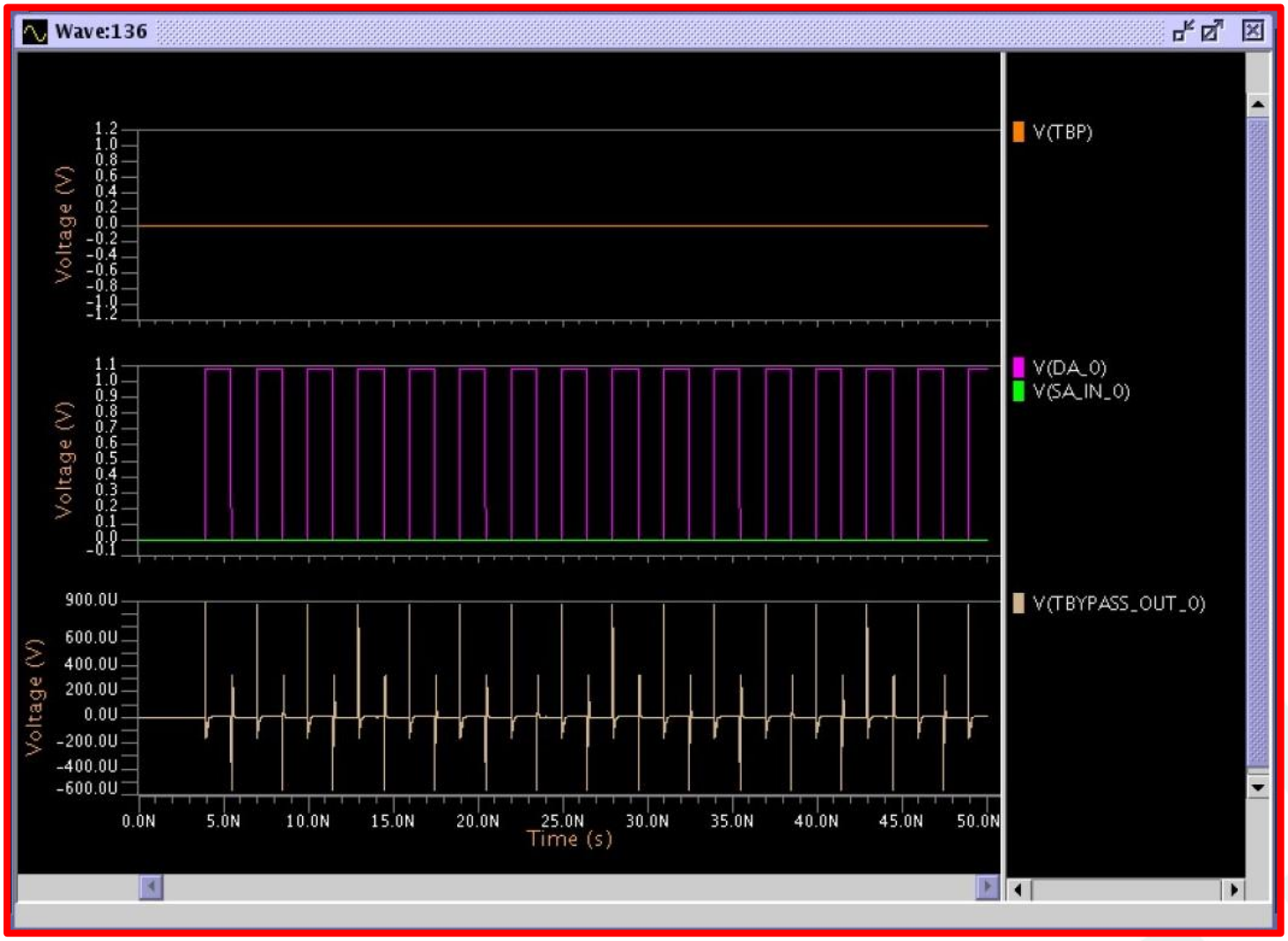

Applications Places System
Tue Apr 26, 2:42 AM saksham19199
Calibre - RVE v2013.1_34.21 : svdb New_Sizing
File View Highlight Tools Window Setup Help
Navigator
Comparison Results
Results
Extraction Results
Comparison Results
ERC
ERC Results
ERC Summary
User Files
LAYOUT_PDSP
Reports
Extraction Report
LVS Report
Separate Properties
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Layout Cell / Type
Source Cell
Nets
Instances
Ports
New_Sizing
New_Sizing
1167L, 1167S
2442L, 2442S
210L, 210S
Cell New_Sizing Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: New_Sizing
SOURCE CELL NAME: New_Sizing
NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 210 210
Nets: 1167 1167
Instances: 1221 1221 MN (4 pins)


Applications Places System
Tue Apr 26, 2:47 AM saksham19199
Virtuoso® Layout Suite XL Editing: Proj_trial1_sc New_Sizing layout
Launch File Edit View Create Verify Connectivity Options Tools Window Floorplan Place Route *Design Kit Calibre Help
cadence
Palette
Layers
PP drawing
cmos065
Name Vis Sel
Layer P... V
VIA1 drav
M2 drav
M2 pin
VIA2 drav
M3 drav
VIA3 drav
M4 drav
Objec...
Objects V S
Objects Grids
mouse L: mouseSingleSelectPt()
M: hiZoomAbsoluteScale(hiGetCurrentWindow() 0.9)
R: _lxHiMousePopUp()
Cmd:

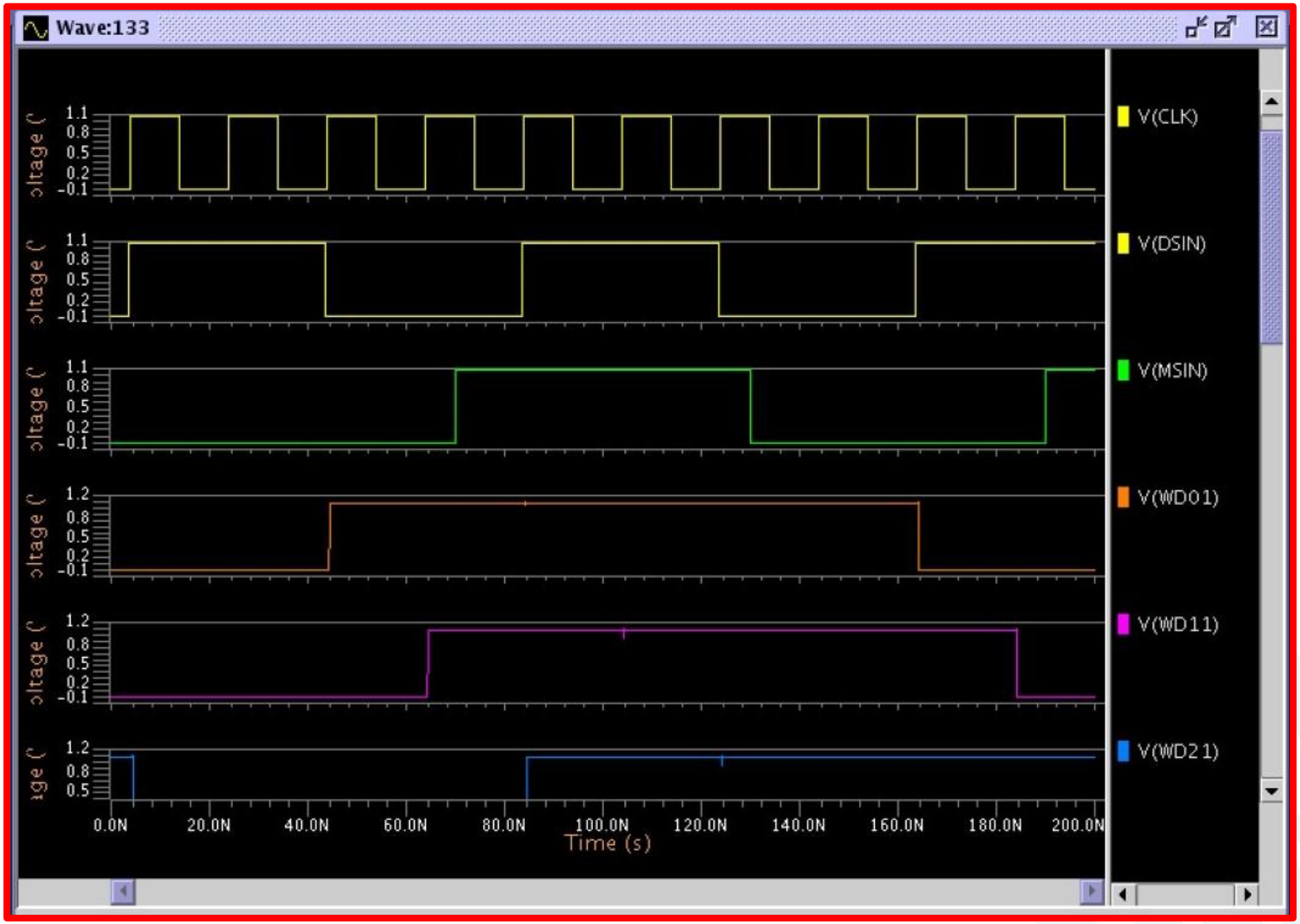
Masking

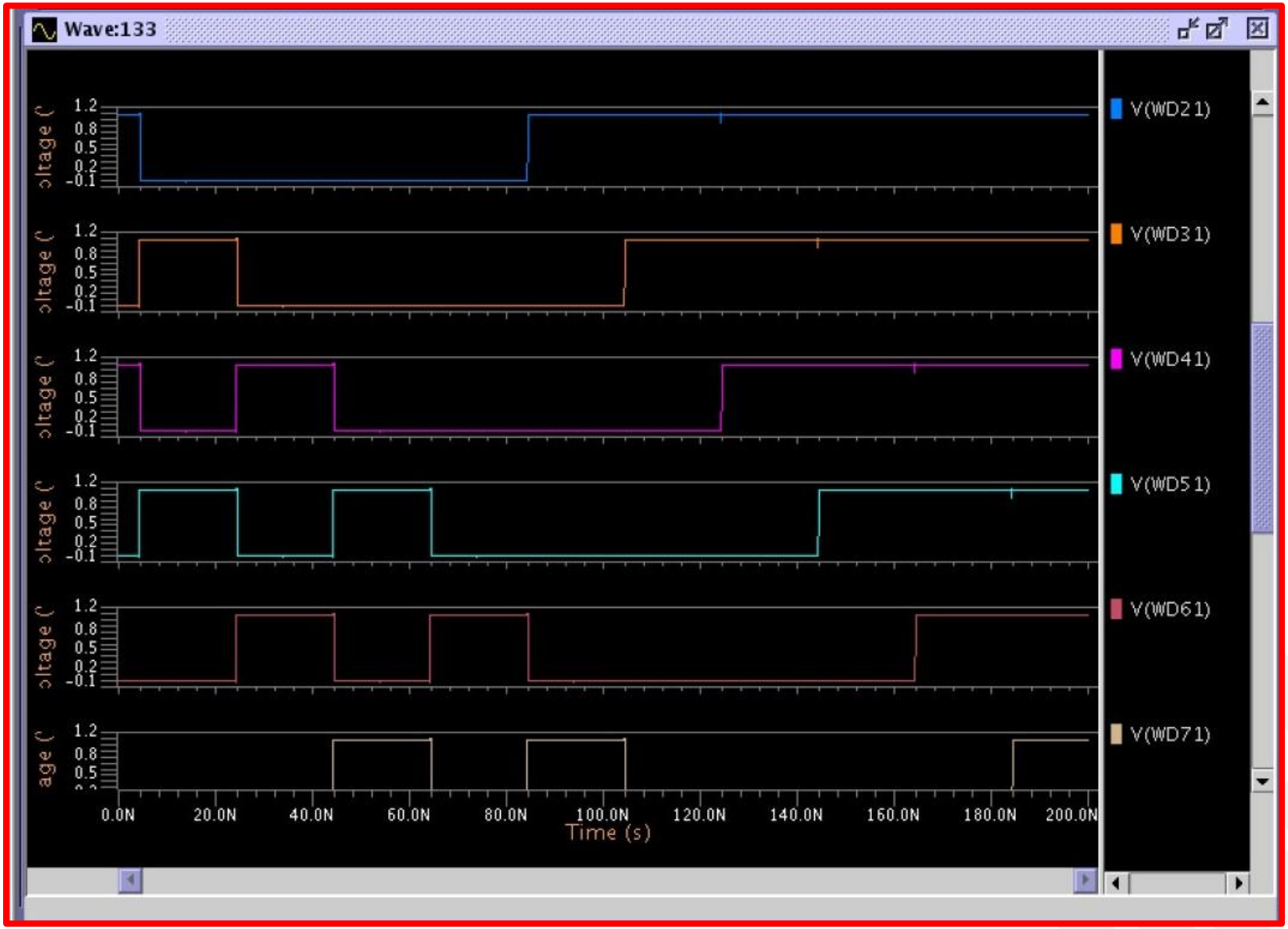

Wave:133
V(DSIN)
V(DSIN)
V(MSIN)
V(WD01)
V(WD02)
1.1
0.8
0.5
0.2
-0.1
1.2
0.8
0.5
0.2
-0.1

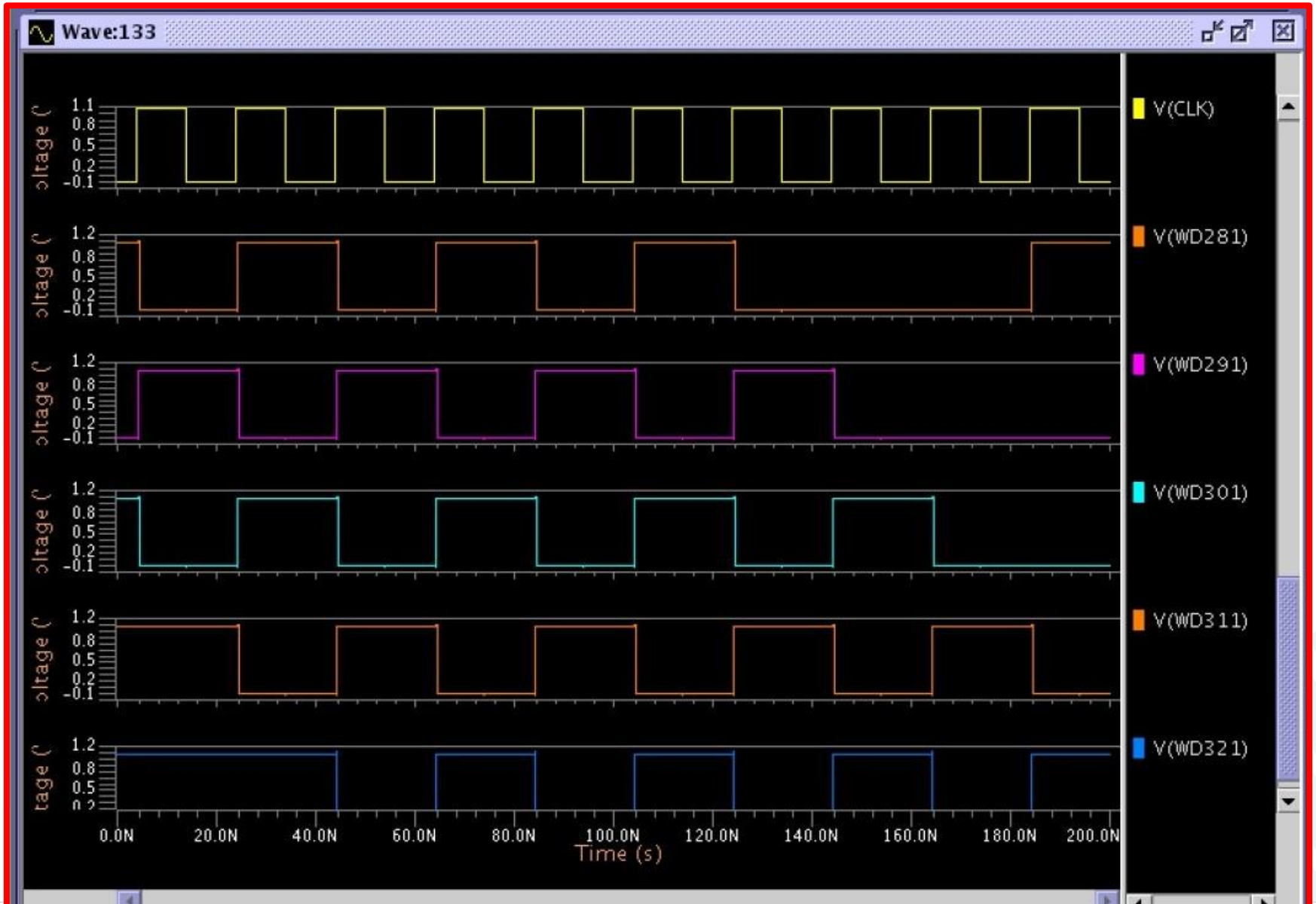
T_by_Pass Disabled



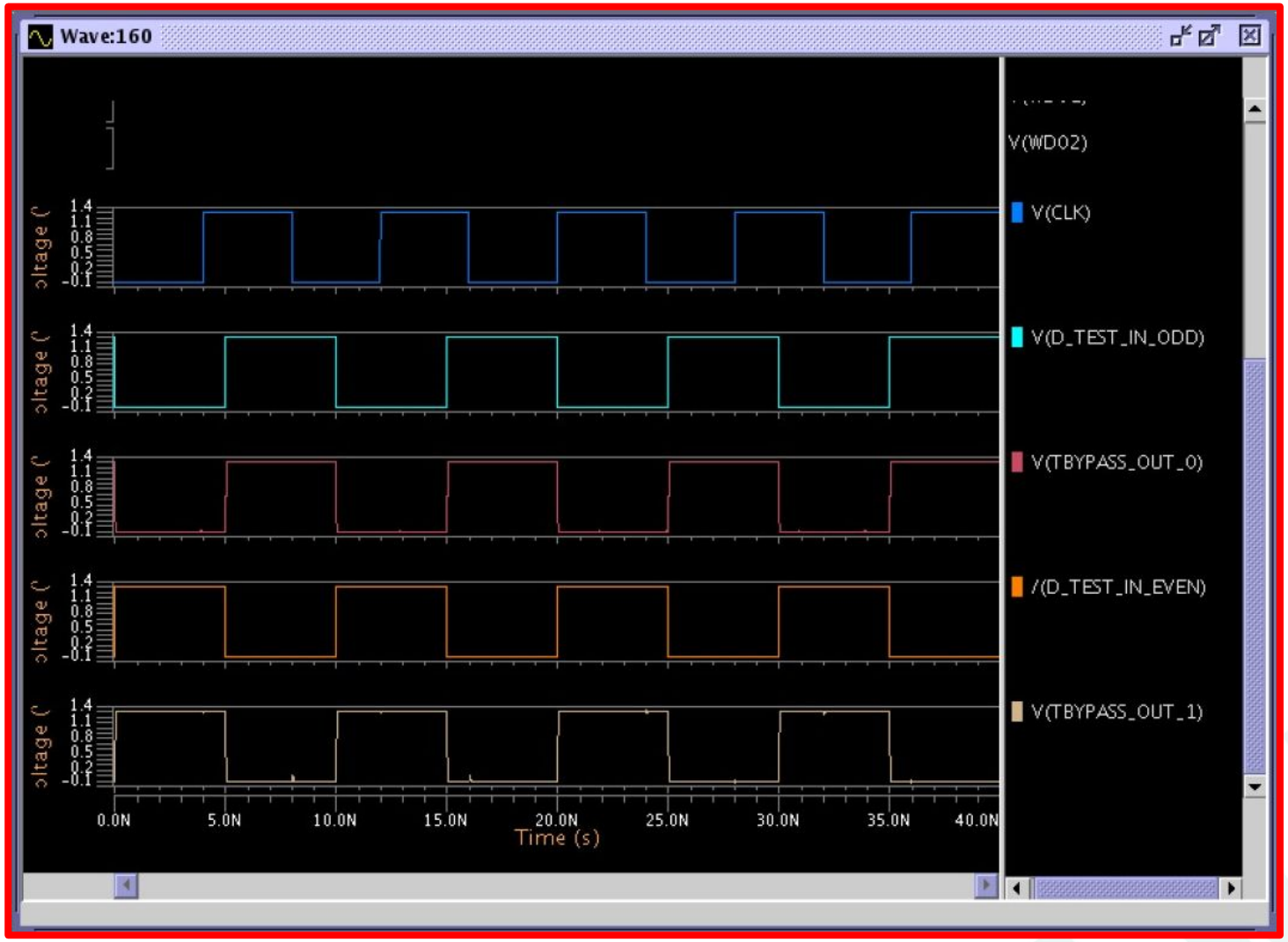
Scan Mode Propagation of WD Signal



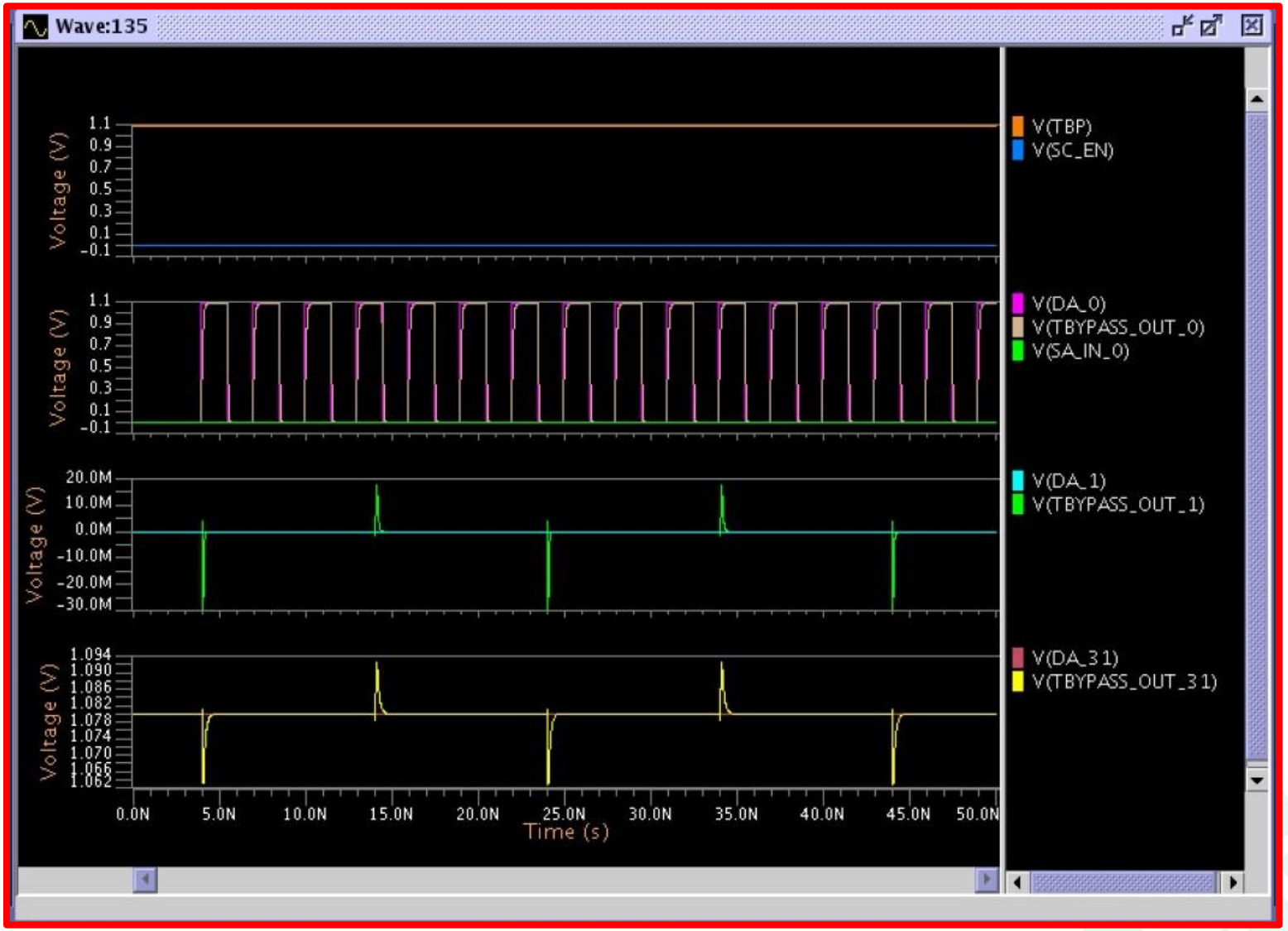

Wave:133
V(WD21)
V(WD31)
V(WD41)
V(WD51)
V(WD61)
V(WD71)
1.2
0.8
0.5
0.2
-0.1
0.0N
20.0N
40.0N
60.0N
80.0N
100.0N
120.0N
140.0N
160.0N
180.0N
200.0N
Time (s)


Wave:133
V(CLK)
V(WD281)
V(WD291)
V(WD301)
V(WD311)
V(WD321)
1.1
0.8
0.5
0.2
-0.1
1.2
0.8
0.5
0.2
-0.1
0.0N
20.0N
40.0N
60.0N
80.0N
100.0N
120.0N
140.0N
160.0N
180.0N
200.0N
Time (s)

TEST ENABLE: EVEN-ODD PINS



T_by_Pass and Parallel Loading



Verification Plan

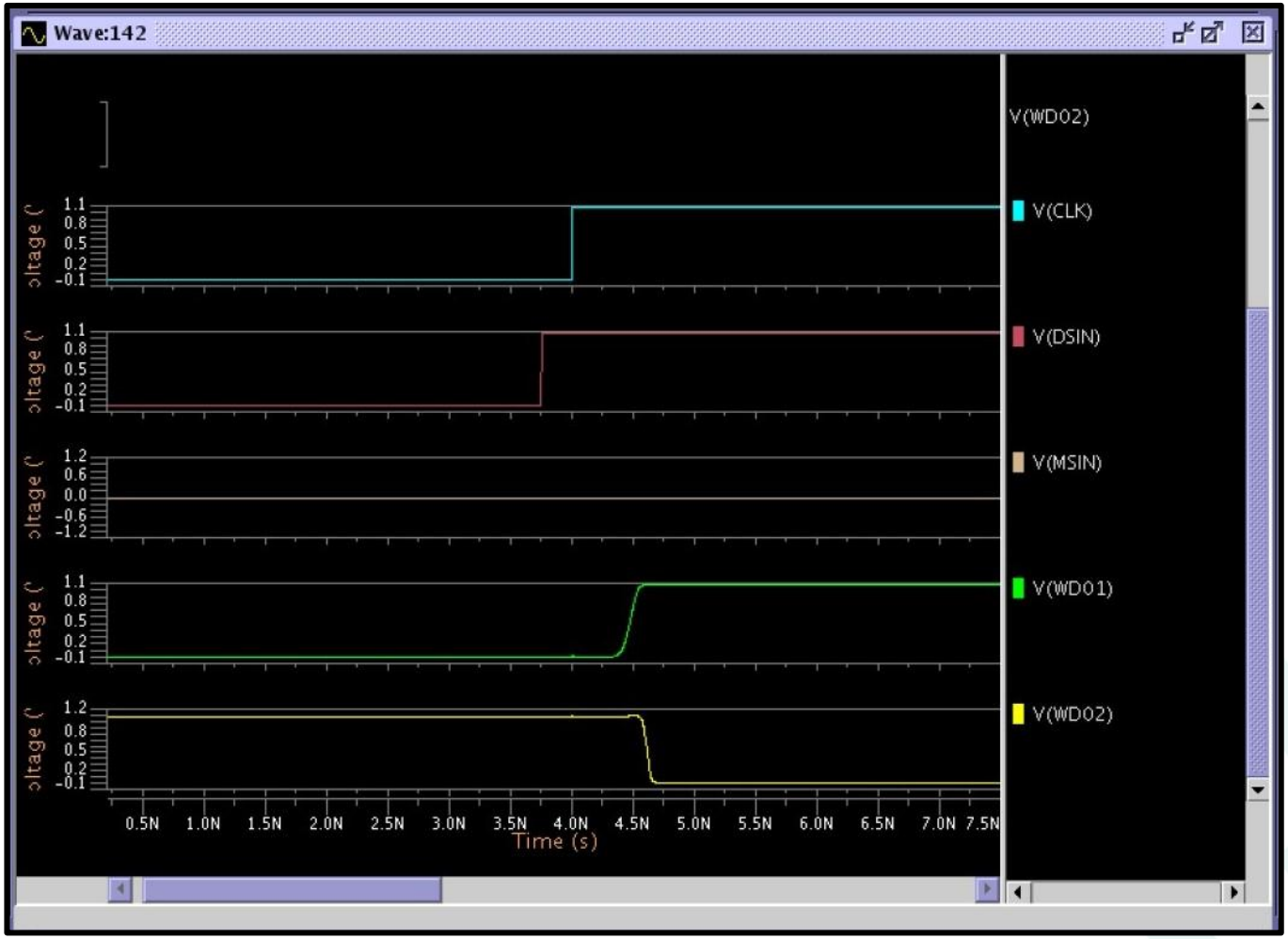
- SS, 1.08, 125 for Setup Time || FF, 1.32, -40
- CRC Pi model on the clock for the last flip flop.
- **Results that you need to measure**
  - Setup Time to be less than 500ps: 255ps
  - Hold Time -ve: -40ps
  - Clk → Wd delay: 60ps
  - Cell Area: 5.8 X 11= 63.8u^2

- Cell refers to [Mux2, 2-Mux3, 2-Flip Flops, 2 Nand Gates]
- We have 33 such cells in out design.
- Tested Functionality of :-
  - Sc_en Mux
  - T-by_pass Mux
  - D- Latch
  - Mask Comb Logic
  - Combination of all these individual elements.

RESULTS

Setup Time : SS || 1.08 || 125

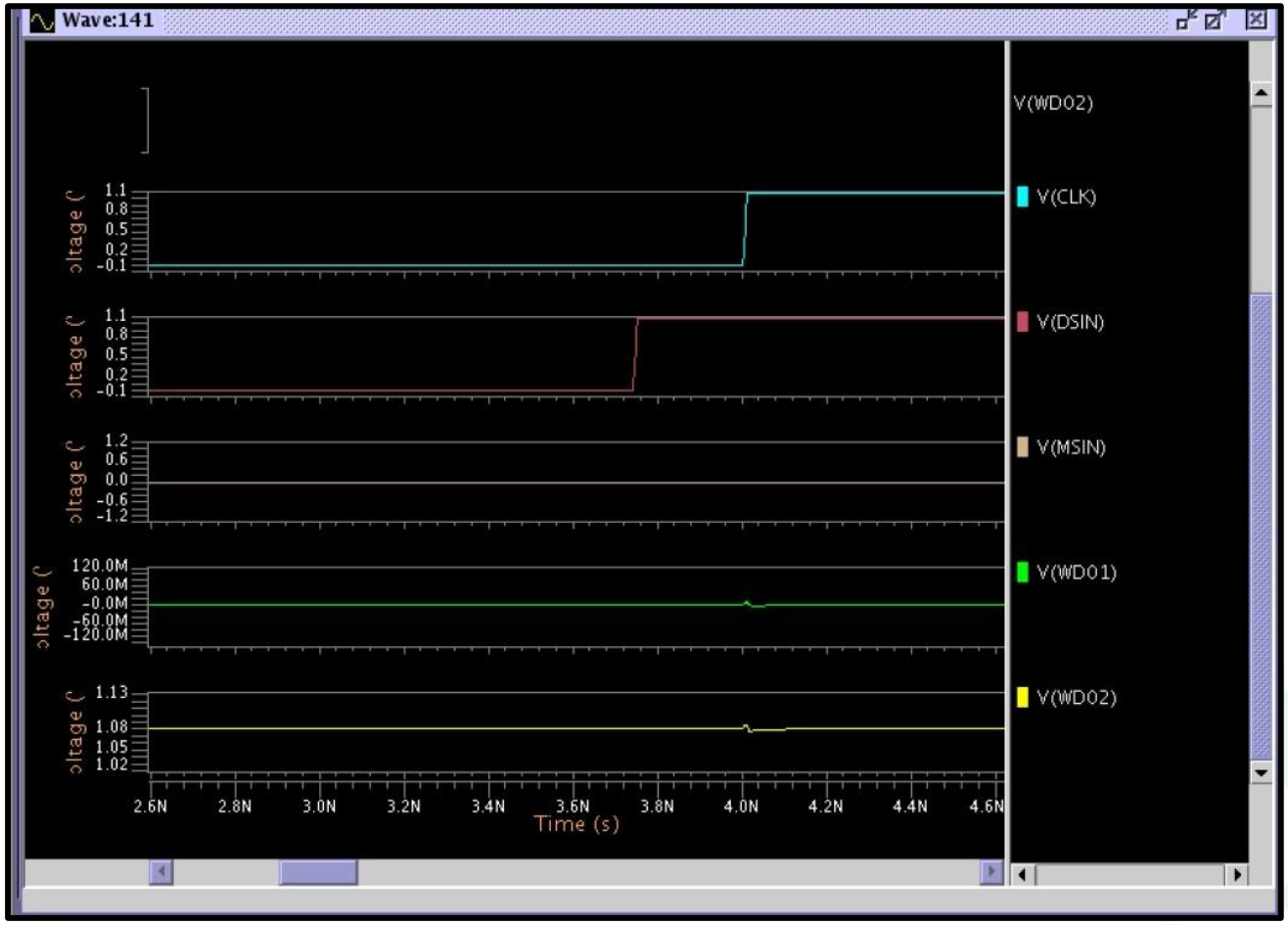
Data transitions 250ps before the clock edge.



Setup Violated

Setup Time : SS || 1.08 || 125

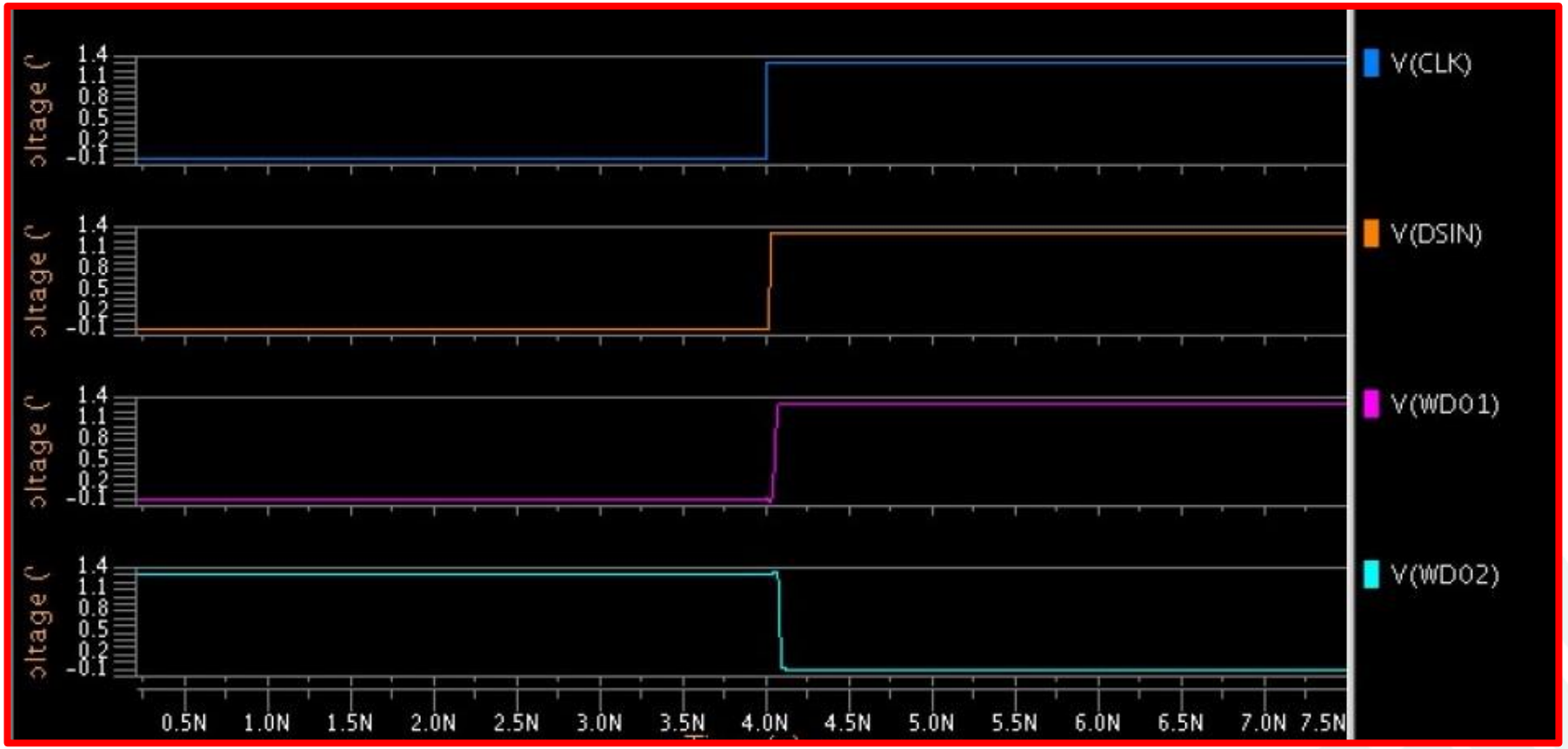
Data transitions 260ps before the clock edge.



Setup much within 500ps (255ps)

Hold Time : FF || 1.32 || -40

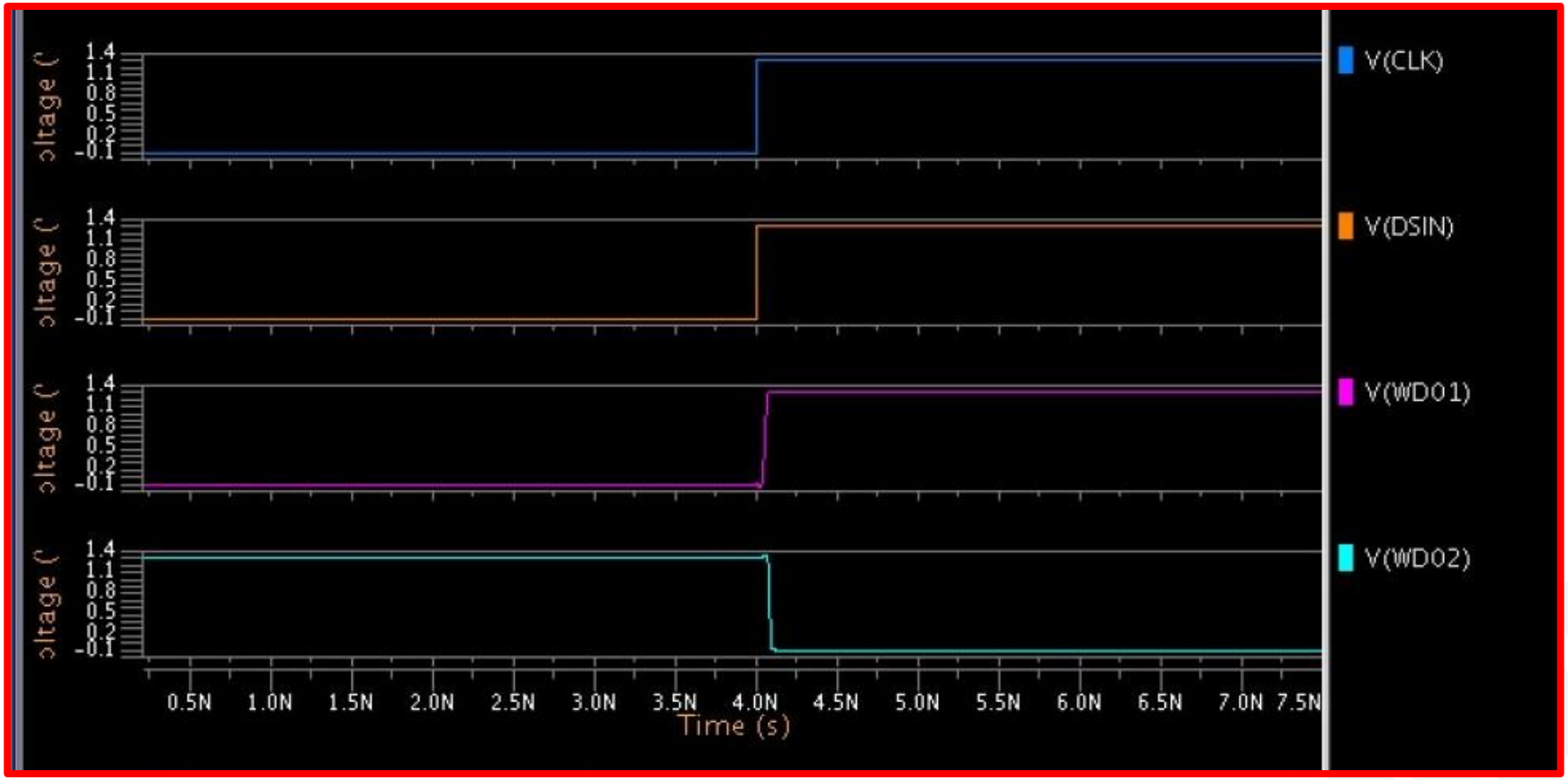
Data Transitions 20ps after the clock edge.



No Violation

Hold Time : FF || 1.32 || -40

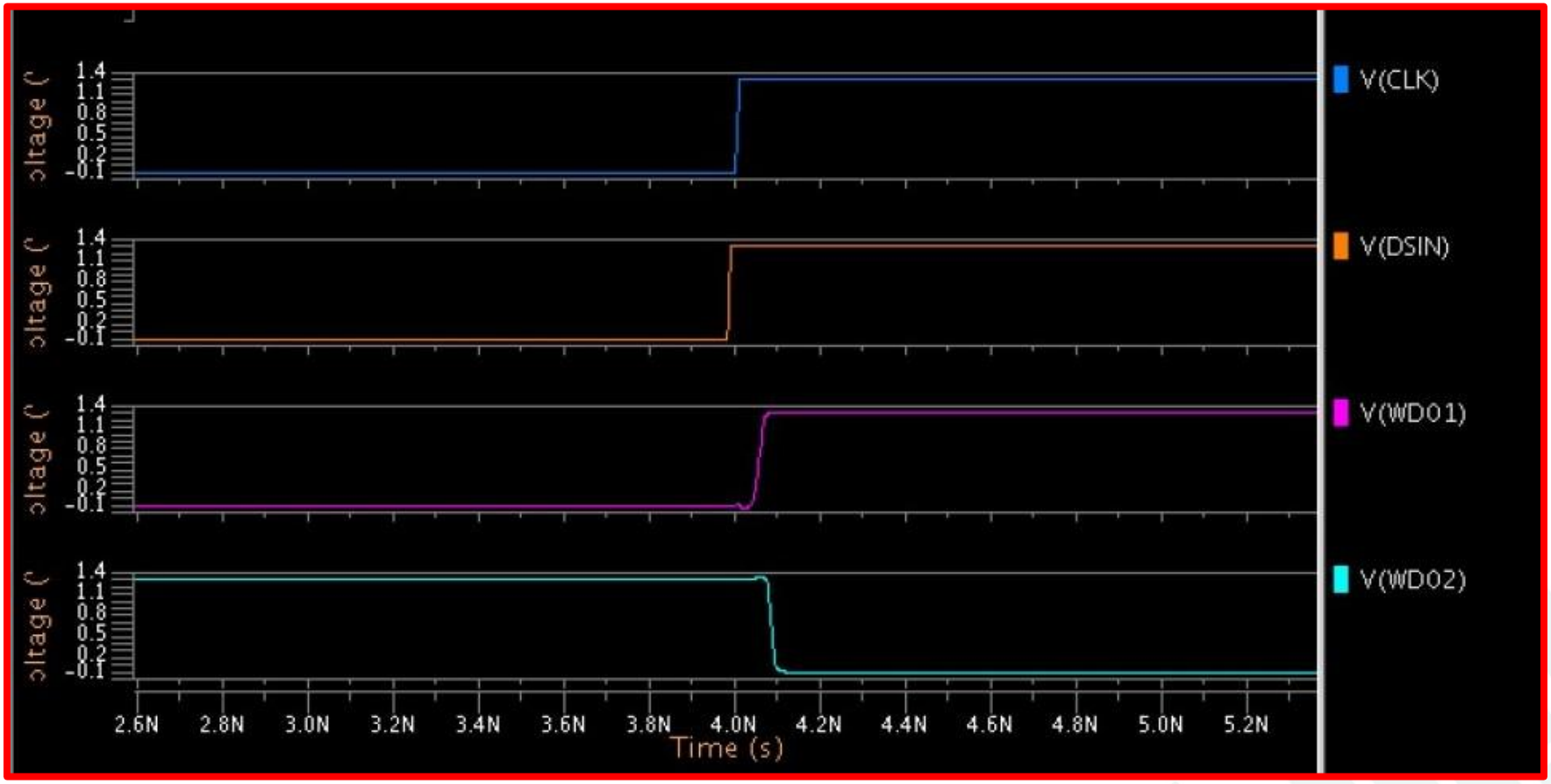
Data Transitions along with clock edge.



No Violation

Hold Time : FF || 1.32 || -40

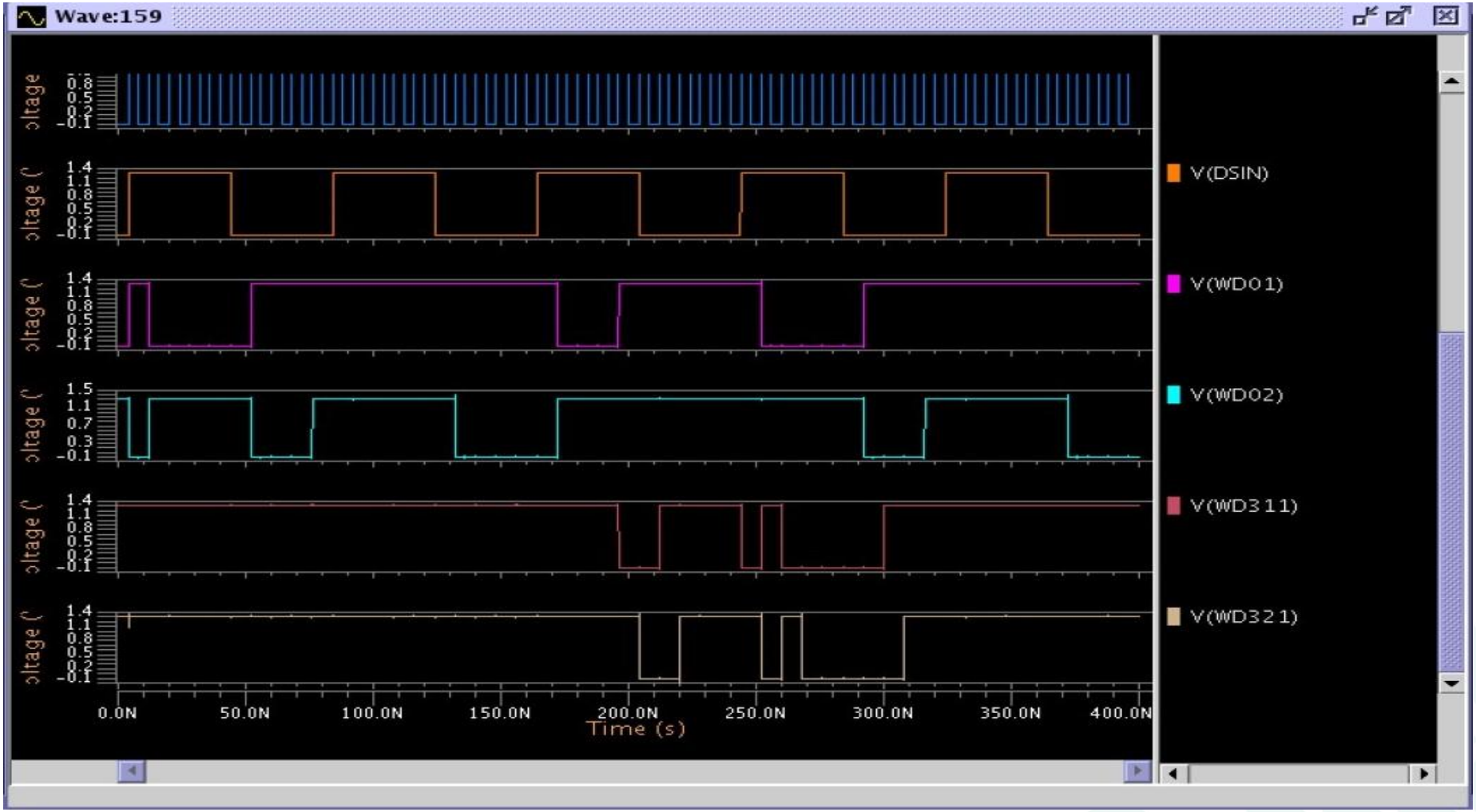
Data Transitions 40ps before the clock edge.



No Violation

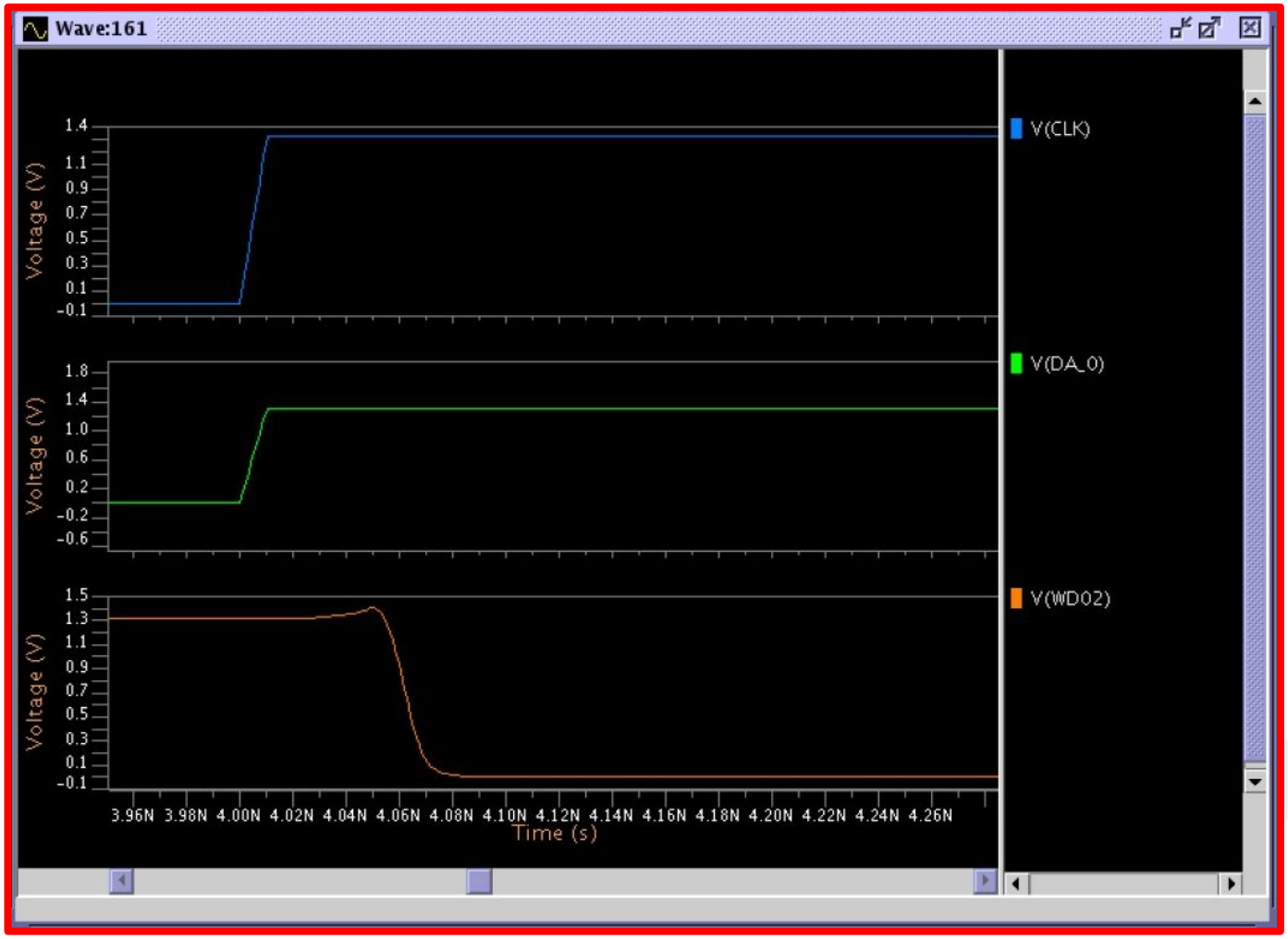
Hold Time : FF || 1.32 || -40

Data Transitions 40ps before the clock edge.



No Violation

CLK → WD DELAY



~60ps : 50% (rise) < – > 50% (fall)

Conclusions and Future Plans

- Technical Conclusions
  - Worked: Functionality and Specification of the design.
  - Didn’t Work: Metal Layers, Area Optimization, Multiple Designs.
  - Answer the Whys?
- Emphasise on learning from the project
  - Gained knowledge about the various Testing Infrastructures
    - More elaborate design with multiple metal layers and longer rails.
  - Creating instances, repeating units and doing smart work.
- Future plans
  - We can try another model in which we use only one scan chain and use combinational logic to evaluate ‘masking’ before. Would lead to an increase in set-up time but reduction of area.
- Special Thanks to Belal Sir for constant guidance and support

References

- https://www.researchgate.net/figure/Transmission-gate-based-41-MUX_fig5_257799438
- https://www.researchgate.net/figure/21-MUX-using-CMOS-logic-only_fig4_349211497
- https://www.electronics-tutorial.net/Digital-CMOS-Design/Pass-Transistor-Logic/4-1-multiplexer-using-CMOS-logic/
- https://www.ijtsrd.com/papers/ijtsrd30554.pdf
- https://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.84.6254&rep=rep1&type=pdf
- https://www.researchgate.net/publication/320065130_Schematic_Design_and_Layout_of_Flipflop_using_CMOS_Technology