A report on

Custom Layout and Schematic Design of a Multi-fingered CMOS inverter for driving a load capacitance of 1pF

By

Akshit Goel	**2016A3PS0317P**
Saksham Consul	**2016A8PS0424P**
Nishad Sahu	**2016A3PS0215P**

Submitted in partial fulfillment of the course

EEE F313/ INSTRF313 – Analog & Digital VLSI Design

Under the Guidance of

Prof. Anu Gupta
Instructor In-charge *EEE F313/ INSTR F313*
EEE Department, BITS Pilani, Pilani Campus

Birla Institute of Technology and Science, Pilani

August- September 2018

Acknowledgement

We would like to thank Dr. Anu Gupta, Dr Nitin Chaturvedi and the entire ADVD team for their constant guidance and support in the project work.

We are also thankful to the TAs; Siddhant Gangwal, Raveesh Garg and Mohit Garg for their help with software related issues and understanding of the various protocols.

Contents

1. **Problem Statement and Interpretation**

Design a CMOS Inverter at 500MHz with load capacitance of 10pF.
(a)Plot the energy and delay graph.
(b)Plot the short circuit and switching power graph.
Model File – tsmc018 (180nm technology)
Supply voltage – 1.8 V

.

Interpretation –

CMOS inverter is the best topology for achieving high voltage swing and minimum delay because of the combination of complementary Pull up and Pull down network. This is why it is one of the most used topology in ICs all over the world. The specification of the inverter given in the question has high frequency as well as a high capacitive load. Initial pen-paper calculations and simulation have yielded a (W/L)p ratio of around 600 using 180 nm technology. So, as it will lead to around 30 fingers which can be cumbersome for the layout, in consultation with course IC Prof. Anu Gupta we decided to work with 1pF capacitor load.

2. Calculation of design parameters

a. Approximation of Wp/Wn for equal drive capability

Concept Used:

- Maximum drive current is at threshold switching voltage which is at Vdd/2 for a CMOS with equal drive capability
- $T_{PHL} = T_{PLH}$ at equal drive capability

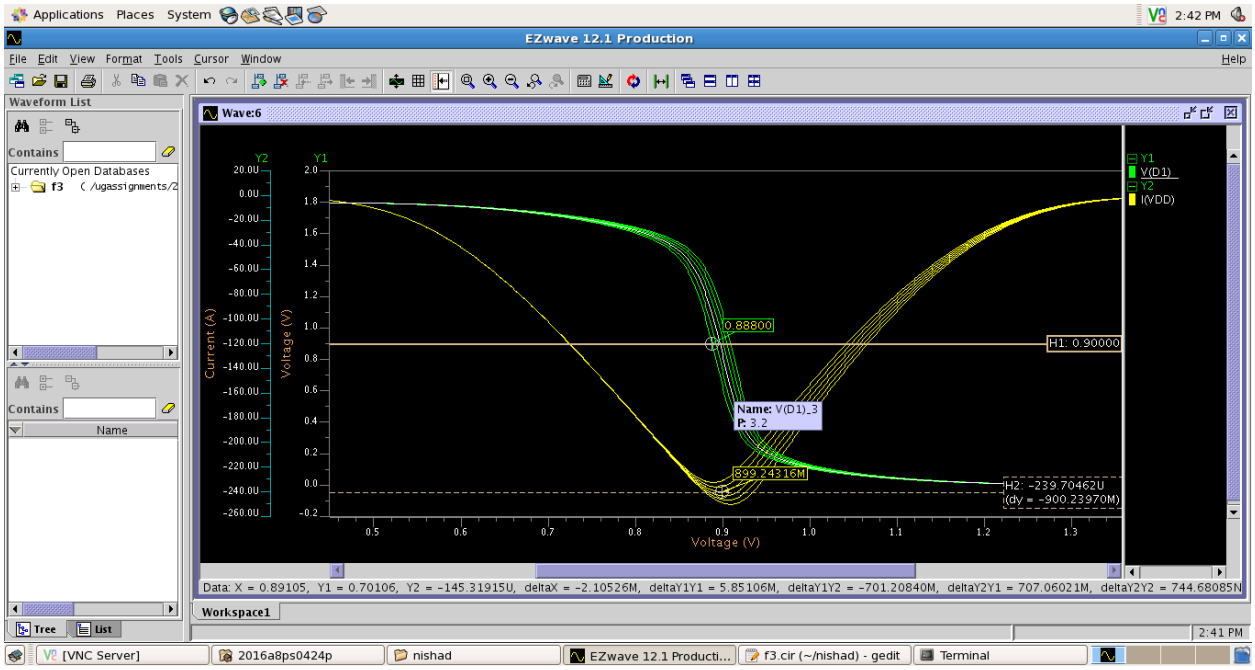


Fig 1: Initial value for Wp/Wn obtained is 3.2

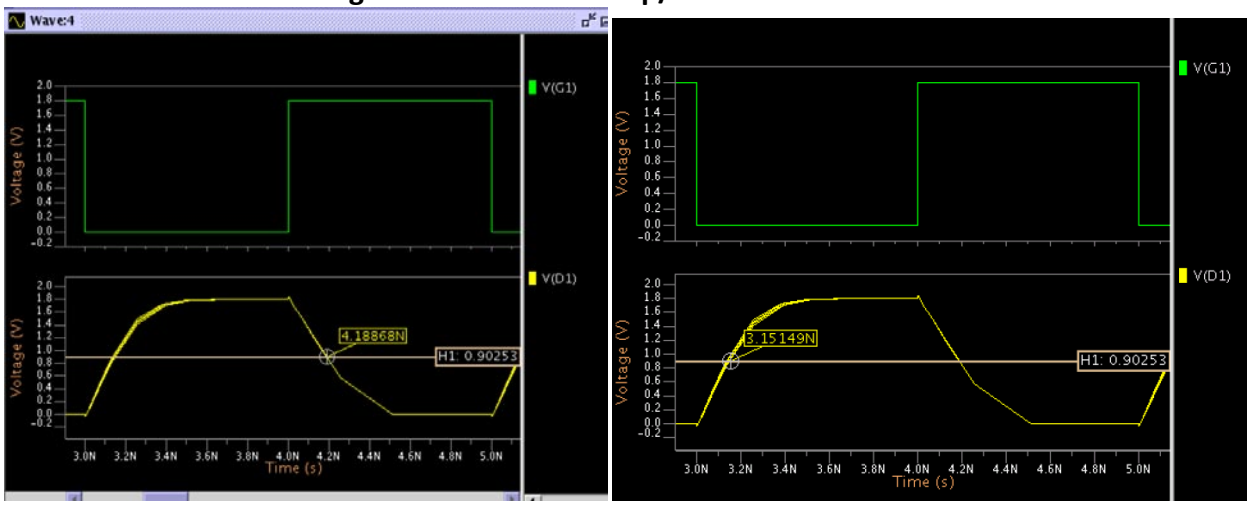


Fig 2: Delay analysis using Wp/Wn =3.2 , (W/L)n=50

From figure 1
T_{PHL} = 0.19 ns (NMOS ‘ON’)
T_{PLH} = 0.15 ns (PMOS ‘ON’)

So, the drive capability of NMOS is less so we need to increase Wn, keeping Wp same. Our final aim is to achieve delay = 0.15 ns which is 7.5 % of the time period, so we increase Wn to 10800N i.e (W/L)n=60.

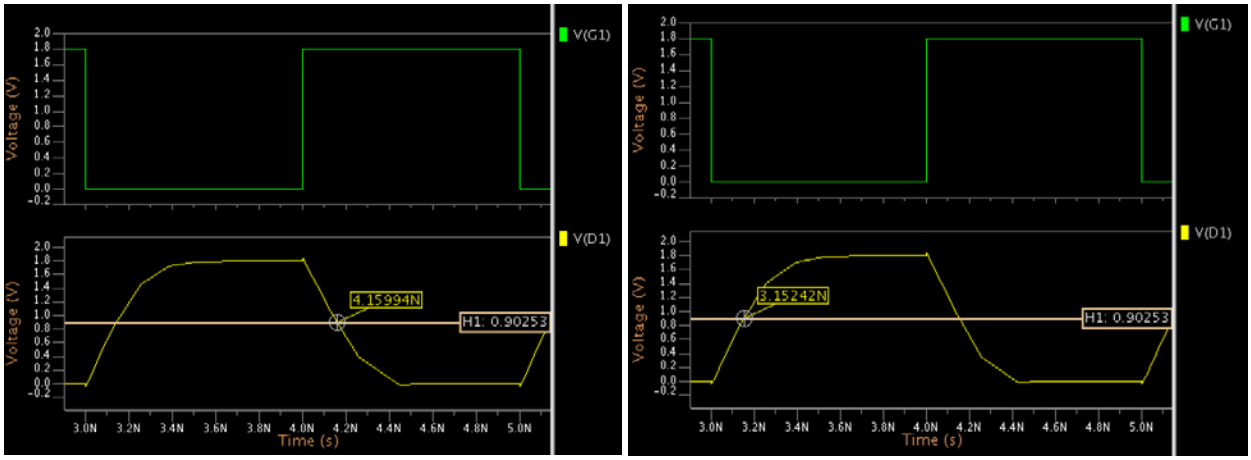


Fig 3: Delay analysis using Wp/Wn =2.67 , (W/L)n=60

From figure 3
T_{PHL} = 0.16 ns (NMOS ‘ON’)
T_{PLH} = 0.15 ns (PMOS ‘ON’)

So, the drive capability of NMOS is still slightly less. So we need to increase Wn and decrease Wp in order to avoid large diffusion area size.

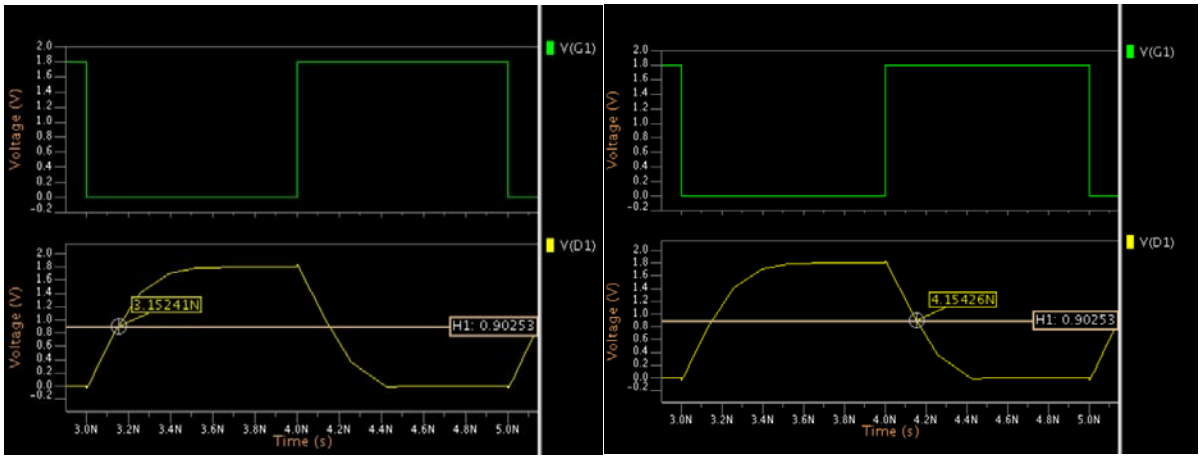


Fig 4: Delay analysis using Wp/Wn =2.42, (W/L)n=62

From figure 4
T_{PHL} = 0.15 ns (NMOS 'ON')
T_{PLH} = 0.15 ns (PMOS 'ON')

So, the drive capability of NMOS and PMOS are equal. Hence, these are the values which will be used in making the layout.

L=180nm
Wn=62 x 180 nm = 11,160 nm
Wp =2.42 x 11,160 = 27000 nm (approx)

3. Custom Layout Design

a. Layout

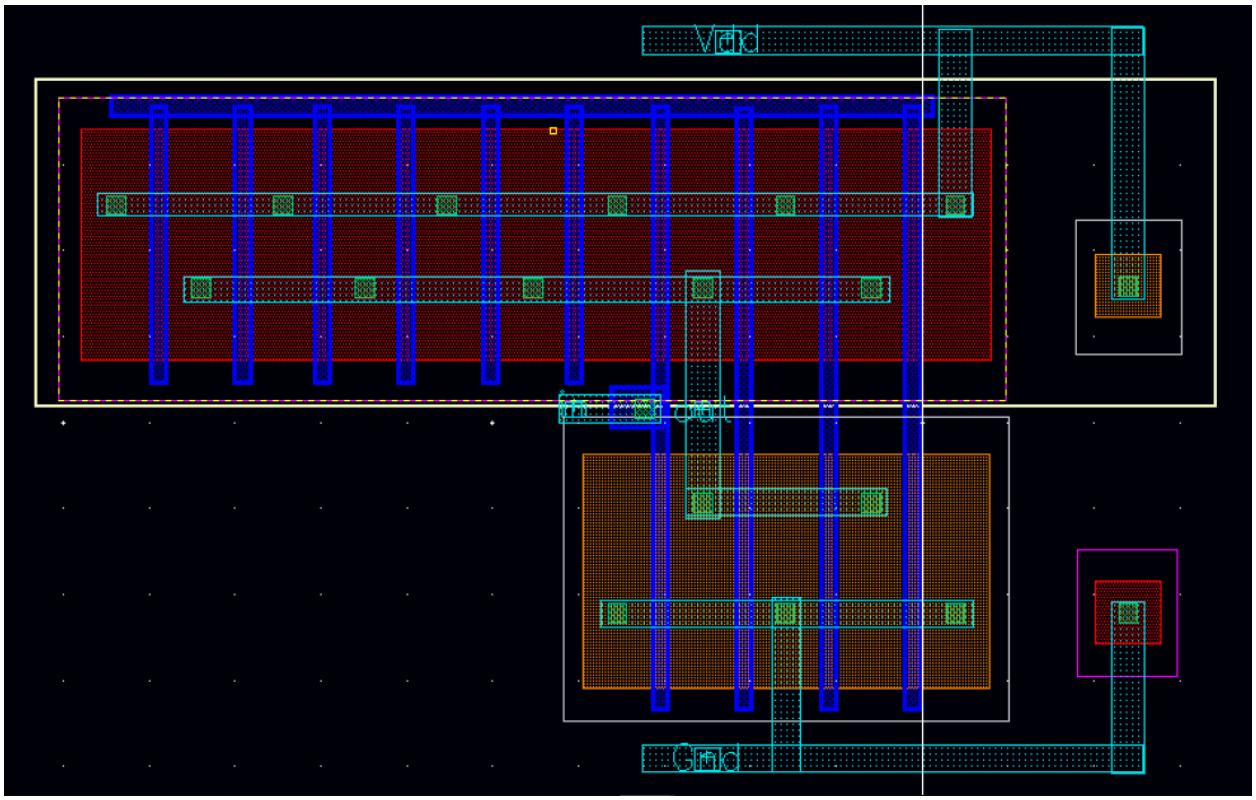


Fig 5: Multi-Fingered Layout using 4 Metal File in Virtuoso Cadence

PMOS has 10 fingers each having W/L = 2700/180 = 15

So, (W/L)p = 150

NMOS has 4 fingers each having W/L = 2790/180 = 15.5

So, (W/L)n = 62

Hence, Wp/Wn = 2.42

b. DRC

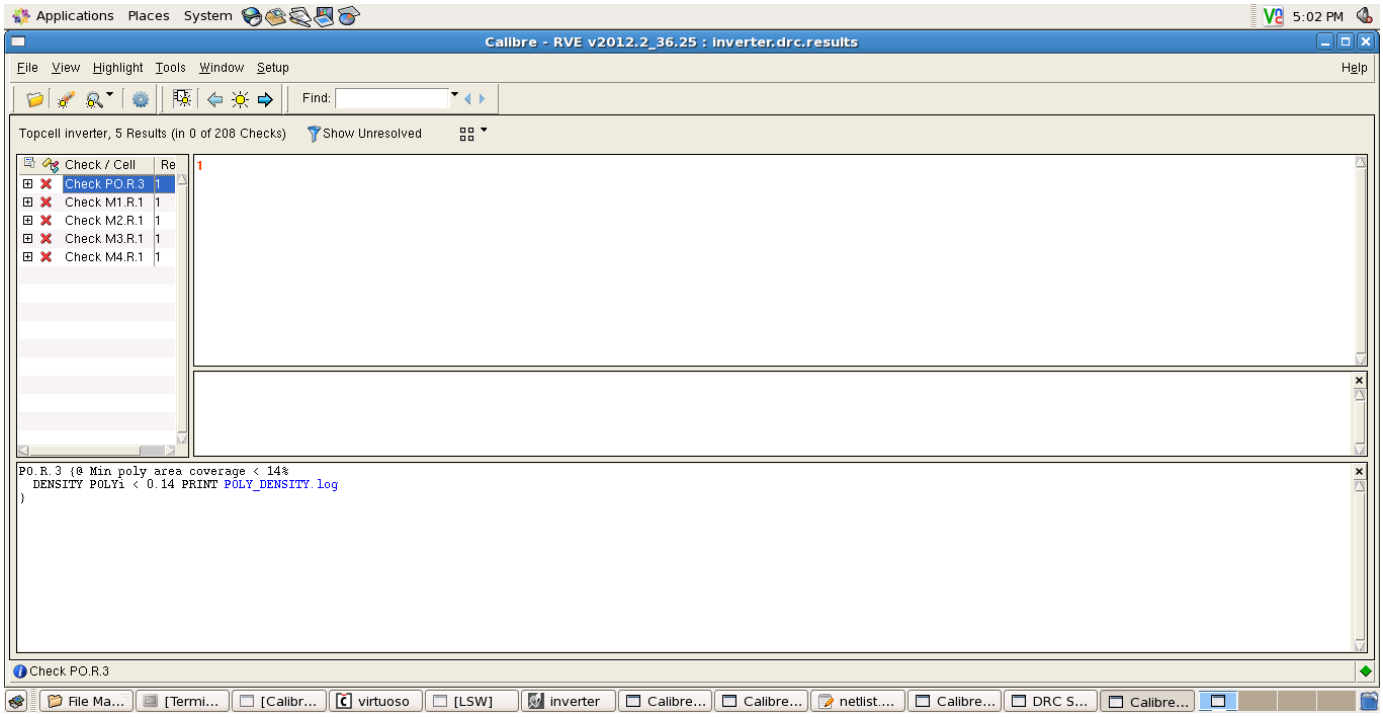


Fig 6: Running Design Rules Check (DRC) using Calibre

DRC was passed successfully (i.e all errors except density errors were removed) and at the same time, care was taken to ensure minimum area to decrease parasitics. Result of this can be seen in PEX section were we obtained output capacitance due to parasitics in Femto Farads in spite of having a multi-fingered layout which occupies large area.

c. LVS

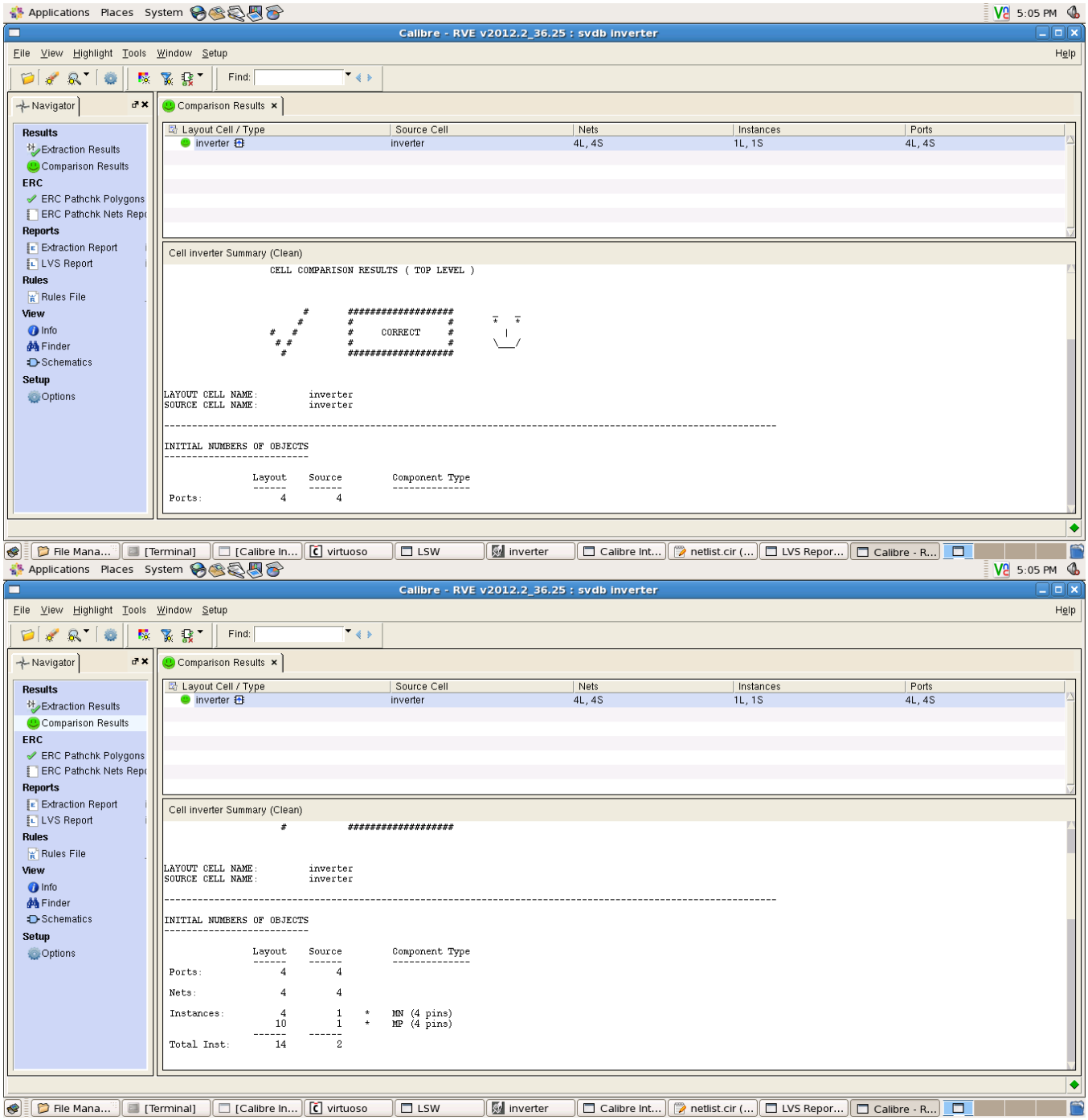


Fig 7: Running Layout VS Schematic (LVS) Check using Calibre

Schematic used for LVS -

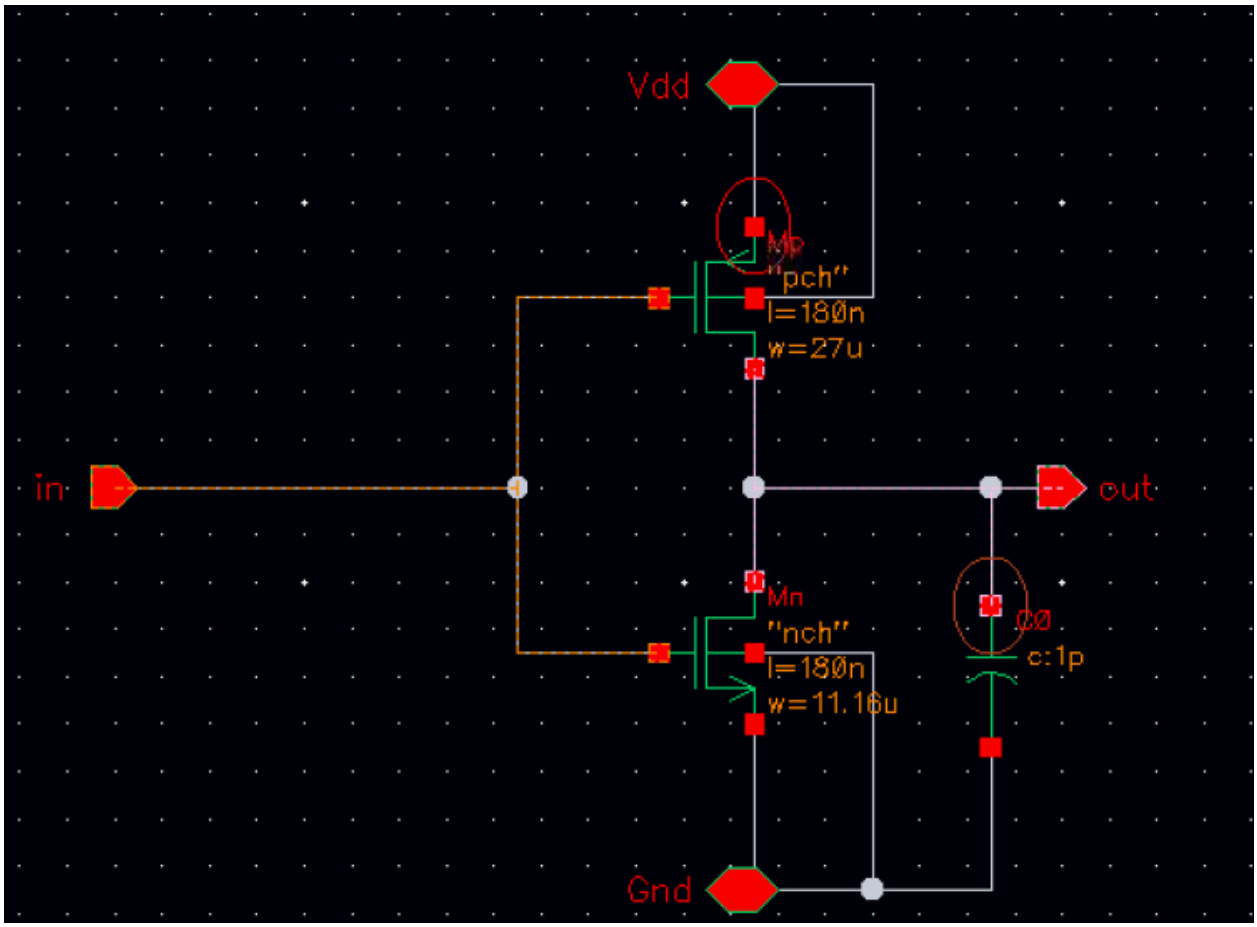


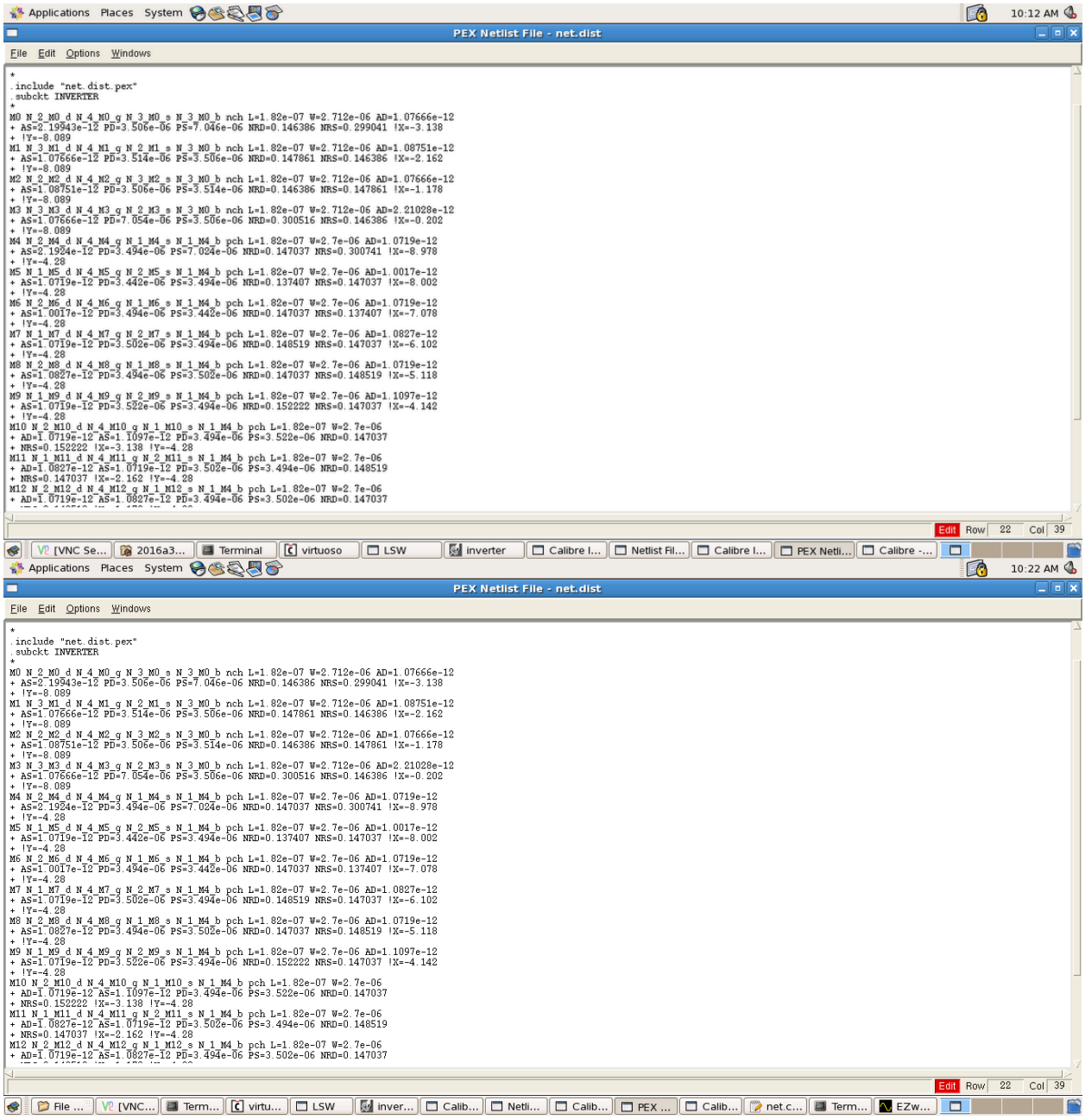
Fig 8: Schematic for LVS

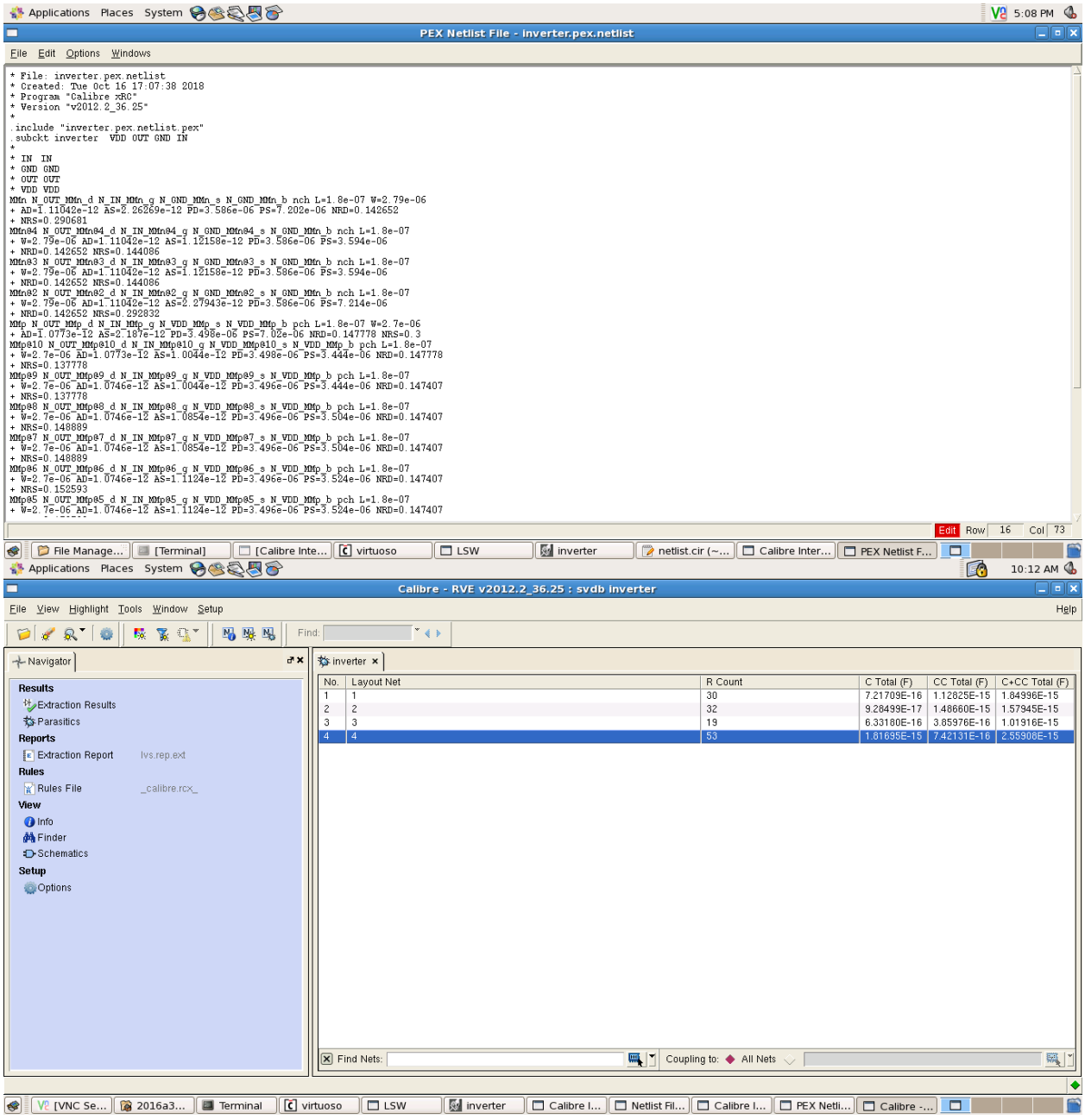
(CLoad was removed)

LVS was done successfully.

d. PEX extraction

Parasitic Extraction (PEX) using Calibre




Applications Places System
5:08 PM
PEX Netlist File - inverter.pex.netlist
File Edit Options Windows
* File: inverter.pex.netlist
* Created: Tue Oct 16 17:07:38 2018
* Program "Calibre xRC"
* Version "v2012.2_36.25"
*
.include "inverter.pex.netlist.pex"
.subckt inverter VDD OUT GND IN
*
* IN IN
* GND GND
* OUT OUT
* VDD VDD
MMn N_OUT_MMn_d N_IN_MMn_g N_GND_MMn_s N_GND_MMn_b nch L=1.8e-07 W=2.79e-06
+ AD=1.11042e-12 AS=2.26269e-12 PD=3.586e-06 PS=7.202e-06 NRD=0.142652
+ NRS=0.290681
MMn04 N_OUT_MMn04_d N_IN_MMn04_g N_GND_MMn04_s N_GND_MMn_b nch L=1.8e-07
+ W=2.79e-06 AD=1.11042e-12 AS=1.12158e-12 PD=3.586e-06 PS=3.594e-06
+ NRD=0.142652 NRS=0.144086
MMn03 N_OUT_MMn03_d N_IN_MMn03_g N_GND_MMn03_s N_GND_MMn_b nch L=1.8e-07
+ W=2.79e-06 AD=1.11042e-12 AS=1.12158e-12 PD=3.586e-06 PS=3.594e-06
+ NRD=0.142652 NRS=0.144086
MMn02 N_OUT_MMn02_d N_IN_MMn02_g N_GND_MMn02_s N_GND_MMn_b nch L=1.8e-07
+ W=2.79e-06 AD=1.11042e-12 AS=2.27943e-12 PD=3.586e-06 PS=7.214e-06
+ NRD=0.142652 NRS=0.292832
MMp N_OUT_MMp_d N_IN_MMp_g N_VDD_MMp_s N_VDD_MMp_b pch L=1.8e-07 W=2.7e-06
+ AD=1.0773e-12 AS=2.187e-12 PD=3.498e-06 PS=7.02e-06 NRD=0.147778 NRS=0.3
MMp010 N_OUT_MMp010_d N_IN_MMp010_g N_VDD_MMp010_s N_VDD_MMp_b pch L=1.8e-07
+ W=2.7e-06 AD=1.0773e-12 AS=1.0044e-12 PD=3.498e-06 PS=3.444e-06 NRD=0.147778
+ NRS=0.137778
MMp09 N_OUT_MMp09_d N_IN_MMp09_g N_VDD_MMp09_s N_VDD_MMp_b pch L=1.8e-07
+ W=2.7e-06 AD=1.0746e-12 AS=1.0044e-12 PD=3.496e-06 PS=3.444e-06 NRD=0.147407
+ NRS=0.137778
MMp08 N_OUT_MMp08_d N_IN_MMp08_g N_VDD_MMp08_s N_VDD_MMp_b pch L=1.8e-07
+ W=2.7e-06 AD=1.0746e-12 AS=1.0854e-12 PD=3.496e-06 PS=3.504e-06 NRD=0.147407
+ NRS=0.148889
MMp07 N_OUT_MMp07_d N_IN_MMp07_g N_VDD_MMp07_s N_VDD_MMp_b pch L=1.8e-07
+ W=2.7e-06 AD=1.0746e-12 AS=1.0854e-12 PD=3.496e-06 PS=3.504e-06 NRD=0.147407
+ NRS=0.148889
MMp06 N_OUT_MMp06_d N_IN_MMp06_g N_VDD_MMp06_s N_VDD_MMp_b pch L=1.8e-07
+ W=2.7e-06 AD=1.0746e-12 AS=1.1124e-12 PD=3.496e-06 PS=3.524e-06 NRD=0.147407
+ NRS=0.152593
MMp05 N_OUT_MMp05_d N_IN_MMp05_g N_VDD_MMp05_s N_VDD_MMp_b pch L=1.8e-07
+ W=2.7e-06 AD=1.0746e-12 AS=1.1124e-12 PD=3.496e-06 PS=3.524e-06 NRD=0.147407
Edit Row 16 Col 73
File Manage... [Terminal] [Calibre Inte... virtuoso LSW inverter netlist.cir (~... Calibre Inter... PEX Netlist F...
Applications Places System
10:12 AM
Calibre - RVE v2012.2_36.25 : svdb inverter
File View Highlight Tools Window Setup
Help
Find:
Navigator
Results
Extraction Results
Parasitics
Reports
Extraction Report lvs.rep.ext
Rules
Rules File _calibre.rcx_
View
Info
Finder
Schematics
Setup
Options
inverter
No. Layout Net R Count C Total (F) CC Total (F) C+CC Total (F)
1 1 30 7.21709E-16 1.12825E-15 1.84996E-15
2 2 32 9.28499E-17 1.48660E-15 1.57945E-15
3 3 19 6.33180E-16 3.85976E-16 1.01916E-15
4 4 53 1.81695E-15 7.42131E-16 2.55908E-15
Find Nets:
Coupling to: All Nets
[VNC Se... 2016a3... Terminal virtuoso LSW inverter Calibre I... Netlist Fil... Calibre I... PEX Netli... Calibre -...

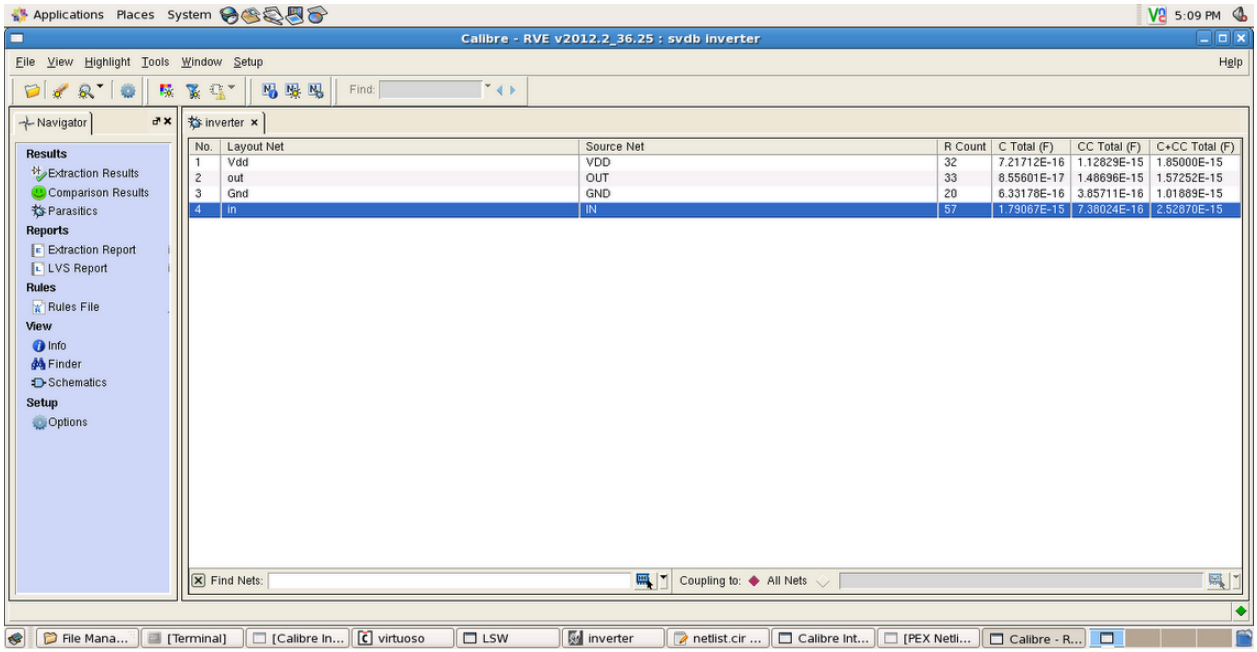


FIG 9 : PEX Extraction (above 5 figures)

So, final output capacitance of was obtained as 1.57e-15 which is negligible compared to 1 pF CLoad i.e. 0.15% of the Load capacitance.

4. Schematic Circuit Simulations

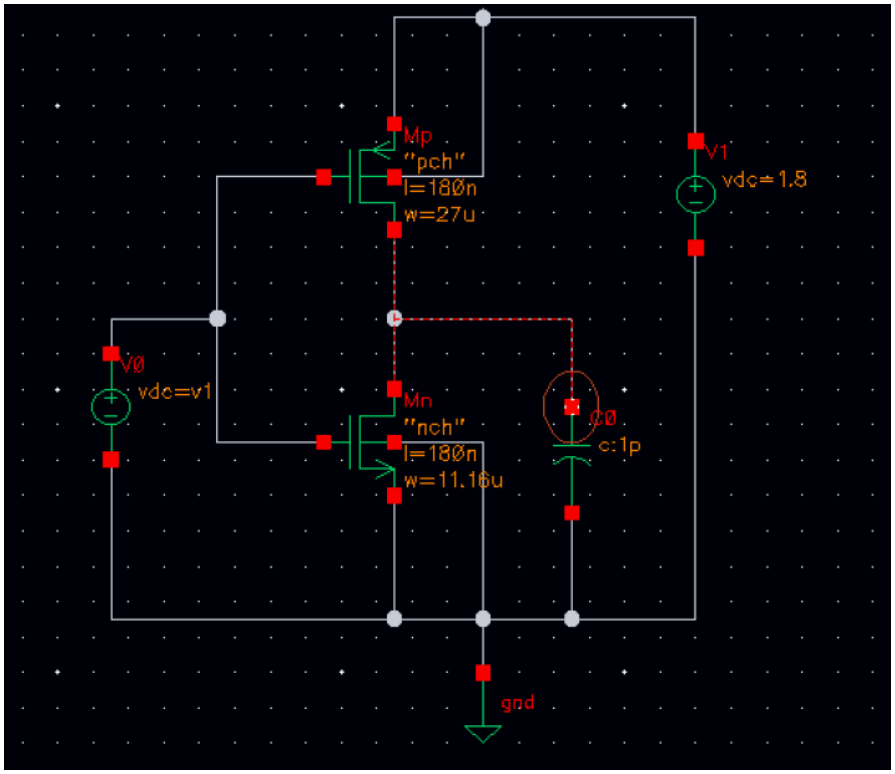


Fig 10: Schematic of the inverter

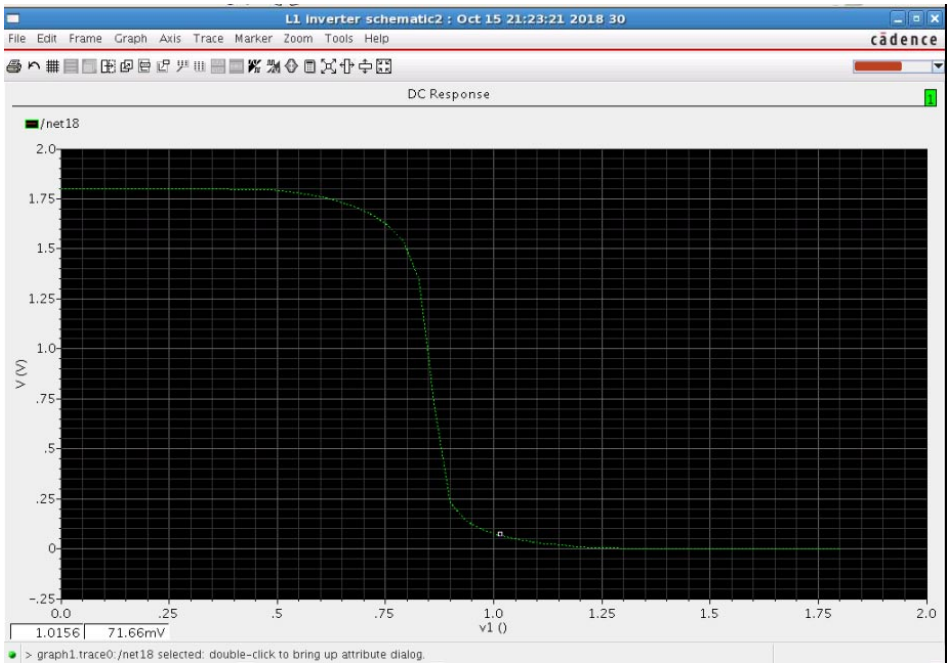


Fig 11: Voltage Transfer characteristics (VTC)

a. Plot the energy and delay graph

Delay graphs

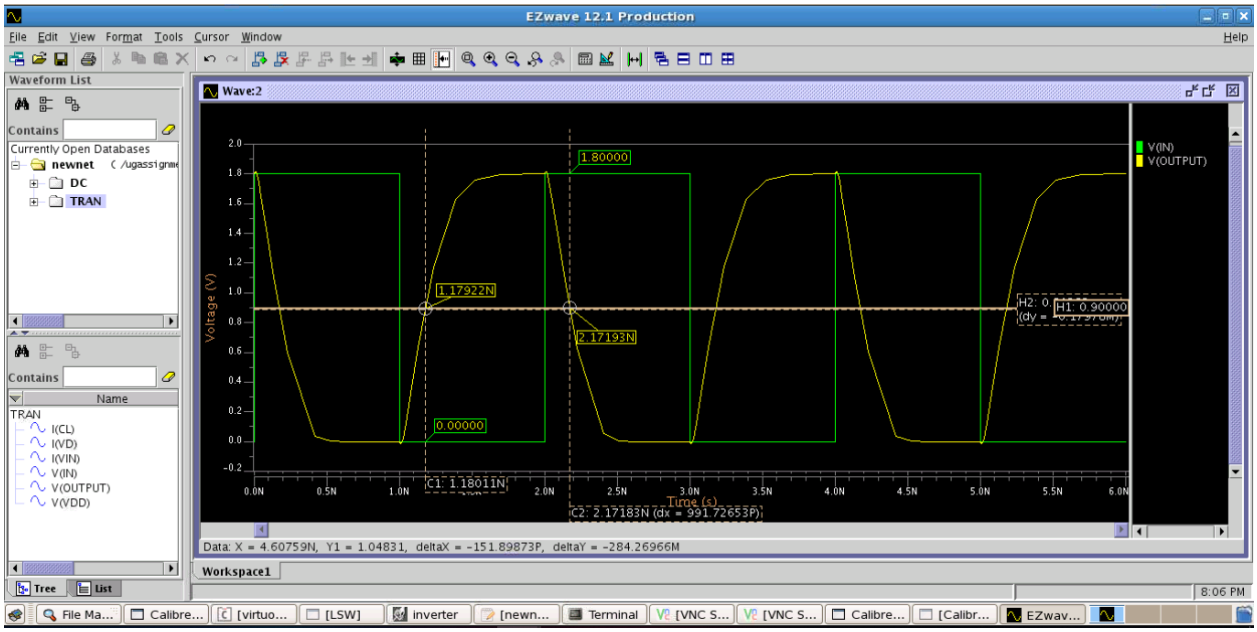
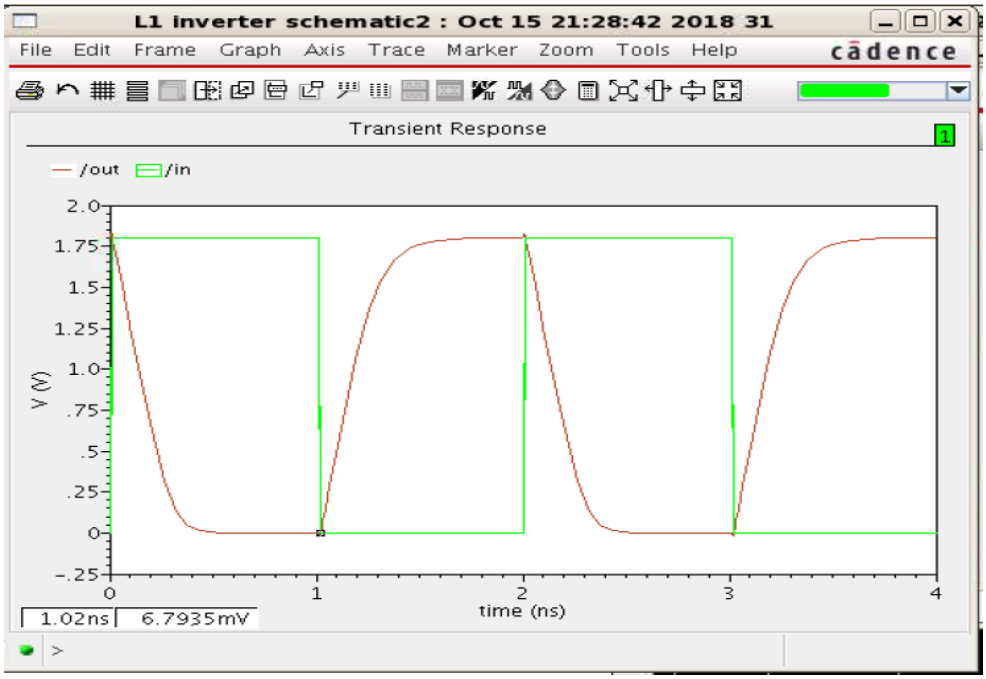


Fig 12: Delay Calculation using ELDO SPICE and Ezwave including PEX extracted parasitic capacitances and Load Capacitance of 1pF



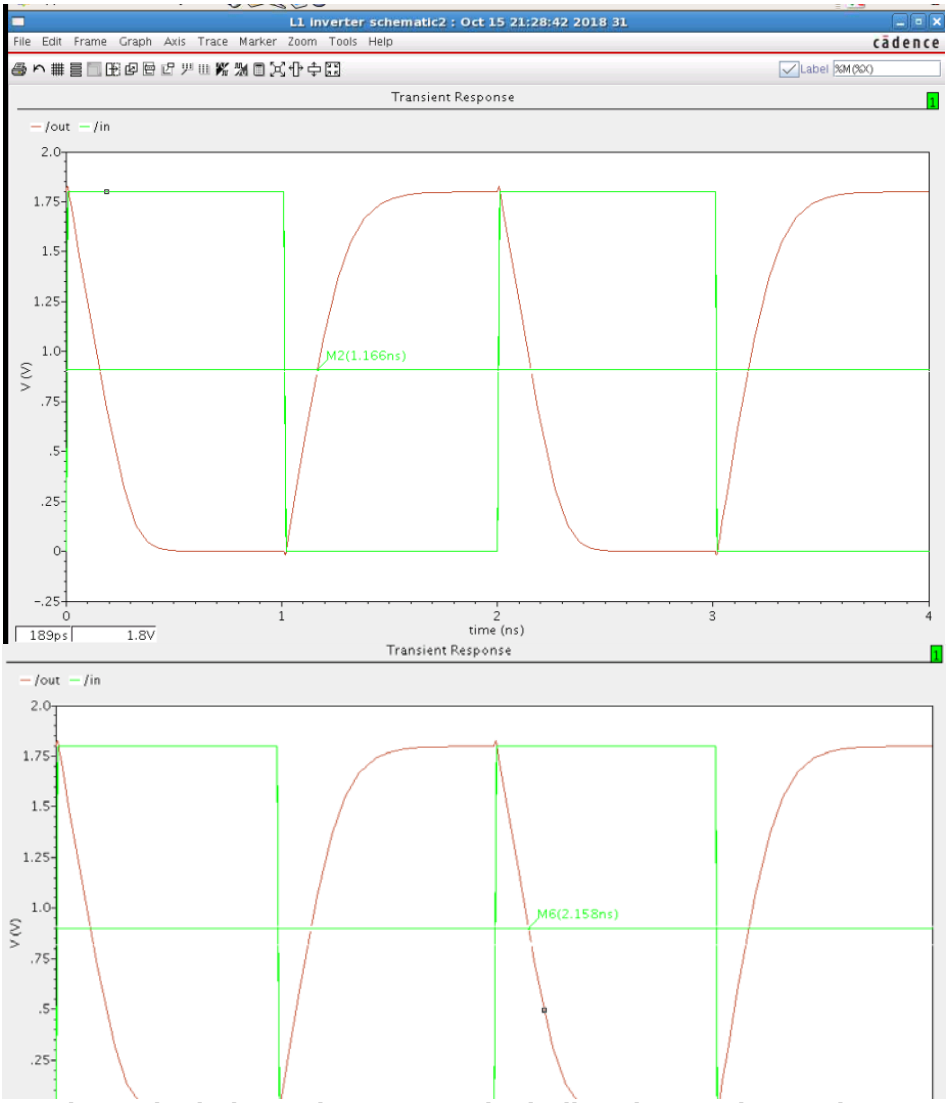


Fig 13: Delay Calculation using Spectre including the Load capacitance of 1pF

Energy Graph

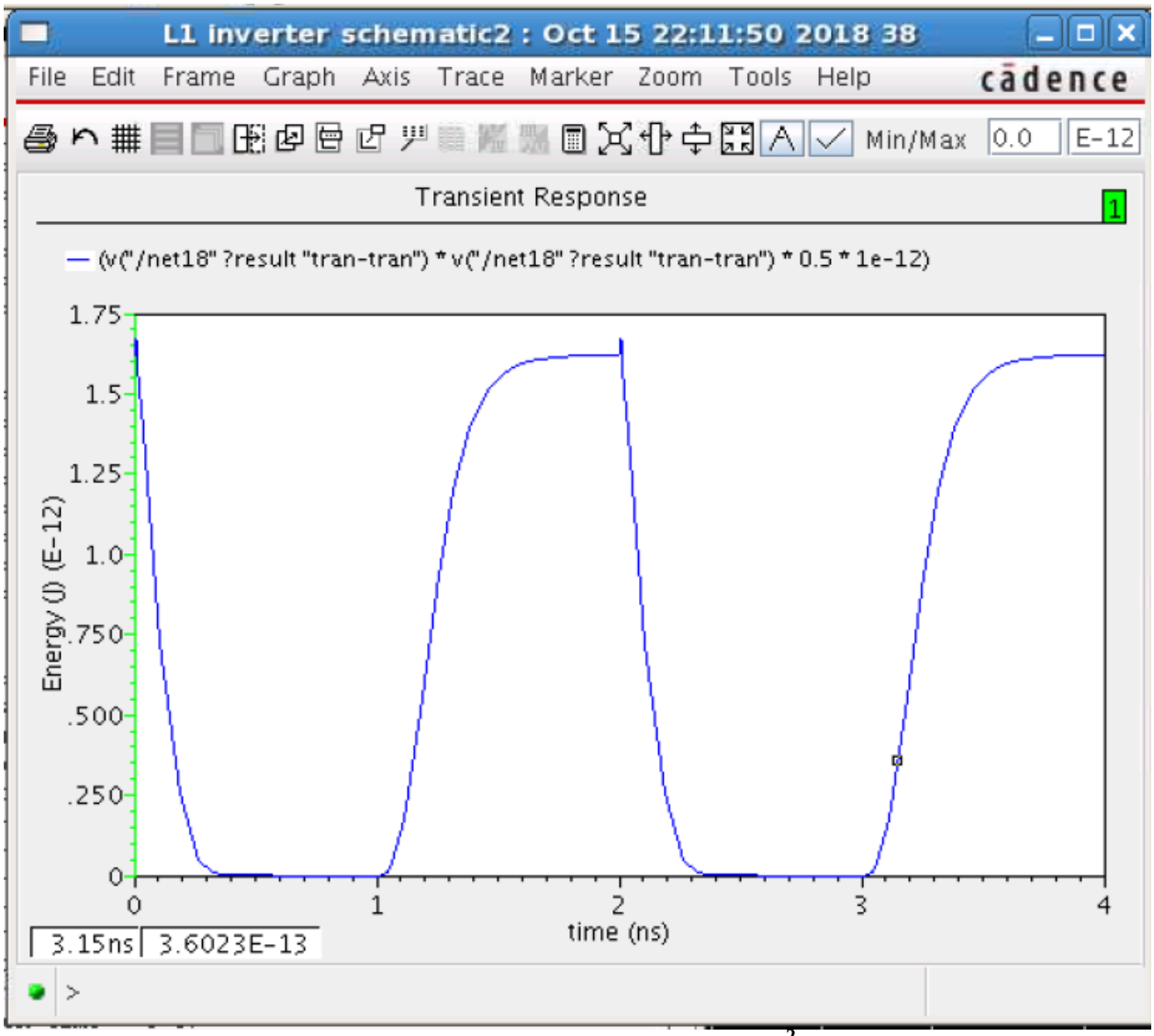


Fig 14: Energy = 0.5 x Cout x Vout^2

b. Plot the short circuit and switching power graph.

Short Circuit Power Graph.

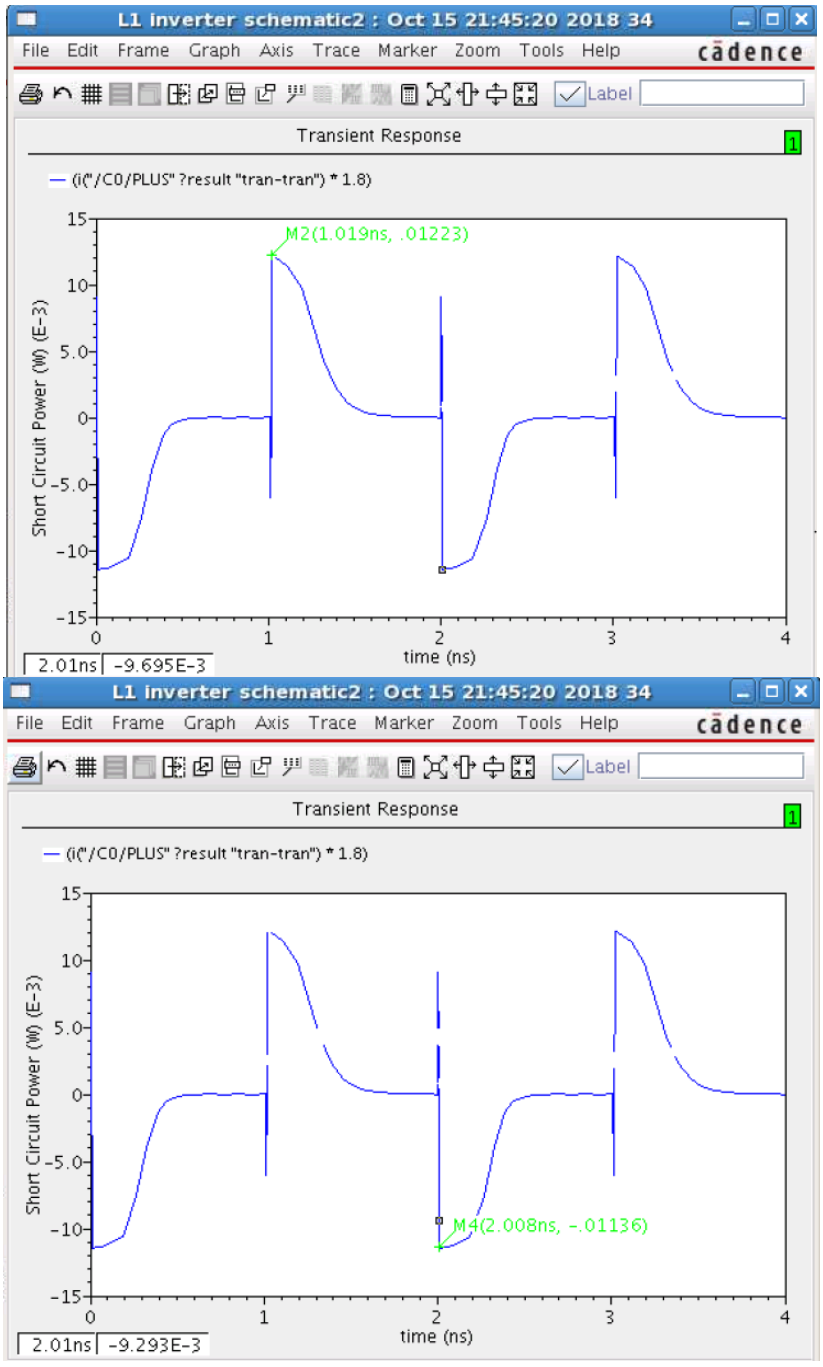


Fig 15: SC Power = I_{DS} x V_{DD}

Switching or Dynamic Power Graph

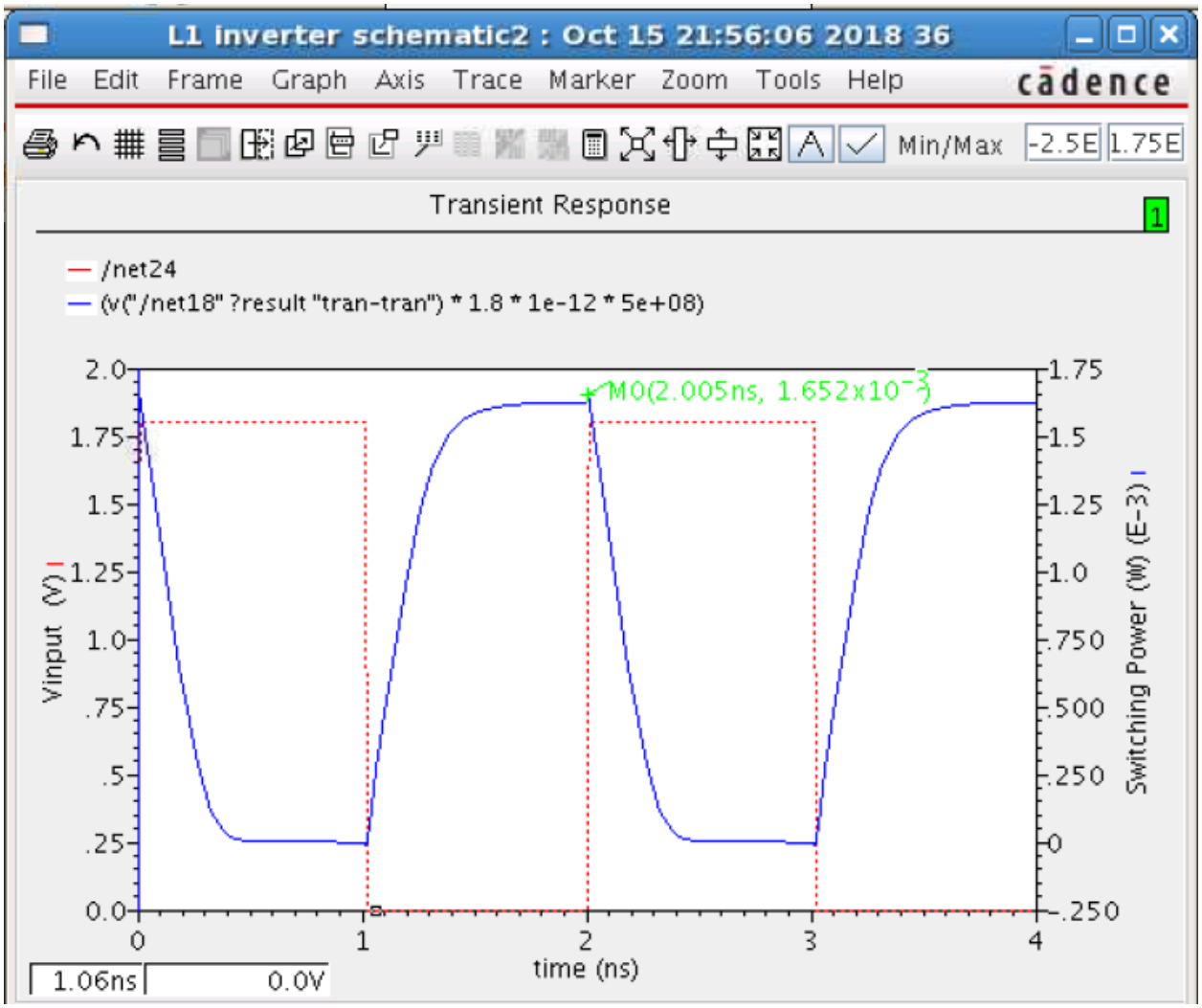


Fig 16: Switching power = (SP) x V_{DD} x V_{OUT} x C_{LOAD} x Frequency

For inverter Switching probability = 1