A report on

***2 Stage Fully Differential Operational- Amplifier Design***

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Submitted in partial fulfillment of the course

**EEE F313/ INSTRF313 – Analog & Digital VLSI Design**

Under the Guidance of

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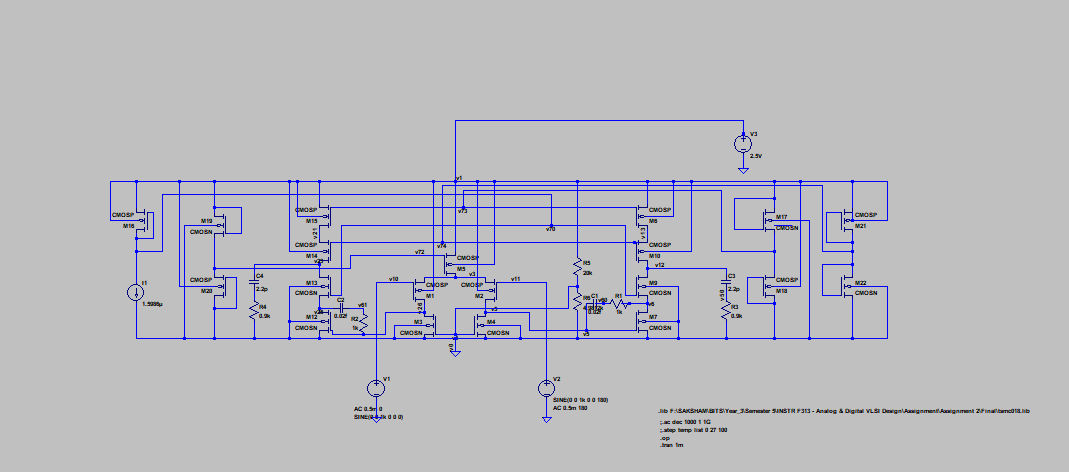


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**Problem Number 50:**

Design a fully differential two stage OPAMP (Differential + gain stage) for the following specification

1. Analysis of all equations of your design, with a systematic derivation of all transistors W/L ratios and simulation of circuit for the following specifications.
2. DC gain ≥ 80dB
3. Power Dissipation ≤ 1mW
4. Show a biasing circuitry to bias all the voltages in your design (except the input)
5. Calculate and plot the following parameters for your OPAMP: DC gain, Bode plot for AC gain and phase, ICMR plot, slew rate, Differential Output Swing (dc + Transient), power consumption and Input and Output Offset Voltage

**Circuit Schematic**

**Transistor Widths**

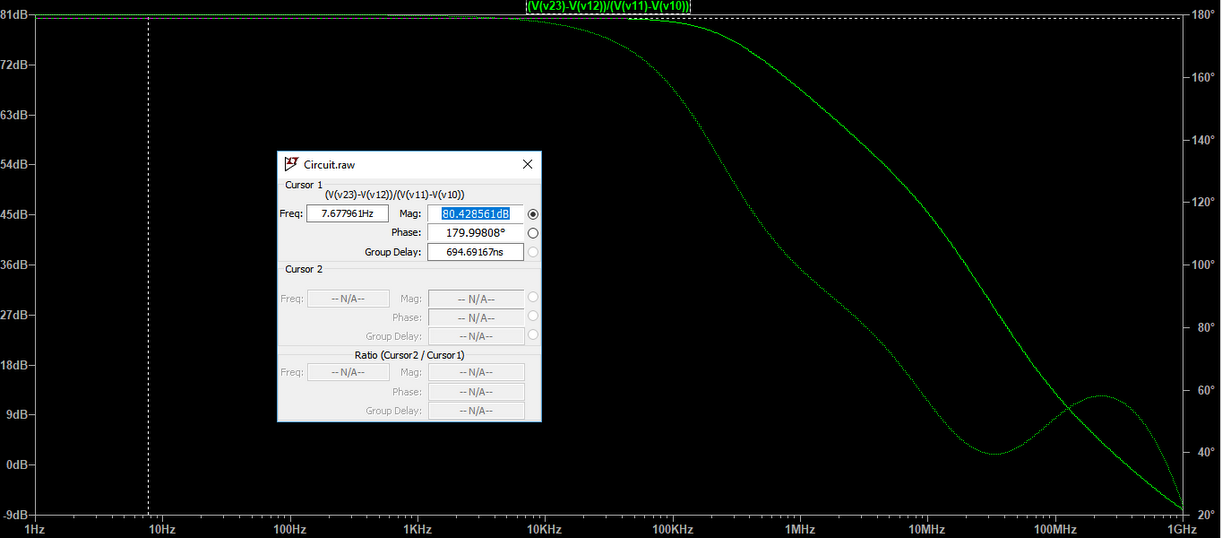
**M1**

**Lengths: 350nm**

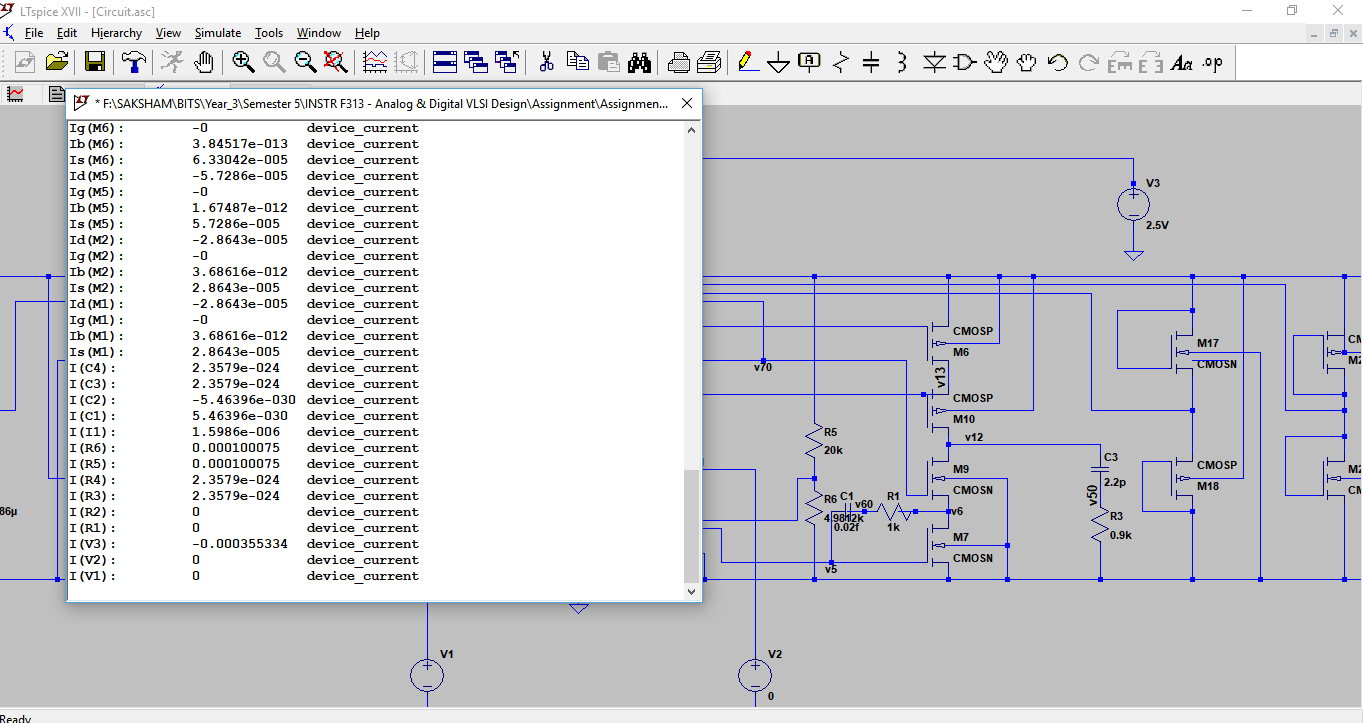
**Load: Cl = 2.2pF**

**DC Gain**

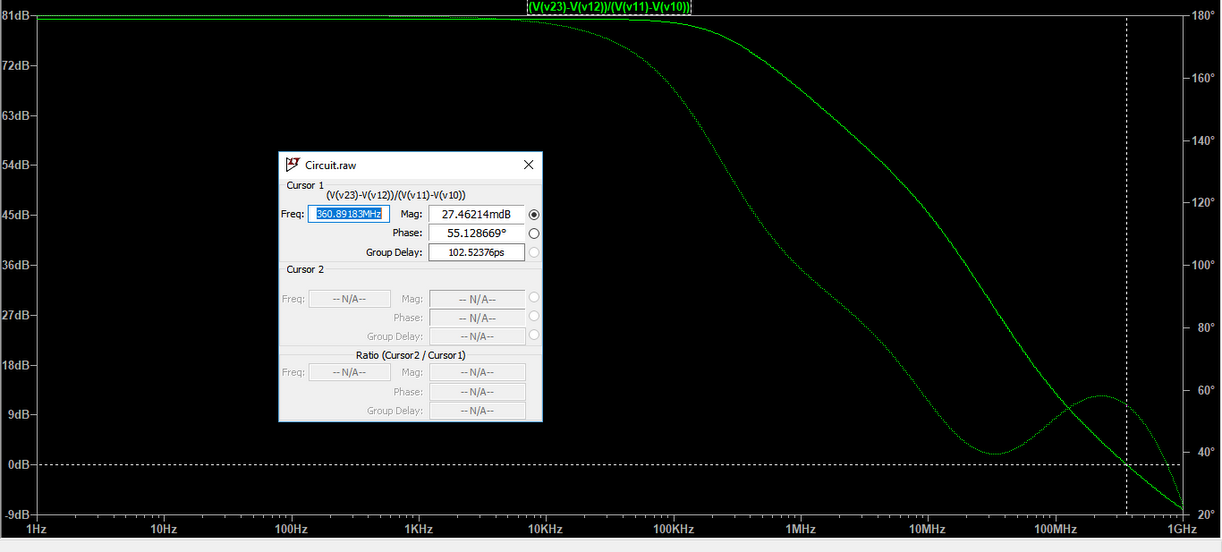
The DC Gain is 80.42dB

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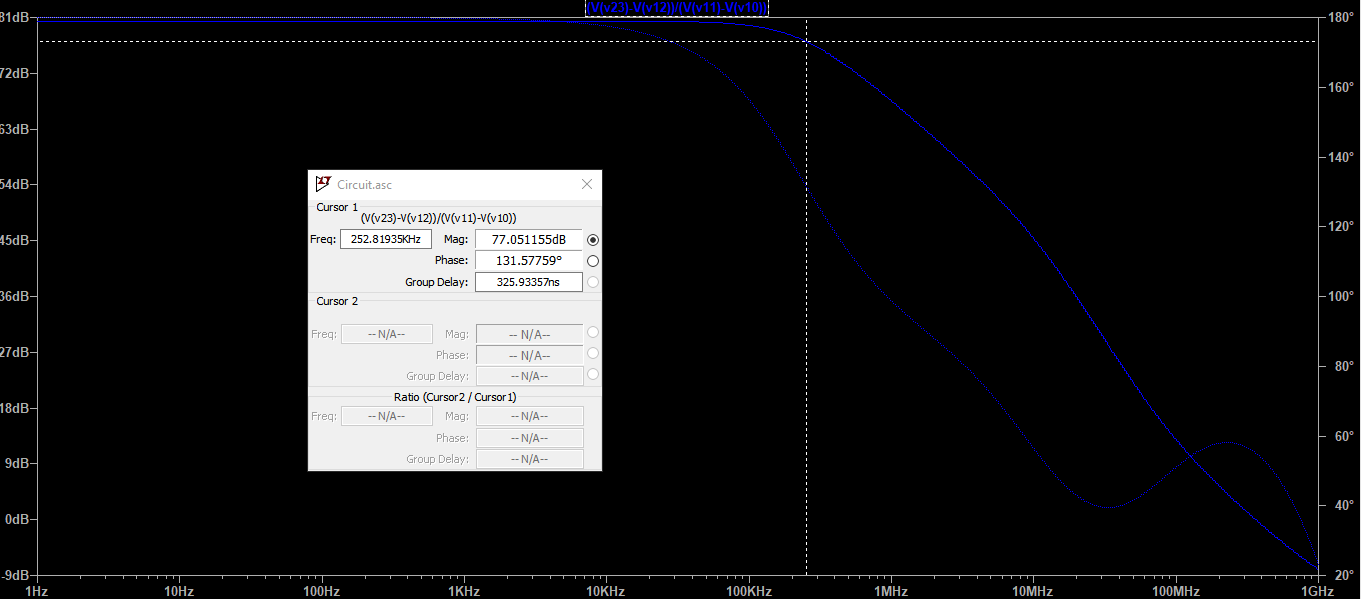
**Power Consumption**

Power Consumption = 2.5 \* 0.355334mA = 0.888mW ≤ 1mW

**Frequency Analysis**

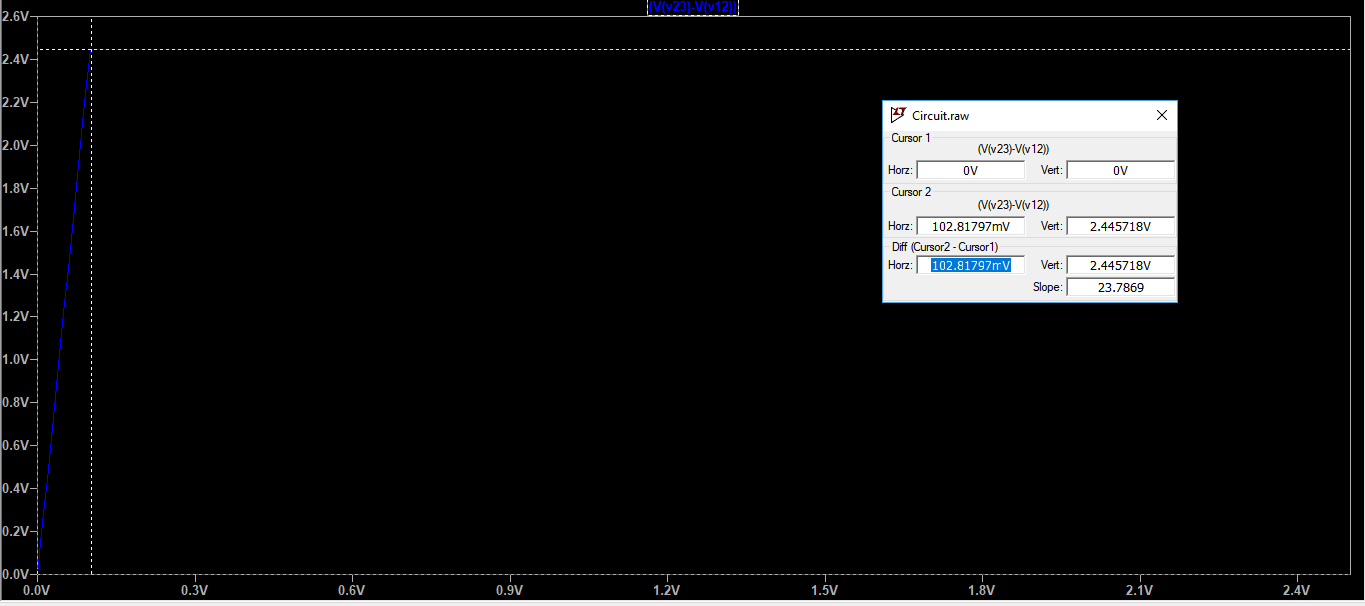
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UGB: 360.89MHz

Phase Margin = -55.12 – (-180) = 124.88

-3dB frequency: 252.819kHz

**ICMR**

ICMR of the OPAMP is 102.819mV

**Input Offset Voltage = 0V**

**Output Offset Voltage = 0V**

**CMRR = Infinite**

**Slew Rate = Photos**

Slew rate of an Op amp is defined as the maximum rate of change of output for the small

change in input. Generally SR is determined from the slope of output waveform during rise or fall of the output when the input is applied. So, we have a positive SR and a negative SR.

**Differential Output Swing (To Do)**