Examples (Simplification)

- $(A + AB) = A$
- $(A+B)(A+C) = A + BC$
- $(AB)' + A' + AB)' = 0$
- $\overline{((AB+C)(\bar{A}\bar{C}+BC)+ABC+\bar{A}\bar{B}}\,Y = \cancel{A(B+C)}$ corrected $\Rightarrow AB$

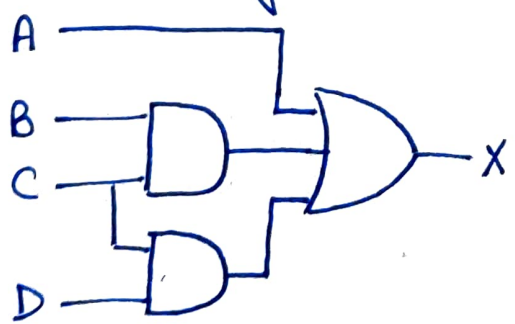
AOI logic → AND, OR, IVERTOR gates only circuit

NAND-NAND logic → NAND gates only

NOR-NOR logic → NOR gates only

- $X = A + BC + CD$

$\Rightarrow$ AOI Logic Circuit



Converting into a NAND-NAND logic

Placing bubbles

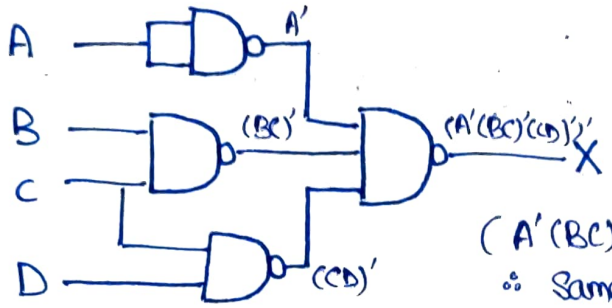
- Bubbled OR ~ NAND
- AND → NAND

NAND - NAND to Inverter

Thus, final

NAND - NAND logic (using only NAND gates)

$X = A + BC + CD$



$(A'(BC)'(CD)')' = A + BC + CD$

∴ Same expression

Same procedure for

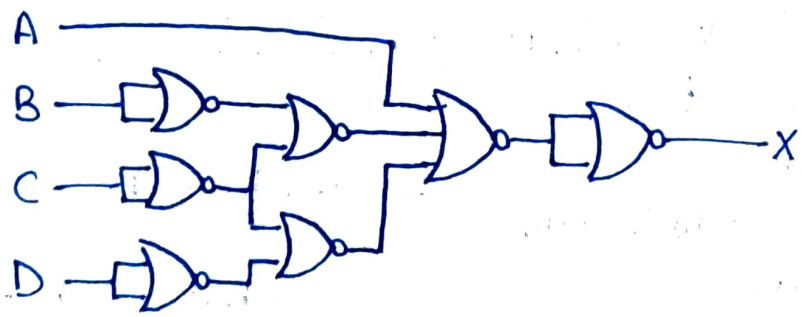
NOR - NOR logic Circuit

- ~~Ble~~ Placing Bubbleds
- Place inverter for the extra bubble

Thus, Final

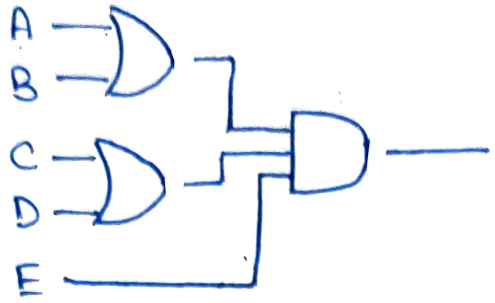
NOR - NOR logic

$X = A + BC + CD$

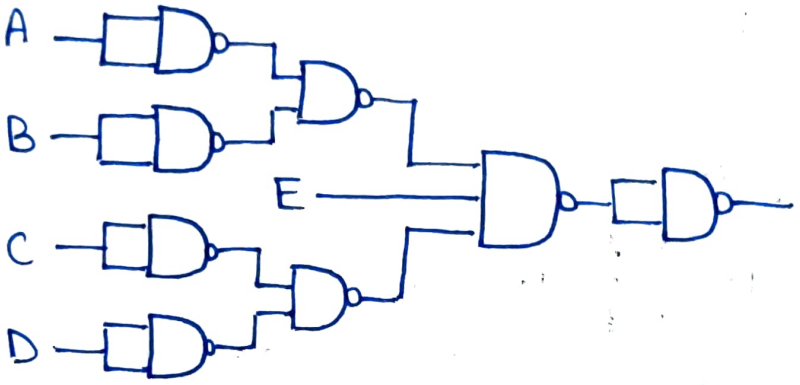


- $X = (A+B)(C+D)E$

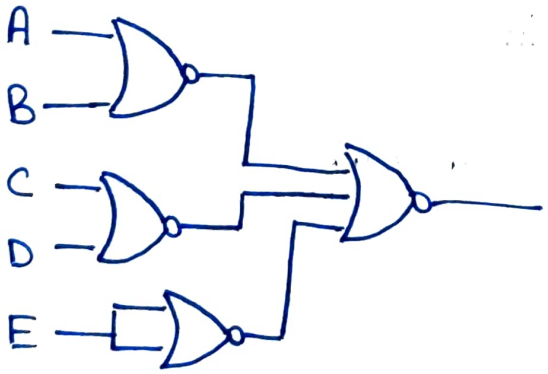
AOI Logic Circuit



NAND-NAND Circuit



NOR-NOR Circuit



- A Reduced circuit is desired always
  => (Reduced circuit = Min no. of gates used)

  For less complexity time less efficiency reasons

  Two forms

  → SOP form (Sum of Products form) • $X = A + BC + CD$

  → POS form (Product of Sum form) • $X = (A+B)(C+D)E$

SOP form

⇒ Circuited Reduced → ~~NOR-NOR~~ logic
NAND-NAND

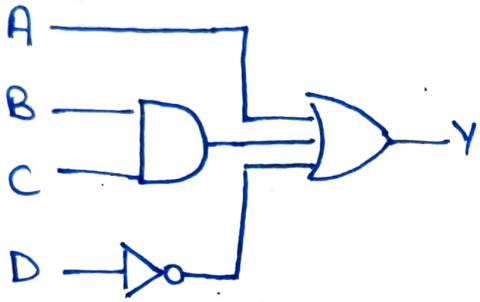
POS form

⇒ Circuite Reduced → NOR-NOR logic

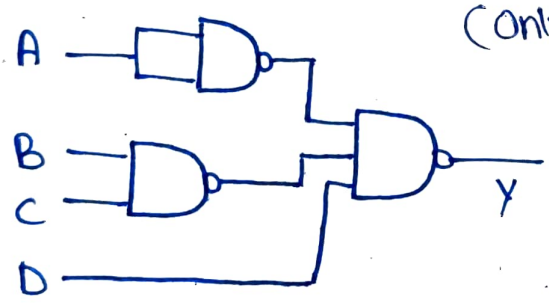
Eg Question,

1) $Y = A + BC + \bar{D}$

- AOI Logic

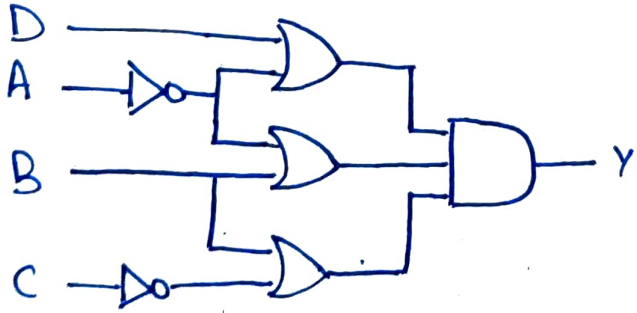


⇒ NAND-NAND logic to be used, Sice SOP form
(Only 3 gates used)



NAND - 3 (better)
NOR - 6

2) $Y = (A'+B)(A'+D)(B+C')$

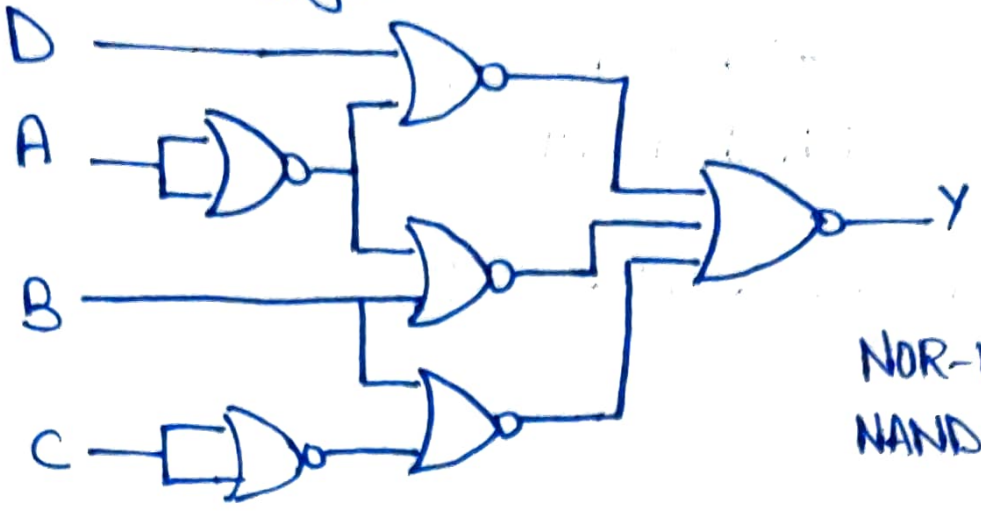


- AOI Logic

Since in POS form

⇒ NOR-NOR logic to be used

NOR-NOR logic



(only 6 gates for NOR)

NOR-NOR => 6 (better)

NAND-NAND => 9