# Computer Organization & Architecture

**Workbook**

**Computer Science Engineering**
**Information Technology**

**GATE**

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**Workbook**

Computer Science Engineering

Information Technology



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## GATE Syllabus

**Computer Organization & Architecture :** Machine instructions and addressing modes. ALU, data-path and control unit. Instruction pipelining, pipeline hazards. Memory hierarchy: cache, main memory and secondary storage; I/O interface (interrupt and DMA mode).

# Contents

# 1 Computer Architecture and CPU Registers

**Q.1** A CPU has 4 bytes instructions. A program (Instructions I1 to I200) starts at address 500 (in decimal). Find the address of following instructions:
(a) I1
(b) I5
(c) I120

**Q.2** A CPU has 4 bytes instructions. A program (Instructions I1 to I200) starts at address 500 (in decimal). What should be the PC value when instruction I6 will be executing in CPU?

**Q.3** A CPU has 4 bytes instructions. A program (Instructions I1 to I200) starts at address 500 (in decimal). What should be the PC value when instruction i will be executing in CPU?

**Q.4** In a microprocessor, the register which holds address of the next instruction to be fetched?
(A) Accumulator
(B) Program Counter
(C) Stack Pointer
(D) Instruction Register

**Q.5** The following register holds the instruction before it goes for decode?
(A) Data Register
(B) Accumulator
(C) Address Register
(D) Instruction Register

**Q.6** Which of the following 2 registers are used to access the memory?
(A) Instruction Register and Program counter
(B) Address Register and Program counter
(C) Program counter and Stack Pointer
(D) Address register and data register

**Q.7** In a CPU which of the following pair of registers should have same capacity of storage?
(A) Instruction Register and Program counter
(B) Address Register and Program counter
(C) Program counter and Stack Pointer
(D) Address register and Data register

**Q.8** Which is not a CPU architecture?
(A) Single Accumulator architecture
(B) General Register architecture
(C) Base Register architecture
(D) Stack architecture

**Q.9** Which of the following is included in the architecture of computer?
1. Addressing Modes, Design of CPU
2. Instruction Set, Data Format
3. Secondary Memory, Operating System

(A) 1 and 2
(B) 2 and 3
(C) 1 and 3
(D) 1, 2 and 3

**Q.10** Consider the following statements :
1. A computer will have a divide instruction
2. Divide instruction will be implemented by a special division unit

Which of the following is correct?
(A) Both 1 and 2 are not architectural design issues.
(B) Both 1 and 2 are not organizational issues.
(C) 1 is an architectural design issue while
2 is an organizational issue.
(D) 1 is an organizational issue while
2 is an architectural design issue.

**Q.11** Which of the following CPU registers will never be storing any memory address?
(A) Program Counter
(B) Address Register
(C) Stack Pointer
(D) None

**Q.12** A CPU has 24-bits instruction. A program starts at address 600 (in decimal). Which of the following is a legal program counter value?
(A) 700 (B) 800
(C) 900 (D) 950

**Q.13** Consider 5 instructions of a program are as follows:

| Instruction | Size in words |
|---|---|
| i | 2 |
| i+1 | 1 |
| i+2 | 2 |
| i+3 | 3 |
| i+4 | 2 |

If the program is loaded from location 5000, and the memory is word addressable then value of PC immediately during the execution of instruction i+3 can be? (Note: All the numbers in decimal)

(A) 5000 (B) 5002

(C) 5004 (D) 5008

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# 2 Micro-Operations

**Q.1** Consider the following program segment. Here R1 and R2 are the general purpose register. Assume that the content of memory location 2000 is 37. All numbers are in decimal. After the execution of this program the value of memory location 2000 is?

| Instructions | Operations |
|---|---|
| MOV R1, #12 | R1 ← #12 |
| MOV R2, (2000) | R2 ← M[2000] |
| SUB R2, R1 | R2 ← R2 – R1 |
| MOV (2000), R3 | M[2000] ← R3 |
| HALT | Stop |

**Q.2** Consider the following program segment. Here R1 and R2 are the general purpose register. Assume that the content of memory location 3000 is 13. All numbers are in decimal. After the execution of this program the value of memory location 3000 is?

| Instructions | Operations |
|---|---|
| MOV R1, #7 | R1 ← #7 |
| MOV R2, (3000) | R2 ← M[3000] |
| ADD R2, R1 | R2 ← R2 + R1 |
| ADD R1, R2 | R1 ← R1 + R2 |
| MOV (3000), R1 | M[3000] ← R1 |
| HALT | Stop |

**Q.3** Consider the following program segment. Here R1 and R2 are the general-purpose register. Assume that the content of memory location 1000 is 5. All the numbers are in decimal. The value of R2 at the end of program execution is?

| | Instructions | Operations |
|---|---|---|
| | MOV R1, (1000) | R1 ← M[1000] |
| | MOV R2, #8 | R2 ← #8 |
| LOOP | ADD R2, R1 | R2 ← R2 + R1 |
| | DEC R1 | R1 ← R1 – 1 |
| | BNZ LOOP | Branch on not zero |
| | HALT | Stop |

**Q.4** Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

| | Instruction | Operation | Instruction Size (no. of words) |
|---|---|---|---|
| | MOV R1,(3000) | R1 ← M[3000] | 2 |
| LOOP: | MOV R2,(R3) | R2 ← M[R3] | 1 |
| | ADD R2,R1 | R2 ← R1 + R2 | 1 |
| | MOV (R3),R2 | M[R3] ← R2 | 1 |
| | INCR3 | R3 ← R3 + 1 | 1 |
| | DEC R1 | R1 ← R1 -1 | 1 |
| | BNZ LOOP | Branch on not zero | 2 |
| | HALT | Stop | 1 |

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal. Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

**[GATE 2007]**

(A) 10 (B) 11
(C) 20 (D) 21

**Q.5** Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

| | Instruction | Operation | Instruction Size (no. of words) |
|---|---|---|---|
| | MOV R1,(3000) | R1 ← M[3000] | 2 |
| LOOP: | MOV R2,(R3) | R2 ← M[R3] | 1 |
| | ADD R2,R1 | R2 ← R1 + R2 | 1 |
| | MOV (R3),R2 | M[R3] ← R2 | 1 |

| | | | |
|---|---|---|---|
| | INCR3 | R3 ← R3 + 1 | 1 |
| | DEC R1 | R1 ← R1 -1 | 1 |
| | BNZ LOOP | Branch on not zero | 2 |
| | HALT | Stop | 1 |

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is:

**[GATE 2007]**

(A) 100 (B) 101

(C) 120 (D) 110

**Q.6** Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

| | **Instruction** | **Operation** | **Instruction Size (no. of words)** |
|---|---|---|---|
| | MOV R1,(3000) | R1 ← M[3000] | 2 |
| LOOP: | MOV R2,(R3) | R2 ← M[R3] | 1 |
| | ADD R2,R1 | R2 ← R1 + R2 | 1 |
| | MOV (R3),R2 | M[R3] ← R2 | 1 |
| | INCR3 | R3 ← R3 + 1 | 1 |
| | DEC R1 | R1 ← R1 -1 | 1 |
| | BNZ LOOP | Branch on not zero | 2 |
| | HALT | Stop | 1 |

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is byte addressable and the word size is 32. If an interrupt occurs during the execution of the instruction "INC R3", what return address will be pushed on to the stack?

**[GATE 2007]**

(A) 1005 (B) 1020

(C) 1024 (D) 1040

**Q.7** Consider the following instruction sequence where registers R1, R2 and R3 are general purpose and MEMORY(X) denotes the content at the memory location X.

| **Instruction** | **Semantics** | **Instruction Size (bytes)** |
|---|---|---|
| MOV R1, (5000) | R1 ← MEMORY[5000] | 4 |
| MOV R2, (R3) | R2 ← MEMORY[R3) | 4 |
| ADD R2. R1 | R2 ← R1+R2 | 2 |
| MOV (R3), R2 | MEMORY[R3) ← R2 | 4 |
| INC R3 | R3 ← R3+1 | 2 |
| DEC R1 | R1 ← R1-1 | 2 |
| BNZ 1004 | Branch if not zero to the given absolute address | 2 |
| HALT | Stop | 1 |

Assume that the content of the memory location 5000 is 10. and the content of the register R3 is 3000. The content of each of the memory locations from 3000 to 3010 is 50. The instruction sequence starts from the memory location 1000. All the numbers are in decimal format. Assume that the memory is byte addressable.

After the execution of the program, the content of memory location 3010 is _____.

**Q.8** 1 micro-operation takes a minimum of

(A) 1 CPU cycle time

(B) 1 memory cycle time

(C) 1 DMA cycle time

(D) None

**Q.9** In RTL language which of the following is the wrong way to specify a memory write?

(A) M[2000] ← R3 (B) M[R2] ← R6

(C) M[x] ← R3 (D) None

**Q.10** Which of following is not wrong about ADD micro-operation and ADD instruction?

(A) Both are same

(B) ADD instruction requires ADD micro-operation

(C) ADD micro-operation Requires ADD-operation

(D) Both are independent

**Q.11** Consider a computer which has 2 word instructions. 1 word size is 2 bytes. In main memory an instruction is stored at location 234 (decimal). The decimal value of PC when this instruction will be execution in CPU?

(A) 234 (B) 236

(C) 238 (D) None

**Q.12** Consider the following program segment. Here R1, R2 and R3 are the general purpose register. Assume that the content of memory location 3000 is 25 and location 2000 is 39. Content of register R2 is 12. All numbers are in decimal. After the execution of this program the value of memory location 2000 is?

| Instructions | Operations |
|---|---|
| MOV R1, #18 | R1 ← #18 |
| MOV (2000), R1 | M[2000] ← R1 |
| ADD R2, (2000) | R2 ← R2 + M[2000] |
| MOV(3000), R2 | M[3000] ← R2 |
| MOV R3, R1 | R3 ← R1 |
| ADD R3, (3000) | R3 ← R3 + M[3000] |
| MOV (2000), R3 | M[2000]← R3 |
| HALT | Stop |

**Q.13** Consider the following program segment. Here R1 and R2 are the general-purpose register. Assume that the content of memory location 3000 is 27 and location 2000 is 16. Content of register R2 is 10. All numbers are in decimal. After the execution of this program the value of R2 is?

| | Instructions | Operations |
|---|---|---|
| | MOV R1, #7 | R1 ← #7 |
| X: | DEC R1 | R1 ← R1 – 1 |
| | JNZ Y | Jump to Y on Non-Zero |
| | ADD R2, (3000) | R2← R2 + M[3000] |
| | JMP Z | Jump to Z |
| Y: | ADD R2, (2000) | R2 ← R2 + M[2000] |
| | JMP X | Jump to X |
| Z: | HALT | Stop |

**Q.14** Which of the following statements is/are not wrong?

(A) 2 micro-operations can be performed simultaneously

(B) Only 1 micro-operation is performed at a time always

(C) Memory read and Memory write both can be performed simultaneously

(D) None

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# 3 CPU Instructions

**Q.1** Consider a digital computer which supports only 2-address instructions each with 14-bits. If address length is 5-bits then maximum and minimum how many instructions the system can support?

**Q.2** Consider a digital computer which supports only 3-address instructions each with 32-bits. If address length is 8-bits then maximum and minimum how many instructions the system can support?

**Q.3** Consider a digital computer which supports 64 2-address instructions. If address length is 9-bits then the length of the instruction is _____ bits?

**Q.4** Consider a digital computer which supports 64 2-address instructions. If address length is 9-bits then the length of the instruction is _____ bits?

In above question: Each instruction must be stored in memory in a byte-aligned fashion. If a program has 200 instructions, then amount of memory required to store the program text is _____ bytes?

**Q.5** Consider a digital computer which supports 32 2-address instructions. Consider the address length is 8-bits. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 300 instructions, then amount of memory required to store the program text is _____ bytes?

**Q.6** A processor has 50 distinct instructions and 16 general purpose registers. Each instruction in system has one opcode field, 2 register operand field and a 10-bits memory address field. The length of the instruction is ____ bits?

**Q.7** A processor has 20 distinct instructions and 32 general purpose registers. A 24-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ____?

**Q.8** A processor has 20 distinct instructions and 32 general purpose registers. A 24-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ____?

In above question: Assume that immediate operand field is an unsigned number, What is its maximum and minimum value possible?

**Q.9** A processor has 20 distinct instructions and 32 general purpose registers. A 24-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ____?

In above question: Assume that immediate operand is a signed number. What is its minimum and maximum value?

**Q.10** Consider a computer which supports only 2-address and 1-address instructions. Each instruction is of 6-bits and each address is of 2-bits. If there are 3 2-address instructions supported by the system then maximum number of 1-address instructions supported by system is?

**Q.11** Consider a computer which supports only 2-address and 1-address instructions. Each instruction is of 6-bits and each address is of 2-bits. If there are 3 2-address instructions supported by the system then maximum number of 1-address instructions supported by system is?

In above instruction what is the range of number of 1-address instructions supported?

**Q.12** Consider a system with 24-bit instructions and 9-bit addresses. If there are 57 2-address instructions then maximum how many 1-address instructions can be formulated in the system?

**Q.13** Consider a system with 32-bit instructions and 12-bit addresses. If there are 254 2-address instructions then maximum how many 1-address instructions can be formulated in the system?

**Q.14** Consider a system with 32-bit instructions and 12-bit addresses. If there are 254 2-address instructions and 8000 1-address instructions then maximum how many 0-address instructions can be formulated?

**Q.15** Consider a system which supports 3-address and 2-address instructions both. It has 30-bit instructions with 8-bit addresses. If there are 'x' 3-address instructions then maximum how many 2-address instructions can be formulated?

**Q.16** Consider a system which supports 2-address and 1-address instructions both. It has 24-bit instructions with 10-bit addresses. If there are 4096 1-address instructions then maximum how many 2-address instructions can be formulated?

**Q.17** Consider a system with 16-bits instructions and 64 CPU registers. The System supported 2 types of instructions : Type-A and Type-B.

Type-A instructions have an opcode, one register operand and one immediate operand of 3-bits Type-B instructions have an opcode, and 2 register operands.

If there are 10 Type-B instructions supported by the system then maximum how many Type-A Instructions supported by the system?

**Q.18** Consider there are 3 types of instructions in system:

1. Register operand instructions: One opcode and 2 registers
2. Memory Operand instructions: One opcode, 1 register and 1 memory address
3. Immediate Operand Instructions: One opcode, 1 register and 1 immediate operand

Number of registers = 64

Number of bits in immediate operand = 10-bits

Memory size = 512Mbytes (byte addressable)

Total Instructions:

1. Reg Operand type: 10
2. Memory Operand type : 12
3. immediate Operand type : 4

Maximum and Minimum instruction length (when system supports variable length instructions), are?

**Q.19** In a simplified computer the instructions are:

| | |
|---|---|
| *OP* $R_i$, $R_j$ | Performs $R_i$ *Op* $R_j$ and stores the result in $R_j$ |
| *OP m*, $R_i$ | Performs *val Op* $R_i$ and stores the result in $R_i$ *val* denotes the content of memory location *m* |
| *MOV m*, $R_i$ | Moves the content of memory location m to register $R_i$ |
| *MOV* $R_i$, *m* | Moves the content of register $R_i$ to memory location *m* |

The computer has only two registers and OP is either ADD or SUB. Consider the following basic block:

t1 = a + b

t2 = c + d

t3 = e – t2

t4 = t1 – t3

**Q.20** Assume that all operands are initially in memory. The final value of the computation should be in memory. What is the minimum number of MOV instructions in the code generated for this basic block?

**Q.21** In a simplified computer the instructions are:

| | |
|---|---|
| *OP* $R_i$, $R_j$ | Performs $R_i$ *Op* $R_j$ and stores the result in $R_i$ |

| | |
|---|---|
| *OP* $R_i$ *,m* | Performs $R_i$ *OP val* and stores the result in $R_i$ *val* denotes the content of memory location *m* |
| *MOV m* , $R_i$ | Moves the content of memory location m to register $R_i$ |
| *MOV* $R_i$ , *m* | Moves the content of register $R_i$ to memory location *m* |

The computer has only two registers and OP is either ADD or SUB. Consider the following basic block:

t1 = a + b

t2 = c + d

t3 = e – t2

t4 = t1 – t3

**Q.22** Assume that all operands are initially in memory. The final value of the computation should be in memory. What is the minimum number of MOV instructions in the code generated for this basic block?

**Q.23** Consider a register-memory architecture system (2-address instructions). For this system the following intermediate code is going to be converted in machine code. Minimum how many registers are required in system so that the code can run without register spill?

Consider first operand is always the register operand and it's the destination for operation too.

t1 = X + Y

t2 = t1 – Z

t3 = t1 + t2

t4 = M + t3

Assume X, Y, Z and M are memory operands

**Q.24** Consider a system which support only 3 address instructions only, and supports 256B memory. If the instruction size is 40-bits then maximum & minimum number of instruction supported by the system are?

**Q.25** Consider a system which support only 2 address instructions only, and supports word addressable memory. The memory has total capacity of 2MB with word size of 4 Bytes. The system supports 350 distinct instructions. How many memory locations are required to store each instruction in the memory?

**Q.26** Consider a system which support only 2 address instructions only, and supports word addressable memory. The memory has total capacity of 2MB with word size of 4 Bytes. The system supports 350 distinct instructions. How many memory locations are required to store each instruction in the memory?

In the above question if a program is to be stored in the memory with 500 instructions, then the amount of memory required to store the entire program is _____ bytes?

**Q.27** The word addressable memory of a computer has 256K words of 32-bit each. The computer has an instruction format with four fields; an operation code field, a mode field to specify one of 8 addressing modes, a register address field to specify one of the 64 processor registers and a memory address field.

1. Specify the instruction format and the number of bits in each field if the instruction is stored exactly in one word in memory?
2. Maximum How many instructions supported by the computer?

**Q.28** A digital computer has a memory unit with 32-bits per word. The instruction set consists of 240 different operations. All the instructions have an operation code part (opcode) and an address part (allowed for only 1 address). Each instructions is stored in one word of memory.

1. How many bits are needed for opcode?
2. How many bits are left for address part of instruction?

3. What is the maximum allowable size of memory (word addressable)?

**Q.29** A computer supports only 3 address instructions with length 35-bits each. There are 129 distinct instructions supported by the system. If the memory used in the system is word addressable with word size of 32 bits. The maximum size memory supported by system is _____ KBytes?

**Q.30** Consider a system which supports 2-address and 1-address instructions. The system uses 16 bits instructions and 5-bits addresses. If there are total 32 2-address instructions then maximum how many 1-address instructions can be formulated?

**Q.31** Consider a system which supports 3-address, 2-address and 1 -address instructions. It has 32-bit instructions with 8-bits addresses. If there are 254 3-address instructions and 1024 1-address instructions then maximum how many 2-address instructions can be formulated?

**Q.32** Consider a system which supports 2-address, 1-address and 0-address instructions. It has 32-bit instructions with 13-bits addresses. If there are 16376 1-address instructions and 65536 0-address instructions then maximum how many 2-address instructions can be formulated?

**Q.33** Consider a system which supports 2-address, 1-address and 0-address instructions. The system has 6 bits addresses. If there are 10 2-address instructions, 364 1-address and 1280 0-address instructions then what is the size of instruction supported by system?

**Q.34** Consider a system which supports 2-address and 1-address instructions. The system has 18 bits instructions. If there are 7 2-address instructions and 1152 1-address instructions, then what is the maximum size of memory supported by system?

**Q.35** Consider a system which support only 3 address instructions only, and supports 256B memory. If the instruction size is 40-bits then maximum & minimum number of instruction supported by the system are?

**Q.36** Consider a system which support only 2 address instructions only, and supports word addressable memory. The memory has total capacity of 2MB with word size of 4 Bytes. The system supports 350 distinct instructions. How many memory locations are required to store each instruction in the memory?

**Q.37** Consider a system which support only 2 address instructions only, and supports word addressable memory. The memory has total capacity of 2MB with word size of 4 Bytes. The system supports 350 distinct instructions. How many memory locations are required to store each instruction in the memory?

In the above question if a program is to be stored in the memory with 500 instructions, then the amount of memory required to store the entire program is _____ bytes?

**Q.38** There is system which uses 32-bits instructions and 13-bits addresses. It supports 2- address and 1-address instructions both. Suppose there are 50 2-address instructions then maximum how many 1-address instructions can be formulated?

**Q.39** There is system which uses 32-bits instructions and 13-bits addresses. It supports 2- address 1-address and 0-address instructions. Suppose there are 60 2-address instructions and 214 1-address instructions then maximum how many 0-address instructions can be formulated?

**Q.40** There is system which uses 20 bits instructions and 8-bits addresses. It supports 2-address and 1-address instructions both. Suppose there are x 2-address instructions, and based on that maximum & minimum 1-address

instructions can be a, b respectively. Then the maximum value of a – b is?

**Q.41** Consider a system which supports 2-address, 1-address and 0-address instructions. The system has 'i' bits instructions and 'a' bits addresses. If there are 'x' 2-address instructions and 'y' 1-address instructions then which of the following is correct for maximum number of 0-address instructions supported by system?

(A) $2^i - 2^a x - y$ (B) $2^i - 2^{2a} x - y$

(C) $2^i - 2^{2a} x - y2^a$ (D) $2^i - 2^a x - y2^a$

**Q.42** Consider a system which supports 2-address, 1-address and 0-address instructions. The system has 'a' bits instructions and supports 2m bytes memory. If there are 't' 2-address instructions and 'w' 1-address and 'z'0-address instructions, then which of the following expression is correct?

(A) $2^a = 2^m t + w + z$

(B) $2^a = 2^{2m} t + 2^m w + z$

(C) $2^a = 2^{3m} t + 2^{2m} w + 2^m z$

(D) $2^a = 2^{2m} t + 2^m w - z$

**Q.43** A CPU has 128 registers, 64KB byte addressable memory and 3Bytes instructions. The CPU supports 3 types of instructions: R-type, I-type and M-type. Each R-type instruction contains an opcode and 2 register names. Each I-type Instruction contains an opcode, a register name and a 9-bit immediate value. Each M-type instruction contains an opcode and a memory address. If there are 85 M-type instructions, 123 I-type instructions then maximum how many R-type instructions the CPU can support?

**Q.44** Consider an AC-based architecture system. For this system the following intermediate code is going to be converted in machine code. Minimum how many registers are required in system so that the code can run without register spill?

Consider second operand can be a register or memory operand

t1 = X + Y
t2 = t1 – Z
t3 = t1 + t2
t4 = t3 + M

Assume X, Y, Z and M are memory operands

**Q.45** Consider there are 4 types of instructions in system:

Type 1: One opcode and 2 registers
Type 2: One opcode and 1 register
Type 3: One opcode and 1 memory address
Type 4: One opcode, 1 register and 1 memory address
Number of registers = 128
Maximum instruction length: 32bits (Variable length instructions)
Total Instructions:
Type-1: 15, Type-2: 20, Type-3: 12, Type-4: 14
Memory address size = _____ bits

**Q.45** Consider a register-based architecture system which can support maximum 2-address instructions. For this system the following intermediate code is going to be converted in machine code. Minimum how many registers are required in system so that the code can run without register spill?

t1 = X + Y
t2 = Z * 2
t3 = t2 + A
t4 = t3 – t1
t5 = t4 + t3

Note: X, Y and Z are memory operands

**Q.46** Consider a register-memory architecture (2-address instructions supported) system. For this system the following intermediate code is going to be converted in machine code. Minimum how many registers are required in system so that the code can run without register spill?

t1 = X + Y
t2 = t1 – Z
t3 = t1 + t2
t4 = M + t3
t5= t2 – t4

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# 4 Addressing Modes

**Q.1** Find operand and effective address for all given addressing modes in the table?

| | Memory | | |
|---|---|---|---|
| 200 | Opcode | Mode | PC = 200 |
| 201 | Address = 500 | | |
| 202 | Next Instruction | | |
| | | | |
| 399 | 450 | | R500=400 |
| 400 | 700 | | |
| | | | |
| 500 | 800 | | XR=100 |
| | | | |
| 600 | 900 | | AC |
| | | | |
| 702 | ..... | | |
| | | | |
| 800 | 300 | | |

| Mode | Effective Address | Operand |
|---|---|---|
| 1. Immediate Mode | | |
| 2. Direct Mode | | |
| 3. Indirect Mode | | |
| 4. Register Mode | | |
| 5. Register Indirect Mode | | |
| 6. Autodecrement Mode | | |
| 7. Indexed Mode | | |
| 8. PC- Relative Mode | | |

**Q.2** An instruction is stored at Location 300 with its address field at location 301. The address field has the value 400. A processor register contains the number 150. Evaluate the effective address, if addressing mode is:

(A) Direct
(B) Immediate
(C) Relative
(D) Register Indirect

**Q.3** In case the code is position independent, the most suitable addressing mode is

(A) Direct mode (B) Indirect mode
(C) Relative mode (D) Indexed mode

**Q.4** The addressing mode that permits relocation, without any change whatsoever in the code, is

(A) Indirect addressing
(B) Base register addressing
(C) Indexed addressing
(D) PC relative addressing

**Q.5** A relative branch mode type instruction is stored in memory at address 300. The branch is made to an address 450.

1. What should be the value of relative address field of the instruction?
2. Determine the value of PC before instruction fetch, after the fetch and after execution phase?

**Q.6** Consider a hypothetical processor with an instruction of type LW R1. 20(R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register

R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for operand in memory?

(A) Immediate Addressing
(B) Register Addressing
(C) Register Indirect Scaled Addressing
(D) Base Indexed Addressing

**Q.7** Consider a three word machine instruction

ADD A[R0], @ B

The first operand (destination) "A [RO]" uses indexed addressing mode with R0 as the index register. The second operand (source) "(5) B" uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

The number of memory cycles needed during the execution cycle of the instruction is

**[GATE 2005]**

**Q.8** Consider the following:

1. Operation code
2. Source operand reference
3. Result operand reference
4. Next instruction reference

Which of the above are typical elements of machine instructions?

(A) 1, 2 and 3 only (B) 1, 2 and 4 only
(C) 3 and 4 only (D) 1, 2, 3 and 4

**Q.9** Which addressing mode helps to access table data in memory efficiently?

(A) Indirect mode
(B) Immediate mode
(C) Auto-increment or Auto-decrement mode
(D) Index mode

**Q.10** An addressing mode in which the location of the data is contained within the mnemonic, is known as

(A) Immediate addressing mode
(B) Implied addressing mode
(C) Register addressing mode
(D) Direct addressing mode

**Q.11** The addressing modes used for source operand in the following instructions are respectively?

(1) R1 ← #5
(2) R1 ← M[5000]
(3) R1 ← M[R2]

(A) Implied, direct, register
(B) Implied, direct, register indirect
(C) Immediate, direct, register indirect
(D) Immediate, direct, register

**Q.15** Consider a PC-relative mode type branch instruction which takes branch on address 770 in memory. The instruction has offset value 150. What is the address of this instruction in memory, if each instruction is stored in memory on 4 locations?

**Q.16** Consider a 6-words instruction, which is of the following type:

| Opcode | Mode 1 | Mode 2 | Address1 | Address 2 |
|---|---|---|---|---|

The first operand (destination) uses register indirect mode and second operand uses indirect mode. Assume each operand is of size 2 words, each address is of 2 words and main memory takes 50ns for 1 byte access. Each word size is 2 bytes. Further assume that the opcode denotes addition operation which copies result of addition of 2 operands.

Total time required in:

(1) Fetch cycle of instruction
(2) Execution cycle of instruction
(3) Instruction cycle of instruction

**Q.17** Which of the following addressing mode(s) is/are used for accessing the array element from memory?

(A) Scaled Mode
(B) Indexed Mode
(C) Base Register Mode
(D) Autodecrement Mode

**Q.18** Which of the following can be the value(s) of PC immediately after the fetch of an instruction which is stored on a location 400?

(A) 400 (B) 399
(C) 401 (D) 402

**Q.19** Consider the system in which in fetch cycle complete instruction is fetched. Which of the following addressing modes do(es) not require memory access for operand after fetch cycle?

(A) Register Mode
(B) Register Indirect Mode
(C) Indirect Mode
(D) Indexed Mode

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# 5 CPU and Control Unit

**Q.1** Consider two processors P1 and P2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P1. If the clock frequency of P1 is 1GHz, then the clock frequency of P2 (in GHz) is _____?

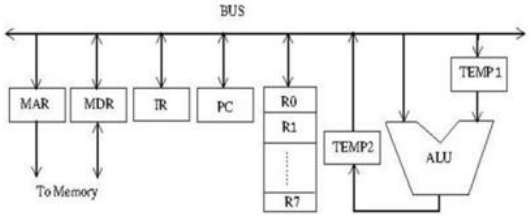
**[GATE 2014]**

**Q.2** Consider a CPU with clock rate of 200MHz. If the CPU has average CPI of 5 then average instruction execution time is?

**Q.3** A CPU runs on 500MHz clock rate and is executing a program which consists 1000 instructions. If the measured average CPI (Cycles per instructions) for the program is 6 then total time required to run the program on CPU is _____microseconds?

**Q.4** A CPU is used for executing n instructions. For executing these n instruction CPU has taken 6 cycles per instruction on average. The CPU operates on 2GHz clock rate. The CPU takes total of 0.75 microseconds to execute these n instructions. Later the same CPU used for executing 2n number of instructions and for executing 2n instructions its CPI (Cycles per Instruction) has been reduced to 5. Total time required by CPU to execute 2n instructions is _____ microseconds (correct up to 2 decimal places)?

**Q.5** Consider the following data path diagram **[GATE 2020]**




**Q.6** Consider an instruction: $R0 \leftarrow R1 + R2$. The following steps are used to execute it over the given data path. Assume that PC is incremented appropriately. The subscripts r and w indicate read and write operations, respectively.

1. $R2_r$, $TEMP1_r$ $ALU_{add}$, $TEMP2_w$
2. $R1_r$, $TEMP1_w$
3. $PC_r$, $MAR_w$, $MEM_r$
4. $TEMP2_r$, $R0_w$
5. $MDR_r$, $IR_w$

Which one of the following is the correct order of execution of the above steps?

**[GATE 2020]**

(A) 2,1,4,5,3 (B) 1,2,4,3,5

(C) 3,5,2,1,4 (D) 3,5,1,2,4

**Q.7** A hardwired CPU uses 10 control signals S1 to S10, in various time step T1 to T5 to implement 4 instruction I1 to I4 as show below:

| | T1 | T2 | T3 | T4 | T5 |
|---|---|---|---|---|---|
| I1 | S1,S3,S5 | S2,S4,S6 | S1,S7 | S10 | S3,S8 |
| I2 | S1,S3,S5 | S8,S9,S10 | S5,S6,S7 | S6 | S10 |
| I3 | S1,S3,S5 | S7,S8,S10 | S2,S6,S9 | S10 | S1,S3 |
| I4 | S1,S2,S5 | S2,S6,S7 | S5,S10 | S6,S9 | S10 |

Which of the following pairs of expressions represent the circuit for generating control signals S5 and S10 respectively

**[GATE 2005]**

(A) S5=T1+I2.T3 and
S10 = (I1+I3).T4+(I2+I4).T5

(B) S5+T1+(I2+I4).T3 and
S10=(I1+I3).T4+(I2+I4).T5

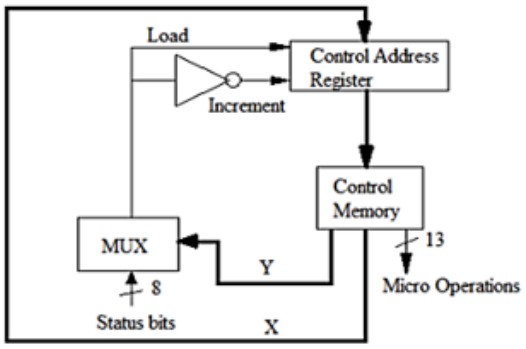
(C) S5+T1+(I2+I4).T3 and
S10=(I2+I3+I4).T3 and S10
= (I2+I3+I4). T2+(I1+I3) . T4+ (I2+I4).T5

(D) S5=T1+(I2+I4).T3 and S10 = (I2+I3). T2+I4. T3+(I1+I3).T4+(I2+I4).T5

**Q.8** The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction

is divided into three fields: a micro-operation field of 13 bits, a next address field (X) and a MUX select field (Y)

There are 8 status bits in the input of the MUX




How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?

**[GATE 2002]**

(A) 10, 3, 1024 (B) 8,5, 256

(C) 5, 8, 2048 (D) 10, 3, 512

**Q.9** A CPU has only three instruction I1, I2, and I3 which use the following signals in time step T1-T5

I1: T1 : Ain, Bout, Cin

T2: PCout, Bin

T3: Zout, Ain

T4: Bin, cout

T5: End

I2: T1: Cin, Bout, Din

T2: Aout, Bin

T3: Zout, Ain

T4: Bin, Cout

T5: End

I3: T1: Din, Aout

T2: Ain, Bout

T3: Zout, Ain

T4: Dout, Ain

T5: End

Which of the following logic function will generate the hardwired control for the signal Ain?

**[GATE 2004]**

(A) T1.I1+T2.I3+T4.I3+T3

(B) (T1+T2+T3).I3+T1.I1

(C) (T1+T2).I1+(T2+T4).I3+T3

(D) (T1+T2).I2+(T1+T3).I1+T3

**Q.10** An instruction set of a processor has 125 signals which can be divided into 5 groups of mutually exclusive signals as follows:

Group 1 : 20 signals, Group 2 : 70 signals, Group 3 : 2 signals, Group 4 : 10 signals, Group 5 : 23 signals.

How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming?

(A) 0 (B) 103

(C) 22 (D) 55

**Q.11** A control unit generates 120 control signals, which are divided into 6 groups of mutually exclusive signals as below:

Group1 = 30

Group2 = 13

Group3 = 12

Group4 = 3

Group5 = 27

Group6 = 35

How many bits can be saved by using vertical micro-programmed control unit as compared to horizontal one?

**Q.12** A micro-programmed control unit is required to generate a total of 25 control signals. Assume that during any microinstruction at most 2 control signals are active. Minimum number of bits required in the control word to generate the required control signals will be?

**Q.13** Consider a microprogrammed control unit which has to support 64 number of instructions. For each instruction execution control unit generates a sequence of 32 control words. Each microinstruction contains 3 fields: 137 control signals to support horizontal control unit, a MUX select field to select one of 16 inputs, and a next address field. The size of control memory needed is?

**Q.14** Design of a vertical microprogrammed control unit requires to generate 40 signals. Out of first 34 those only 3 signals can be active at a time. And for

remaining 6, anyone can be active anytime. The microinstruction of the control unit stores control signal information along with 3-bit mux select and 10-bits address field. The size of control memory required is?

**Q.15** Consider a processor with byte-addressable memory. Assume that all registers, including program counter (PC) and Program Status Word (PSW), are size of two bytes. A stack in the main memory is implemented from memory location $(0100)_{16}$ and it grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is $(016E)_{16}$. The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:

- Store the current value of PC in the stack
- Store the value of PSW register in the stack
- Load the statring address of the subroutine in PC

The content of PC just before the fetch of a CALL instruction is $(5.FA0)_{16}$. After execution of the CALL instruction, the value of the stack pointer is:

**[GATE 2015]**

(A) $(016A)_{16}$ (B) $(016C)_{16}$
(C) $(0170)_{16}$ (D) $(0172)_{16}$

**Q.16** The main difference(s) between a CISC and a RISC processor is/are that a RISC processor typically

**[GATE 1999]**

(A) Has fewer instructions
(B) Has fewer addressing modes
(C) Has more registers
(D) Is easier to implement using hard-wired logic

**Q.17** Consider the following processor design characteristics:

I. Register-to-register arithmetic operations only
II. Fixed-length instruction format
III. Hardwired control unit

Which of the characteristics above are used in the design of a RISC processor?

**[GATE 2018]**

(A) I and II only (B) II and III only
(C) I and III only (D) I, II and III

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# 6 IO Organization

**Q.1** How many 8-bit characters can be transmitted per second over 9600 baud serial communication link using a parity synchronous mode of transmission with 1 start bit, 8 data bits, 2 stop bits and 1 parity bit?

**Q.2** An asynchronous serial communication is employing 8 character bits, 1 parity bit, 2 start bits and 1 stop bit. To maintain a rate of 700 char/sec the minimum transfer rate should be required is _____ bits/sec?

**Q.3** How many 8-bit characters can be transmitted using a parity synchronous mode of transmission with 1 start bit, 8 data bits, 2 stop bits and 1 parity bit.

1. What is the efficiency of the transmission line?
2. If the transfer rate of the line is 2000 bits per second, then effective transfer rate is?

**Q.4** Consider a device which operates with 50KBPS operating speed. The device is operating on program control mode of IO and it has to transfer data of 10B from it. The data is transferred byte wise. Size of status register is 2Bytes. Total time needed to perform the data transfer is _____ microseconds?

(Note: The status is checked only once, in the beginning)

**Q.5** The following are some events that occur after a device controller issues an interrupt while process L is under execution.

- P. The processor pushes the process status of L onto the control stack
- Q. The processor finishes the execution of the current instruction
- R. The processor executes the interrupt service routine
- S. The processor pops the process status of L from the control stack
- T. The processor loads the new PC value based on the interrupt

Which of the following is the correct order in which the events above occur?

(A) QPTRS (B) PTRSQ
(C) TRPQS (D) QTPRS

**Q.6** Consider a CPU which takes 0.05 microseconds as interrupt overhead time when a device generates interrupt for CPU, and CPU accepts it. After that CPU takes 6 cycles to service the interrupt. If CPU runs on 10MHz clock rate then total time CPU spends for interrupt service is _____ microseconds?

**Q.7** A device with data transfer rate 20 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 10 microsecond.

1. Total time required in programmed IO for 10 bytes data transfer?
2. Total time required in interrupt IO for 10 bytes data transfer?
3. What is the minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode?

**Q.8** Consider a device operating on 1MBPS speed and transferring the data to memory using cycle stealing mode of DMA. If it takes 2 microseconds to transfer 16 bytes data to memory when it is ready/prepared. Then percentage of time CPU is blocked due to DMA is?

**Q.9** A hard disk with a transfer rate of 10 Mbytes/ second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation? **[GATE 2004]**

(A) 5.0% (B) 1.0%
(C) 0.5% (D) 0.1%

**Q.10** On a non-pipelined sequential processor, a program segment, which is the part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.

Initialize the address register
Initialize the count to 500
LOOP:Load a byte from device
Store in memory at address given by address register
Increment the address register
Decrement the count
If count !=0 go to LOOP

Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.

The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory.

What is the approximate speed up when the DMA controller based design is used in a place of the interrupt driven program based input-output?

**[GATE 2011]**

**Q.11** The DMA controller has data count register of size 8-bits. The memory is byte addressable. The maximum number of bytes the DMA can transfer to memory at a time without giving the control of the buses back to CPU?

**Q.12** The DMA controller has data count register of size 8-bits. The memory is byte addressable.

1. Minimum how many times DMA needs to take control from CPU to transfer a file of 500 bytes?
2. Minimum how many times DMA needs to take control from CPU to transfer a file of 15K bytes?

**Q.13** The size of the data count register of a DMA controller is 16bits. The processor needs to transfer a file of 29,154 kilobytes from disk to main memory.

The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____.

**[GATE 2016]**

**Q.14** A device with data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 4 microsecond. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode?

**Q.15** CPU can select a specific IO device for communication through?

(A) Address Bus (B) Data Bus
(C) Control Bus (D) None

**Q.16** Which of the following is connected to CPU directly

(A) Keyboard (B) Hard-disk
(C) RAM (D) All

**Q.17** Which of the following is/are true?

1. Data format used in IO devices may differ from CPUs format
2. IO devices are slower than CPU
3. IO devices are slower than main memory

(A) Only 1 (B) Only 1 & 2
(C) Only 1 & 3 (D) All 1, 2 & 3

**Q.18** Which of the following functionalities are provided by IO processor?

1. IO interfacing
2. DMA controller
3. IO Instruction execution

(A) Only 1 (B) Only 1 & 2
(C) Only 1 & 3 (D) All 1, 2 & 3

**Q.19** Which of the following is true regarding IO mapped IO as compared to memory mapped IO?

1. ALU operation can not be performed on IO data directly
2. IO devices have their own address space
3. Less number of Instructions to access IO
4. Less number of IO devices connected

(A) Only 2 & 3 (B) Only 2 & 4
(C) Only 2, 3 & 4 (D) All 1, 2, 3 & 4

**Q.20** Which of the following is true regarding memory mapped IO as compared to IO mapped IO?

1. ALU operation can not be performed on IO data directly
2. IO devices do not have their own address space
3. Some memory wastage
4. More number of IO devices connected

(A) Only 2 & 3 (B) Only 2 & 4
(C) Only 2, 3 & 4 (D) All 1, 2, 3 & 4

**Q.21** Consider a serial asynchronous transmission line which uses 1 start bit and 2 stop bits along with 8 bits data. The efficiency of the line is _____ %?

**Q.22** Consider a device operating on 8MBPS speed and transferring the data to memory using cycle stealing mode of DMA. If it takes 250 nanoseconds to transfer 16 bytes data to memory when it is ready/prepared. Then percentage of time CPU is blocked due to DMA is?

**Q.23** A device is constantly transferring the data with 20KBPS speed to memory using DMA. Assume that the transmission time to memory from IO once the data (1 byte) is ready is 5microseconds. Further assume that a file of 5KB needs to be transferred to memory.

1. % of time CPU is blocked due to DMA in burst mode
2. % of time CPU is blocked die to DMA in Cycle stealing mode

**Q.24** Which of the following is/are true?

(A) Any IO operation can be performed always after current instruction execution in CPU

(B) DMA controller can start data transfer immediately after getting DMA request from IO

(C) CPU generates memory read/write signal for DMA transfer

(D) CPU generates Interrupt acknowledgement immediately after receiving the interrupt always.

**Q.25** If a word preparation time in IO device and word transfer time to memory from IO device are same. Then?

(A) 100% time CPU is blocked due to DMA in cycle stealing mode

(B) 50% time CPU is blocked due to DMA in cycle stealing mode

(C) 100% time CPU is blocked due to DMA in burst mode

(D) 50% time CPU is blocked due to DMA in burst mode

**Q.26** Consider a DMA controller which has data count register of size 6-bits. A file is to be transferred using DMA controller from IO to memory of size 12KB. Select True statement(s)?

(A) Maximum time DMA controller will take control from CPU is 196

(B) Minimum time DMA controller will take control from CPU is 196

(C) Minimum time DMA controller will take control from CPU is 1

(D) Minimum time DMA controller will take control from CPU is 195

**Q.27** Which of the following is/are not false?

(A) DMA controller is a special purpose processor

(B) CPU can perform some operation during DMA transfer

(C) CPU can enable DMA hold acknowledgement after instruction fetch cycle

(D) DMA transfer stops when starting address becomes zero

**Q.28** Which of the following is/are true?

(A) DMA transfer is always faster than interrupt IO

(B) Interrupt IO is always faster than programmed IO

(C) A system can use either DMA transfer mode or Interrupt IO for data transfer between memory and IO

(D) DMA can transfer the data from IO to CPU also.

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# 7 Memory Management

**Q.1** Memory is represented as?
(A) A×B where A = No. of memory locations, B = No. of bits in each location
(B) $2^a$×B where a = No. of address bits, B = No. of bits in each location
(C) B×A where, B = No. of bits in each location, A = No. of memory locations
(D) (A) & (B) both

**Q.2** A memory has 14-bits address bus. Then how many memory locations are there?
(A) 16K (B) 16384
(C) $2^{14}$ (D) All

**Q.3** The memory cycle time of a memory is 500nsec. The maximum rate with which the memory can be accessed?
Note: Consider memory as byte addressable.
(A) 500 Bytes / Sec
(B) 2000 Bytes / Sec
(C) 2 Mbytes / Sec
(D) 2 GBytes / Sec

**Q.4** A processor can support a maximum memory of 4 GB, where the memory is word addressable (a word consists of two bytes). The size of the address bus of the processor is at least _____ bits?

**[GATE 2016]**

**Q.5** Consider a memory of size 2K × 8-bits. What is the size of decoder needed to access the cells of the memory uniquely?

If there are m input lines n output lines for a decoder that is used to uniquely address a byte addressable 1 KB RAM, then the minimum value of m+n is _____?

**[GATE 2020]**

**Q.6** Consider 2 4-bits unsigned values A and B. What will be the maximum size of result for :
1. Addition of A and B
2. Multiplication of A and B

**Q.7** The amount of ROM needed to store the table for multiplication of two 4-bit unsigned integer is?
(A) 64 bits (B) 128 bits
(C) 1 K bits (D) 2 K bits

**Q.8** A ROM chip of $2048 \times 16$ bits has four select inputs and operates from a 5-volt power supply. How many pins are needed for the IC package?

How many 64 bytes RAM chips are needed to provide a memory capacity of 1K bytes?

**Q.9** Total memory capacity is _____ Mbytes, if we use 16 chips of size 512Kbytes each?

**Q.10** How many 32 K × 1 RAM chips are needed to provide a memory capacity of 256K bytes?
(A) 8 (B) 32
(C) 64 (D) 128

**[GATE 2009]**

**Q.11** (a) How many $128 \times 8$ bits RAM chips are needed to provide a memory capacity of 2048 bytes?
(b) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?
(c) How many lines must be decoded for chip select? Specify the size of decoder?

**Q.12** How many $128 \times 8$ bits RAM chips are needed to provide a memory capacity of $128 \times 16$ bits?

**Q.13** How many 32K × 1 RAM chips are needed to provide a memory capacity of 256 K bytes?
(A) 8 (B) 32
(C) 64 (D) 128

**[GATE 2009]**

**Q.14** Consider a DRAM which can be refreshed in 10ns. The refresh period is 0.05 microseconds.
1. % of time taken in refresh?
2. % of time remaining for read write is?

**Q.15** A main memory unit with a capacity of 4 megabytes is built using 1M × 1-bit DRAM chips. Each DRAM chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is?

(A) 100 nanoseconds

(B) $100\times2^{10}$ nanoseconds

(C) $100\times2^{20}$ nanoseconds

(D) $3200\times2^{20}$ nanoseconds

**[GATE 2010]**

**Q.16** Consider a main memory system that consists of 8 memory modules attached to the system bus, which is one word wide. When a write request is made, the bus is occupied for 100 nanoseconds (ns) by the data, address, and control signals. During the same 100 ns, and for 500 ns thereafter, the addressed memory module executes one cycle accepting and storing the data. The (internal) operation of different memory modules may overlap in time, but only one request can be on the bus at any time. The maximum number of stores (of one word each) that can be initiated in 1 millisecond is ____?

**[GATE 2014]**

**Q.17** The memory cycle time of a memory is 500nsec. The maximum rate with which the memory can be accessed?

**Note :** Consider memory as byte addressable.

(A) 500 Bytes / Sec

(B) 2000 Bytes / Sec

(C) 2 Mbytes / Sec

(D) 2 GBytes / Sec

**Q.18** The address bus width of a memory of size 4096×8 bits is?

(A) 10 (B) 11

(C) 12 (D) 13

**Q.19** A memory M is defined as number of words multiplied by the number of bits per word. The number of address and data lines needed for the memory M = 2K × 32 bits are?

(A) 10 address, 32 data lines

(B) 11 address, 8 data lines

(C) 11 address, 32 data lines

(D) 32 address, 12 data lines

**Q.20** Consider a memory which has 0.2GBPS writing rate. What is the memory access time?

(A) 2ns (B) 5ns

(C) 10ns (D) 20ns

**Q.21** Once a memory operation is performed then to make itself ready for the next operation memory takes 0.5ns. From the previous question what should be the memory cycle time?

(A) 2.5 ns (B) 5.5 ns

(C) 10.5 ns (D) 20.5 ns

**Q.22** Consider a memory of size 4GB, what should be size of address bus if memory is?

1. Byte addressable
2. Word addressable (1 word = 2 words)
3. Word addressable (1 word = 8 words)

**Q.23** Consider a memory with maximum size of X bytes. Memory is word addressable with word size of w bytes. The size of the address bus of the processor is at least _____ bits?

(A) $\text{Log}_2(X/W)$ (B) $2^{(x/w)}$

(C) X/W (D) $\text{Log}_2(X)$

**Q.24** A CPU has 16-bit address bus and 8-bits data bus. The maximum size of memory supported by the system is?

**Q.25** When the power supply of ROM is switched off, its content?

(A) Become all zeros

(B) Become all ones

(C) Remain Same

(D) Become Garbage (Unpredictable)

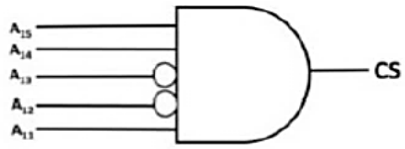
**Q.26** **Statement 1 :** Static RAM memory devices retain data for as long as power is supplied.

**Statement 2 :** Statis RAM is used when the size of read/write memory required is large

(A) Both statements are correct
(B) Only 1 is correct
(C) Only 2 is correct
(D) Both are incorrect

**Q.27** The amount of ROM needed to store the table for multiplication of two 8-bit unsigned integer is?
If there are m input lines n output lines for a decoder that is used to uniquely address a byte addressable S-KB RAM, if the value of m is 12 then
1. The value of n is?
2. The value of S is _____?

**Q.28** The chip select logic for a certain DRAM chip in a memory system design is shown below. Assume that the memory system has 16 address lines denoted by A15 to A0. What is the range of address (in hexadecimal) of the memory system that can get enabled by the chip select (CS) signal?




(A) C800 to CFFF (B) CA00 to CAFF
(C) C800 to C8FF (D) DA00 to DFFF

**Q.29** How many $8K \times 8$ bits RAM chips are needed to provide a memory capacity of $64K \times 16$ bits? And how the chips are arranged?

**Q.30** A 64-bits wide main memory unit with a capacity of 4GB is built using $256M \times$ 16-bits RAM chips. How many chips are required to construct such memory and how are the chips arranged?

**Q.31** A 32-bits wide main memory unit with a capacity of 16GB is built using $128M \times$8-bits RAM chips. If there are x-horizontal arrangements of chips are there, with y number of chips in each horizontal arrangement then the value of 10x+y is?

**Q.32** A RAM chip has a capacity of 1024 words of 8 bits each (1K × 8). The number of 2×4 decoders with enable line needed to construct a 16K × 16 RAM from 1K × 8 RAM is _____? **[GATE 2013]**

**Q.33** A 32KB RAM is formed by 16 numbers of a particular type of SRAM IC. If each IC needs 14 address bits, what is the IC capacity?
(A) 32 kbits (B) 16 kbits
(C) 8 kbits (D) 4 kbits

**Q.34** A 32–bit wide main memory unit with a capacity of 1 GB is built using 256M X 4-bit DRAM chips. The number of rows of memory cells in the DRAM chip is $2^{14}$. The time taken to perform one refresh operation is 50 nanoseconds. The refresh period is 2 milliseconds. The percentage (rounded to the closet integer) of the time available for performing the memory read/write operations in the main memory unit is _____?

**[GATE 2018]**

**Q.35** A DRAM chip of $512K \times 8$ bits has 256 rows of cells with 2 k cells in each row. If DRAM takes 20ns for 1 refresh then total refresh time of the DRAM is _____ Microseconds?

**Q.36** A DRAM chip of $64M \times 16$ bits has 128K rows of cells y cells in each row. If DRAM takes x-ns for 1 refresh then total refresh time of the DRAM is _____ Microseconds, if x = 2 * $\log_2$y?

**Q.37** A DRAM chip of $256K \times 8$ bits has x rows of cells with y cells in each row? If DRAM takes 20ns for 1 refresh and 2.56 milliseconds for entire chip refresh then the value of x+y is _____?

❑❑❑

# 8 Cache Memory

**Q.1** Assume that for a certain processor, a read request takes 200 nanoseconds o n a cache miss and 25 nanoseconds on a cache hit. Suppose while running a p rogram, it was observed that 60% of th e processor's read requests result in a cache hit. The average read access tim e in nanoseconds is_____?

**Q.2** In a two-level hierarchy, if the top level has an access time of 8 ns and the bottom level has an access time of 60 ns, what is the hit rate on the top level required to give an average access time of 10ns?

**Q.3** In previous question if hit rate of the top-level memory is 100%, then the access time of bottom level memory will be _____ns?

**Q.4** A computer system contains a cache. Uncached memory access takes 7 times longer than access to cache. If cache has a hit ratio 0.9. The ratio of cached memory access time to uncached memory access time is?

**Q.5** In a two-level hierarchy, the top level has an access time of 10 ns and hit rate of 90%. If the block transfer from main memory to cache takes 500ns in case of miss then average memory access time is _____?

**Q.6** A direct mapped cache memory of 1 MB has a block size of 256 bytes. The cache has an access time of 3 ns and a hit rate of 94%. During a cache miss, it takes 20ns to bring the first word of a block from the main memory, while each subsequent word takes 5 ns. The word size is 64 bits. The average memory access time in ns (round off to 1 decimal place) is _____ ?

**[GATE 2010]**

**Q.7** What hit rate is required for cache to reduce the effective memory access time from 200ns to 65ns if cache access time is 50ns?

**Q.8** A computer system has a cache with cache access time Tc = 10ns, hit ratio of 80% and average memory access time of Tm = 20ns. The access time for physical memory Tp is _____ ns?

**[ESE 2017]**

**Q.9** A computer uses 32-bit architecture. In a memory system, the cache has an access time of 15 ns and the byte addressable main memory has an access time of 100 ns, the hit rate of the cache is 90%. If the block size of cache is 32words then average memory access time is _____?

(**Note :** Consider the system uses Locality of Reference)

**Q.10** A cache line has 128 bytes. The main memory has addressing latency 64ns and access bandwidth 1GB/s. The time required to fetch the entire cache line from the main memory is _____ ns?

**[ESE 2017]**

**Q.11** Consider a system using a cache. The cache is having 70% hit ratio and is 9 times faster than main memory. The average memory access time then/ increased due to some program execution and the new one is 40% more than older one of 90ns. What is the hit ratio of new cache design?

**Q.12** Consider a memory hierarchy which takes 500 nanoseconds for access when there is a miss in cache and takes 100 nanoseconds for access when there is a hit in cache. Assume if among all memory references 90% of the references are having a hit on cache then average memory access time is _____ nanoseconds?

**Q.13** A computer uses 32-bit architecture. In a memory system, the cache has an access time of 20 ns and the byte addressable main memory has an access time of 200 ns, the hit rate of

the cache is 90%. If the block size of cache is 16 words then average memory access time (rounded up to 1 decimal place)is _____ microseconds?

**Note :** In case of miss, a block is acces sed from main memory

**Q.14** Consider a memory system which includes new cache. The cache access time is 50ns. The hit rate is needed at cache to reduce the average memory access time from 250ns to 80ns if cache is used; is _____ %?

**Q.15** Assume that for a certain processor, a read request takes 50 nanoseconds on a cache miss and 5 nanoseconds on a cache hit. Suppose while running a program, it was observed that 80% of the processor's read requests result in a cache hit. The average read access time in nanoseconds is _____?

**Q.16** A system has a write through cache with access time of 100ns and hit ratio of 90%. The main memory access time is 1000ns. The 70% of memory references are for read operations.

1. Average memory access time for read operations only
2. Average memory access time for write operations only
3. Average memory access time for read-write operations both
4. Effective Hit ratio

**Q.17** The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations; 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is?

**[GATE 2014]**

**Q.18** A memory hierarchy has a write through cache with access time of 60ns and hit ratio of 80%. The main memory access time is 500ns. The 75% of memory references are for read operations.

1. Average memory access time for read operations only
2. Average memory access time for write operations only
3. Average memory access time for read-write operations both
4. Effective Hit ratio

**Q.19** Consider system with a write back cache. The cache has an access time of 10ns. 90% of the all memory accesses are referring only cache. The main memory block access time is 750ns. The 15% of the cache blocks are only needed write back. Calculate the average memory access time?

**Q.20** Consider a write through cache which can provide only 63.75% of effective hit rate. If among all memory references 75% references are for read then what is the hit ratio of cache for only read operations?

**Q.21** Consider a write through cache which can provide only 61.92% of effective hit rate. If among all memory references 28% references are for write then what is the hit ratio of cache for only read operations?

**Q.22** Size of data sent to main memory from CPU :

1. For write hit, when a write through cache is used?
2. For write miss, when a write through cache is used?
3. For write hit, when a write back cache is used?
4. For write miss, when a write back cache is used?

**Q.23** Size of data sent from main memory to cache (write allocate):

1. For write hit, when a write through cache is used?
2. For write miss, when a write through cache is used?

3. For write hit, when a write back cache is used?
4. For write miss, when a write back cache is used?

**Q.24** Size of data sent from main memory to cache ( no write allocate):

1. For write hit, when a write through cache is used?
2. For write miss, when a write through cache is used?
3. For write hit, when a write back cache is used?
4. For write miss, when a write back cache is used?

**Q.25** The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations; 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is?

**[GATE 2014]**

**Q.26** Consider a direct mapped cache of size 64KB with block size 16 Bytes. The CPU generates 32 bit addresses.

1. Number of bits for byte offset?
2. Number of blocks in cache?
3. The number of bits needed for cache indexing?
4. The number of tag bits?
5. Tag Directory size?

**Q.27** Consider a direct mapped cache of size 32KB. The CPU generates 32 bit addresses. The number of tag bits in main memory address are?

Block Size = 16 bytes
Size of Cache memory = 128 KB
Size of Main memory address = 34-bits
Direct Mapping
For each block apart from tag 1 valid bit and 1 modifies bit are stored in cache
Bits in byte offset?
Bits in cache block number?
Bits in tag?
Tag Directory size?

**Q.28** A computer has a 512Kbyte, 4-way set associative, write back data cache with block size of 16 Bytes. The processor sends 34 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit

1. The number of bits in the tag field of an address is
2. The size of the cache tag directory is

**Q.29** Main memory address: 34-bits
Cache Size: 512KB
Block Size: 32 Bytes
Direct Mapping
No. of bits required for Byte Offset = ?
No of bits required for main memory block no. = ?
Index-bits = ?
Tag-bits = ?
Size of Tag Directory = ?

**Q.30** Blocks in Main memory = $2^{23}$
Blocks in Cache memory = $2^{16}$
Block Size: 64 Bytes
Direct Mapping
No. of bits required for Byte Offset = ?
No of bits required for main memory a ddress = ?
Index-bits = ?
Tag-bits = ?
Size of Tag Directory = ?

**Q.31** 32-bit architecture CPU
Main Memory Size = 4GB
Cache Size = 256KB
Block Size = 16 Words
Direct Mapping
No. of bits required for Byte Offset = ?
No of bits required for main memory a ddress = ?
No of bits required for main memory b lock no. = ?
Index-bits = ?
Tag-bits = ?
Size of Tag Directory = ?

**Q.32** Consider a direct mapped cache of size 256MB. Cache controller maintains 10-bits tag for each block in cache. Maximum size of main memory supported in the system is?

**Q.33** The size of memory required at cache controller to store metadata is 2 KBytes. The metadata includes tag bits, 1 modified bit and 1 valid bit. The cache contains 1 K blocks of 32bytes each and organized as direct mapped. The size of main memory is____ Mbytes?

**Q.34** Consider a direct mapped cache of size 256KB. The CPU generates x-bit addresses. The number of tag bits in main memory address are 14 bits then value of x is?

**Q.35** A computer has a 512Kbyte, 4-way set associative, write back data cache with block size of 16 Bytes. The processor sends 34 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit

1. The number of bits in the tag field of an address is
2. The size of the cache tag directory is

**Q.36** The width of the physical address on a machine is 36 bits. The width of the tag field in a 256 KB 8-way set associative cache is _____ bits ?

**Q.37** Consider a machine with a byte addressable main memory of $2^{20}$ bytes, block size of 16 bytes and a direct mapped cache having $2^{12}$ cache lines. Let the addresses of two consecutive bytes in main memory be (E201F)16 and $(E2020)_{16}$. What are the tag and cache line address (in hex) for main memory address $(E201F)_{16}$?

(A) E, 201 (B) F, 201
(C) E, E20 (D) 2, 01F

**[GATE 2015]**

**Q.38** Consider a Direct Mapped Cache with 8 cache blocks (numbered 0-7). If the memory block requests are in the following order

3, 5, 2, 8, 0, 63, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24.

Which of the following memory blocks will not be in the cache at the end of t he sequence?

(A) 3 (B) 18
(C) 20 (D) 30

**[GATE 2017]**

**Q.39** Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 block and the request for memory blocks is in the following order:

0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155

Which one of the following memory block will not be in cache if LRU replacement
policy is used?

(A) 3 (B) 8
(C) 129 (D) 216

**[GATE 2019]**

**Q.40** Consider a fully associative cache with 8 cache blocks (numbered 0–7) and the following sequence of memory block requests :

4,3,25,8,19,6,25,8,16,35,45,22,8,3,16,25,7

If LRU replacement policy is used, which cache block will have memory block 7?

(A) 4 (B) 5
(C) 6 (D) 7

**[GATE 2009]**

**Q.41** A certain processor deploys a single-level cache. The cache block size is 8 words and the word size is 4 bytes. The memory system uses a 60 MHz clock. To service a cache-miss, the memory controller first takes 1 cycle to accept the starting address of the block, it then takes 3 cycles to fetch all the eight words of the block, and finally transmits the words of the requested block at the rate of 1 word per cycle.

The maximum bandwidth for the memory system when the program running on the processor issues a series of read operations is _____ × $10^6$ bytes/sec. **[GATE 2019]**

**Q.42** Direct Mapping Question: Assume a computer has 32 bit addresses. Each block stores 64 bytes. A direct-mapped cache has 512 blocks. In which block (line) of the cache would we look for each of the following addresses?

(A) 1A2BC012 (B) FFFF00FF
(C) 12345678 (D) C109D532

**Q.43** Consider a cache with $2^{13}$ blocks of size 32Bytes each. The CPU generates address of 32-bits. The cache controller stores 1 valid bit, 1 modified bit and tag-bits for each metadata entry. The cache controller has a maximum memory of 18Kbytes to store the metadata. The cache is organized as k-way set associative. Maximum value of k to utilize the cache controller memory maximum is?

(A) 1 (Direct mapping)
(B) 2
(C) 4
(D) 8

**Q.44** A computer system uses 16 bit memory addresses. It has 2K bytes cache, organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. When a program is executed, the processor reads data sequentially from the following word addresses :

28, 144, 2176, 2180, 128, 2176

All the above addresses are shown in decimal values. Assume that the cache is initially empty. Number of misses after completing all the requests is?

(A) 3 (B) 4
(C) 5 (D) 9

**Q.45** A computer system with a word length of 32 bits has a 16 MB byte-addressable main memory and a 64 KB, 4-way set associative cache memory with a block size of 256 bytes. Consider the following four physical addresses represented in hexadecimal notation.

A1=0x42C8A4
A2=0x546888
A3=0x6A289C
A4=0x5E4880

Which one of the following is TRUE?

(A) A1 and A4 are mapped to different c ache sets.
(B) A2 and A3 are mapped to the same cache set.
(C) A3 and A4 are mapped to the same cache set.
(D) A1 and A3 are mapped to the same cache set.

**[GATE 2020]**

**Q.46** Consider a machine with a byte addressable main memory of $2^{16}$ bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50 x 50 two-dimensional array of bytes is stored in the main memory starting from memory location 1100H. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

How many data cache misses will occur in total?

**[GATE 2017]**

**Q.47** Which of the following lines of the data cache will be replaced by new blocks in accessing the array for the second time?

(A) line 4 to line 11
(B) line 4 to line 12
(C) line 0 to line 7
(D) line 0 to line 8

**[GATE 2007]**

**Q.48** Consider a direct mapped write back data cache of size 2KB with block size of 128 bytes. The cache is considered to be empty initially. The byte addressable main memory has size 1Mbytes. Further consider that there is an array A[35][20] with each element occupies 4 bytes. The base address of array is $(1A300)_{16}$. The array is accessed 4 times. And between the accesses, there is no any data cache changes happen. Hit ratio of cache for the array access is?

**Q.49** A CPU has a 32KB direct mapped cache with 128 byte-block size. Suppose A is two dimensional array of size 512 x 512 with elements that occupy 8-bytes each. Consider the following two C code segments. PI and P2.

| **P1 :** | **P2 :** |
|---|---|
| for (i=0; i<512; i++)<br>{<br>for (j=0; j<512; j++)<br>{<br>x +=A[i] [j];<br>}<br>} | for (i=0; i<512; i++)<br>{<br>for (j=0; j<512; j++)<br>{<br>x +=A[j] [i];<br>}<br>} |

**Q.50** $P_I$ and $P_2$ are executed independently with the same initial state, namely, the array A is not in the cache and i, j, x are in registers. Let the number of cache misses experienced by $P_1$ be $M_1$ and that for $P_2$ be $M_2$.

The value of $M_1$ is :

**Q.51** An access sequence of cache block address is of length N and contains n unique block addresses. The number of unique block addresses between two consecutive accesses to the same block address is bounded above by k. What is the miss ration is the access sequence is passed through a cache of associativity A >= k exercising least-recently used replacement policy.

(A) n/N (B) l/N

(C) 1/A (D) k/n

**Q.52** Consider a 2–way set associative cache with 256 blocks and uses LRU replacement. Initially the cache is empty. Conflict misses are those misses which occur due to the contention of multiple blocks for the same cache set. Compulsory misses occur due to first time access to the block. The following sequence of access to memory blocks :

0,128,256,128,0,128,256,128,1,129,257,129,1,129,257,129

is repeated 10 times. The number of conflict misses experienced by the cache is ___ ? **[GATE 2017]**

**Q.53** A 2-way set associative cache with LRU cache replacement contains 8 blocks. The CPU requests for main memory blocks in following sequence:

8, 12, 0, 1, 5, 8, 1, 12, 5, 3, 9, 3, 6, 7, 3, 2, 7, 15, 2, 16, 11, 14, 2, 9, 14, 10, 11

Calculate the following :

1. Number of misses
2. Number of hits
3. Hit ratio
4. Miss ratio
5. Number of cold, capacity and conflict misses

**Q.54** A CPU has a 32KB direct mapped cache with 128 byte-block size. Suppose A is two dimensional array of size 512 x 512 with elements that occupy 8-bytes each. Consider the following two C code segments. PI and P2.

| **P1 :** | **P2 :** |
|---|---|
| for (i=0; i<512; i++)<br>{<br>for (j=0; j<512; j++)<br>{<br>x +=A[i] [j];<br>}<br>} | for (i=0; i<512; i++)<br>{<br>for (j=0; j<512; j++)<br>{<br>x +=A[j] [i];<br>}<br>} |

Which of the following array element b lock will be mapped to same cache blo ck as block of array data A[1][2]?

(A) A[5][10] (B) A[7][4]

(C) A[9][3] (D) A[9][17]

**Q.55** Cache Size = 128KB

Block size = 32 bytes

Main memory address = 29-bits

4-way set associative cache

1. Tag size?
2. Tag Directory size?
3. Comparator required?
4. MUX required?

**Q.56** A CPU has 32-bit memory address and a 256 KB cache memory. The cache is o rganized as a 4-way set associative ca che with cache block size of 16 bytes.

A. What is the number of sets in the c ache?

B. What is the size (in bits) of the tag field per cache block?
C. What is the number and size of comparators required for tag matching?
D. How many address bits are required to find the byte offset within a cache block?
E. What is the total amount of extra memory (in bytes) required for the tag bits?

**[GATE 2001]**

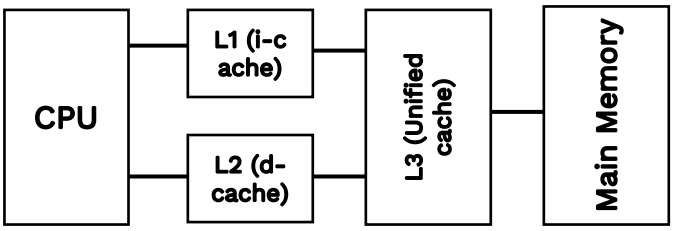
**Q.57** Consider two cache organizations. First one is 32 KB 2-way set associative with 32 byte block size, the second is of same size but direct mapped. The size of an address is 32 bits in both cases . A 2-to-l multiplexer has latency of 0.6 ns while a fc-bit comparator has latency of k/10 ns. The hit latency of the set associative organization is $h_1$ while that of direct mapped is $h_2$.
The value of h\ is :
(A) 2.4 ns (B) 2.3 ns
(C) 1.8 ns (D) 1.7 ns

**[GATE 2006]**

**Q.58** Consider a 3-level memory hierarchy with L1 cache, L2 cache and a main memory. The hit ratios of L1 is 90% and of L2 is 95%. The access times of L1, L2 and main memory are 15s, 60ns and 350ns respectively. The average memory access time is _____ ns?

**Q.59** Consider a 3-level memory hierarchy with L1 cache, L2 cache and a main memory. The probability of access of L1 is 95%, of L2 is 4.5% and of main memory is 0.5%. The access times of L1, L2 and main memory are 10ns, 50ns and 400ns respectively. The average memory access time is _____ ns?

**Q.60** The multilevel memory hierarchy is given.
The hit ratio of L1, L2, L3 and main memory are 0.8, 0.9, 0.95 and 1.0 respectively.
The access times of respective memories are 10ns, 10ns, 50ns and 500ns. Among total memory references 60% of them are for data.




1. Average memory access time for only instructions access
2. Average memory access time for only data access
3. Average memory access time

**Q.61** The read access times and the hit ratios for different caches in a memory hierarchy are as given below:
The read access time of main memory in 90nanoseconds. Assume that the caches use the referred-word-first read policy and the write-back policy. Assume that all the caches are direct mapped caches. Assume that the dirty bit is always 0 for all the blocks in the caches. In execution of a program, 60% of memory reads are for instruction fetch and 40% are for memory operand fetch. The average read access time in nanoseconds (up to 2 decimal places) is _____?

| Cache | Read access time (in nanoseconds) | Hit ratio |
|---|---|---|
| *I*-cache | 2 | 0.8 |
| *D*-cache | 2 | 0.9 |
| *L2*-cache | 8 | 0.9 |

**Q.62** Direct Mapping Question: Assume a computer has 32 bit addresses. Each block stores 64 bytes. A direct-mapped cache has 512 blocks. In which block (line) of the cache would we look for each of the following addresses?
(A) 1A2BC012 (B) FFFF00FF
(C) 12345678 (D) C109D532

**Q.63** Consider a cache with $2^{13}$ blocks of size 32Bytes each. The CPU generates address of 32-bits. The cache controller stores 1 valid bit, 1 modified bit and tag-bits for each metadata entry. The cache controller has a maximum memory of 18Kbytes to store the metadata. The cache is organized as k-way set associative. Maximum

value of k to utilize the cache controller memory maximum is?

(A) 1 (Direct mapping)

(B) 2

(C) 4

(D) 8

**Q.64** A computer system uses 16 bit memory addresses. It has 2K bytes cache, organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. When a program is executed, the processor reads data sequentially from the following word addresses :

28, 144, 2176, 2180, 128, 2176

All the above addresses are shown in decimal values. Assume that the cache is initially empty. Number of misses after completing all the requests is?

(A) 3 (B) 4

(C) 5 (D) 9

**Q.65** A computer system with a word length of 32 bits has a 16 MB byte-addressable main memory and a 64 KB, 4-way set associative cache memory with a block size of 256 bytes. Consider the following four physical addresses represented in hexadecimal notation.

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Which one of the following is TRUE?

(A) A1 and A4 are mapped to different cache sets.

(B) A2 and A3 are mapped to the same cache set.

(C) A3 and A4 are mapped to the same cache set.

(D) A1 and A3 are mapped to the same cache set.

**[GATE 2020]**

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# 9 Magnetic Disk

**Q.1** Consider a disk with 32 platters each with 2 recording surfaces. There are 128 tracks per surface and 32 sectors per track. Each sector has equal capacity of 1KBytes. Calculate :

(A) Number of surfaces in disk:

(B) Number of tracks on disk:

(C) Number of sectors in disk:

(D) Number of bytes on disk:

(E) Number of bits for disk addressing:

**Q.2** Consider a disk with 16 platters, 2 surfaces per platter, 2K tracks per surface, 4K sectors per track and 4096 Bytes per sector. Disk rotates with 6000 rpm. Seek time is 5ms.

(A) Find capacity of disk

(B) Number of bits required for addressing the disk?

(C) Find disk access time?

**Q.3** A disk has each track capacity of 2MB and it takes 20msec for 1 rotation. The transfer
rate of the disk is?

**Q.4** A disk has each track with 1k sectors each with 4KB capacity and it takes 10msec for 1 rotation. The transfer rate of the disk is?

**Q.5** Consider a disk with 16 platters, 2 surfaces per platter, 2K tracks per surface, 4K sectors per track and 4096 Bytes per sector. Disk rotates with 6000 rpm. Seek time is 5ms.
Find the disk transfer rate?

**Q.6** Consider a disk with 16 platters, 2 surfaces per platter, 1K tracks per surface, 2K sectors per track and 2048 Bytes per sector. Disk rotates with 3000 rpm. Seek time is 10ms.
If the disk is used in cycle stealing mode of DMA, such that whenever 64-bits word is available, it will be transferred in 16ns. What is the % of time CPU is blocked?

**Q.7** Consider a disk with 8 platters, 2 surfaces per platter, 2K tracks per surface, 1K sectors per track and 2K Bytes per sector. Disk rotates with 3000 rpm. Seek time is 10ms. The read write head is currently at 4th sector on outer most track, and the desired sector is 504th sector on inner track. Then what is the rotational latency and disk access time?

**Q.8** Consider a disk pack with a seek time of 4 milliseconds and rotational speed of 10000 rotations per minute (RPM). It has 600 sectors per track and each sector can store 512 bytes of data. Consider a file stored in the disk. The file contains 2000 sectors. Assume that every sector access necessitates a seek, and the average rotational latency for accessing each sector is half of the time for one complete rotation. The total time (in milliseconds) needed to read the entire file is _____.

**[GATE 2015]**

(A) 14020 (B) 14000

(C) 25030 (D) 15000

**Q.9** Assume that a disk takes 0.1ms for 1 track movement for the seek when the head is on the highest speed. To achieve highest speed the starting inertia takes 0.2ms and to stop to desired track the stopping inertia also takes 0.2ms. During start and stop inertia the head can travel one track. Calculate the seek time for following head movements:

(A) From track 5 to 11

(B) From track 26 to 17

(C) From track 18 to 19

**Q.10** Consider a disk with 1000 sectors per track. Disk rotates with 6000 rpm. Seek time is 10ms. Calculate the disk access time?

**Q.11** An application loads 100 libraries at startup. Loading each library requires exactly one disk access. The seek time of the disk to a random location is given as 10ms. Rotational speed of disk is 6000rpm. If all 100 libraries are loaded from random locations on the disk, how long does it take to load all libraries? (The time to transfer data from the disk block once the head has been positioned at the start of the block may be neglected)

**[GATE 2010]**

(A) 0.5 s (B) 1.25 s

(C) 1.5 s (D) 1.0 s

**Q.12** The transfer time T of the disk is

(A) $\frac{2b}{rN}$ (B) $\frac{rb}{N}$

(C) $\frac{rN}{b}$ (D) $\frac{b}{rN}$

Where:

b = number of bytes to be transferred

N = number of bytes on a track

r = rotation speed in rps

**Q.13** Consider a disk with an average seek time of 4 ms, rotational delay of 2 ms, rotation speed of 15000 r.p.m. and 512-byte sectors with 500 sectors per track. A file occupies all of the sectors on 5 adjacent tracks. After reading the first track, if remaining tracks can be read with no seek time, then the time required in sequential organization to transfer the file will be nearly

(A) 0.01 second (B) 0.034 second

(C) 0.34 second (D) 3.4 seconds

Q.14 The total average read or write time $T_{totai}$ is

(A) $T_S + \frac{1}{2r} + \frac{b}{N}$ (B) $T_s + \frac{1}{2r} + \frac{b}{rN}$

(C) $\frac{T_s}{rN} + \frac{b}{N}$ (D) $T_s + 2r + \frac{b}{rN}$

where,

Ts = average seek time

b = number of bytes to be transferred

N = number of bytes on a track

r = rotation speed, in revolutions per second

**Q.15** Consider a disk drive with the following specifications :

16 surfaces, 512 tracks/surface, 512 sectors/track, 1 KB/sector, rotation speed 3000 rpm. The disk is operated in cycle stealing mode whereby whenever one 4 byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a

4 byte word from the memory in each DMA cycle. Memory cycle time is 40 nsec. The maximum percentage of time that the CPU gets blocked during DMA operation is:

(A) 10 (B) 25

(C) 40 (D) 50

**Q.16** Consider a disk with 8 platters, 2 surfaces per platter, 2K tracks per surface, 1K sectors per track and 2K Bytes per sector. Disk rotates with 3000 rpm. Seek time is 10ms. The read write head is currently at $4^{th}$ sector on outer most track, and the desired sector is $504^{th}$ sector on inner track. Then what is the rotational latency and disk access time?

**Q.17** A hard disk has 16 sectors per track, 4 platters each with 2 recording surfaces and 32 cylinders. The address of a sector is given as a triple ⟨c,h,s⟩, where c is the cylinder number, h is the surface number and s is the sector number. Thus, the $0^{th}$ sector is addressed as ⟨0,0,0⟩, the 1st sector as ⟨0,0,1⟩, and so on.

The address ⟨12, 6 ,12⟩ corresponds to sector number?

**Q.18** A hard disk has 16 sectors per track, 4 platters each with 2 recording surfaces and 32 cylinders. The address of a sector is given as a triple ⟨c,h,s⟩, where c is the cylinder number, h is the surface number and s is the sector number. Thus, the $0^{th}$ sector is addressed as ⟨0,0,0⟩, the 1st sector as ⟨0,0,1⟩, and so on.

The address of $867^{th}$ sector?

**Q.19** Consider a hard disk with 36 recording surfaces (0-35) having 10000 cylinders (0-9999) and each track contains 64 sectors (0-63). Data in disk are organized cylinder-wise and the addressing format is <cylinder no., surface no., sector no.>. A file in the disk is stored starting from address <1660, 28, 38>.

1. What is the sector number of the first sector of the file in the disk?
2. If a file is stored on 55788 sectors in contiguous manner, then what is the sector number of the last sector of the file?
3. Calculate the address in format <c, h, s> for the last sector of the file?

**Q.20** Consider a hard disk with 16 recording surfaces (0-15) having 16384 cylinders (0-16383) and each track contains 64 sectors (0-63). Data storage capacity of in each sector is 512 Bytes. Data are organized cylinder-wise and addressing format is <cylinder no., surface no., sector no.>. A file of size 42797 KB is stored in the disk and the starting disk location of the file is <1200, 9, 40>. What is the cylinder number of the last sector of the file, if it is stored in a contiguous manner?

**[GATE 2013]**

**Q.21** A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple ⟨c,h,s⟩, where c is the cylinder number,h is the surface number and s is the sector number. Thus, the $0^{th}$ sector is addressed as ⟨0,0,0⟩, the $1^{st}$ sector as ⟨0,0,1⟩, and so on.

**[GATE 2009]**

**Q.22** The address ⟨400,16 ,29⟩ corresponds to sector number:

**[GATE 2009]**

(A) 505035 (B) 505036
(C) 505037 (D) 505038

**Q.23** The address of $1039^{th}$ sector is

**[GATE 2009]**

(A) ⟨0,15,31⟩ (B) ⟨0,16,30⟩
(C) ⟨0,16,31⟩ (D) ⟨0,17,31⟩

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# 10 Pipeline

**Q.1** A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns.

1. Determine the speedup ratio of the pipeline for 100 tasks.
2. What is the maximum speedup that can be achieved?

**Q.2** Consider 6 segment pipeline with segment delay of segments as 20ns, 26ns, 21ns, 21ns, 24ns and 28ns respectively. Calculate processing time of pipeline for 1000 tasks?

**Q.3** The time delay of the four segments in pipeline are as shown follows:

$t_1$=50 ns,$t_2$=30 ns, $t_3$=95 ns, and $t_4$=45 ns.

The interface registers delay time $t_r$=5 ns.

How long would it take to process 100 tasks in the pipeline?

**Q.4** How can we reduce the total time about the one-half of the time calculated in above question?

**Q.5** Consider a non-pipelined processor with a clock rate of 4 gigahertz and average cycles per instruction of 5. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 5 gigahertz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is _____.

**Q.6** Consider 5 segment pipeline with segment delay of segments as 120ns, 126ns, 121ns, 110ns, 118ns and 120ns respectively. The intermediate buffer delay is 5ns. Consider that the system is used for performing 100 tasks.

(A) What is the latency of non-pipeline system

(B) What is the latency of pipeline system

(C) What is the throughput of pipeline system

(D) What is the throughput of pipeline system in ideal case

**Q.7** The stage delays in a 5-stage pipeline are 60ns, 50ns, 55ns and 80ns. The last stage (with delay 80ns) is replaced with a functionally equivalent design involving two stages with respective delays 60ns and 35ns. The throughput increase of the pipeline is _____ percent?

**Q.8** Consider a 6-stage pipeline with delays 2, 4, 3, 5, 3 and 4 cycles. This pipeline is upgraded to a new 8-segment pipeline in which each segment delay is 2 cycle.

1. How much time is saved using new pipeline over old one for 100 tasks?
2. What is the speed up of new pipeline as compared to old pipeline 100 tasks?

**Q.9** Consider a 6-stage pipeline with cycle time of 18ns. Calculate processing time of pipeline for 500 tasks?

**Q.10** Consider a non-pipelined system which takes 100ns to perform a task. The same task can be performed using a 6 segment pipeline with cycle time of 19ns.

1. Calculate speed up of pipeline for 1000 tasks?
2. What is the maximum speed up?

**Q.11** Consider 6 segment pipeline with segment delay of segments as 140ps, 109ps, 160ps, 154ps, 125ps and 170ps respectively. Pipeline uses an intermediate buffer after every segment with a delay of 10ps. Time required by pipeline for processing of 1000 tasks is _____ nanoseconds?

**Note :** ps = picoseconds

In the above question calculate the speed up ratio of the pipeline as compared to corresponding non-pipeline system?

**Q.15** A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be

(A) 120.4 microseconds
(B) 160.5 microseconds
(C) 165.5 microseconds
(D) 590.0 microseconds

**Q.16** Consider the following processors (ns stands for nanoseconds). Assume that the
pipeline registers have zero latency.

**P1 :** Four-stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns.

**P2 :** Four-stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns.

**P3 :** Five-stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns.

**P4 :** Five-stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns.

Which processor has the highest peak clock frequency?

(A) P1 (B) P2
(C) P3 (D) P4

**Q.17** Consider a non-pipelined processor with a clock rate of 5GHz and an average cycles of 4 per instruction. The same processor is upgraded to a pipelined processor with 6 stages and the clock speed of 4GHz. Assume that there are no stalls in the pipeline.

(A) The speed up achieved in the pipeline for 1000 instructions is?
(B) The speed up achieved in the pipeline in ideal conditions is?
(C) The CPI of the pipeline for 1000 instructions is?
(D) The CPI of the pipeline for in ideal conditions is?
(E) MIPS count of the pipeline processor in ideal condition is?

**Q.18** The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. The throughput increase of the pipeline is _____ percent.

**Q.19** Consider a program which contains 50 instructions I1, I2 , I3 ..... I50. Further consider a 5-stage pipeline with stages as: Instruction Fetch, Decode, Operand Fetch, Execution and Write-Back. The program contains only 1 branch instruction which is instruction I5 and its target is instruction I48. If during the execution of the program the branch is taken then number of cycles required to execute this program in the given pipeline is _____ ?

**Q.20** In the above question if the pipeline has cycle time 15ns then total time required to execute the program is _____ ns?

**Q.21** Consider a program which contains 200 instructions I1, I2 , I3 ..... I200. Further consider a 5-stage pipeline with stages as: Instruction Fetch, Decode, Operand Fetch, Execution and Write Back. The program contains only 1 branch instruction which is instruction I5 and its target is instruction I18. If during the execution of the program the branch is taken then number of cycles required to execute this program in the given pipeline is _____ ?

**Q.22** Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delay for FI, DI, FO, EI and WO are 9 ns, 8 ns, 12 ns, 10 ns and 11 ns, respectively. There are intermediate storage buffer after each stage and the delay of each buffer is 1 ns. A program consisting of 20 instructions I1, I1, I3, ...., I20 is executed in this pipelined processor. Instruction

I7 is only the branch instruction, and its branch target is I17. If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is?

**Q.23** Consider a program which contains 50 instructions I1, I2, I3 ..... I500. Further consider a 5-stage pipeline with stages as: Instruction Fetch, Decode, Operand Fetch, Execution and Write-Back. The program contains 3 branch instructions, information of those given in a table below. The number of cycles required to execute this program in the given pipeline is _____ ?

| Branch Instruction | Target Instruction | Branch Taken or Not |
|---|---|---|
| I9 | I29 | Taken |
| I234 | I332 | Not Taken |
| I443 | I491 | Taken |

**Q.24** In above question Consider pipeline stage delays are 12ns, 15ns, 13ns, 17ns and 14ns, then

(A) Total time required to execute the program is?

(B) Calculate average CPI?

(C) Calculate MIPS count?

**Q.25** Consider a pipelined processor with the following four stages :

IF : Instruction Fetch

ID : Instruction Decode and Operand Fetch

EX : Execute

WB : Write Back

The IF, ID, and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction needs 3 clock cycle in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD R2, R1, R0 R2←R1+R0

MUL R4, R3, R2 R4←R3*R2

SUB R6, R5, R4 R6←R5-R4

**Q.26** The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB), The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards.

The number of clock cycles required for completion of execution of the sequence of instruction is _____?

**[GATE 2018]**

**Q.27** Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below:

| | $S_1$ | $S_2$ | $S_3$ | $S_4$ |
|---|---|---|---|---|
| I1 | 2 | 1 | 1 | 1 |
| I2 | 1 | 3 | 2 | 2 |
| I3 | 2 | 1 | 1 | 3 |
| I4 | 1 | 2 | 2 | 2 |

What is the number of cycles needed to execute the following loop?

For (i = 1 to 2) (I1; I2;I3;I4;)

**Q.28** Count the number of RAW, WAW and WAR dependencies?

ADD R2, R1, R0 R2 ←R1+R0

MUL R4, R3, R2 R4 ←R3*R2

SUB R6, R5, R4 R6 ←R5-R4

ADD R6, R7, R8 R6 ←R7+R8

MUL R7, R1, R2 R7 ←R1*R2

SUB R1, R3, R4 R1 ←R3-R4

**Q.29** Consider the following sequence of instructions, which is to be executed on a 5 stage pipeline: IF, ID, OF, EX and WB. Each stage takes one cycle for each instruction.

Total Cycles required to execute this sequence

1. When pipeline uses operand forwarding
2. When pipeline does not use operand forwarding

| | | |
|---|---|---|
| ADD | R2, R1, R0 | R2 ← R1+R0 |
| MUL | R4, R3, R2 | R4 ← R3*R2 |
| SUB | R6, R5, R4 | R6 ← R5-R4 |
| ADD | R6, R7, R8 | R6 ← R7+R8 |
| MUL | R7, R1, R2 | R7 ← R1*R2 |
| SUB | R1, R3, R4 | R1 ← R3-R4 |

**Q.30** Consider the following sequence of instructions, which is to be executed on a 5 stage pipeline: IF, ID, OF, EX and WB. Each stage takes one cycle for each instruction.

Total Cycles required to execute this sequence

1. When pipeline uses operand forwarding
2. When pipeline does not use operand forwarding

| | | |
|---|---|---|
| ADD | R2, R1, R0 | R2 ← R1+R0 |
| MUL | R4, R3, R2 | R4 ← R3*R2 |
| LOAD | R7, (1000) | R7 ← M[1000] |
| ADD | R6, R7, R8 | R6 ← R7+R8 |
| MUL | R7, R1, R2 | R7 ← R1*R2 |
| SUB | R1, R3, R4 | R1 ← R3-R4 |

**Q.31** Consider a 5-stage pipeline which is executing a program of 1000 instructions. Among all instructions 200 instructions cause 2 stall cycles each.

(A) Calculate CPI of pipeline?

(B) If pipeline cycle time is 3ns then what is average instruction execution time?

(C) Calculate CPI of pipeline in ideal conditions?

(D) If pipeline cycle time is 3ns then what is average instruction execution time in ideal conditions?

**Q.32** Consider a 5-stage instruction pipeline, where all stages take equal delay. When an application is executing on this 5-stage pipeline, consider 20% of the instructions incur 3 pipeline stall cycles is.

(a) Average CPI for pipeline?

(b) Average instruction execution time for pipeline?

I The speedup of pipeline achieved with respect to non-pipeline?

**Q.33** An instruction pipeline has five stages where each stage takes 3 nanoseconds and all instructions use all five stages. Branch instructions are not overlapped, i.e., the instruction after the branch is not fetched till the branch instruction is completed. Under ideal conditions.

Calculate the average instruction execution time assuming that 10% of all instruction executed are branch instructions. Ignore the fact that some branch instructions may be conditional.

**Q.34** If a branch instruction is a conditional branch instruction, the branch need not be taken when the condition is false. If the branch is not taken, the following instructions can be overlapped. When 70% of all branch instructions are conditional branch instructions, and 40% of the conditional branch instructions are such that the branch is taken, calculate the average instruction execution time?

**Q.35** Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 25% of the instructions incur 2 pipeline stall cycles is

**[GATE 2014]**

**Q.36** An instruction pipeline has five stages where each stage takes 2 nanoseconds and all instructions use all five stages. Branch instructions are not overlapped, i.e., the instruction after the branch is not fetched till the branch instruction is completed. Under ideal conditions.

Calculate the average instruction execution time assuming that 20% of all instruction executed are branch

instructions. Ignore the fact that some branch instructions may be conditional.

**[GATE 2000, Part 1]**

**Q.37** If a branch instruction is a conditional branch instruction, the branch need not be taken. If the branch is not taken, the following instructions can be overlapped. When 80% of all branch instructions are conditional branch instructions, and 50% of the conditional branch instructions are such that the branch is taken, calculate the average instruction execution time?

**[GATE 2000, Part 2]**

**Q.38** A processor Xi operating at 2 GHz has a standard 5—stage RISC instruction pipeline having a base CPI (cycles per instruction) of one without any pipeline hazards. For a given program P that has 30% branch instructions, control hazards incur 2 cycles stall for every branch. A new version of the processor $X_2$ operating at same clock frequency has an additional branch predictor unit (BPU) that completely eliminates stalls for correctly predicted branches. There is neither any savings nor any additional stalls for wrong predictions. There are no structural hazards and data hazards for $X_1$ and $X_2$. If the BPU has a prediction accuracy of 80%, the speed up (rounded off to two decimal places) obtained by $X_2$ over $X_1$ in executing P is_____.

**[GATE 2022]**

**Q.39** Consider a pipelined processor with 5 stages. Instruction Fetch (IF). Instruction Decode (ID). Execute (EX). Memory Access (MEM), and Write Back (WB). Each stage of the pipeline, except the EX stage, takes one cycle. Assume that the ID stage merely decodes the instruction and the register read is performed in the EX stage. The EX stage takes one cycle for ADD instruction and two cycles for MUL instruction. Ignore pipeline register latencies.

Consider the following sequence of 8 instructions:

ADD, MUL, ADD, MUL, ADD, MUL, ADD, MUL

Assume that every MUL instruction is data-dependent on the ADD instruction just before it and every ADD instruction (except the first ADD) is data-dependent on the MUL instruction just before it. The Speedup is defined as follows:

$$\text{Speedup} = \frac{\text{Execution time without operand forwarding}}{\text{Execution time with operand forwarding}}$$

The Speedup achieved in executing the given instruction sequence 011 the pipelined processor (rounded to 2 decimal places) is _____.

**[GATE 2021]**

**Q.40** An instruction pipeline has five stages, namely, instruction fetch (IF), instruction decode and register fetch (ID/RF), instruction execution (EX), memory access (MEM), and register writeback (WB) with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns, respectively (ns stands for nanoseconds). To gain in terms of frequency, the designers have decided to split the ID/RF stage into three stages (ID, RF1, RF2) each of latency 2.2/3 ns. Also, the EX stage is split into two stages (EX1, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages. A program has 20% branch instructions which execute in the EX stage and produce the next instruction pointer at the end of the EX stage in the old design and at the end of the EX2 stage in the new design. The IF stage stalls after fetching a branch instruction until the next instruction pointer is computed. All instructions other than the branch instruction have an average CPI of one in both the designs. The execution times of this program on the old and the new design are P and Q nanoseconds, respectively. The value of P/Q is

**[GATE 2014]**

**Q.41** A processor $X_1$ operating at 2 GHz has a standard 5—stage RISC instruction pipeline having a base CPI (cycles per instruction) of one without any pipeline hazards. For a given program P that has 30% branch instructions, control hazards incur 2 cycles stall for every branch. A new version of the processor $X_2$ operating at same clock frequency has an additional branch predictor unit (BPU) that completely eliminates stalls for correctly predicted branches. There is neither any savings nor any additional stalls for wrong predictions. There are no structural hazards and data hazards for $X_1$ and $X_2$. If the BPU has a prediction accuracy of 80%, the speed up (rounded off to two decimal places) obtained by $X_2$ over $X_1$ in executing P is _____

**[GATE 2022]**

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# 11 Floating Point Representation

**Q.1** Consider a 16-bit register used to store floating point numbers. The mantissa i s normalized signed fraction number. E xponent is represented in excess-32 fo rm. What is the 16-bit value for $+(11.5)_{10}$ in this register?

**Q.2** What is the 4-digit hexadecimal value f or $+ (11.5)_{10}$ in above questions register?

**Q.3** What is the 4-digit hexadecimal value for $+(37.75)_{10}$ in above question's register?

**Q.4** Consider a 16-bit register used to store floating point numbers. The mantissa is implicitly normalized signed fraction number. Exponent is represented in excess-64 form. What is the 16-bit value for $+(13.25)_{10}$ in this register?

**Q.5** The data given below. Solve the problems and choose the correct answer.

| | **16 bits** | |
|---|---|---|
| **S** | **E** | **M** |
| Sign | Excess-64 Exponent | Mantissa |

Mantissa is a pure fraction in sign - ma gnitude form. The decimal number 0.23 $9 \times 2^{13}$ has the following hexadecimal r epresentation without normalization a nd rounding off?

(A) 0D24 (B) 0D4D

(C) 4D0D (D) 4D3D

**[GATE 2005]**

**Q.6** The data given below. Solve the problems and choose the correct answer.

| | **16 bits** | |
|---|---|---|
| **S** | **E** | **M** |
| Sign | Excess-64 Exponent | Mantissa |

The normalized representation for the above format is specified as follows. T he mantissa has an implicit preceding t he binary (radix) point. Assume that on ly 0's are padded in while shifting a fiel d. The normalized representation of th e above $0.239 \times 2^{13}$ is?

(A) 0A20 (B) 1134

(C) 4DD0 (D) 4AE8

**[GATE 2005]**

**Q.7** A certain well-known computer family represents the exponents of its floating-point numbers as "excess-64" integers; i.e., a typical exponent $e_6e_5e_4e_3e_2e_1e_0$ represents the number :

(A) $e = -64 + \sum_{i=0}^{6} 2^i e_i$

(B) $e = -64 + \sum_{i=0}^{6} 2e_i$

(C) $e = 64 - \sum_{i=0}^{6} 2^i e_i$

(D) $e = 64 - \sum_{i=0}^{6} 2e_i$

**Q.8** Consider a 24-bit register used to stor e floating point numbers. The mantissa is implicitly normalized signed fraction number. Exponent is represented in ex cess-64 form. What is the 6-digit hexa decimal value for $-(43.625)_{10}$ in this re gister?

**Q.9** Consider a 24-bit register used to stor e floating point numbers. The mantissa is explicitly normalized signed fraction number. Exponent is represented in ex cess-128 form. What is the 6-digit hexa decimal for $-(31.375)_{10}$ in this register?

**Q.10** Consider a 16-bit register used to store floating point numbers. The mantissa is explicitly normalized signed fraction number. Exponent is represented in ex cess-32 form. What is the 6-digit hexa decimal for $-(0.5625)_{10}$ in this register?

**Q.11** The value of a float type variable is rep resented using the single- precision 32 -bit floating point format IEEE-754 sta ndard that uses 1bit for sign, 8 bits for biased exponent and 23 bits for mantis sa. A float type variable X is assigned t he decimal value of −27.625. The repre sentation of X in hexadecimal notation is?

**Q.12** The value represented by the following 32-bits in IEEE-754 representation is?

0100000111100000...00

**Q.13** The value represented by the following 32-bits in IEEE-754 representation is?

0000000001100000...00

**Q.14** Maximum value represented in IEEE-75 4 single precision?

**Q.15** Minimum positive value represented in IEEE-754 single precision?

**Q.16** Minimum positive normalized value rep resented in IEEE-754 single precision?

**Q.17** How to represent +1 and -1 in IEEE-754 single precision floating point number?

**Q.18** How to represent +0.0000101 in IEEE-7 54 single precision floating point numb er?

**Q.19** Is it possible that a value is represente d in IEEE-754 double precision floating point number and it can not be represe nted in single precision? If yes then giv e an example?

**Q.20** The value of a float type variable is represented using the single- precision 32-bit floating point format IEEE-754 standard that uses 1bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A float type variable X is assigned the decimal value of –14.25. The representation of X in hexadecimal notation is

(A) C1640000H (B) 416C0000H

(C) 41640000H (D) C16C0000H

**[GATE 2014]**

**Q.21** Consider three registers R1, R2, and R3 that store numbers in IEEE–754 single precision floating point format. Assume that R1 and R2 contain the values (in hexadecimal notation) 0x42200000 and 0xC1200000, respectively.

If R3 = R1 / R2, what is the value stored in R3 ?

(A) 0x40800000 (B) 0xC0800000

(C) 0x83400000 (D) 0xC8500000

**[GATE 2020]**

**Q.22** Given the following binary number in 32 bit (single precision) IEEE-754 format :

00111110011011010000009000000000

The decimal value closest to this floating-point number is :

(A) 1.45 x $10^{1}$ (B) 1.45 x $10^{-1}$

(C) 2.27 x $10^{-1}$ (D) 2.27 x $10^{1}$

**[GATE 2017]**

**Q.23** Consider the following representation of a number in IEEE 754 single-precision floating point format with a bias of 127.

5 : 1 E : 10000001 F :

11110000000000000000000

Here S, E and F denote the sign, exponent and fraction components of the floating point representation.

The decimal value corresponding to the above representation (rounded to 2 decimal places) is

**[GATE 2021]**

**Q.24** The format of the single-precision floating-point representation of a real number as per the IEEE 754 standard is as follows :

| Sign | Exponent | mantissa |
|---|---|---|

Which one of the following choices is correct with respect to the smallest normalized positive number represented using the standard?

1. exponent = 00000001 and mantissa = 00000000000000000000001
2. exponent = 00000001 and mantissa = 00000000000000000000000
3. exponent = 00000000 and mantissa = 00000000000000000000000

   exponent = 00000000 and mantissa = 00000000000000000000001

**[GATE 2021]**

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