Summary in Graph

Exam Summary (GO Classes CS Test Series 2025 | Digital Logic | Subject Wise Test 1)

Qs. Attempted:	**0** (0 + 0)	**Correct Marks:**	**0** (0 + 0)
Correct Attempts:	**0** (0 + 0)	**Penalty Marks:**	**0** (0 + 0)
Incorrect Attempts:	**0** (0 + 0)	**Resultant Marks:**	**0** (0 + 0)

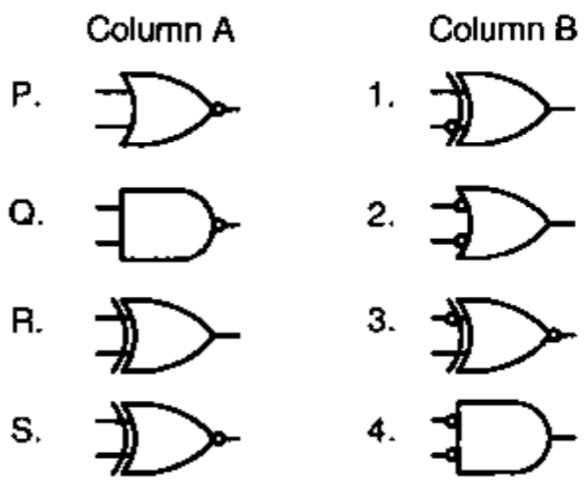
Total Questions:	**30** (10 + 20)
Total Marks:	**50** (10 + 40)
Exam Duration:	**90 Minutes**
Time Taken:	**0 Minutes**

EXAM RESPONSE | EXAM STATS | FEEDBACK

Technical

Q #1 | Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

Match the logic gates in Column A with their equivalents in Column B.

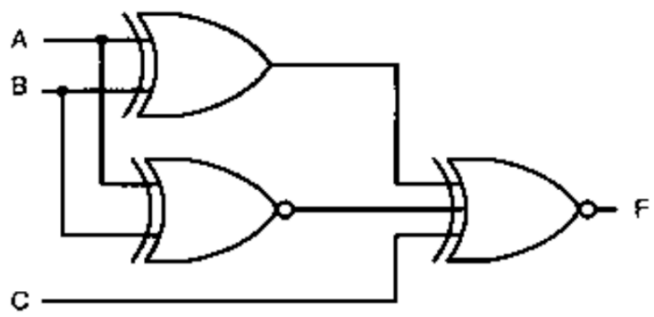


A. P-2, Q-4, R-1, S-3
B. P-4, Q-2, R-1, S-3
C. P-2, Q-4, R-3. S-1
D. P-4, Q-2, R-3, S-1

Your Answer: | Correct Answer: D | Not Attempted | Time taken: 00min 00sec | Discuss

Q #2 | Numerical Type | Award: 1 | Penalty: 0 | Digital Logic

Consider the following logic circuit:



The number of input combinations $(\mathrm{A}, \mathrm{B}, \mathrm{C})$ for which the output F becomes 1 is ?

Your Answer: | Correct Answer: 4 | Not Attempted | Time taken: 00min 00sec | Discuss

Q #3 | Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

A decoder may be described as

A. Multiple-input single-output logic circuit which converts coded inputs into a coded output where the input and output codes are different.
B. Single-input single-output logic circuit which converts the coded input into a coded output where the input and output codes are different.
C. Multiple-input multiple-output logic circuit which converts coded inputs into coded outputs where the input and output codes are different.
D. Single-input multiple-output logic circuit which converts the coded input into coded outputs where the input and output codes are different.

Your Answer: | Correct Answer: C | Not Attempted | Time taken: 00min 03sec | Discuss

Q #4 | Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles.

A. an AND gate
B. an OR gate
C. an XOR gate
D. a NAND gate

Your Answer: | Correct Answer: C | Not Attempted | Time taken: 00min 00sec | Discuss

Q #5 | Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

$\mathrm{X} = 01110$ and $\mathrm{Y} = 11001$ are two 5-bit binary numbers represented in two's complement format. The sum of X and Y represented in two's complement format using 6 bits is

A. 100111
B. 001000
C. 000111

D. 101001

Your Answer: | Correct Answer: C | Not Attempted | Time taken: 00min 00sec | Discuss

Q #6 | Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

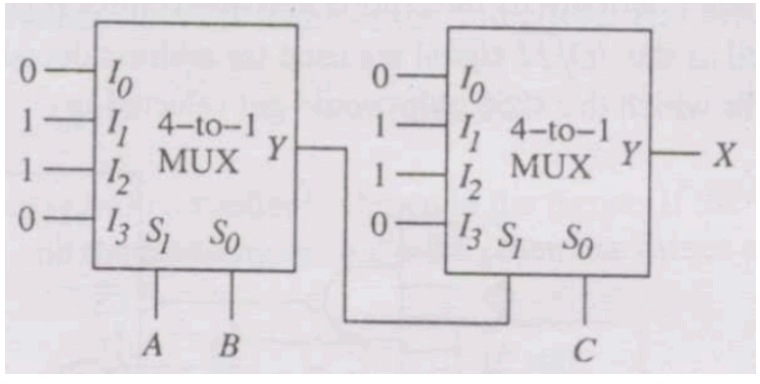
The Boolean expression $Y = \overline{\mathrm{A}}\ \overline{\mathrm{B}}\ \overline{\mathrm{C}}\ \mathrm{D} + \overline{\mathrm{A}}\ \mathrm{B}\ \mathrm{C}\ \overline{\mathrm{D}} + \mathrm{A}\ \overline{\mathrm{B}}\ \overline{\mathrm{C}}\ \mathrm{D} + \mathrm{A}\ \mathrm{B}\ \overline{\mathrm{C}}\ \overline{\mathrm{D}}$ can be minimized to

A. $Y = \overline{\mathrm{A}}\ \overline{\mathrm{B}}\ \overline{\mathrm{C}}\ \mathrm{D} + \overline{\mathrm{A}}\ \mathrm{B}\ \overline{\mathrm{C}} + \mathrm{A}\ \overline{\mathrm{C}}\ \mathrm{D}$
B. $Y = \overline{\mathrm{A}}\ \overline{\mathrm{B}}\ \overline{\mathrm{C}}\ \mathrm{D} + \mathrm{B}\ \mathrm{C}\ \overline{\mathrm{D}} + \mathrm{A}\ \overline{\mathrm{B}}\ \overline{\mathrm{C}}\ \mathrm{D}$
C. $Y = \overline{\mathrm{A}}\ \mathrm{B}\ \mathrm{C}\ \overline{\mathrm{D}} + \overline{\mathrm{B}}\ \overline{\mathrm{C}}\ \mathrm{D} + \mathrm{A}\ \overline{\mathrm{B}}\ \overline{\mathrm{C}}\ \mathrm{D}$
D. $Y = \overline{\mathrm{A}}\ \mathrm{B}\ \mathrm{C}\ \overline{\mathrm{D}} + \overline{\mathrm{B}}\ \overline{\mathrm{C}}\ \mathrm{D} + \mathrm{A}\ \mathrm{B}\ \overline{\mathrm{C}}\ \overline{\mathrm{D}}$

Your Answer: | Correct Answer: D | Not Attempted | Time taken: 00min 00sec | Discuss

Q #7 | Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

In the following circuit, X is given by



A. $\mathrm{X} = \mathrm{A}\ \overline{\mathrm{B}}\ \overline{\mathrm{C}} + \overline{\mathrm{A}}\ \mathrm{B}\ \overline{\mathrm{C}} + \overline{\mathrm{A}}\ \overline{\mathrm{B}}\ \mathrm{C} + \mathrm{A}\ \mathrm{B}\ \mathrm{C}$
B. $\mathrm{X} = \overline{\mathrm{A}}\ \mathrm{B}\ \mathrm{C} + \mathrm{A}\ \overline{\mathrm{B}}\ \mathrm{C} + \mathrm{A}\ \mathrm{B}\ \overline{\mathrm{C}} + \overline{\mathrm{A}}\ \overline{\mathrm{B}}\ \overline{\mathrm{C}}$
C. $\mathrm{X} = \mathrm{A}\ \mathrm{B} + \mathrm{B}\ \mathrm{C} + \mathrm{A}\ \mathrm{C}$
D. $\mathrm{X} = \overline{\mathrm{A}}\ \overline{\mathrm{B}} + \overline{\mathrm{B}}\ \overline{\mathrm{C}} + \overline{\mathrm{A}}\ \overline{\mathrm{C}}$

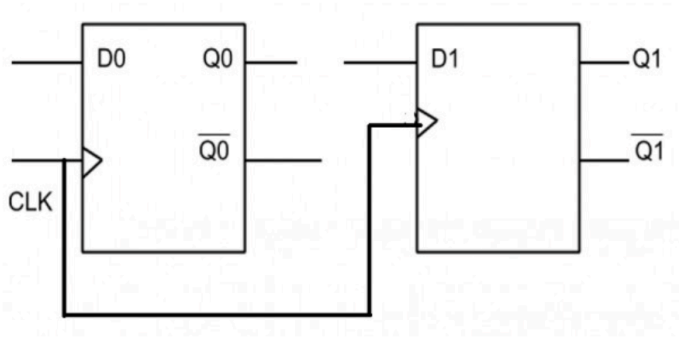
Your Answer: | Correct Answer: A | Not Attempted | Time taken: 00min 00sec | Discuss

Q #8 | Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

Two D Flip flops are connected as a synchronous counter that goes through following sequence

$$00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00$$

Inputs D_0 and D_1 should be connected as?$(\text{Flip flop } \mathrm{D}_1 \text{ provides the } \mathrm{MSB})$



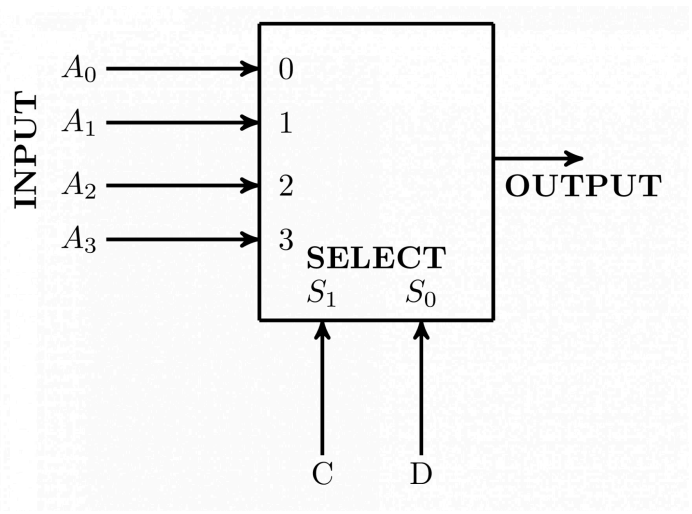
A. $\overline{\mathrm{Q}_1}$ and Q_0
B. $\overline{\mathrm{Q}_0}$ and Q_1

C. $\overline{Q}_1 Q_0$ and $\overline{Q}_0 Q_1$
D. $\overline{Q}_0 \overline{Q}_1$ and $Q_0 Q_1$

Your Answer: | Correct Answer: A | Not Attempted | Time taken: 00min 00sec | Discuss

Q #9 | Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

Consider the 2–bit multiplexer (MUX) shown in the figure. For OUTPUT to be the XOR of C and D, the values for A_0, A_1, A_2, and A_3 are _____.



A. $A_0 = 0, A_1 = 0, A_2 = 1, A_3 = 1$
B. $A_0 = 1, A_1 = 0, A_2 = 1, A_3 = 0$
C. $A_0 = 0, A_1 = 1, A_2 = 1, A_3 = 0$
D. $A_0 = 1, A_1 = 1, A_2 = 0, A_3 = 0$

Your Answer: | Correct Answer: C | Not Attempted | Time taken: 00min 00sec | Discuss

Q #10 | Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

What is the minimum (most negative) value of a 32-bit two's complement integer?

A. -2^{32}
B. $-2^{32} + 1$
C. -2^{31}
D. $-2^{31} + 1$

Your Answer: | Correct Answer: C | Not Attempted | Time taken: 00min 00sec | Discuss

Q #11 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

Consider the Boolean function $F(w, x, y, z) = wy + xy + \overline{w}\, xyz + \overline{w}\, \overline{x}\, y + xz + \overline{x}\, \overline{y}\, \overline{z}$. Which one of the following is the complete set of essential prime implicants?

A. $w, y, xz, \overline{x}\, \overline{z}$
B. w, y, xz
C. $y, \overline{x}\, \overline{y}\, \overline{z}$
D. $y, xz, \overline{x}\, \overline{z}$

Your Answer: | Correct Answer: D | Not Attempted | Time taken: 00min 00sec | Discuss

Q #12 Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

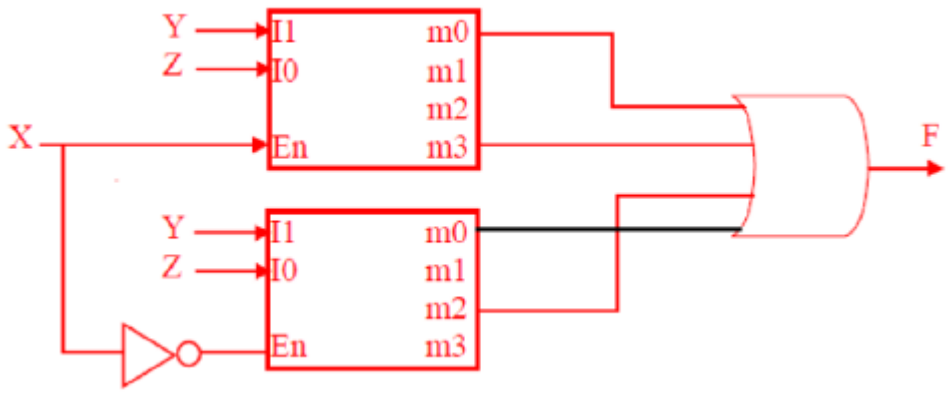
P, Q, and R are the decimal integers corresponding to the 4-bit binary number 1100 considered in signed magnitude, 1's complement, and 2's complement representations, respectively. The 6-bit 2's complement representation of $(\mathrm{P}+\mathrm{Q}+\mathrm{R})$ is _____.

A. 110101
B. 110010
C. 111101
D. 111001

Your Answer: | **Correct Answer: A** | Not Attempted | Time taken: 00min 00sec | Discuss

Q #13 Multiple Select Type | Award: 2 | Penalty: 0 | Digital Logic

The circuit below uses two 2-to-4 decoders, and inverter, and an OR gate to implement a function $\mathrm{F}(\mathrm{X}, \mathrm{Y}, \mathrm{Z})$. X is the most significant bit.



$\mathrm{F}(\mathrm{X}, \mathrm{Y}, \mathrm{Z})$ can be expressed as (Encircle all that applies):

A. $\sum \mathrm{m}(0, 3, 4, 6)$
B. $\sum \mathrm{m}(0, 2, 4, 7)$
C. $\prod \mathrm{M}(1, 3, 5, 6)$
D. $\prod \mathrm{M}(1, 2, 5, 7)$

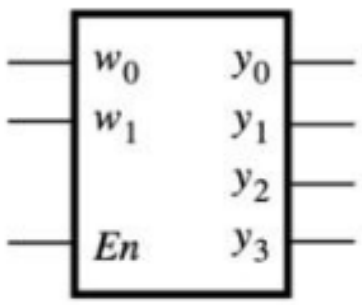
Your Answer: | **Correct Answer: B;C** | Not Attempted | Time taken: 00min 00sec | Discuss

Q #14 Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

A demultiplexer can be implemented using a decoder circuit.
For example, the 2-to-4 decoder can be used as a 1-to-4 demultiplexer. Which input of decoder serves as the data input for the demultiplexer?

En	w_1	w_0	y_0	y_1	y_2	y_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	$\times$	$\times$	0	0	0	0

(a) Truth Table of Decoder



(b) Graphical symbol

A. w_0
B. E_n
C. w_1
D. We can not implement a demultiplexer using a decoder.

Your Answer: | Correct Answer: B | Not Attempted | Time taken: 00min 00sec | Discuss

Q #15 Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

If $(1235)_x = (3033)_y$, where x and y indicate the bases of the corresponding numbers, then

A. $x = 7$ and $y = 5$
B. $x = 8$ and $y = 6$
C. $x = 6$ and $y = 4$
D. $x = 9$ and $y = 7$

Your Answer: | Correct Answer: B | Not Attempted | Time taken: 00min 00sec | Discuss

Q #16 Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

A function of Boolean variables X, Y and Z is expressed in terms of the min-terms as

$$F(X, Y, Z) = \Sigma(1, 2, 5, 6, 7)$$

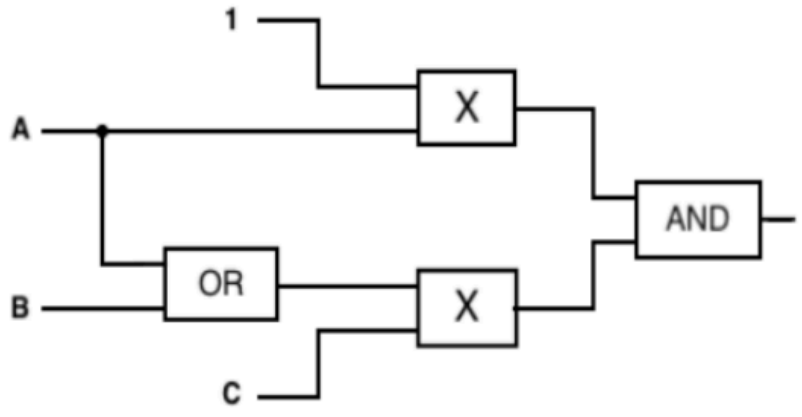
Which one of the product of sums given below is equal to the function $F(X, Y, Z)$?

A. $(\overline{X} + \overline{Y} + \overline{Z}) \cdot (\overline{X} + Y + Z) \cdot (X + \overline{Y} + \overline{Z})$
B. $(X + Y + Z) \cdot (X + \overline{Y} + \overline{Z}) \cdot (\overline{X} + Y + Z)$
C. $(\overline{X} + \overline{Y} + Z) \cdot (\overline{X} + Y + \overline{Z}) \cdot (X + \overline{Y} + Z) \cdot (X + Y + \overline{Z}) \cdot (X + Y + Z)$
D. $(X + Y + \overline{Z}) \cdot (\overline{X} + Y + Z) \cdot (\overline{X} + Y + \overline{Z}) \cdot (\overline{X} + \overline{Y} + Z) \cdot (\overline{X} + \overline{Y} + \overline{Z})$

Your Answer: | Correct Answer: B | Not Attempted | Time taken: 00min 00sec | Discuss

Q #17 Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

The combinatorial circuit shown below takes three 1-bit inputs: A, B, and C, and produces one 1-bit output. The relationship between the inputs and the output is shown below as a truth table. The circuit contains two identical, unknown gates X.



A	B	C	Out
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

What is gate X ?

A. AND
B. XNOR
C. NAND
D. XOR

Your Answer: | Correct Answer: D | Not Attempted | Time taken: 00min 00sec | Discuss

Q #18 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

A logic circuit implements the boolean function $F = \overline{X} \cdot Y + X \cdot \overline{Y} \cdot \overline{Z}$. It is found that the input combination $X = Y = 1$ can never occur. Taking this into account, a simplified expression for F is given by

A. $\overline{X} + \overline{Y} \cdot \overline{Z}$
B. $X + Z$
C. $X + Y$
D. $Y + X \cdot \overline{Z}$

Your Answer: | Correct Answer: D | Not Attempted | Time taken: 00min 00sec | Discuss

Q #19 | Multiple Select Type | Award: 2 | Penalty: 0 | Digital Logic

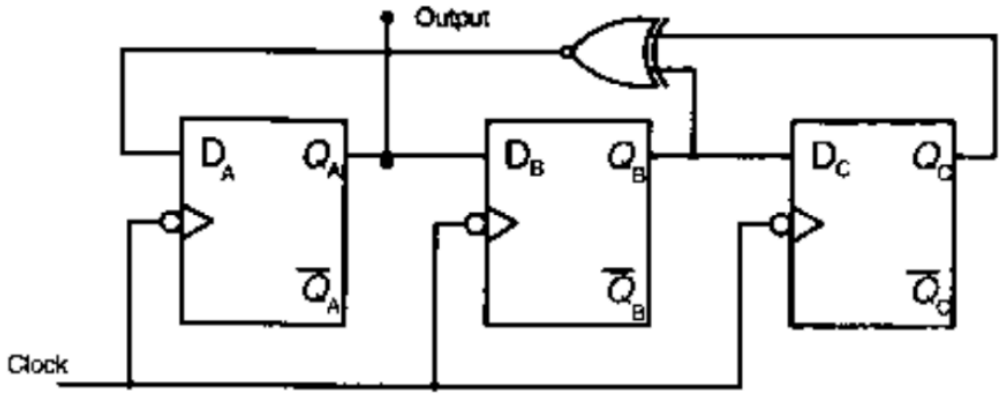
Consider a Boolean gate (D) where the output Y is related to the inputs A and B as, $Y = A + \overline{\overline{B}}$, where $+$ denotes logical OR operation. The Boolean inputs $'0'$ and $'1'$ are also available separately. Using instances of only D gates and inputs $'0'$ and $'1'$, _____ (select the correct option(s)).

A. NAND logic can be implemented
B. OR logic cannot be implemented
C. NOR logic can be implemented
D. AND logic cannot be implemented

Your Answer: | Correct Answer: A;C | Not Attempted | Time taken: 00min 00sec | Discuss

Q #20 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

Assuming that all flip-flops are in reset condition initially. the count sequence observed at $\mathrm{Q_A}$ in the circuit shown is

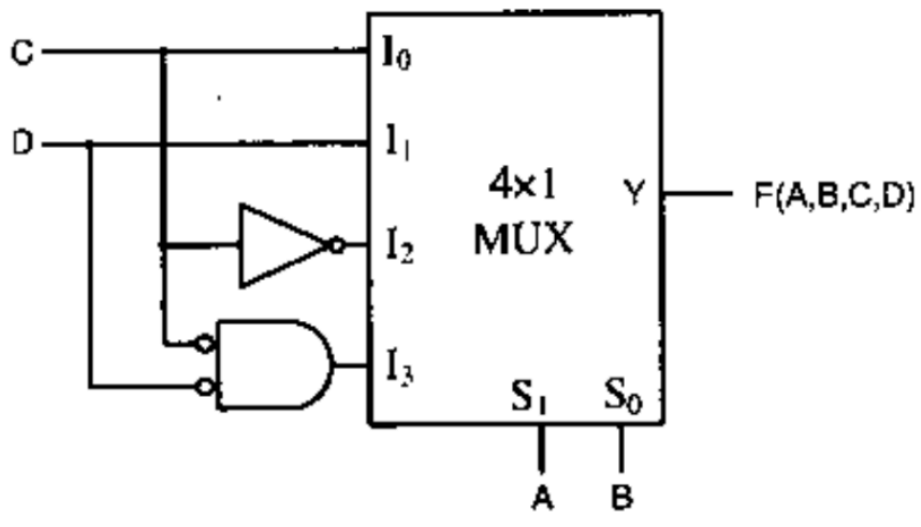


A. 0010111 . . .
B. 0001011 . . .
C. 0101111 . . .
D. 0110100 . . .

Your Answer: | **Correct Answer: D** | Not Attempted | Time taken: 00min 00sec | Discuss

Q #21 Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

The Boolean function realized by the logic circuit shown is



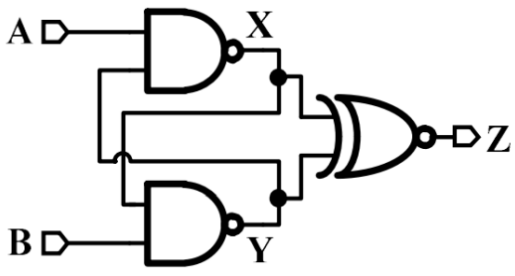
A. $\mathrm{F} = \Sigma_m(0, 1, 3, 5, 9, 10.14)$
B. $\mathrm{F} = \Sigma_m(2, 3, 5, 7, 8, 12, 13)$
C. $\mathrm{F} = \Sigma_m(1, 2, 4, 5, 11, 14, 15)$
D. $\mathrm{F} = \Sigma_m(2, 3, 5, 7, 8, 9, 12)$

Your Answer: | **Correct Answer: D** | Not Attempted | Time taken: 00min 00sec | Discuss

Q #22 Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

In the circuit diagram shown below, the logic gates operate with a supply voltage of $1\ \mathrm{V}$. NAND and XNOR have $200\ \mathrm{ps}$ and $400\ \mathrm{ps}$ input-to-output delay, respectively.

At time $t = \mathrm{T}$, $\mathrm{A}(t) = 0, \mathrm{B}(t) = 1$ and $\mathrm{Z}(t) = 0$. When the inputs are changed to $\mathrm{A}(t) = 1, \mathrm{B}(t) = 0$ at $t = 2\mathrm{T}$, a $1\ \mathrm{V}$ pulse is observed at Z. The pulse width of the $1\ \mathrm{V}$ pulse is _____ ps.

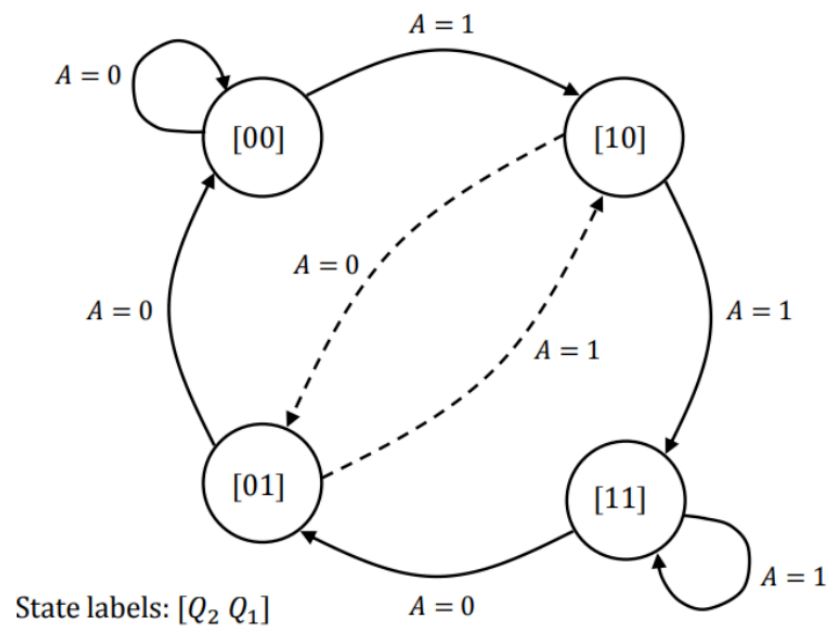


A. 100
B. 200
C. 400
D. 600

Your Answer: | Correct Answer: B | Not Attempted | Time taken: 00min 00sec | Discuss

Q #23 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

An synchronous finite state machine (FSM) with input "A" has the function described in the following state diagram and is to be implemented using two synchronously clocked D-Type flip-flops D_1, D_2 as the state registers.



The Flip-Flop outputs are $\{Q_2, Q_1\}$ where Q_1, Q_2 are output of D_1, D_2 respectively and Q_1 represents the least significant bit of the FSM output.

Then which of the following is true?

A. $D_1 = A, D_2 = Q_1$
B. $D_1 = Q_2, D_2 = A$
C. $D_1 = Q_2, D_2 = Q_1 \oplus A$
D. None of the above

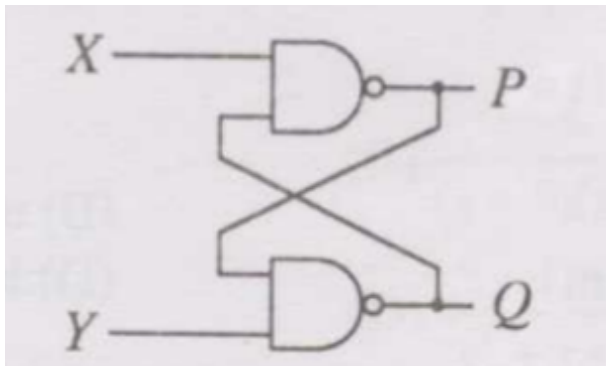
Your Answer: | Correct Answer: B | Not Attempted | Time taken: 00min 00sec | Discuss

Q #24 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

The following binary values were applied to the X and Y inputs of the NAND latch shown in the figure in the sequence indicated below:

$$X = 0, Y = 1; \qquad X = 0, Y = 0; \qquad X = 1, Y = 1.$$

The corresponding stable P, Q outputs will be

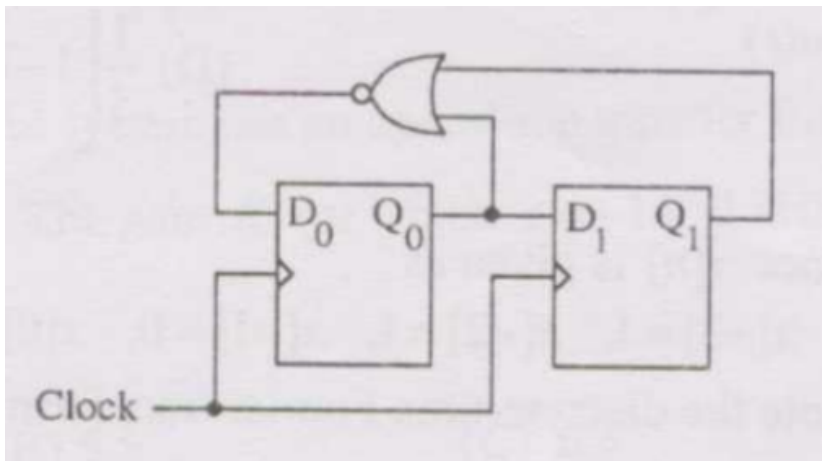


A. $P = 1, Q = 0;$ $P = 1, Q = 0;$ $P = 1, Q = 0$ or $P = 0, Q = 1$
B. $P = 1, Q = 0;$ $P = 0, Q = 1$ or $P = 0, Q = 1;$ $P = 0, Q = 1$
C. $P = 1, Q = 0;$ $P = 1, Q = 1;$ $P = 1, Q = 0$ or $P = 0, Q = 1$
D. $P = 1, Q = 0;$ $P = 1, Q = 1;$ $P = 1, Q = 1$

Your Answer: | Correct Answer: C | Not Attempted | Time taken: 00min 00sec | Discuss

Q #25 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

For the circuit shown, the counter state $(Q_1 Q_0)$ follows the sequence



A. $00, 01, 10, 11, 00, \ldots$
B. $00, 01, 10, 00, 01, \ldots$
C. $00, 01, 11, 00, 01, \ldots$
D. $00, 10, 11, 00, 10, \ldots$

Your Answer: | Correct Answer: B | Not Attempted | Time taken: 00min 00sec | Discuss

Q #26 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

Match the Boolean expression with its minimal realization

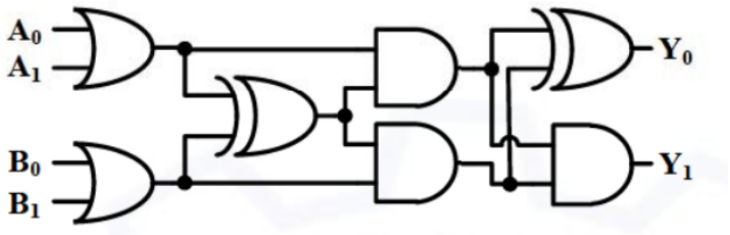
	Boolean expression		Minimal realization
P	$\overline{X}\,\overline{Y}\,\overline{Z} + \overline{X}\,Y\,\overline{Z} + \overline{X}YZ$	K	$X(Y+Z)$
Q	$XYZ + X\overline{Y}Z + XY\overline{Z}$	L	$\overline{X}(Y+\overline{Z})$
R	$XY + XYZ + XY\overline{Z} + \overline{X}YZ$	M	Z
S	$\overline{X}\,\overline{Y}Z + \overline{X}YZ + X\overline{Y}Z + XYZ$	N	$Y(X+Z)$

A. P-K, Q-L, R-N, S-M
B. P-L, Q-K, R-N, S-M
C. P-L, Q-N, R-M, S-K
D. P-M, Q-K, R-L, S-N

Your Answer: | Correct Answer: B | Not Attempted | Time taken: 00min 00sec | Discuss

Q #27 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

In the circuit shown below, Y is a 2-bit $(Y_1 Y_0)$ output of the combinational logic. What is the maximum value of Y for any given digital inputs, $A_1 A_0$ and $B_1\ B_0$?

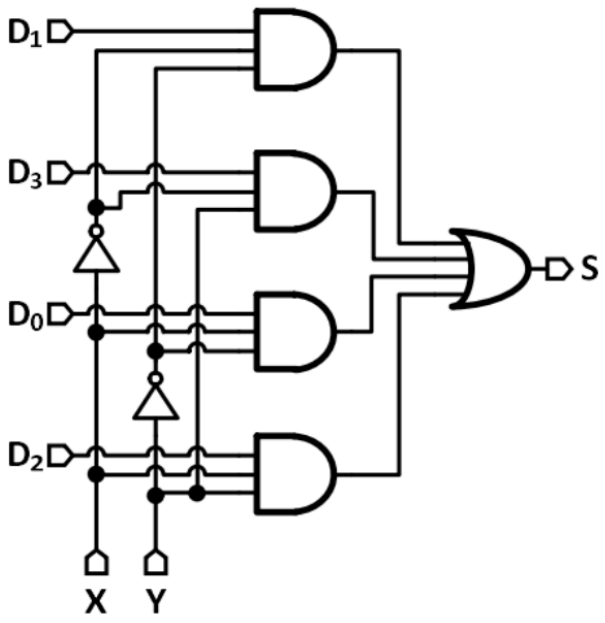


A. 01
B. 10
C. 00
D. 11

Your Answer: | Correct Answer: A | Not Attempted | Time taken: 00min 00sec | Discuss

Q #28 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

Input bits X and Y are added by using the combinational logic as shown below. S represents the sum of the two bits. For a correct implementation of the sum, the signals $\mathrm{D}_0, \mathrm{D}_1, \mathrm{D}_2, \mathrm{D}_3$ are, respectively.



A. $1, 0, 0, 1$
B. $0, 1, 0, 1$
C. $1, 0, 1, 1$
D. $0, 1, 1, 0$

Your Answer: | Correct Answer: A | Not Attempted | Time taken: 00min 00sec | Discuss

Q #29 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

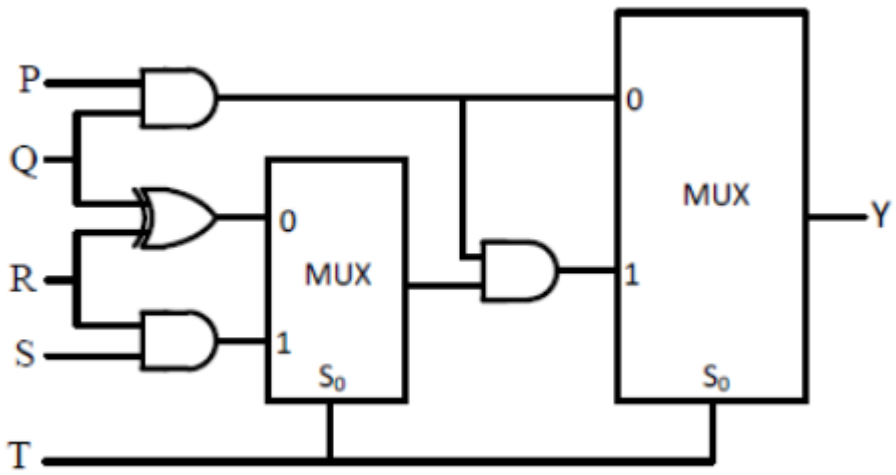
Let $b_q b_{q-1} \ldots b_0$ be the binary representation of integer b. The integer 3 is a divisor of b if and only if

A. $b_1 = b_0 = 1$
B. The sum of the binary digits b_i is divisible by 3.
C. The alternating sum $b_0 - b_1 + b_2 - \ldots$ is zero.
D. The alternating sum $b_0 - b_1 + b_2 - \ldots$ is divisible by 3.

Your Answer: | Correct Answer: D | Not Attempted | Time taken: 00min 00sec | Discuss

Q #30 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

The propagation delays of the XOR gate, AND gate and multiplexer (MUX) in the circuit shown in the figure are $4\ \mathrm{ns}, 2\ \mathrm{ns}$ and $1\ \mathrm{ns}$, respectively.



If all the inputs $\mathrm{P}, \mathrm{Q}, \mathrm{R}, \mathrm{S}$ and T are applied simultaneously and held constant, the maximum propagation delay of the circuit is

A. $3\ \mathrm{ns}$
B. $5\ \mathrm{ns}$
C. $6\ \mathrm{ns}$
D. $7\ \mathrm{ns}$

Your Answer: **Correct Answer: C** Not Attempted Time taken: 00min 00sec Discuss

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