

# Computer Organisation and Architecture

## Cache Memory

DPP XXXX**[MCQ]**

1. Consider a processor that can support a maximum memory of 8GB, where the memory is word-addressable (a word consists of 2 bytes). Then the size of the address bus of the processor is at least \_\_\_\_\_ bits.
- (a) 31                      (b) 32  
(c) 33                      (d) 34

**[NAT]**

2. Assume a direct mapped cache having 8 cache lines, each cache line consists of 2 words and each word is of one byte. The address bus consists of 7 bits, then the tag field of the cache consists of \_\_\_\_\_ bits.

**[NAT]**

3. Assume a 32-bit addressable physical memory and 2 MB cache block of size 8 kB each, then how many bits are required in the tag field of the cache address if the cache is 4-way set associative \_\_\_\_\_

**[MCQ]**

4. Consider a 16-Kbyte cache with the following features, each block will hold 32 bytes of data (not including tag, valid, gve"í +."Vj g"ecej g"y qwf"dg"4-way set associative, physical addresses are 32 bits and data is addressed to the word and words are of 32 bits long. Then how many blocks would be in this cache and how many bits of tag are stored with each block entry?
- (a) 512, 19                      (b) 512, 22  
(c) 256, 20                      (d) 512, 21

**[MCQ]**

5. Consider a 16 KB, two-way associative cache with 32-Byte cache line and a 64 bits address space, there will be p bits used for index. Let suppose if that same

cache were fully associative, you need q bits to be used for the index then the value for  $p + q =$  \_\_\_\_\_.

- (a) 6                      (b) 7  
(c) 8                      (d) 9

**[NAT]**

6. Consider a system having 512KB, 16-way set associative  $L_2$  cache with a 128 byte cache line size, Then how many cache lines are present? \_\_\_\_\_

**[NAT]**

7. Assume a cache with 32-bit address, 768 blocks and a block size of 128 bytes, tags are 17 bits then what is the associativity of the cache \_\_\_\_\_?

**[MCQ]**

8. Assume a direct mapped cache memory with 16 cache block (0 to 15) and a main memory having 256 blocks (0 to 255). Assume that, initially the cache did not have any memory block, Consider the following sequence of memory block references:  
3, 180, 43, 2, 191, 881, 190, 14, 181, 44, 186 and 253, Then which memory blocks will be present in the cache after the above sequence of memory block reference?
- (a) 2, 3, 180, 43, 2, 191, 190, 88, 14, 181, 44, 186  
(b) 2, 3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 181, 44, 186, 253  
(c) 2, 3, 180, 181, 881, 186, 43, 44, 253, 14, 191  
(d) None of the above

**[MCQ]**

9. Assume the access patterns x, y, z, y, x where each letter corresponds to a unique cache block and also assume that there was no access to any block before this and all conflicts are random. Then what is the probability of the second access to x being a hit on a direct mapped cache with 4 line (closest to)?
- (a) 40%                      (b) 50%  
(c) 80%                      (d) 100%









