VGA Interfacing with FPGA

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NEED FOR THE STUDY

The objective is to make a video card that stores a low-bit (low resolution and colour-accurate) image and a VGA interface to display on an LCD monitor. As we know, VGAs are used in old displays as a medium to transmit data to be displayed.

A stand-alone VGA interface cannot display anything; thus, a supporting graphics card or video card is required to fetch and send the data in proper order. This project could be extended to output a simple game on a screen and can be played by user input from FPGA.

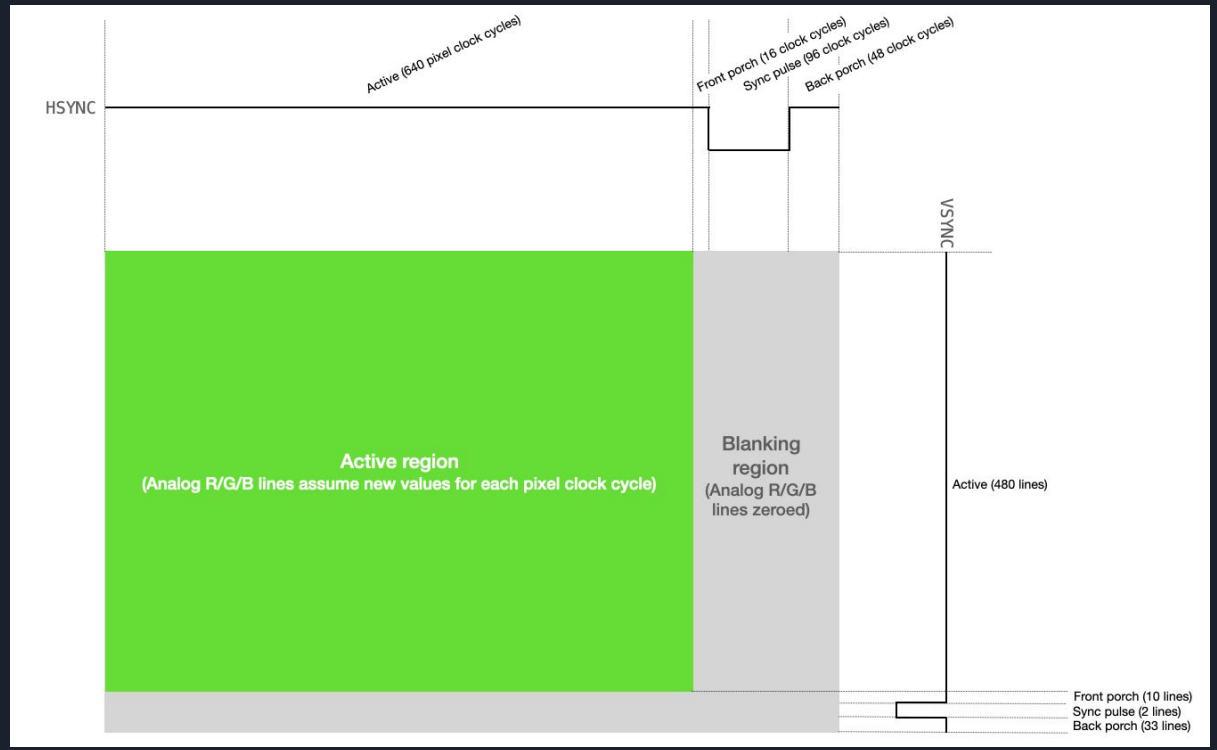
INTRODUCTION

VGA, an abbreviation of Video Graphics Array, is a connector that displays content on analog screens.
VGA is a 15-pin connector that can display at different resolutions and refresh rates.

Pinout diagram and schematics

Pin 1 RED Red pixel value
Pin 2 GREEN Green pixel value
Pin 3 BLUE Blue pixel value
Pin 4 ID2/RES N/A
Pin 5 GND Ground (H-sync)
Pin 6 RED_RTN Red return
Pin 7 GREEN_RTN Green return
Pin 8 BLUE_RTN Blue return
Pin 9 KEY/PWR
Pin 10 GND Ground (V-sync)
Pin 11 ID0/RES N/A
Pin 12 ID1/SDA N/A
Pin 13 HSYNC Horizontal Sync
Pin 14 VSYNC Vertical Sync
Pin 15 ID3/SCL N/A

Active Area


Active (640 pixel clock cycles)
Front porch (16 clock cycles)
Sync pulse (96 clock cycles)
Back porch (48 clock cycles)
HSYNC
VSYNC
Active region
(Analog R/G/B lines assume new values for each pixel clock cycle)
Blanking region
(Analog R/G/B lines zeroed)
Active (480 lines)
Front porch (10 lines)
Sync pulse (2 lines)
Back porch (33 lines)

WORKING

The horizontal and vertical sync signals are digital waveforms that synchronise the signal timing with the monitor. In simple words, horizontal and vertical sync with the pixel clock results in displayed pixel coordinates.

Since these are digital signals, they are provided directly by the FPGA. The colour magnitudes, i.e. R, G and B, are 0V-0.7V analog signals.

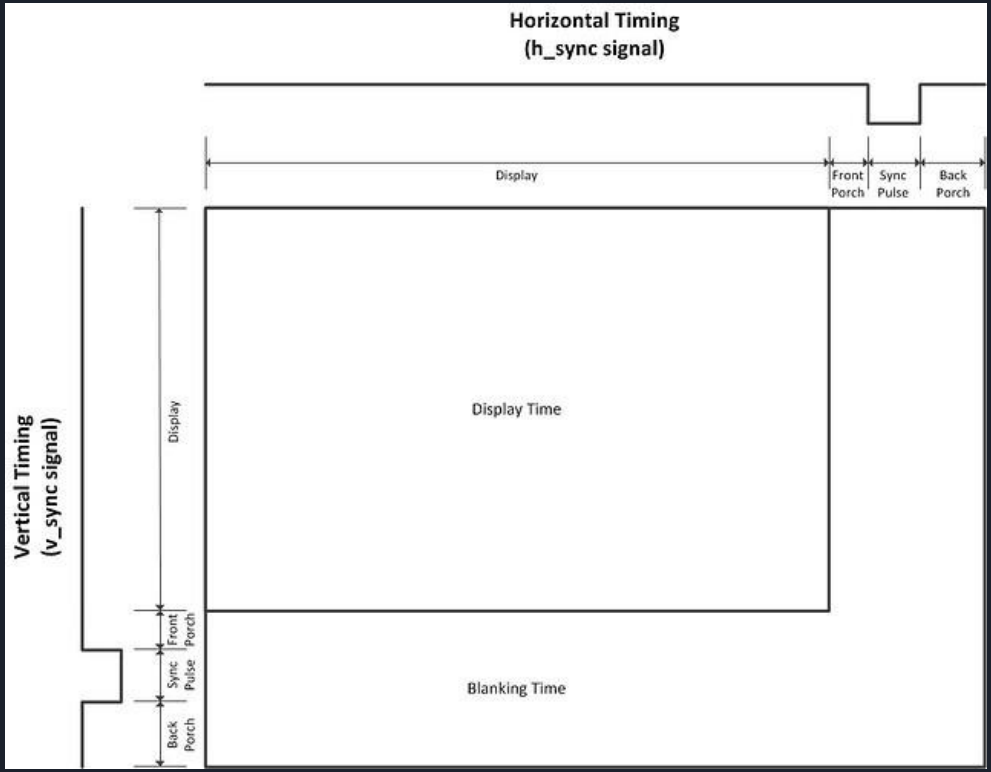
Signal Timing

VGA interface works on standardised modes, with a specific resolution and refresh rate. Each mode has defined timing parameters and frequency. The appendix in the next slide lists the signal timing specifications for numerous VGA modes.

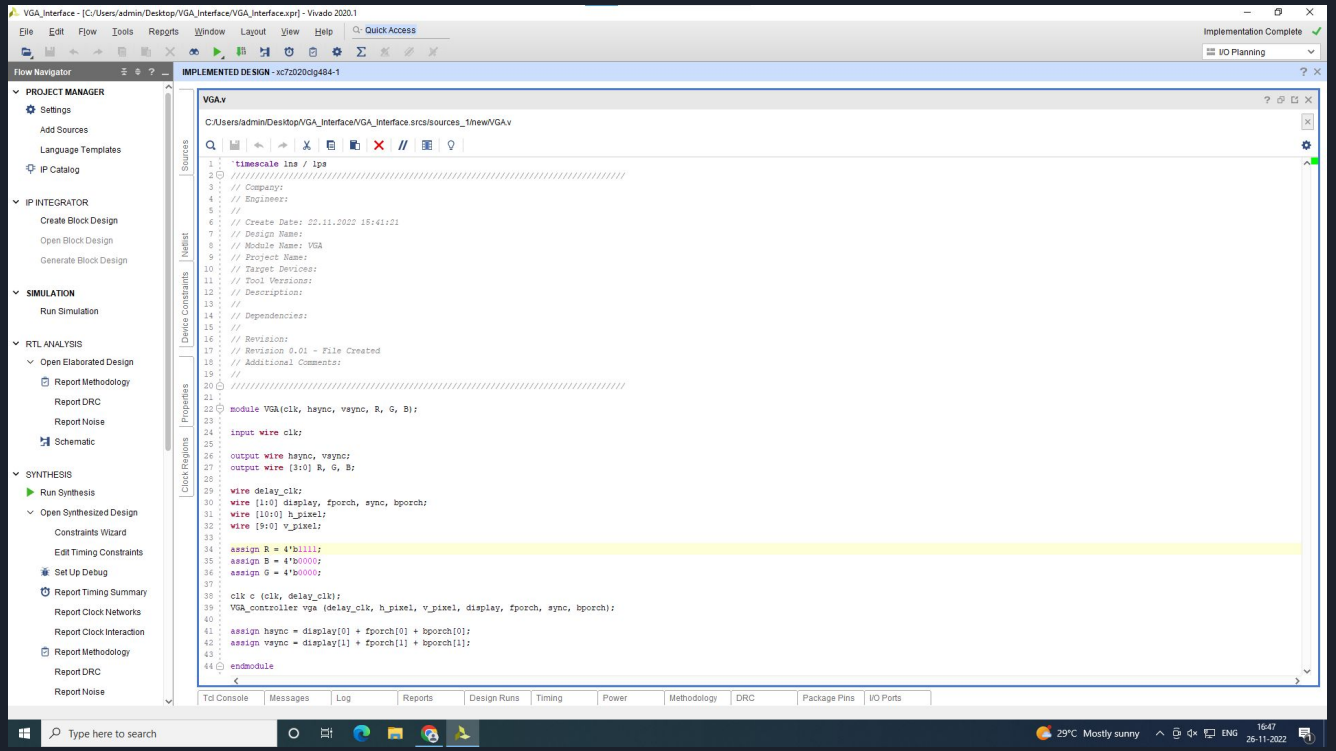
Signal Timing

			Horizontal (pixel clocks)				Vertical (rows)					
Resolution	Refresh Rate (Hz)	Pixel Clock (MHz)	Display	Front Porch	Sync Pulse	Back Porch	Display	Front Porch	Sync Pulse	Back Porch	Hsync Polarity	Vsync Polarity
640x350	70	25.175	640	16	96	48	350	37	2	60	p	n
640x350	85	31.5	640	32	64	96	350	32	3	60	p	n
640x400	70	25.175	640	16	96	48	400	12	2	35	n	p
640x400	85	31.5	640	32	64	96	400	1	3	41	n	p
640x480	60	25.175	640	16	96	48	480	10	2	33	n	n
640x480	73	31.5	640	24	40	128	480	9	2	29	n	n
640x480	75	31.5	640	16	64	120	480	1	3	16	n	n
640x480	85	36	640	56	56	80	480	1	3	25	n	n
640x480	100	43.16	640	40	64	104	480	1	3	25	n	p
720x400	85	35.5	720	36	72	108	400	1	3	42	n	p
768x576	60	34.96	768	24	80	104	576	1	3	17	n	p
768x576	72	42.93	768	32	80	112	576	1	3	21	n	p
768x576	75	45.51	768	40	80	120	576	1	3	22	n	p
768x576	85	51.84	768	40	80	120	576	1	3	25	n	p
768x576	100	62.57	768	48	80	128	576	1	3	31	n	p
800x600	56	36	800	24	72	128	600	1	2	22	p	p
800x600	60	40	800	40	128	88	600	1	4	23	p	p
800x600	75	49.5	800	16	80	160	600	1	3	21	p	p
800x600	72	50	800	56	120	64	600	37	6	23	p	p
800x600	85	56.25	800	32	64	152	600	1	3	27	p	p
800x600	100	68.18	800	48	88	136	600	1	3	32	n	p
1024x768	43	44.9	1024	8	176	56	768	0	8	41	p	p
1024x768	60	65	1024	24	136	160	768	3	6	29	n	n
1024x768	70	75	1024	24	136	144	768	3	6	29	n	n

Theory of Operation



Code Screenshots



Code Screenshots - Clock Design

VGA_Interface - [C:/Users/admin/Desktop/VGA_Interface/VGA_Interface.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Quick Access

Implementation Complete

I/O Planning

Flow Navigator

PROJECT MANAGER
- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR
- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Open Elaborated Design
  - Report Methodology
  - Report DRC
  - Report Noise
  - Schematic

SYNTHESIS
- Run Synthesis
- Open Synthesized Design
  - Constraints Wizard
  - Edit Timing Constraints
  - Set Up Debug
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Noise

IMPLEMENTED DESIGN - xc7z020clg484-1

clk.v | VGA.v

C:/Users/admin/Desktop/VGA_Interface/VGA_Interface.srcs/sources_1/new/clk.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 22.11.2022 16:22:22
// Design Name:
// Module Name: clk
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////

//to produce 25MHz signals
module clk(clk, del_clk);
input wire clk;
output reg del_clk;

reg [1:0] cnt;

always @(posedge clk)
begin
    cnt = cnt + 1;
    del_clk = cnt[1];
end

endmodule
```

Tcl Console | Messages | Log | Reports | Design Runs | Timing | Power | Methodology | DRC | Package Pins | I/O Ports

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Code Screenshots- Vertical Counter

h_counter.v

C:/Users/admin/Desktop/VGA_Interface/VGA_Interface.srcs/sources_1/new/h_counter.v

```
/*
 * h_sync info::
     * pixel clk = 108MHz
     * display = 1152 ticks
     * front porch = 64 ticks
     * sync pulse = 128 ticks
     * back porch = 256 ticks
     * TOTAL == 1600 ticks
 */
/*
 * h_sync info 25MHz::
     * pixel clk = 25MHz
     * display = 640 ticks
     * front porch = 16 ticks
     * sync pulse = 96 ticks
     * back porch = 48 ticks
     * TOTAL == 800 ticks
 */
module h_counter (clk, display, front_porch, sync_pulse, back_porch, h_pixel);
    input wire clk;
    output reg display, front_porch, sync_pulse, back_porch;
    output reg [10:0] h_pixel;

    initial
    begin
        h_pixel = 11'b0;
        display = 1'b1;
        front_porch = 1'b0;
        sync_pulse = 1'b1;
        back_porch = 1'b0;
    end
    always @(posedge clk)
    begin
        if (h_pixel == 799)
        begin
            display = 1'b1;
            front_porch = 1'b0;
            sync_pulse = 1'b1;
            back_porch = 1'b0;

            h_pixel = 11'b0;
        end
        else if (h_pixel >= 752)
        begin
            display = 1'b0;
            front_porch = 1'b0;
            sync_pulse = 1'b1;
            back_porch = 1'b1;

            h_pixel = h_pixel + 1;
        end
        else if (h_pixel >= 656)
        begin
            display = 1'b0;
```

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Code Screenshots- Horizontal Counter

v_counter.v

C:/Users/admin/Desktop/VGA_Interface/VGA_Interface.srcs/sources_1/new/v_counter.v

```
/*
 * v_sync info::
     * pixel clk = 108MHz
     * display = 864 ticks
     * front porch = 1 ticks
     * sync pulse = 3 ticks
     * back porch = 32 ticks
     * TOTAL == 900 ticks
 */
/*
 * v_sync info::
     * pixel clk = 25MHz
     * display = 480 ticks
     * front porch = 10 ticks
     * sync pulse = 2 ticks
     * back porch = 33 ticks
     * TOTAL == 525 ticks
 */
module v_counter (clk, display, front_porch, sync_pulse, back_porch, v_pixel);
    input wire clk;
    output reg display, front_porch, sync_pulse, back_porch;
    output reg [9:0] v_pixel;

    initial
    begin
        v_pixel = 9'b0;
        display = 1'b1;
        front_porch = 1'b0;
        sync_pulse = 1'b1;
        back_porch = 1'b0;
    end
    always @(negedge clk)
    begin
        if (v_pixel == 524)
        begin
            display = 1'b1;
            front_porch = 1'b0;
            sync_pulse = 1'b1;
            back_porch = 1'b0;

            v_pixel = 9'b0;
        end
        else if (v_pixel >= 492)
        begin
            display = 1'b0;
            front_porch = 1'b0;
            sync_pulse = 1'b1;
            back_porch = 1'b1;

            v_pixel = v_pixel + 1;
        end
        else if (v_pixel >= 490)
        begin
            display = 1'b0;
```

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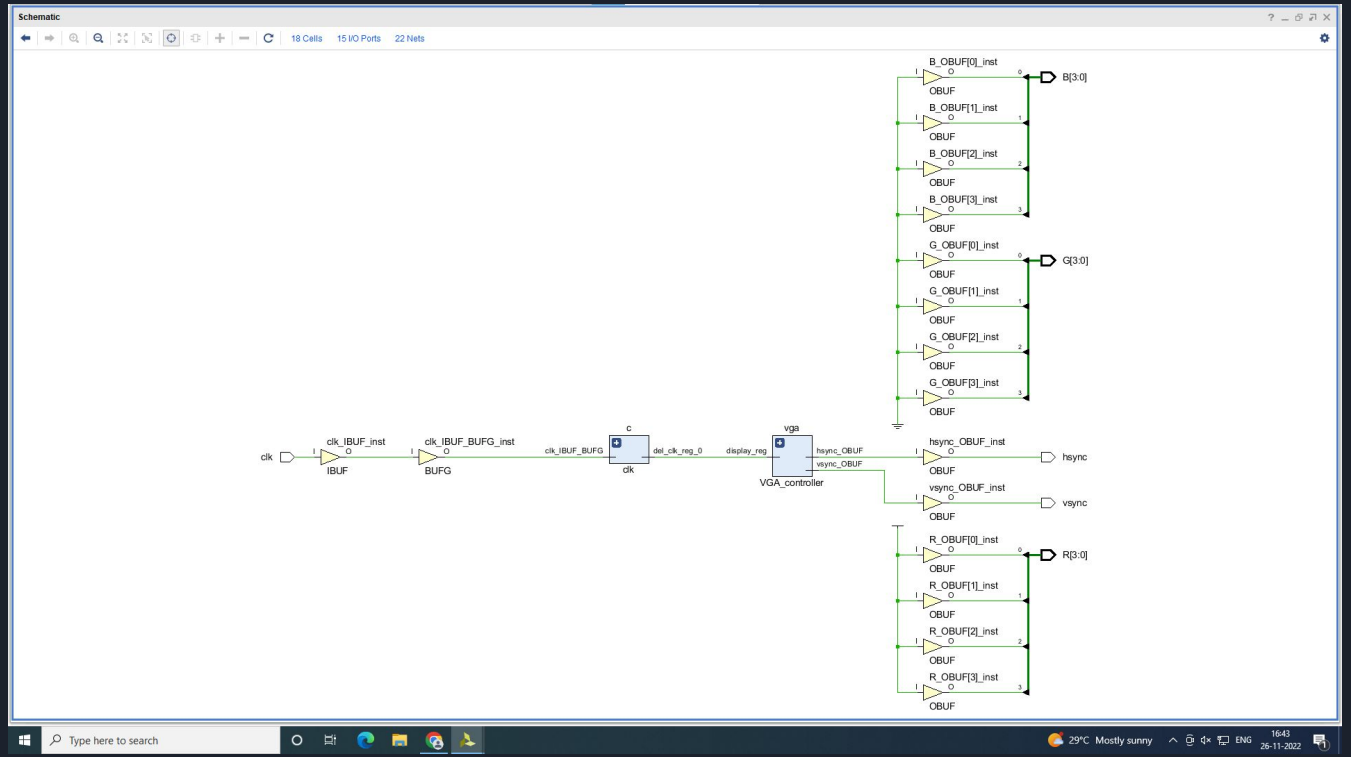
Schematic


Schematic
18 Cells
15 I/O Ports
22 Nets
B_OBUF[0]_inst
OBUF
B[3:0]
B_OBUF[1]_inst
B_OBUF[2]_inst
B_OBUF[3]_inst
G_OBUF[0]_inst
G[3:0]
G_OBUF[1]_inst
G_OBUF[2]_inst
G_OBUF[3]_inst
clk
clk_IBUF_inst
IBUF
clk_IBUF_BUFG_inst
BUFG
clk_IBUF_BUFG
c
clk
del_clk_reg_0
display_reg
vga
VGA_controller
hsync_OBUF
vsync_OBUF
hsync_OBUF_inst
hsync
vsync_OBUF_inst
vsync
R_OBUF[0]_inst
R[3:0]
R_OBUF[1]_inst
R_OBUF[2]_inst
R_OBUF[3]_inst
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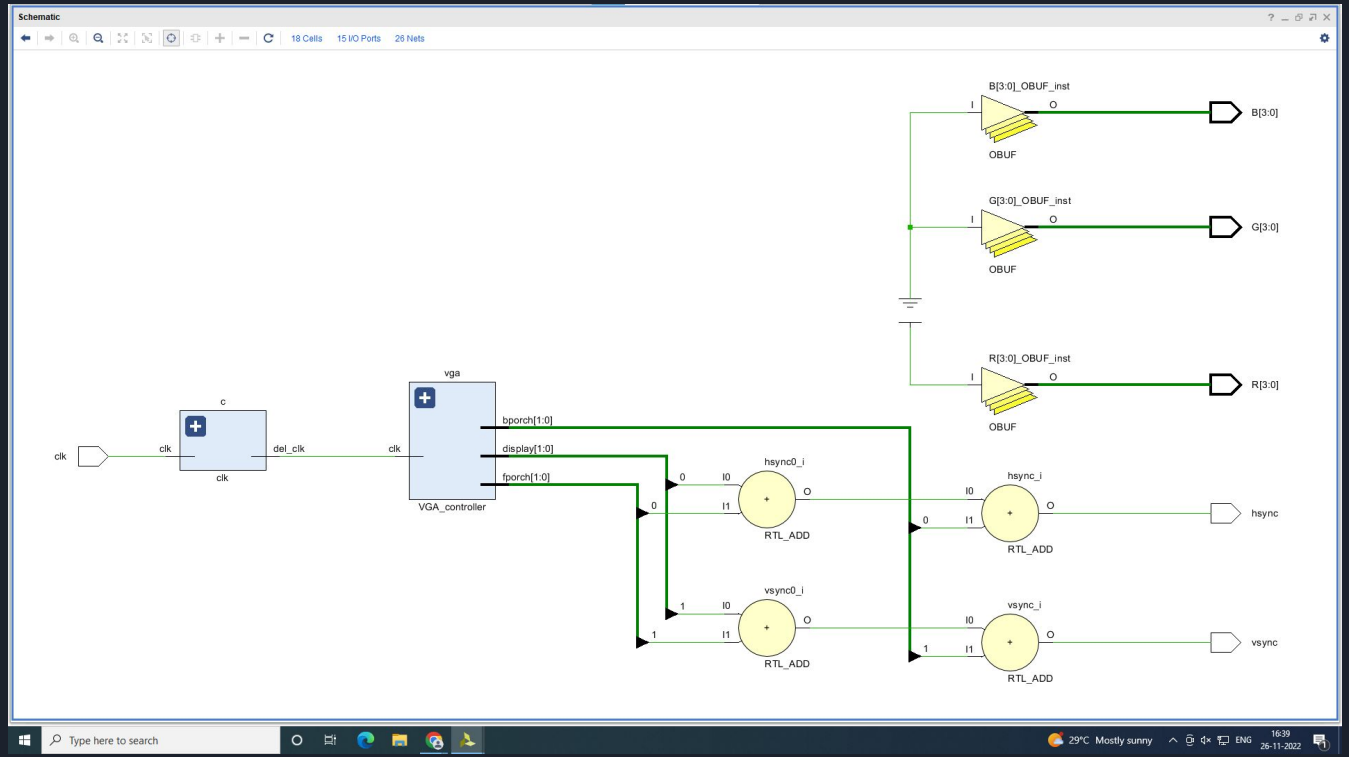
Schematic


Schematic
18 Cells
15 I/O Ports
26 Nets
B[3:0]_OBUF_inst
OBUF
B[3:0]
G[3:0]_OBUF_inst
OBUF
G[3:0]
R[3:0]_OBUF_inst
OBUF
R[3:0]
vga
c
clk
del_clk
bporch[1:0]
display[1:0]
fporch[1:0]
VGA_controller
hsync0_i
hsync_i
vsync0_i
vsync_i
RTL_ADD
hsync
vsync
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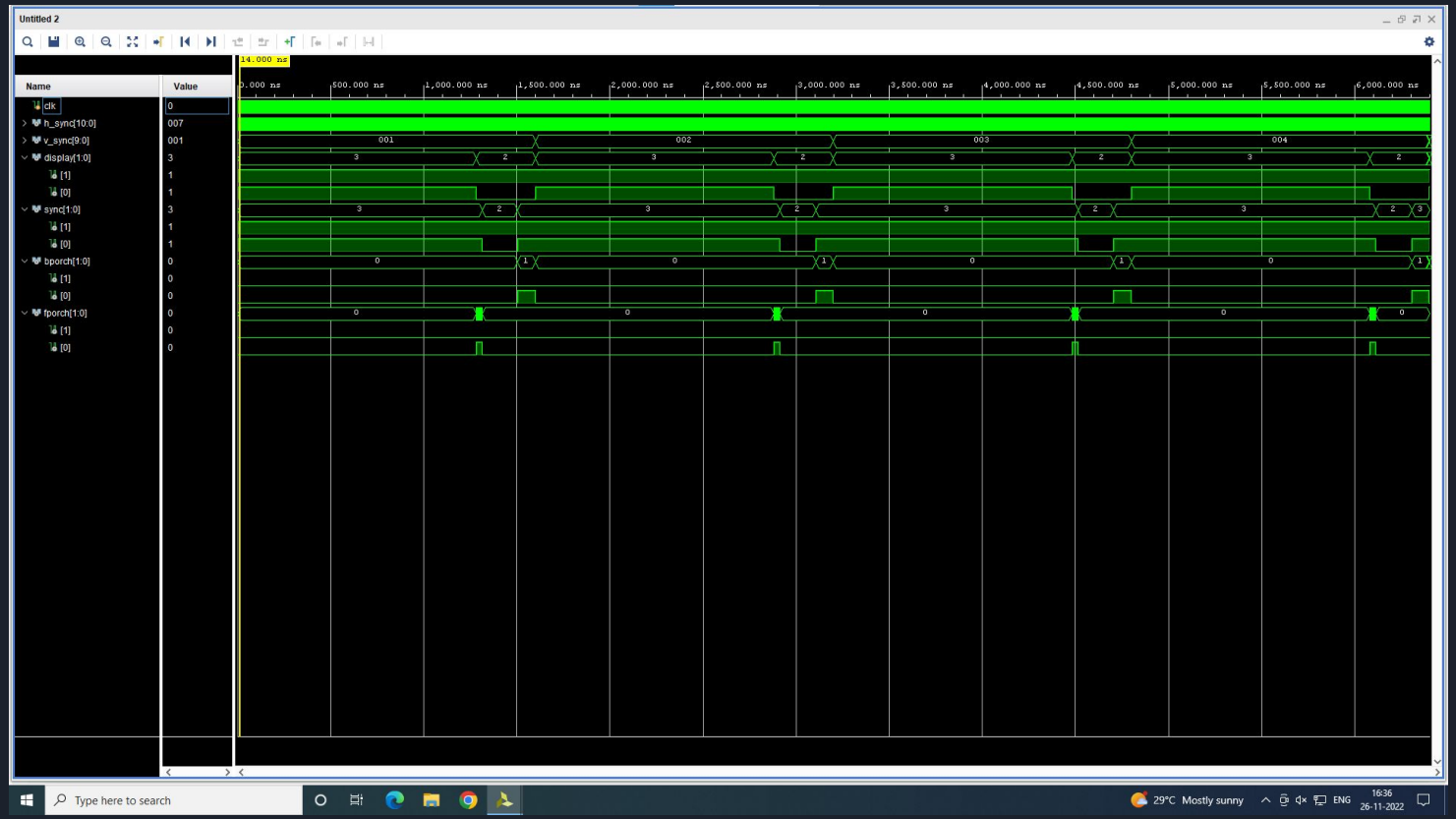
Waveform


Untitled 2
Name
Value
clk
h_sync[10:0]
v_sync[9:0]
display[1:0]
sync[1:0]
bporch[1:0]
fporch[1:0]
14.000 ns
500.000 ns
1,000.000 ns
1,500.000 ns
2,000.000 ns
2,500.000 ns
3,000.000 ns
3,500.000 ns
4,000.000 ns
4,500.000 ns
5,000.000 ns
5,500.000 ns
6,000.000 ns
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ENG
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26-11-2022

Power Utilization

Package | Device | h_counter_tb.v | v_counter.v | h_counter.v | clk.v | VGA.v | **Project Summary**

Overview | Dashboard

Summary: 1 warning

Implemented DRC Report

Worst Negative Slack (WNS):	NA
Total Negative Slack (TNS):	NA
Number of Failing Endpoints:	NA
Total Number of Endpoints:	NA

Implemented Timing Report

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

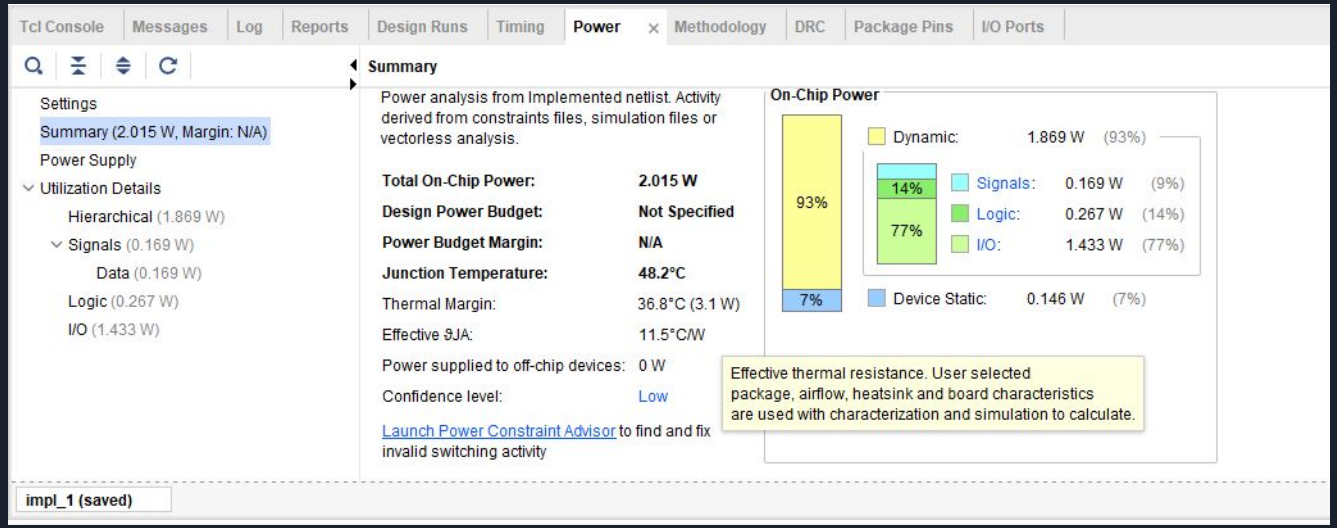
Resource	Utilization	Available	Utilization %
LUT	37	53200	0.07
FF	29	106400	0.03
IO	15	200	7.50
BUFG	1	32	3.13

Power **Summary** | On-Chip

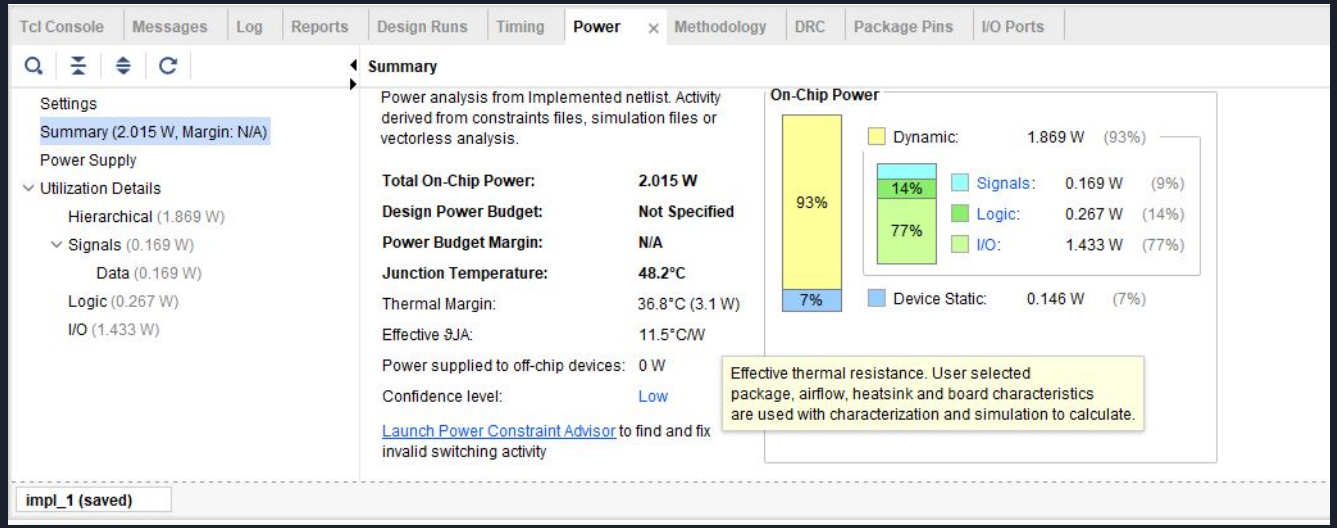
Total On-Chip Power:	**2.015 W**
Junction Temperature:	**48.2 °C**
Thermal Margin:	36.8 °C (3.1 W)
Effective ϑJA:	11.5 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report

Power Utilization



Power Utilization



CONCLUSION

VGA interface is one of many video interfaces used in this modern world. It is widely used in old generation HD and CRT monitors.
They were the standard interface back then but now is replaced by new standards like HDMI and DisplayPort.
This project helped us understand the working of CRT monitors and how to raster pixels on a screen. Along with these, we also learned how to transmit colour data to any monitor and how to read data sheets to implement something on your own.
Verilog codes and concepts taught in the FPGA Lab coursework helped us implement this project and its code from scratch.

REFERENCES

https://forum.digikey.com/t/vga-controller-vhdl/12794

https://en.wikipedia.org/wiki/VGA_connector

https://www.pcmag.com/encyclopedia/term/vga

https://youtu.be/l7rce6IQDWs

https://www.slideshare.net/sskrishnajith/snake-game-on-fpga-in-verilog