

August
29, 2018

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* SOP = O/P = 1

* D, \bar{A}
 $1, A$

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

TRUTH TABLE

* $\sum m_1 + m_4 + m_5 + m_7$
 $= \bar{a}\bar{b}c + a\bar{b}\bar{c} + a\bar{b}c + abc$

Experiment 3

* Aim : Realising given truth table using SOP form.

* Apparatus Required : Digital IC trainer, probes

* Theory :

(*) SUM OF PRODUCT (SOP) : It is a form of expression in Boolean algebra in which different product terms of inputs are being summed together. This product is not arithmetical multiply but it is Boolean logical AND & the sum is Boolean logical OR.

(*) STANDARD SUM OF PRODUCT : This is also known as Sum of Min terms or Canonical Form. Here, canonical means "Standardised".

Each & every variable should be present in each and every term of the equation.

$$Y_2 \leq (m_1, m_2, m_3, m_4)$$

EQUATION: Derived from the truth table:

$$\begin{aligned} Y_2 &= \bar{a}\bar{b}c + \bar{a}\bar{b}\bar{c} + a\bar{b}c + abc \\ &= \bar{a}\bar{b}c + a\bar{b}\bar{c} + ac(\bar{b} + b) \\ &= \bar{a}\bar{b}c + a\bar{b}\bar{c} + ac \end{aligned}$$

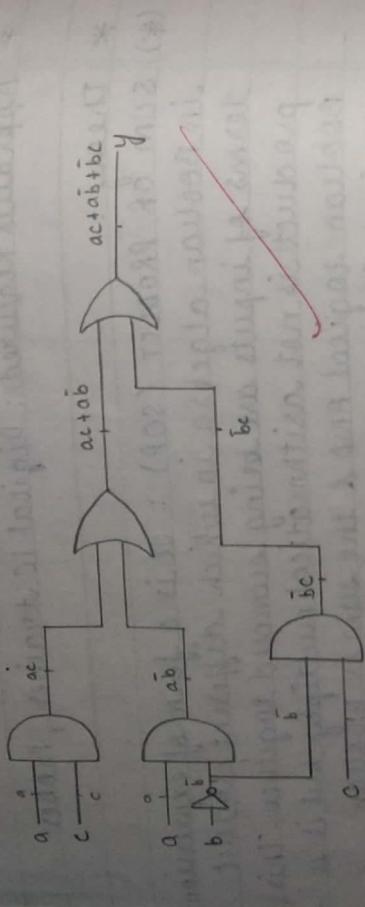
Teacher's Signature

Exercises

$$\begin{aligned}
 & 2 \bar{a}\bar{b}c + a(\bar{b}\bar{c} + c) \\
 & 2 \bar{a}\bar{b}c + a(\bar{b} + c) \\
 & 2 \bar{a}\bar{b}c + a\bar{b} + ac \\
 & 2 \bar{b}(\bar{a}c + a) + ac \\
 & 2 \bar{b}(c + a) + ac \\
 & = \bar{b}c + \bar{b}a + ac
 \end{aligned}$$

* Result : Realising given truth table using SOP form is verified.

~~29/10/16~~



Ques. Realise the given function using 4 input AND gate.

Ans. Given function

$$f(a, b, c) = \sum m(0, 1, 2, 3, 4, 5, 6)$$

$$= \bar{a}\bar{b}\bar{c} + \bar{a}\bar{b}c + \bar{a}b\bar{c} + \bar{a}bc + ab\bar{c} + abc$$

Using 4 input AND gate

$$f(a, b, c) = \bar{a}\bar{b}\bar{c}$$

$$\begin{aligned}
 & f(a, b, c) = \bar{a}\bar{b}\bar{c} \\
 & f(a, b, c) = (\bar{a} \cdot \bar{b}) \cdot \bar{c} \\
 & f(a, b, c) = \bar{a} \cdot (\bar{b} \cdot \bar{c})
 \end{aligned}$$

Experiment 4

* Aim : Realising given truth table using POS form

* Apparatus required: Digital IC trainer, probes

* Theory :

(*) PRODUCT OF SUM (POS) : A Boolean function expressed as a product of sum terms, i.e. as an AND of OR terms containing uncomplemented or complemented terms. Variables: the functions is also realizable as the NOR of a group of NOR terms.

(*) STANDARD PRODUCT OF SUM (S POS) : This is also known as product of NOR terms or canonical form. Here,

canonical means 'standardised'.

Each & every variable should be present in each & every term of the equation

$$Y = \prod (M_1, M_2, M_3, M_4)$$

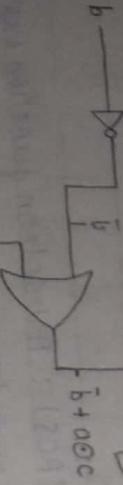
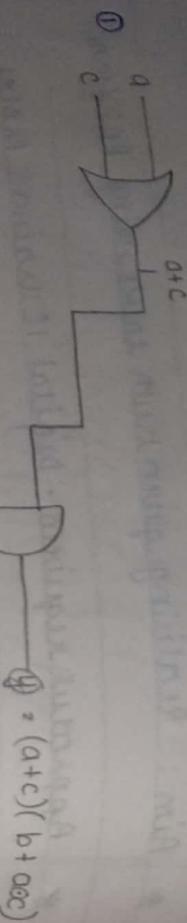
EQUATION: Derived from the truth table:

$$Y = (a+b+c)(a+\bar{b}+c)(a+b+\bar{c})(\bar{a}+\bar{b}+\bar{c}) \\ = [(a+a\bar{b}+a\bar{c})+(a\bar{b}+b\bar{b}+bc)+(ac+\bar{b}c+c\bar{c})] \\ \cdot [(a\bar{a}+a\bar{b}+a\bar{c})+(\bar{a}\bar{b}+\bar{b}\bar{b}+\bar{b}c)+(\bar{a}\bar{c}+\bar{b}\bar{c}+c\bar{c})]$$

QUESTION

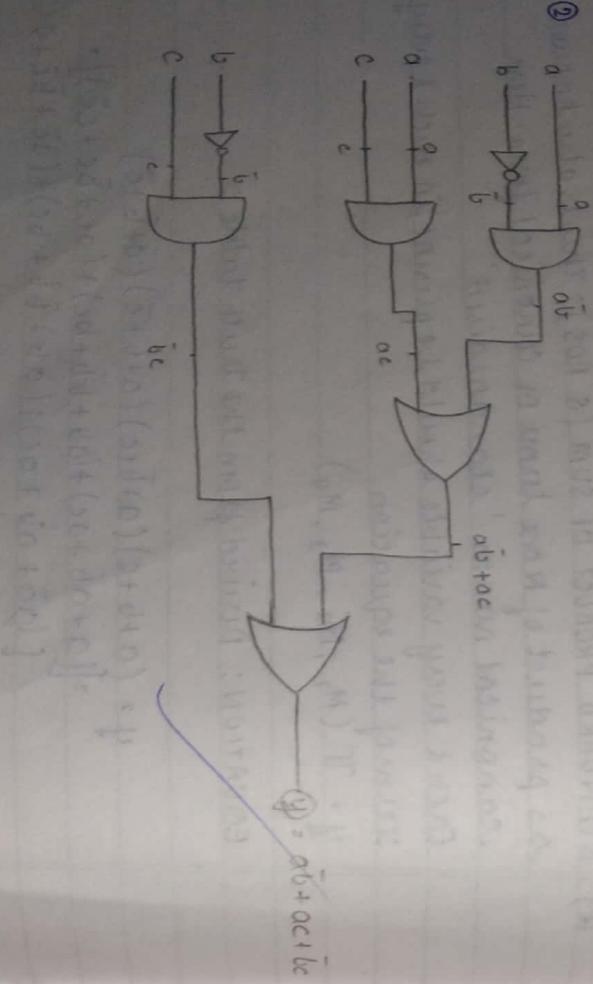
$$Y = (a + a\bar{b} + a\bar{c} + ab + b\bar{c} + c)(\bar{a}\bar{b} + \bar{a}\bar{c} + \bar{a}\bar{b} + \bar{b} + \bar{b}c + \bar{a}\bar{c} + \bar{b}\bar{c})$$

$$Y = [a(1 + \bar{b} + \bar{c} + \bar{b} + c) + c(\bar{b} + \bar{b} + 1)][\bar{b}(a + \bar{a} + 1 + c + \bar{c}) + ac + \bar{a}\bar{c}]$$



* Result: Realizing given truth table using POS form is verified.

12/19/18



EXPERIMENT 05

* Aim : Design and implementation of Half-adder and Half-subtractor.

* Apparatus required: Adder kit / Digital IC trainer, Probes

* Theory : ADDER
Adder is a combinational circuit which is used to perform addition operation.

Classification : It is classified in 2 types :

- a) Half adder
- b) Full adder

a) HALF ADDER : The half adder is an ex. of a simple, functional digital circuit built from two logic gates. The half adder adds two one bit binary numbers (A,B). The output is the sum of the two bits (S) and carry (C).

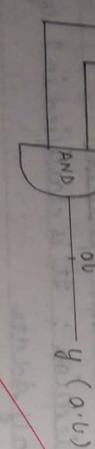
TRUTH TABLE :

A	B	Sum (S)	Carry (C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

CIRCUIT DIAGRAM:



(2) Product:



(2) Carry:

$a \bar{b}$	0	1
0	0	0
1	0	1

$$y = a \cdot b$$

* Result : Truth table of Half adder is verified.

K-MAP :

$a \bar{b}$	0	1
0	0	1
1	1	0

$$y = \bar{a}b + a\bar{b} = a \oplus b$$

EXPERIMENT 06

* Aim: To design and implementation of half subtractor.

* Apparatus required : Adder kit / Digital IC trainer, probes

* Theory: SUBTRACTION

Subtractor is a combination circuit which is used to perform subtraction operation.

Classification : It is classified into 2 types:

- Half subtractor
- Full subtractor

a) HALF SUBTRACTOR : The half subtractor is an ex. of a simple functional digital circuit built from two logic gates. The half subtractor subtracts two one-bit binary numbers (A & B). The output is the ~~diff~~^{diff} of two bits (d) and borrow (B^-).

TRUTH TABLE :

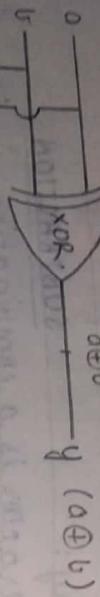
A	B	diff (d)	Borrow (B^-)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

K-MAP:

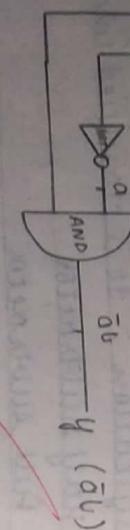
circuit DIAGRAM

(1) Difference :	$a \vee b$	0	-
	0	0	1
	1	1	0

$y = \bar{a}b + a\bar{b} = a \oplus b$



(ii) Borrow :



(2) Borrow :

$a \backslash b$	0	1
0	0	1
1	0	0

$$y = \bar{a} \cdot b$$

* Result : Truth table of half subtraction is verified.

Ques. (a) $\begin{array}{l} 1 \\ 0 \\ - \\ 1 \\ \hline \end{array}$

~~Ans. (b) $\begin{array}{l} 1 \\ 0 \\ - \\ 1 \\ \hline \end{array}$~~

EXPERIMENT 07

* Aim: Design and implementation of Half-Adder

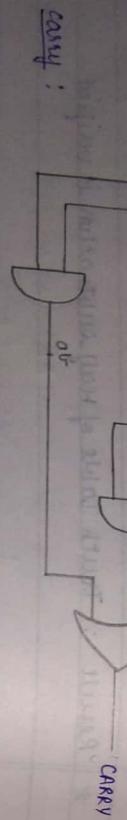
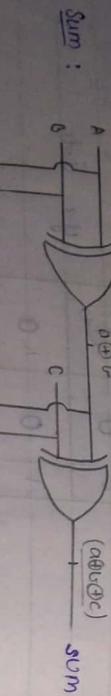
* Apparatus required : adder kit / digital IC trainer , Probe

* theory: ADDER

Adder is a combinational circuit which is used to perform addition operation

Classification: It is classified in 2 types :

- Half Adder
- Full Adder



b) FULL ADDER: A full adder is a logical circuit that performs an addition operation on three one-bit binary numbers. The full adder produces a sum of the three inputs and carry value.

TRUTH TABLE

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	1
1	1	1	0	1

Teacher's Signature _____

K-MAP :

(a) sum :	a $\bar{b}c$	00	01	11	10
	0		1		1
	-		1		1
	-		1		1

$$y = a\bar{b}\bar{c} + \bar{a}\bar{b}\bar{c} + ab\bar{c} + \bar{a}bc$$

$$= a \oplus b \oplus c$$

(b) carry :

a $\bar{b}c$	00	01	11	10
0			1	
-		1	1	1
-	1	1	1	1

$$y = ac + bc + abc$$

Truth table of Full Adder is verified. : RESULT

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EXPERIMENT - 08

* Aim: Design and implementation of Full-subtractor

* Apparatus Required: Digital IC Trainer Kit / Probes

* Theory: SUBTRACTOR

Subtractor is a combinational circuit which is used to perform subtraction operation classification : It is classified in 2 types:

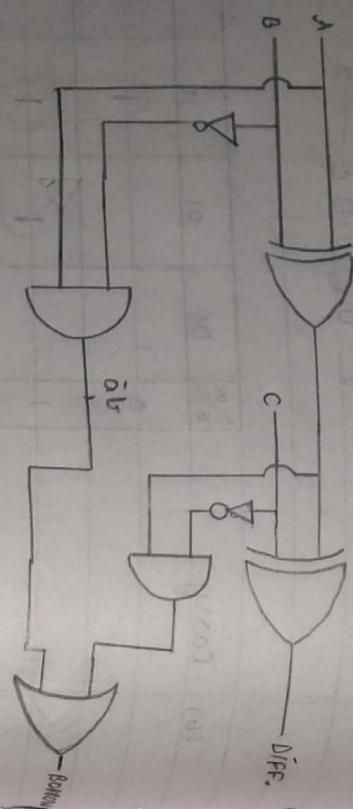
- Half subtractor
- Full subtractor

b) FULL SUBTRACTOR: It is a combinational circuit used to

perform subtraction operation on 3 one-bit binary inputs. It generates 2 kinds of output - the difference and the borrow out.

TRUTH TABLE :

A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



K-MAP :

	$a\bar{b}c$	00	01	11	10
	0		1		1
	1	1		1	

$$Y = \bar{a}\bar{b}c + \bar{a}b\bar{c} + ab\bar{c} + \bar{a}bc$$

	$a\bar{b}c$	00	01	11	10
	0		1		1
	1		1		

$$Y = \bar{a}c + bc + \bar{a}b$$

* Result : Truth table of full subtractor is verified.

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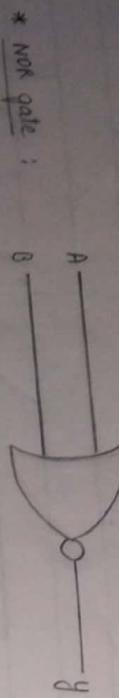
EXPERIMENT - 09

* Aim : Verifying if NOR gate is a universal gate .

* Apparatus Required : Digital IC trainer kit , probes .

Theory :

~~UNIVERSAL GATES~~ : An universal gate is a gate which can implement any Boolean function without need to use any other gate type .



$$* \text{ NOR gate : } \\ Y = \overline{A+B}$$

~~NOR GATE~~ : It is a logical gate that implements logical NOR - it behaves according to the truth table to the right . A high output results if both the inputs to the gate are low ; if one or both inputs are high , a low output results .

$$\text{EXPRESSION : } Y = \overline{A+B}$$

TRUTH TABLE

A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

* NOT gate :



$$Y = \bar{A}$$

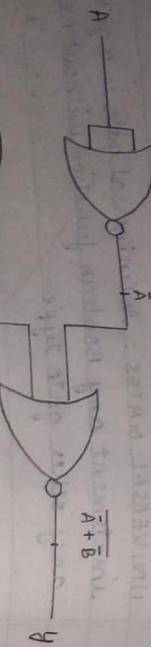
a) NOT Gate : It implements logical negation

$$\text{EXPRESSION : } Y = \bar{A}$$

TRUTH TABLE :

A	$y = \bar{A}$
0	1
1	0

* AND gate :



implies

$y = \bar{A} + \bar{B}$

implies $y = \bar{A} \cdot \bar{B}$

c) OR gate : It implements logical conjunction.

EXPRESSION : $y = A + B$

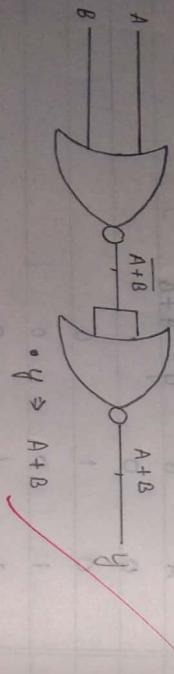
TRUTH TABLE :

A	B	$y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

* OR gate :

$$A + B = y$$

EQUIVALENT



EXPRESSION : $y = A \cdot B$

TRUTH TABLE :

A	B	$y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

* XOR gate :

$$y = A + B$$

implies

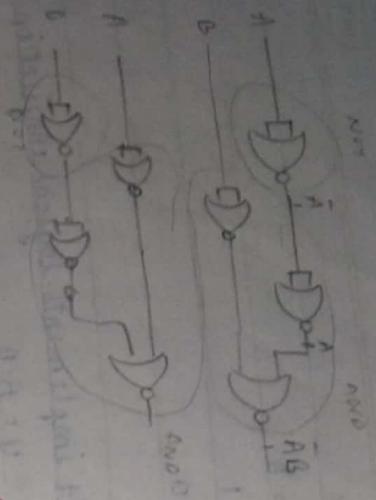
$y = A + B - A \cdot B$

d) XOR gate : It implements an exclusive OR

EXPRESSION : $y = A \oplus B = \bar{A}B + A\bar{B}$

TRUTH TABLE :

Teacher's Signature _____



~~It is indeed an universal gate.~~

e) XNOR gate: It implements logical equality.

$$\text{EXPRESSION : } Y = A \odot B = \bar{A} \bar{B} + AB$$

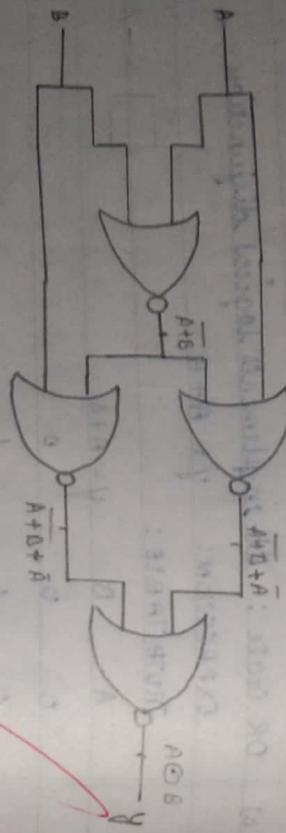
TRUTH TABLE:

A	B	$Y = A \odot B = \bar{A} \bar{B} + AB$
0	0	1
0	1	0
1	0	0
1	1	1

* XOR gate :

$$\text{A universal logical function: } \bar{A} \bar{B} + A \bar{B} + A \bar{B} + \bar{A} B$$

* RESULT: NOR gate is indeed an universal gate and can be used to represent any gate.



$$Y_2: A \odot B = \bar{A} \bar{B} + AB$$

~~It is indeed an universal gate.~~

1. Jadiya & Bhagat, 11 : Date 20/02/2022
2. Jadiya & Bhagat, 11 : Date 20/02/2022

30/10/18

EXPERIMENT - 10

PAGE NO.:	/ /
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* Aim : Designing and implementation of Multiplexer

* Apparatus required : Multiplexer Kit, Probe.

* Theory :

MUX

The multiplexer, shortened to "MUX" or "MPX", is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal.

Multiplexers operate like very fast acting multiple position rotary switches connecting or controlling multiple input lines called 'channels' one at a time to the output.

2:1 Mux :

- a) Inputs : $2^n = 2 \times 1 = 2$

- b) Output : 1

- c) Selection line : 1

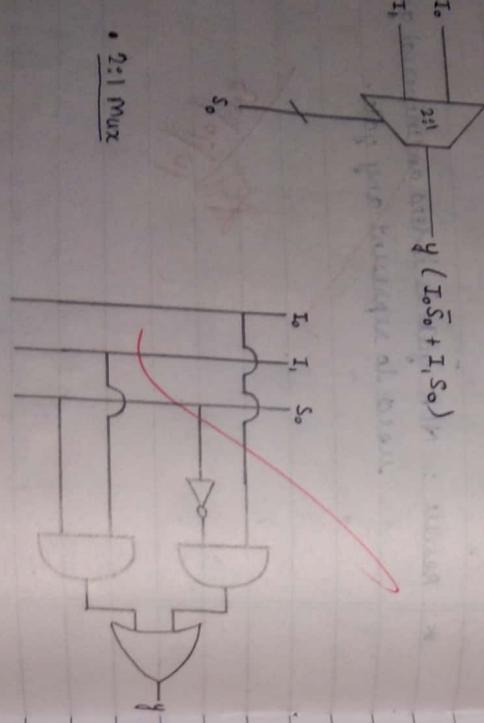
- d) Truth Table :

S_0	Output (y)
0	I_0
1	I_1

$= I_0 S_0 + I_1 \bar{S}_0$

- e) expression : $y = I_0 S_0 + I_1 \bar{S}_0$

Teacher's Signature _____



• 2:1 Mux

• 4:1 MUX :

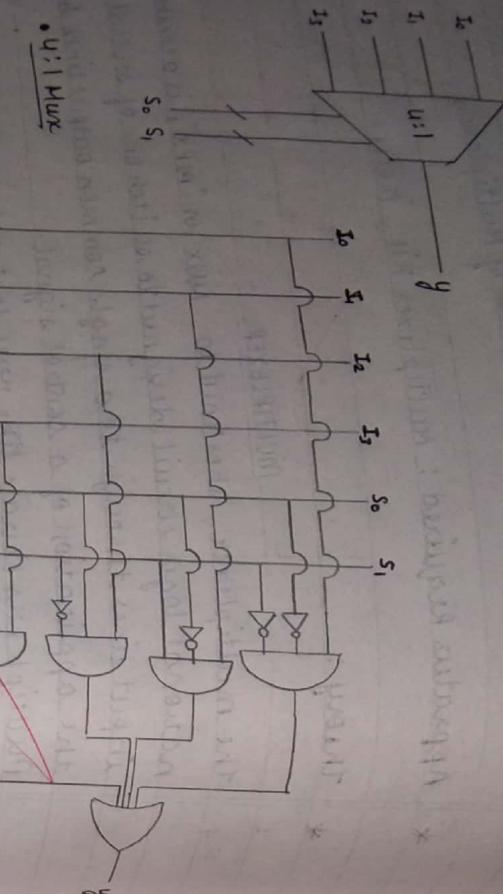
- a) Inputs : $2^n = 2 \times 2 = 4$
 b) Outputs : 1
 c) Selection lines : 2

- d) Truth Table :

S_0	S_1	Output (y)
0	0	$I_0 = I_0 \bar{S}_0 \bar{S}_1$
0	1	$I_1 = I_1 \bar{S}_0 S_1$
1	0	$I_2 = I_2 S_0 \bar{S}_1$
1	1	$I_3 = I_3 S_0 S_1$

- e) Expression :

$$I_0 \bar{S}_0 \bar{S}_1 + I_1 \bar{S}_0 S_1 + I_2 S_0 \bar{S}_1 + I_3 S_0 S_1$$



- 4:1 MUX

• 4:1 MUX
 4 inputs : binary address
 * 2 selection lines
 * 1 output
 * 4 outputs

- 4:1 MUX

• 4:1 MUX
 4 inputs : binary address
 * 2 selection lines
 * 1 output
 * 4 outputs

- 4:1 MUX

• 4:1 MUX
 4 inputs : binary address
 * 2 selection lines
 * 1 output
 * 4 outputs

- 4:1 MUX

• 4:1 MUX
 4 inputs : binary address
 * 2 selection lines
 * 1 output
 * 4 outputs

- 4:1 MUX

• 4:1 MUX
 4 inputs : binary address
 * 2 selection lines
 * 1 output
 * 4 outputs

- 4:1 MUX

• 4:1 MUX
 4 inputs : binary address
 * 2 selection lines
 * 1 output
 * 4 outputs

- 4:1 MUX

• 4:1 MUX
 4 inputs : binary address
 * 2 selection lines
 * 1 output
 * 4 outputs

- 4:1 MUX

• 4:1 MUX
 4 inputs : binary address
 * 2 selection lines
 * 1 output
 * 4 outputs

- 4:1 MUX

• 4:1 MUX
 4 inputs : binary address
 * 2 selection lines
 * 1 output
 * 4 outputs

- 4:1 MUX

• 4:1 MUX
 4 inputs : binary address
 * 2 selection lines
 * 1 output
 * 4 outputs

- 4:1 MUX

• 4:1 MUX
 4 inputs : binary address
 * 2 selection lines
 * 1 output
 * 4 outputs

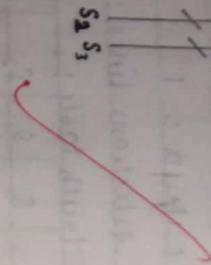
c) Expression : $I_0 \bar{S}_0 \bar{S}_1 \bar{S}_2 + I_1 \bar{S}_0 \bar{S}_1 S_2 + I_2 \bar{S}_0 S_1 \bar{S}_2 + I_3 S_0 \bar{S}_1 \bar{S}_2 + I_4 S_0 \bar{S}_1 S_2 + I_5 S_0 S_1 \bar{S}_2 + I_6 S_0 S_1 S_2$

16:1 Mux :

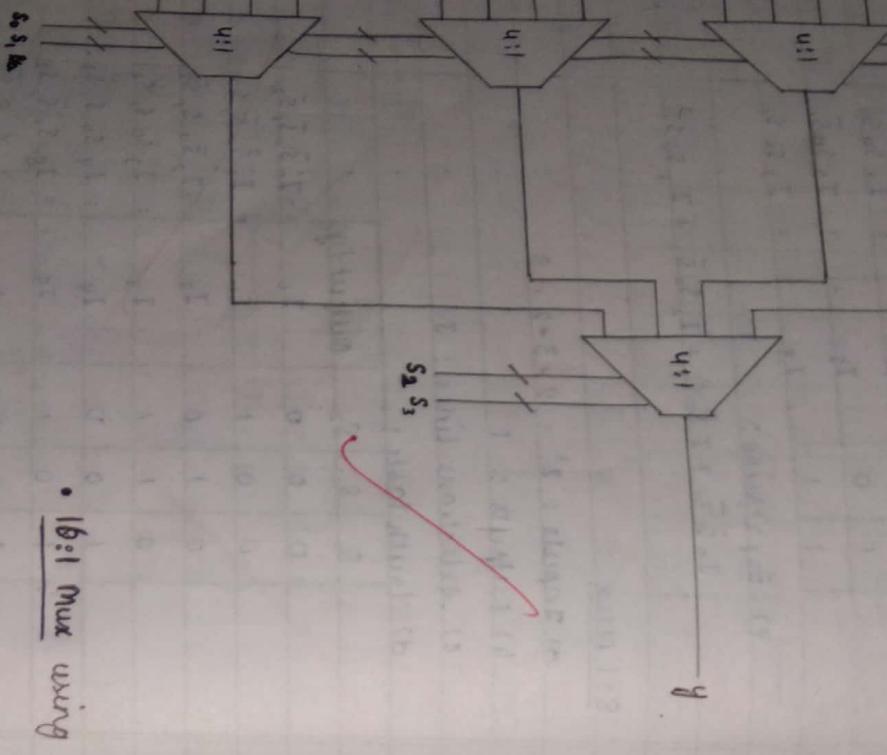
- a) Inputs : $2^4 = 2 \times 2 \times 2 \times 2 = 16$
- b) Outputs : 1
- c) Selection lines : 4

d) Truth Table :

	S_0	S_1	S_2	S_3	Output(y)
	0	0	0	0	I_0
	0	0	0	1	I_1
	0	0	1	0	I_2
	0	0	1	1	I_3
	0	1	0	0	I_4
	0	1	0	1	I_5
	0	1	1	0	I_6
	0	1	1	1	I_7
	1	0	0	0	I_8
	1	0	0	1	I_9
	1	0	1	1	I_{10}
	1	1	0	0	I_{11}
	1	1	0	1	I_{12}
	1	1	1	1	I_{13}
	1	1	1	0	I_{14}
	1	1	1	1	I_{15}



- 16:1 Mux using 4:1 Mux



Ans

* Result : truth table of multiplexer is verified.

Teacher's Signature

* AIM : Designing and implementation of De-Multiplexer.

* APPARATUS REQUIRED : Demultiplexer Kit, Passes.

* THEORY :

DE - MULTIPLEXER

The demultiplexer is also known as "De-MUX" or "De-MUX", is a combinational logic circuit designed to switch one input line through to several output lines by the application of a control signal.

* 1:2 ^{DE} MUX :

- a) Input = 1
- b) Output = $2^n = 2^1 = 2$
- c) Selection line = 1
- d) Truth table :

S_0	Y_0	Y_1
0	I_0	0
1	0	I_0

$$= I_0 \bar{S}_0$$

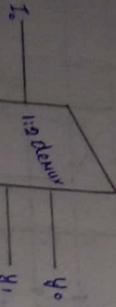
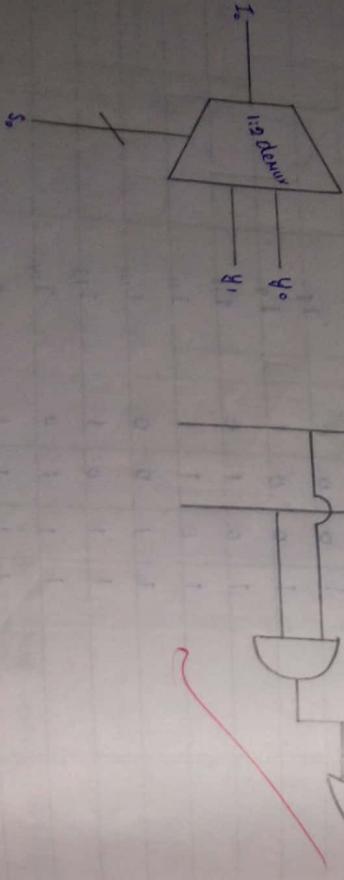
$$= I_0 S_0$$

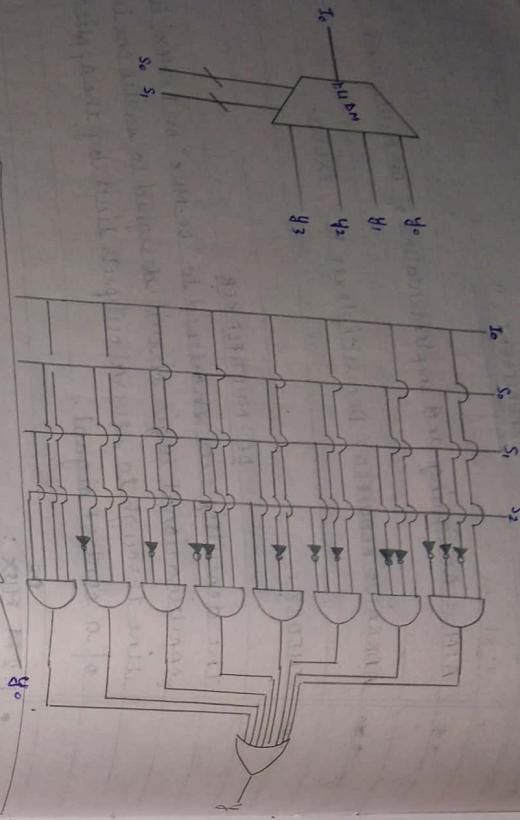
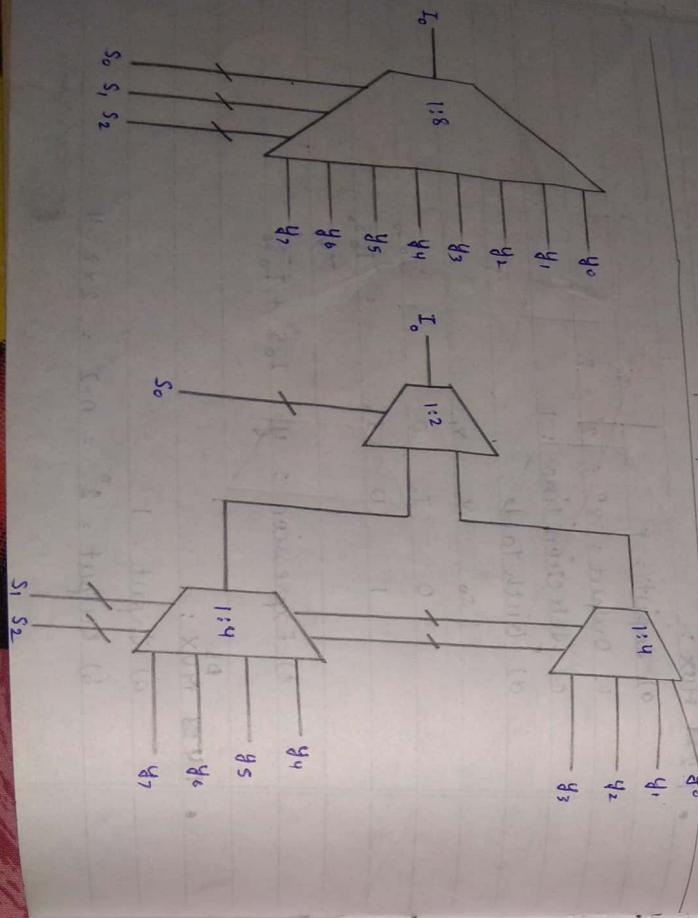
e) Expression : $Y = I_0 \bar{S}_0 + I_0 S_0$

* 1:4 ^{DE} MUX :

- a) Input = 1
- b) Output = $2^n = n = 2^2 = 4$

Teacher's Signature





c) Selection line = 2

d) truth table :

$S_0 \quad S_1 \quad Y_0 \quad Y_1 \quad Y_2 \quad Y_3 \quad Y_4 \quad Y_5 \quad Y_6 \quad Y_7$
0 0 $I_0 \quad 0 \quad 0 \quad 0 \quad = Y_0 = I_0 S_0 S_1$
0 1 $I_0 \quad 0 \quad 0 \quad = Y_1 = I_0 \bar{S}_0 S_1$
1 0 $0 \quad I_0 \quad 0 \quad = Y_2 = I_0 S_0 \bar{S}_1$
1 1 $0 \quad 0 \quad 0 \quad = Y_3 = I_0 S_0 S_1$

• 1:8 MUX :

a) Input = 1

b) Output = $2^3 = 8$

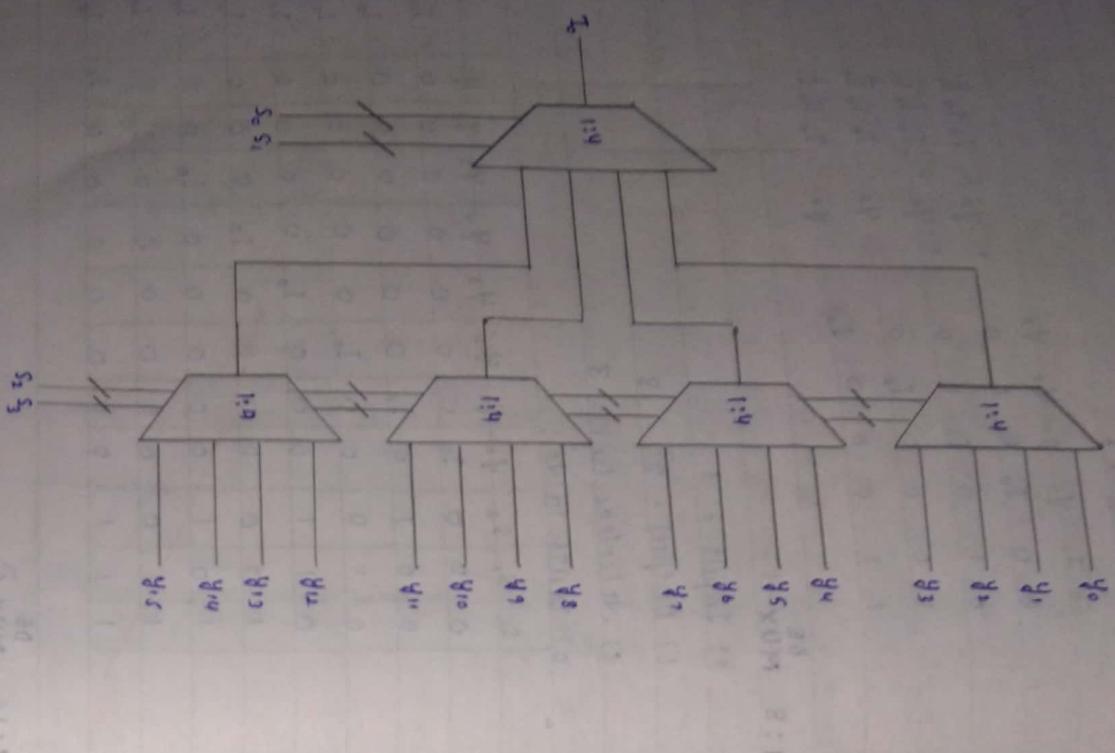
c) Selection line = 3

d) truth table :

$S_0 \quad S_1 \quad S_2 \quad Y_0 \quad Y_1 \quad Y_2 \quad Y_3 \quad Y_4 \quad Y_5 \quad Y_6 \quad Y_7$
0 0 0 $I_0 \quad 0 \quad = I_0 \bar{S}_0 \bar{S}_1 \bar{S}_2$
0 0 1 $I_0 \quad 0 \quad = I_0 \bar{S}_0 \bar{S}_1 S_2$
0 1 0 $I_0 \quad 0 \quad = I_0 \bar{S}_0 S_1 \bar{S}_2$
0 1 1 $I_0 \quad 0 \quad = I_0 \bar{S}_0 S_1 S_2$
1 0 0 $0 \quad I_0 \quad 0 \quad = I_0 S_0 \bar{S}_1 \bar{S}_2$
1 0 1 $0 \quad I_0 \quad 0 \quad = I_0 S_0 \bar{S}_1 S_2$
1 1 0 $0 \quad 0 \quad I_0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad = I_0 S_0 S_1 \bar{S}_2$
1 1 1 $0 \quad 0 \quad I_0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad = I_0 S_0 S_1 S_2$

- 1:16 MUX :
- 1:16 MUX :
- 1:16 MUX :
- 1:16 MUX :

Teacher's Signature _____



* RESULT : truth table of De-multiplexer is verified.

S_0	S_1	S_2	S_3	y_0	y_1	y_2	y_3	y_4	y_5	y_6	y_7	y_8	y_9	y_{10}	y_{11}	y_{12}	y_{13}	y_{14}	y_{15}
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

c) Selection line : 4

d) Truth table :