Bangladesh University of Engineering and Technology

Department of Computer Science and Engineering

CSE 404 July 2017 Semester

Digital System Design Sessional

Very Simple Computer Design and Simulation

Instruction Set Assignment

Group No.	Instruction Set
A1 G1	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADD [address]; SUB immediate; CMP B; XCHG; JNC address; JNE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; ROL; ROR; OR [address]; XOR B;
A1 G2	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADC immediate; SBB [address]; CMP B; DEC; JZ address; JG address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; RCL; RCR; AND immediate; OR B;
A1 G3	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADC immediate; SBB [address]; CMP B; NEG; JNZ address; JL address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; XCHG; CMC; AND B; OR [address]
A1 G4	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADD [address]; SUB immediate; CMP B; NEG; JO address; JE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; SHL; SHR; OR B; XOR immediate;
A1 G5	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADD immediate; SUB immediate; CMP B; DEC; JNO address; JNE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; ROL; ROR; AND [address]; XOR B;
A1 G6	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADC [address]; SBB [address]; CMP B; DEC; JNO address; JG address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; RCL; RCR; AND B; XOR B;
A2 G1	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADC immediate; SBB [address]; CMP B; DEC; JZ address; JG address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; RCL; RCR; AND immediate; OR B;
A2 G2	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADC [address]; SBB immediate; CMP B; NEG; JC address; JE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; XCHG; NOT; AND B; XOR immediate;
A2 G3	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADC immediate; SBB immediate; CMP B; TEST B; JNZ address; JL address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; STS; CLS; AND [address]; OR B;

A2 G4	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADD immediate; SUB [address]; CMP B; XCHG; JO address; JE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; SHL; SHR; OR B; XOR [address];
A2 G5	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADD [address]; SUB [address]; CMP B; INC; JZ address; JL address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; RCL; RCR; AND B; XOR immediate;
A2 G6	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADD immediate; SUB immediate; CMP B; NEG; JNC address; JNE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; STZ; CLZ; AND [address]; OR [address];
B1 G1	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADD immediate; SUB [address]; CMP B; TEST B; JC address; JE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; SHL; SHR; AND B; XOR immediate;
B1 G2	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADC [address]; SBB [address]; CMP B; NOT; JC address; JNE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; RCL; RCR; AND B; XOR B;
B1 G3	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADC immediate; SBB immediate; CMP B; XCHG; JC address; JE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; STZ; CLZ; AND immediate; OR [address];
B1 G4	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADD immediate; SUB [address]; CMP B; TEST B; JC address; JE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; SHL; SHR; AND B; XOR immediate;
B1 G5	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADD immediate; SUB immediate; CMP B; DEC; JNO address; JNE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; ROL; ROR; AND [address]; XOR B;
B1 G6	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADC [address]; SBB [address]; CMP B; NEG; JZ address; JL address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; STS; CLS; OR B; XOR B;
B2 G1	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADD immediate; SUB immediate; CMP B; NEG; JO address; JNE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; XCHG; CMC; OR [address]; XOR B;
B2 G2	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADC [address]; SBB [address]; CMP B; DEC; JNO address; JG address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; RCL; RCR; AND B; XOR B;
B2 G3	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADC [address]; SBB [address]; CMP B; INC; JNZ address; JL address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; SHL; SHR; AND immediate; XOR immediate;
B2 G4	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN;

	OUT; ADD B; ADC B; SUB B; SBB B; ADD immediate; SUB immediate; CMP B; NEG; JNC address; JNE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; STZ; CLZ; AND [address]; OR [address];
B2 G5	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADC [address]; SBB immediate; CMP B; NOT; JZ address; JL address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; STC; CLC; OR immediate; XOR [address];
B2 G6	LDA address; STA address; MOV Acc, B; MOV B, Acc; MOV Acc, immediate; IN; OUT; ADD B; ADC B; SUB B; SBB B; ADD immediate; SUB immediate; CMP B; NEG; JO address; JNE address; PUSH; POP; CALL address; RET; JMP; HLT; NOP; XCHG; CMC; OR [address]; XOR B;

Semantics of Instructions

Instruction	Description
LDA address	Acc ← Memory [address]
STA address	Memory [address] ← Acc
MOV Acc, B	Acc ← B
MOV B, Acc	B ← Acc
MOV Acc, immediate	Acc ← immediate
IN	Acc ← input_port
OUT	Output_port ← Acc
ADD B	Acc ← Acc + B
ADC B	Acc ← Acc + B + C (Contents of Carry Flag)
SUB B	Acc ← Acc – B
SBB B	Acc ← Acc – B – Bo (Contents of Carry Flag)
ADD [address]	Acc ← Acc + Memory [address]
ADC [address]	Acc ← Acc + Memory [address] + C (Contents of Carry Flag)
SUB [address]	Acc ← Acc – Memory [address]
SBB [address]	Acc ← Acc – Memory [address] – Bo (Contents of Carry Flag)
ADD immediate	Acc ← Acc + immediate
ADC immediate	Acc ← Acc + immediate + C (Contents of Carry Flag)
SUB immediate	Acc ← Acc – immediate
SBB immediate	Acc ← Acc – immediate – Bo (Contents of Carry Flag)
PUSH	Pushes the content of Accumulator to the stack
POP	Pops off stack to Accumulator
CALL address	Calls a subroutine (at the specified address) unconditionally
RET	Returns from current subroutine to the caller unconditionally
JMP address	Jumps unconditionally to the address
HLT	Halts execution
AND B	Acc ← Acc . B
OR B	Acc ← Acc | B
XOR B	Acc ← Acc ⊕ B
AND [address]	Acc ← Acc . Memory [address]
OR [address]	Acc ← Acc | Memory [address]
XOR [address]	Acc ← Acc ⊕ Memory [address]
AND immediate	Acc ← Acc . immediate
OR immediate	Acc ← Acc | immediate
XOR immediate	Acc ← Acc ⊕ immediate
NOT	Acc ← !Acc

NEG	Acc ← - Acc
XCHG	Acc ↔ B (Exchanges contents of Accumulator and B)
SHL	Acc ← Acc << 1, C (Carry) ← Acc [MSB], Acc [LSB] ← 0
SHR	Acc ← Acc >> 1, C (Carry) ← Acc [LSB], Acc [MSB] ← 0
ROL	Acc ← Acc << 1, Acc [LSB] ← Acc [MSB], C (Carry) ← Acc [MSB]
ROR	Acc ← Acc >> 1, Acc [MSB] ← Acc [LSB], C (Carry) ← Acc [LSB]
RCL	Acc ← Acc << 1, Acc [LSB] ← C (Carry), C (Carry) ← Acc [MSB]
RCR	Acc ← Acc >> 1, Acc [MSB] ← C (Carry) , C (Carry) ← Acc [LSB]
INC	Acc ← Acc + 1
DEC	Acc ← Acc – 1
CMP B	Accumulator will be unchanged. Set flags according to (Acc – B).
TEST B	Accumulator will be unchanged. Set flags according to (Acc . B)
CMC	Complements the Carry flag
CLC	Clears the carry flag
STC	Sets the carry flag
CLS	Clears the sign flag
STS	Sets the sign flag
CLZ	Clears the zero flag
STZ	Sets the zero flag
JC address	Jumps to the address if carry flag is set
JNC address	Jumps to the address if carry flag is not set
JZ address	Jumps to the address if zero flag is set
JNZ address	Jumps to the address if zero flag is not set
JO address	Jump if overflow
JNO address	Jump if no overflow
JE address	Jump if equal
JNE address	Jump if not equal
JG address	Jump if greater
JL address	Jump if less
NOP	No Operation

Guide Lines

Design: The Control unit should be microprogrammed. Efficiency of design will be judged based on two principles: A) Firstly, the fewer the T-states of instruction cycle, the better the design. B) Secondly, for architecture, the fewer the MSI/LSI chips requirement, the better the design.

- The bus will be of 8-bit address bus and 4-bit data bus.
- There will be two independent unit inside the processor – Fetch Unit and Execution Unit.
- In addition, you should be able to write programs (comprising instructions from the instruction set assigned to you) on a normal PC and then send the appropriate machine codes through communication ports to the microcomputer implemented by you.

Report: Contents of the report are recommended as follows:

- Introduction
- Instruction Set
- Block Diagram
- Complete Circuit diagram in drawing paper
- Timing diagram (At least for 5 instructions including call/ ret)
- Explanation of all blocks, instructions, control signals
- How to write and to execute a program in this machine
- Special Features [if any, Optional]
- ICs used with count
- Discussion

Apart from this specification, you may add relevant information that you think necessary. Your report should be a superset of the specified guidelines. But precision will matter. **Both hardcopy and softcopy (Proteous file) of the report should be submitted**.

Deadlines: Follow Course Outline

Reference:

- ***Albert Malvino, Jerald Brown,*** Digital Computer Electronics