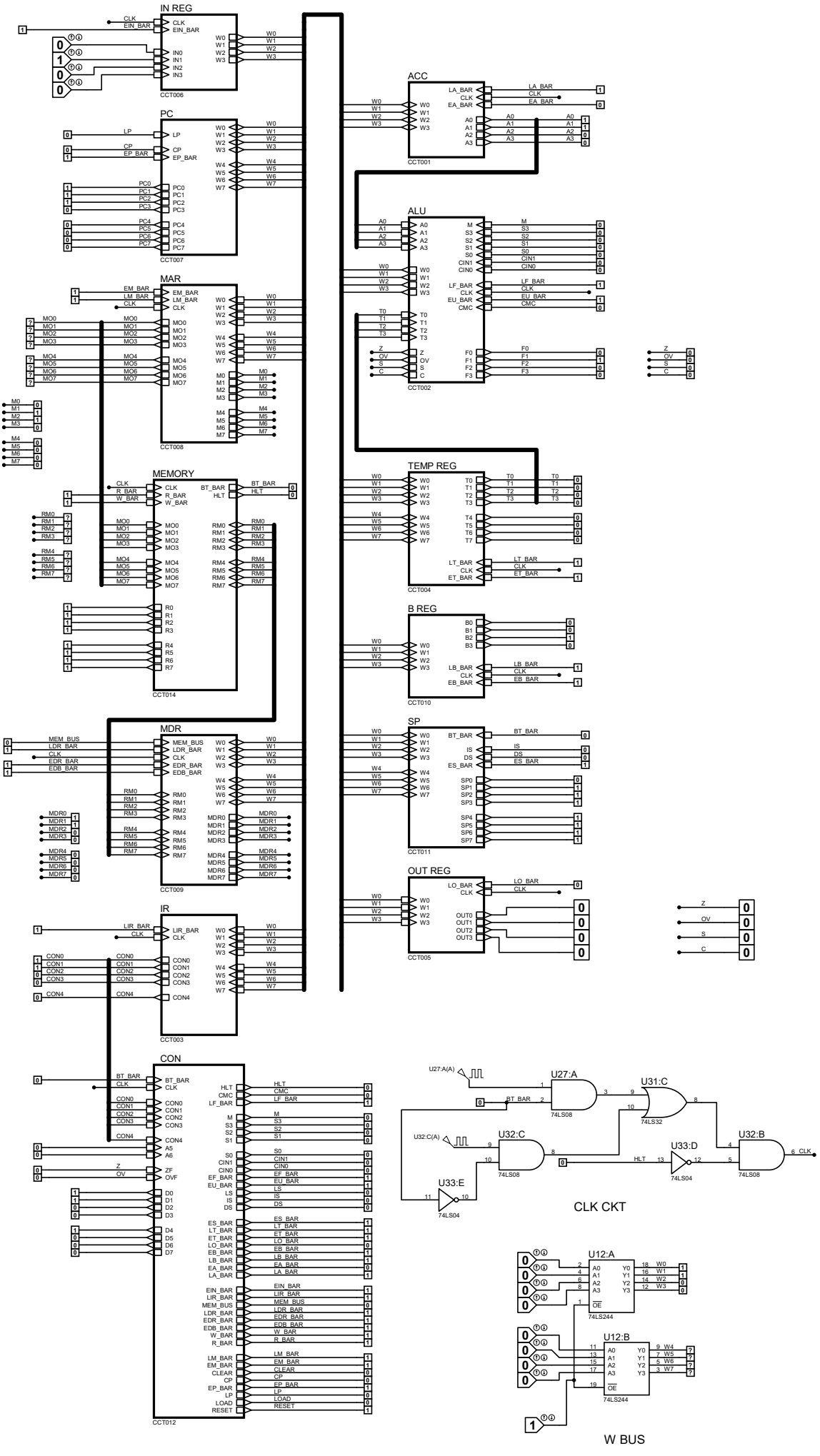
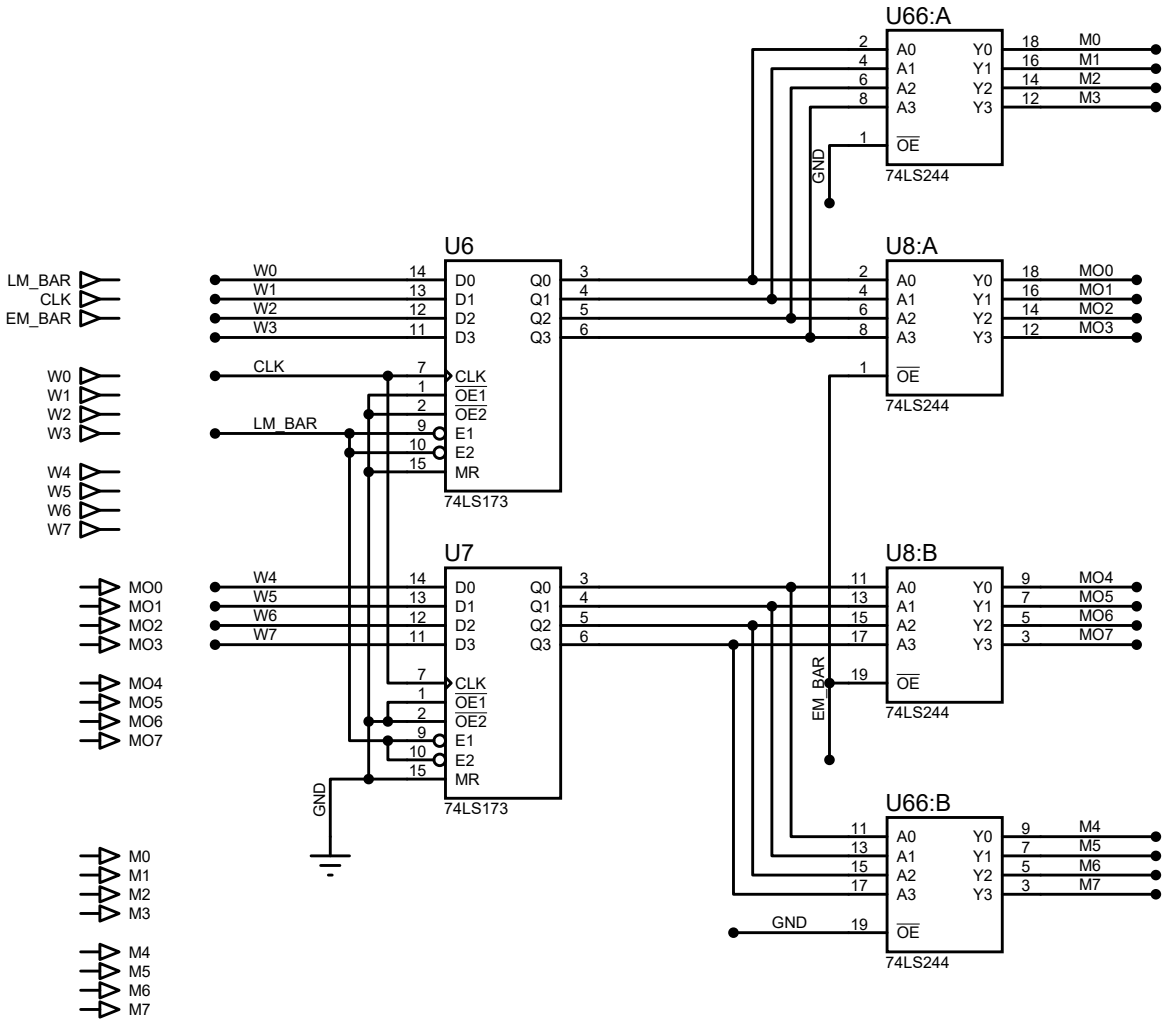
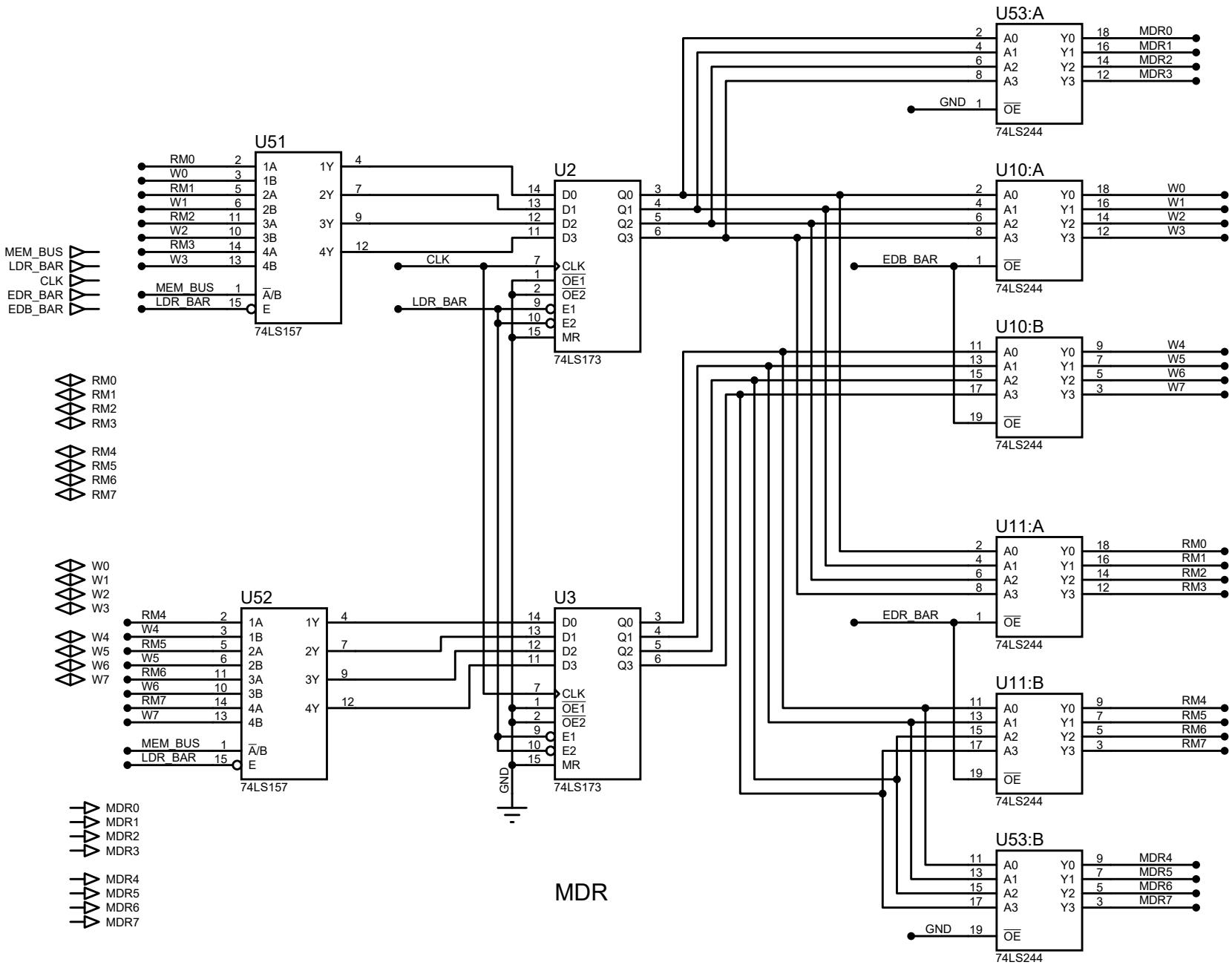
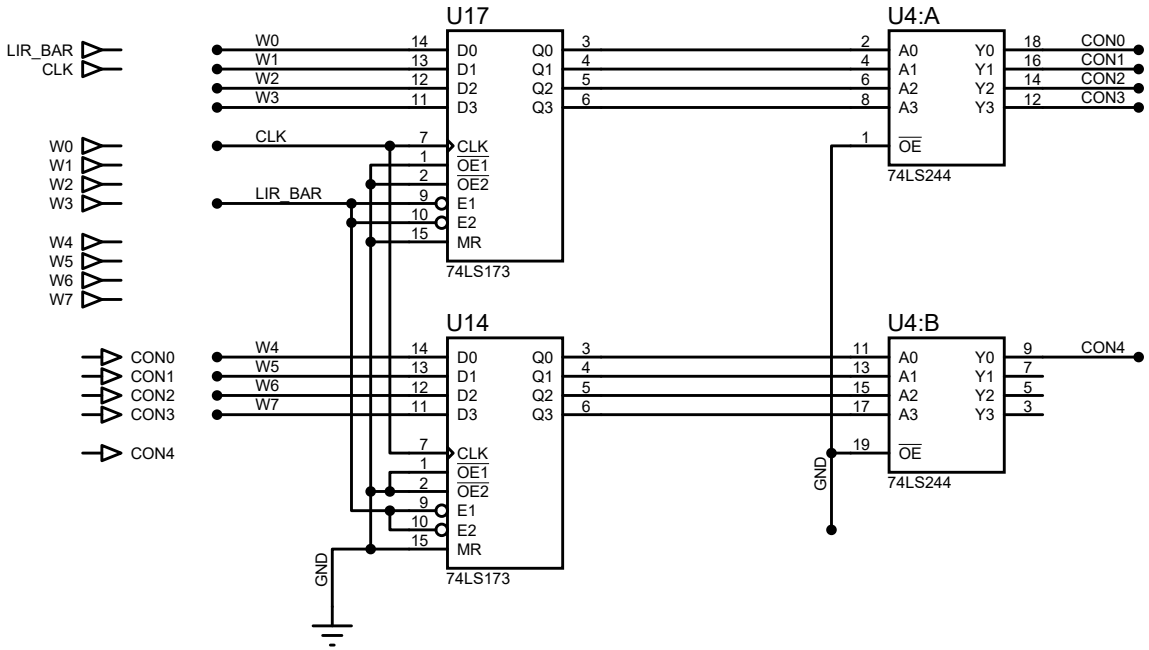

IN REG
CCT006
PC
CCT007
MAR
CCT008
MEMORY
CCT014
MDR
CCT009
IR
CCT003
CON
CCT012
ACC
CCT001
ALU
CCT002
TEMP REG
CCT004
B REG
CCT010
SP
CCT011
OUT REG
CCT005
U27:A
74LS08
U31:C
74LS32
U32:C
74LS08
U33:D
74LS04
U32:B
74LS08
U33:E
74LS04
CLK CKT
U12:A
74LS244
U12:B
74LS244
W BUS

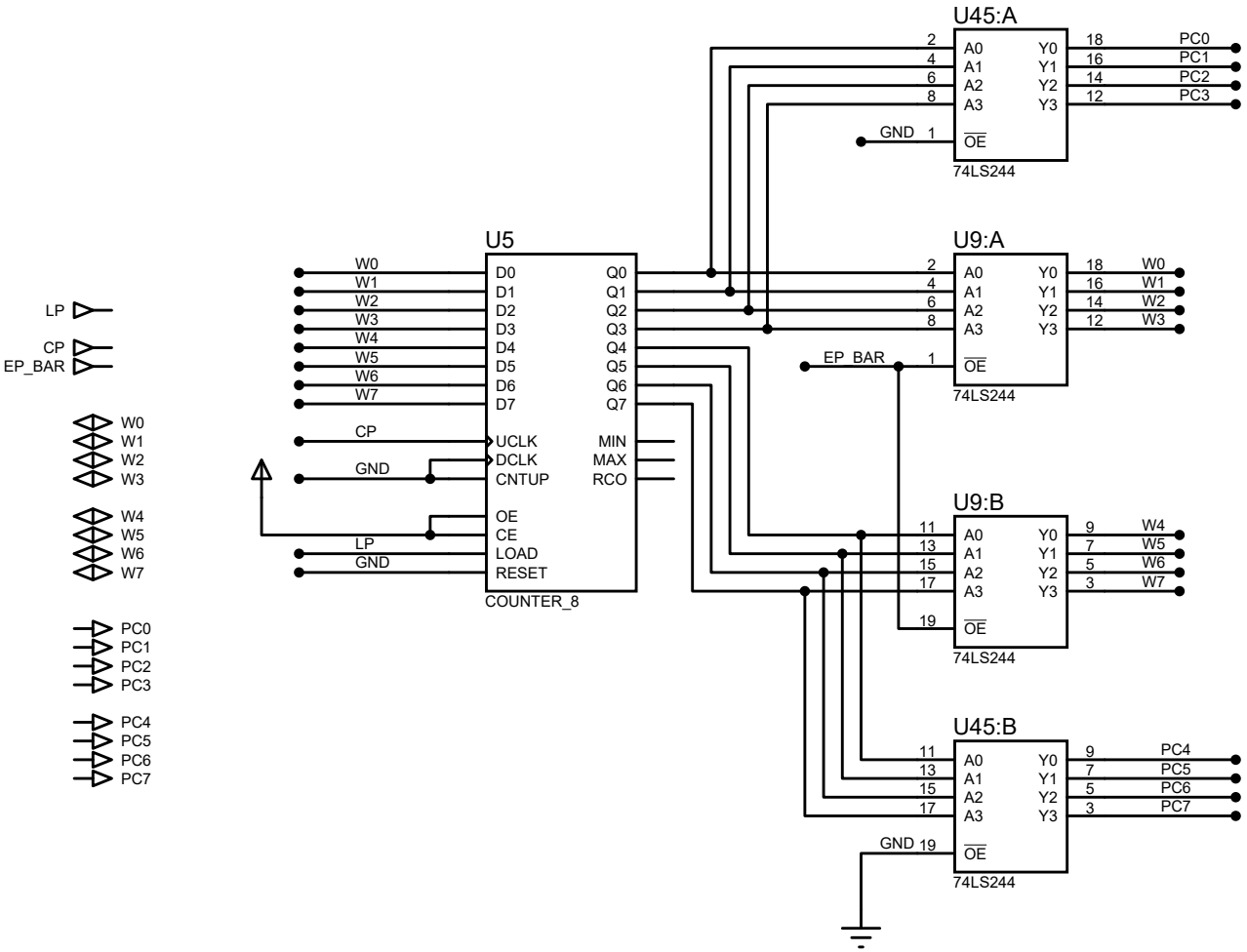

U66:A
U6
U8:A
U7
U8:B
U66:B
LM_BAR
CLK
EM_BAR
W0
W1
W2
W3
W4
W5
W6
W7
MO0
MO1
MO2
MO3
MO4
MO5
MO6
MO7
M0
M1
M2
M3
M4
M5
M6
M7
GND
74LS173
74LS244
D0
D1
D2
D3
Q0
Q1
Q2
Q3
OE1
OE2
E1
E2
MR
A0
A1
A2
A3
Y0
Y1
Y2
Y3
OE

MAR

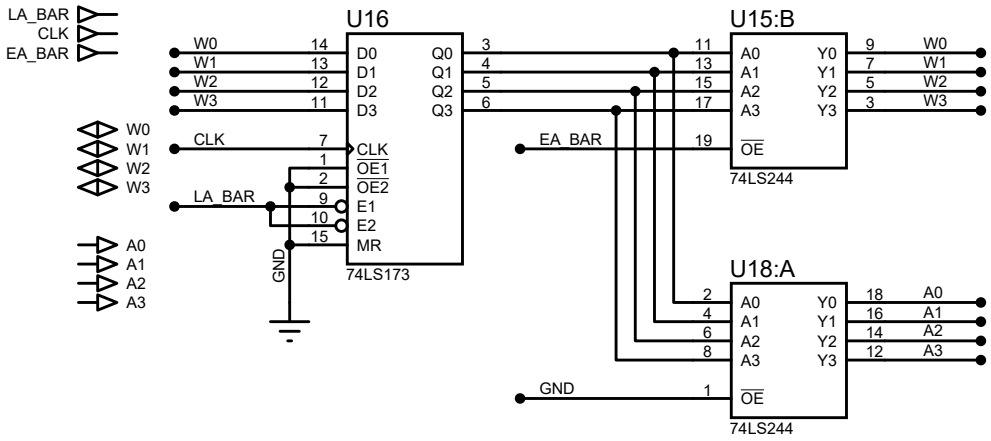

MEM_BUS
LDR_BAR
CLK
EDR_BAR
EDB_BAR
RM0
RM1
RM2
RM3
RM4
RM5
RM6
RM7
W0
W1
W2
W3
W4
W5
W6
W7
MDR0
MDR1
MDR2
MDR3
MDR4
MDR5
MDR6
MDR7
U51
74LS157
U52
74LS157
U2
74LS173
U3
74LS173
GND
U53:A
U10:A
U10:B
U11:A
U11:B
U53:B
74LS244
MDR


U17
U4:A
U14
U4:B
LIR_BAR
CLK
W0
W1
W2
W3
W4
W5
W6
W7
CON0
CON1
CON2
CON3
CON4
D0
D1
D2
D3
Q0
Q1
Q2
Q3
CLK
OE1
OE2
E1
E2
MR
74LS173
A0
A1
A2
A3
Y0
Y1
Y2
Y3
OE
74LS244
GND

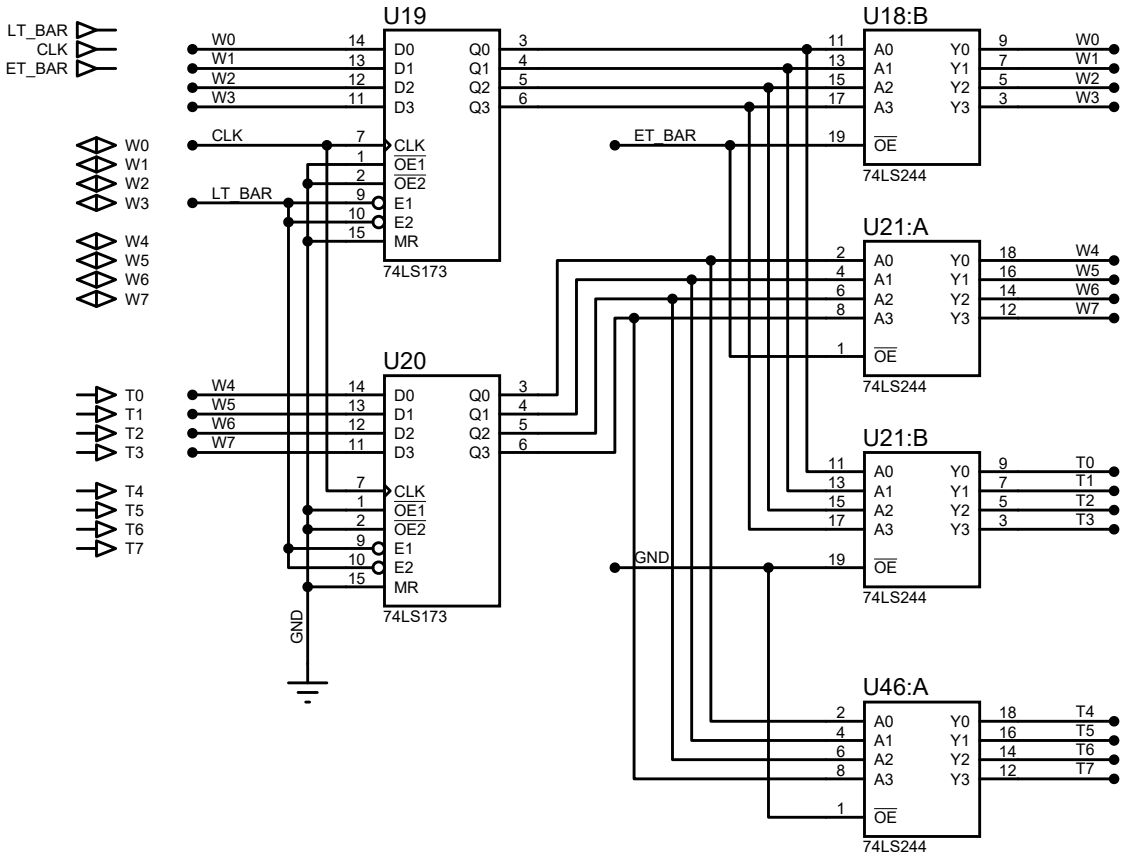
IR


LP
CP
EP_BAR
W0
W1
W2
W3
W4
W5
W6
W7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
U5
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
UCLK
DCLK
CNTUP
MIN
MAX
RCO
OE
CE
LOAD
RESET
COUNTER_8
U45:A
U9:A
U9:B
U45:B
A0
A1
A2
A3
Y0
Y1
Y2
Y3
OE
74LS244
GND
EP_BAR

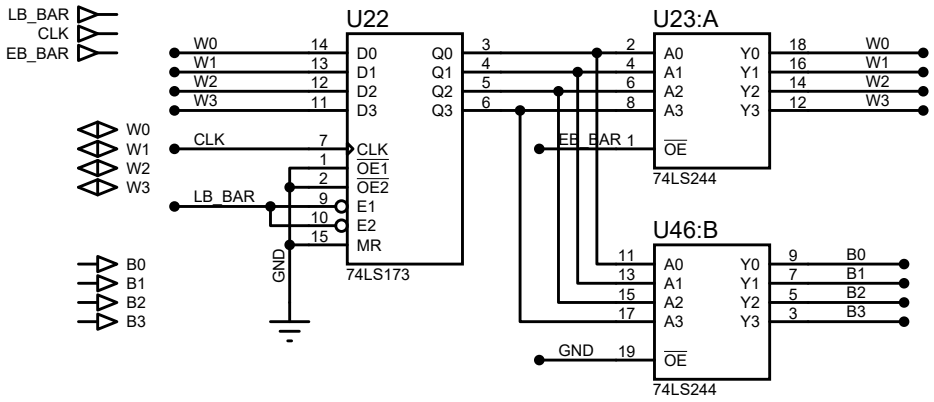
PC


LA_BAR
CLK
EA_BAR
W0
W1
W2
W3
A0
A1
A2
A3
U16
D0
D1
D2
D3
Q0
Q1
Q2
Q3
CLK
OE1
OE2
E1
E2
MR
GND
74LS173
U15:B
A0
A1
A2
A3
Y0
Y1
Y2
Y3
OE
74LS244
U18:A
74LS244
EA_BAR
GND

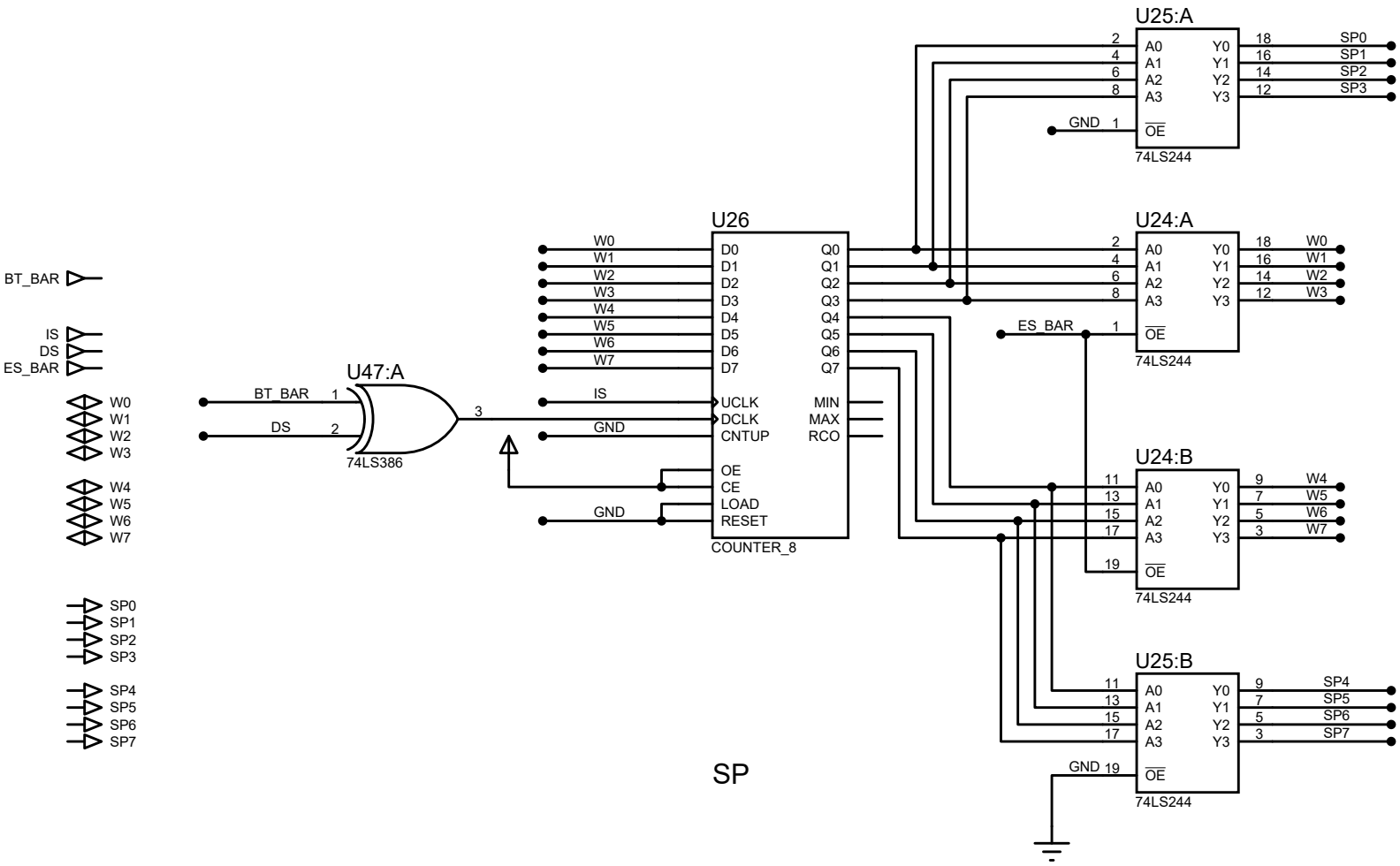
ACC

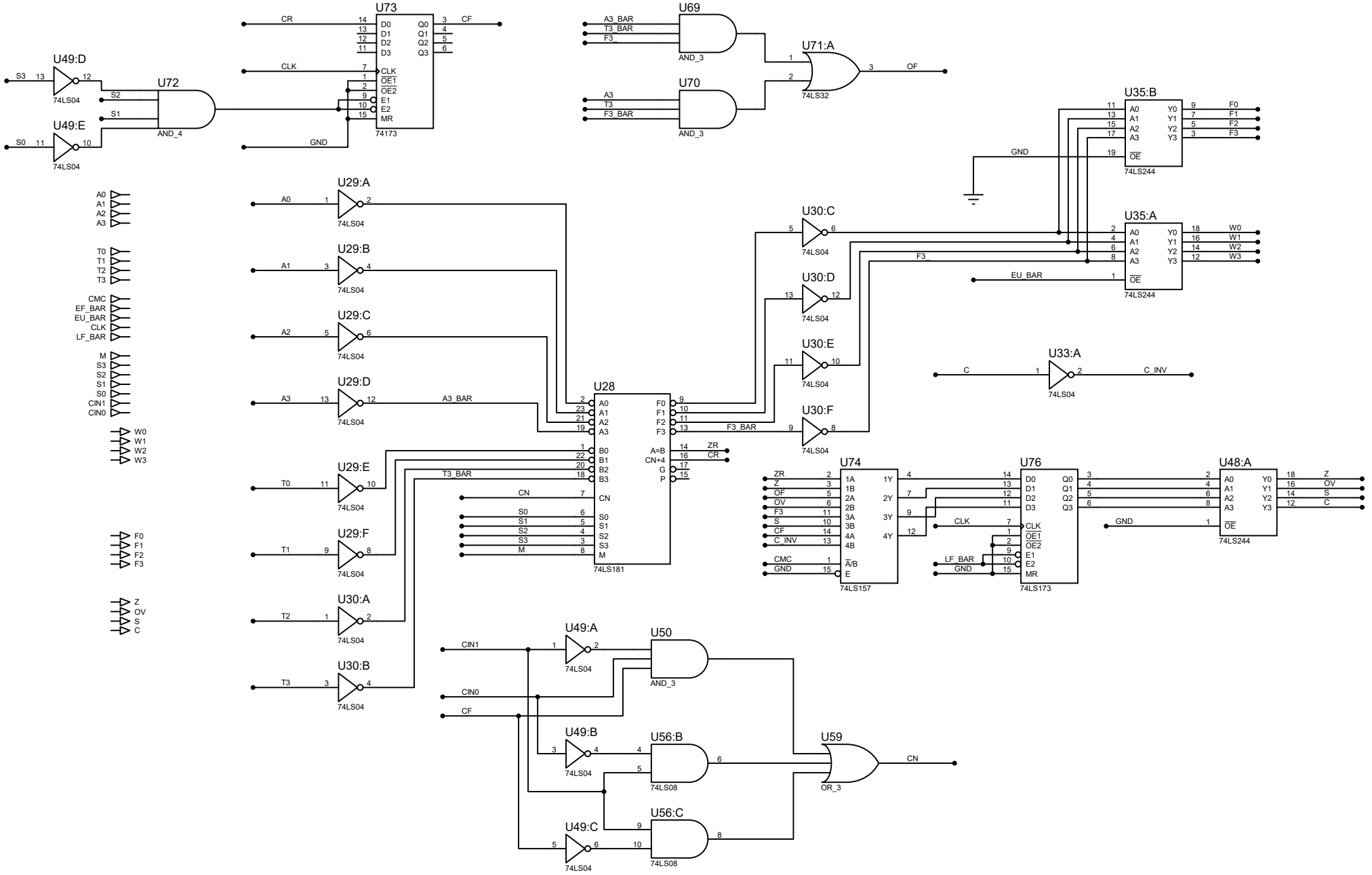

LT_BAR
CLK
ET_BAR
W0
W1
W2
W3
W4
W5
W6
W7
T0
T1
T2
T3
T4
T5
T6
T7
U19
D0
D1
D2
D3
Q0
Q1
Q2
Q3
CLK
OE1
OE2
E1
E2
MR
74LS173
U20
GND
U18:B
A0
A1
A2
A3
Y0
Y1
Y2
Y3
OE
74LS244
U21:A
U21:B
U46:A

TEMP REG

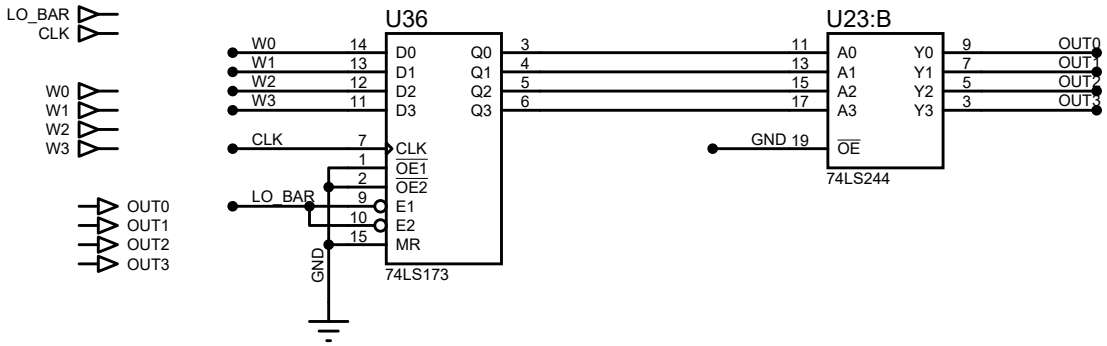

LB_BAR
CLK
EB_BAR
W0
W1
W2
W3
B0
B1
B2
B3
U22
D0
D1
D2
D3
Q0
Q1
Q2
Q3
CLK
OE1
OE2
E1
E2
MR
GND
74LS173
U23:A
A0
A1
A2
A3
Y0
Y1
Y2
Y3
OE
74LS244
U46:B
74LS244
GND

B REG

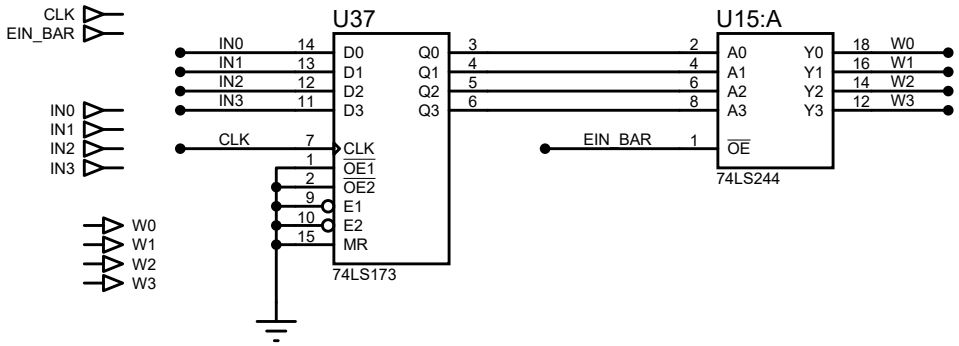

BT_BAR
IS
DS
ES_BAR
W0
W1
W2
W3
W4
W5
W6
W7
SP0
SP1
SP2
SP3
SP4
SP5
SP6
SP7
U47:A
BT_BAR
DS
74LS386
U26
D0
D1
D2
D3
D4
D5
D6
D7
UCLK
DCLK
CNTUP
OE
CE
LOAD
RESET
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
MIN
MAX
RCO
COUNTER_8
U25:A
U24:A
U24:B
U25:B
A0
A1
A2
A3
Y0
Y1
Y2
Y3
OE
74LS244
GND
ES_BAR
SP


U49:D
U49:E
U72
AND_4
74LS04
U73
74173
CR
CLK
GND
CF
U69
U70
U71:A
74LS32
AND_3
A3_BAR
T3_BAR
F3_
A3
T3
F3_BAR
OF
U35:B
U35:A
74LS244
GND
EU_BAR
U29:A
U29:B
U29:C
U29:D
U29:E
U29:F
U30:A
U30:B
U30:C
U30:D
U30:E
U30:F
U28
74LS181
U33:A
C
C_INV
U74
74LS157
U76
74LS173
U48:A
LF_BAR
U49:A
U49:B
U49:C
U50
U56:B
U56:C
74LS08
U59
OR_3
CIN1
CIN0
CF
CN
A0
A1
A2
A3
T0
T1
T2
T3
CMC
EF_BAR
EU_BAR
CLK
LF_BAR
M
S3
S2
S1
S0
CIN1
CIN0
W0
W1
W2
W3
F0
F1
F2
F3
Z
OV
S
C

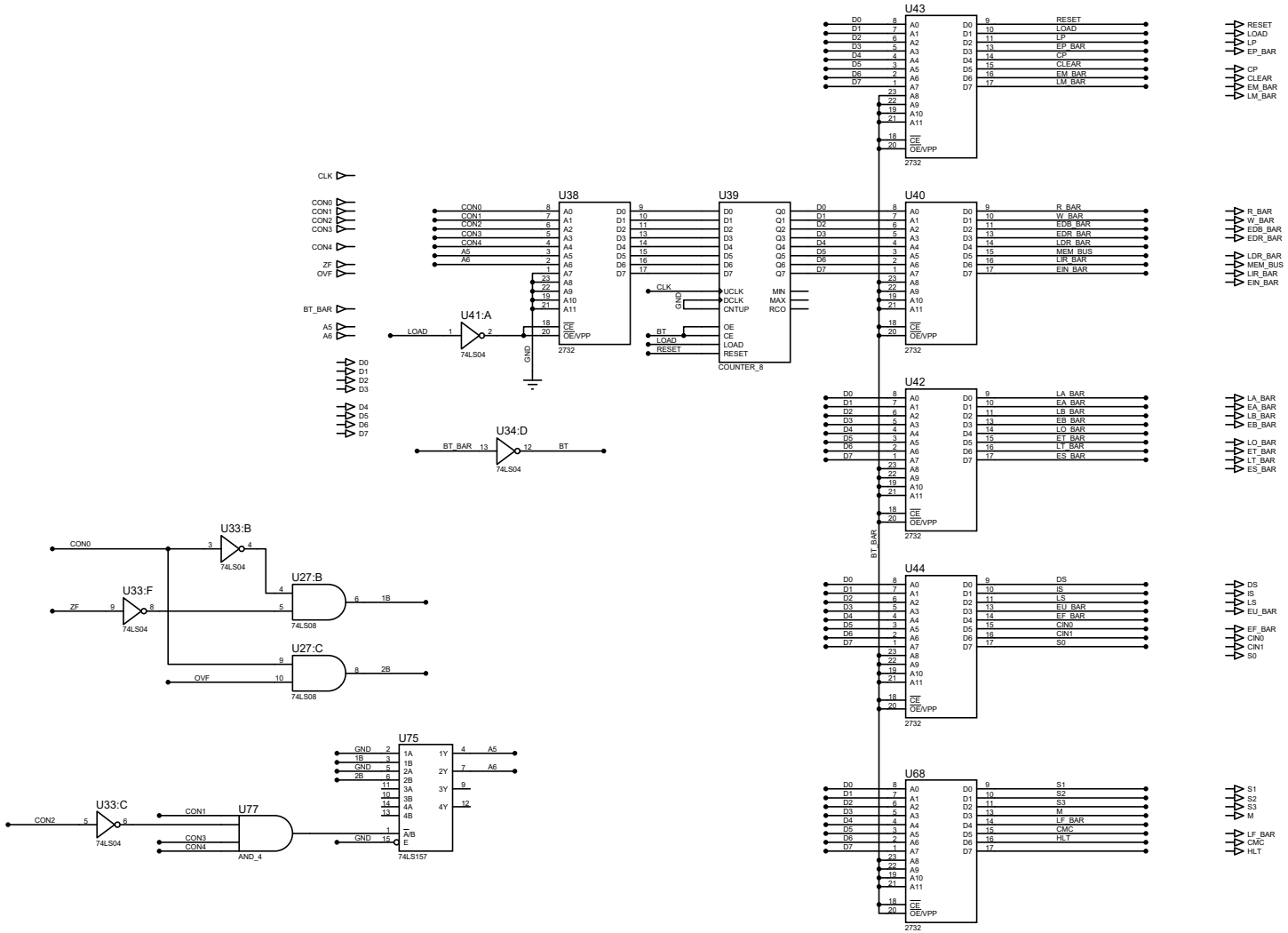
ALU


LO_BAR
CLK
W0
W1
W2
W3
OUT0
OUT1
OUT2
OUT3
U36
D0
D1
D2
D3
CLK
OE1
OE2
E1
E2
MR
Q0
Q1
Q2
Q3
74LS173
GND
U23:B
A0
A1
A2
A3
OE
Y0
Y1
Y2
Y3
74LS244

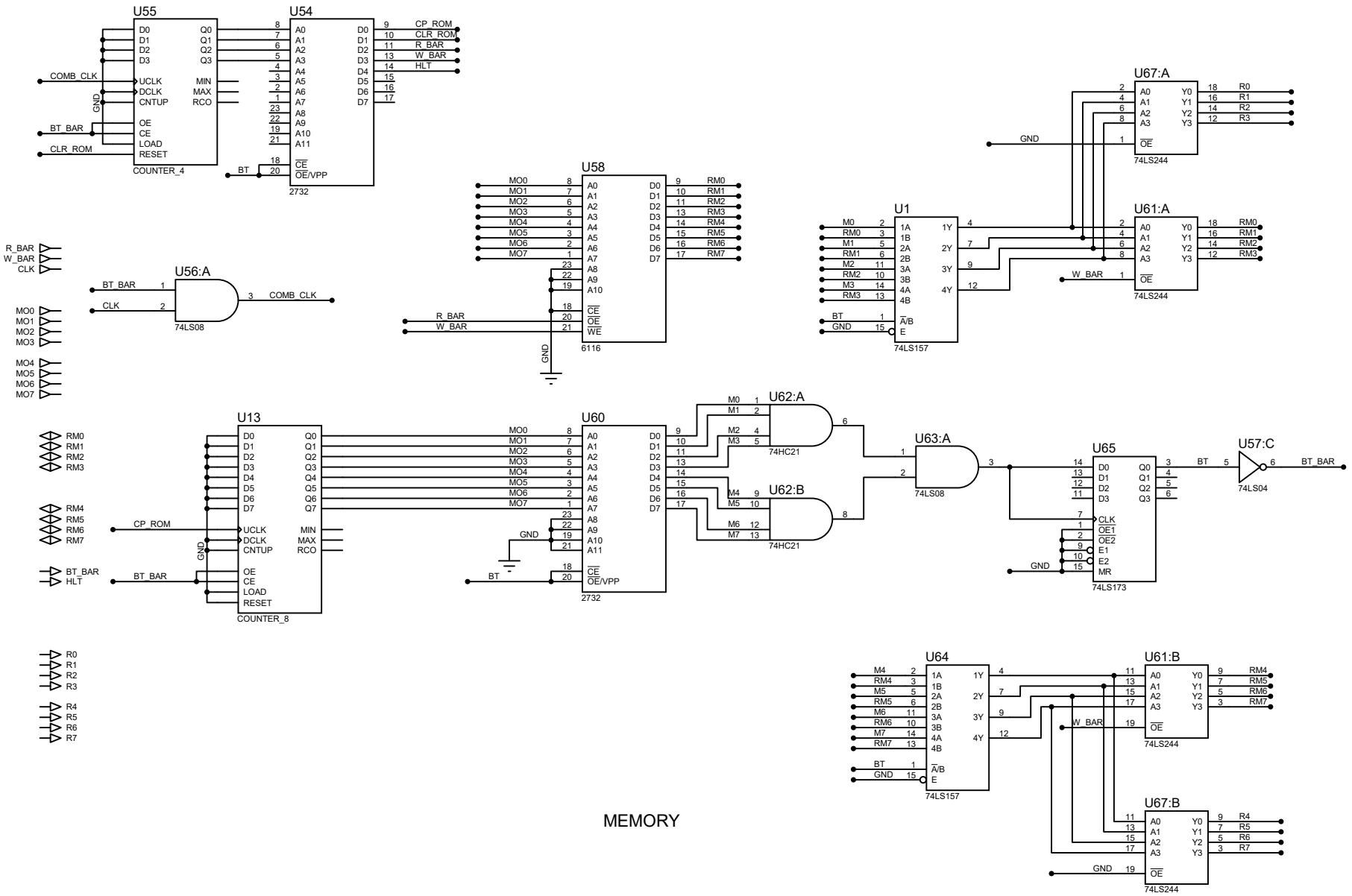
OUT REG


CLK
EIN_BAR
IN0
IN1
IN2
IN3
W0
W1
W2
W3
U37
IN0 14
IN1 13
IN2 12
IN3 11
CLK 7
1
2
9
10
15
D0
D1
D2
D3
CLK
OE1
OE2
E1
E2
MR
Q0 3
Q1 4
Q2 5
Q3 6
74LS173
U15:A
2
4
6
8
1
A0
A1
A2
A3
OE
EIN_BAR
Y0 18
Y1 16
Y2 14
Y3 12
W0
W1
W2
W3
74LS244

IN REG


U43
U38
U39
U40
U41:A
U34:D
U42
U44
U68
U33:B
U27:B
U33:F
U27:C
U33:C
U77
U75
AND_4
74LS04
74LS08
74LS157
2732
COUNTER_8
CLK
CON0
CON1
CON2
CON3
CON4
ZF
OVF
BT_BAR
LOAD
BT
RESET
LOAD
LP
EP_BAR
CP
CLEAR
EM_BAR
LM_BAR
R_BAR
W_BAR
EDB_BAR
EDR_BAR
LDR_BAR
MEM_BUS
LIR_BAR
EIN_BAR
LA_BAR
EA_BAR
LB_BAR
EB_BAR
LO_BAR
ET_BAR
LT_BAR
ES_BAR
DS
IS
LS
EU_BAR
EF_BAR
CIN0
CIN1
S0
S1
S2
S3
M
LF_BAR
CMC
HLT
1B
2B
OVF
CON1
CON2
CON3
CON4
A5
A6
GND

CON


U55
COUNTER_4
U54
2732
U58
6116
U56:A
74LS08
U1
74LS157
U67:A
74LS244
U61:A
74LS244
U13
COUNTER_8
U60
2732
U62:A
74HC21
U62:B
74HC21
U63:A
74LS08
U65
74LS173
U57:C
74LS04
U64
74LS157
U61:B
74LS244
U67:B
74LS244
COMB_CLK
BT_BAR
CLR_ROM
CP_ROM
R_BAR
W_BAR
HLT
MEMORY