Project
VLSI for Digital signal processing

Topic: 9 tap FIR filter implementation

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What is a Filter???

A filter is a device or process that removes unwanted components or features from a signal.

Application:
1.Audio processing (removing noise)
2.Image processing (smoothing or sharpening)
3.Communication systems (selecting signal bands)

what is FIR filters???

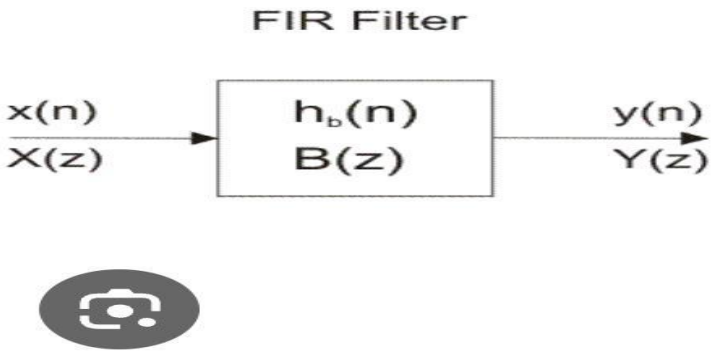
A Finite Impulse Response (FIR) filter has a finite duration response to an impulse input.
An FIR filter of order is defined by the difference equation:
$y[n] = b0x[n] + b1x[n-1] + b2x[n-2] + \ldots. + bnx[n-N]$

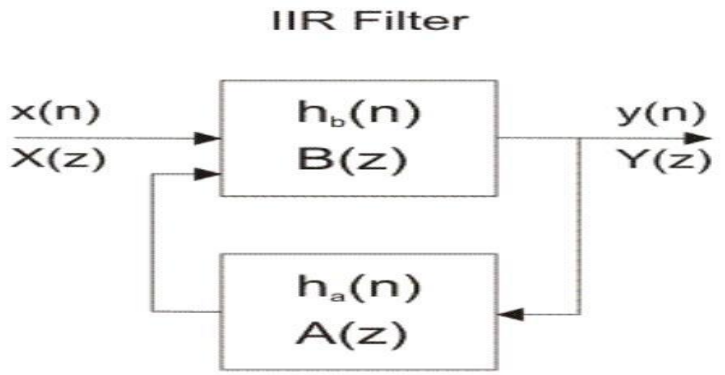
Impulse Response:

The impulse response of an FIR filter is just its coefficients:
$h[n] = \{b0, b1, ..., bN\}$

Properties of FIR

1. Linear Phase:
2. Always Stable:
3. Simple Impleme
4. No IIR Feedbac





9 tap FIR filter

We have made a 9 tap FIR filter with the following specifications and using 6 stage pipelined structure:

Input frequency (fc) :10 MHz

Sampling frequency (fs) : 100 MHz

f1=2MHz, f2=30MHz

Coeff 0 = 57.	coeff4 = 8879	coeff 8=166
Coeff1 =166.	coeff 5 =7187	
Coeff2 = 962.	coeff 6=3629	
Coeff3 = 3629.	coeff 7=962	

Non pipelined design

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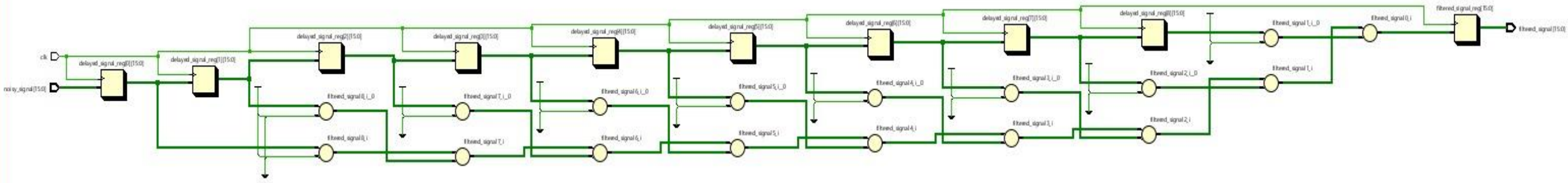
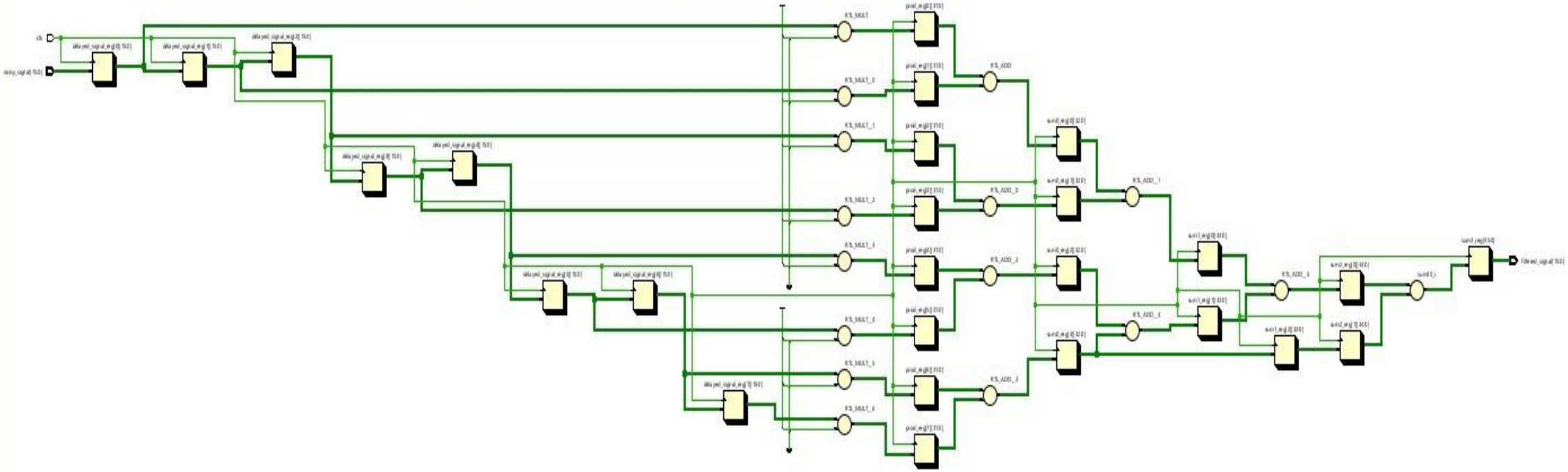
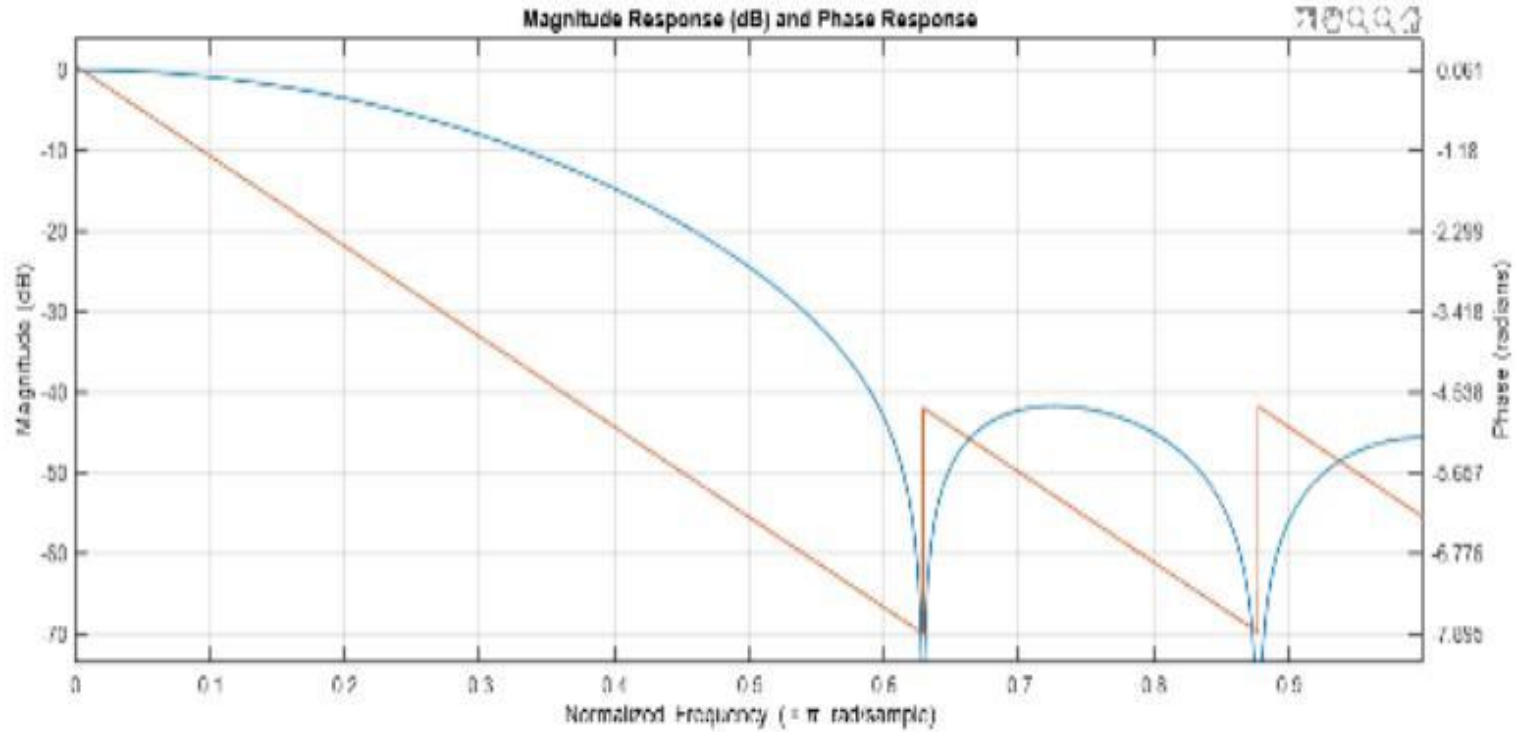


Pipelined design





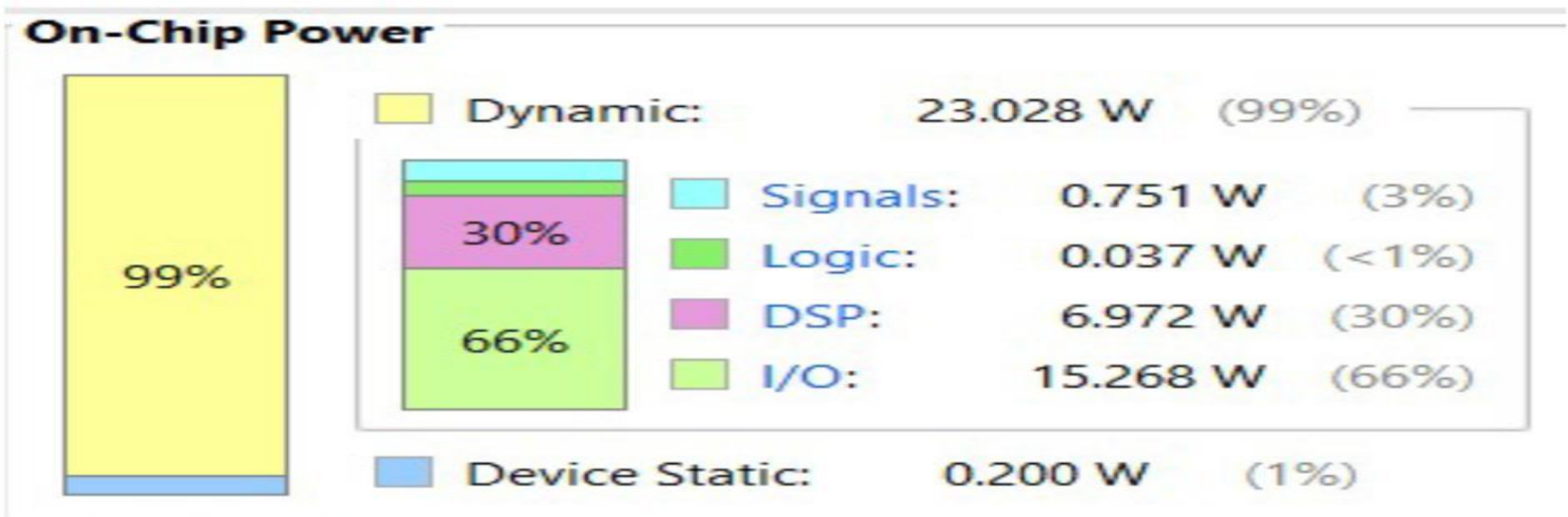
magnitute and phase response

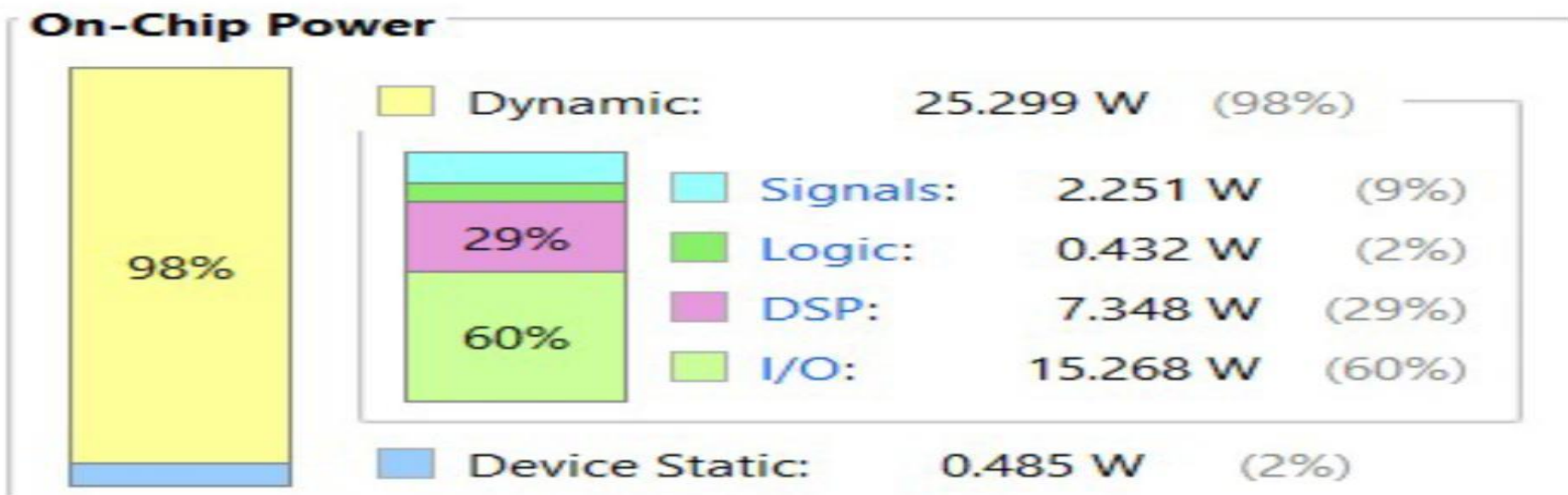
Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	D
Path 1	∞	8	1	filtered_signal1/CLK	filtered_signal0__6/PCIN[0]	13.728	13.728	0.000	∞		
Path 2	∞	8	1	filtered_signal1/CLK	filtered_signal0__6/PCIN[10]	13.728	13.728	0.000	∞		
Path 3	∞	8	1	filtered_signal1/CLK	filtered_signal0__6/PCIN[11]	13.728	13.728	0.000	∞		
Path 4	∞	8	1	filtered_signal1/CLK	filtered_signal0__6/PCIN[12]	13.728	13.728	0.000	∞		
Path 5	∞	8	1	filtered_signal1/CLK	filtered_signal0__6/PCIN[13]	13.728	13.728	0.000	∞		
Path 6	∞	8	1	filtered_signal1/CLK	filtered_signal0__6/PCIN[14]	13.728	13.728	0.000	∞		
Path 7	∞	8	1	filtered_signal1/CLK	filtered_signal0__6/PCIN[15]	13.728	13.728	0.000	∞		

timing analysis of non pipelined

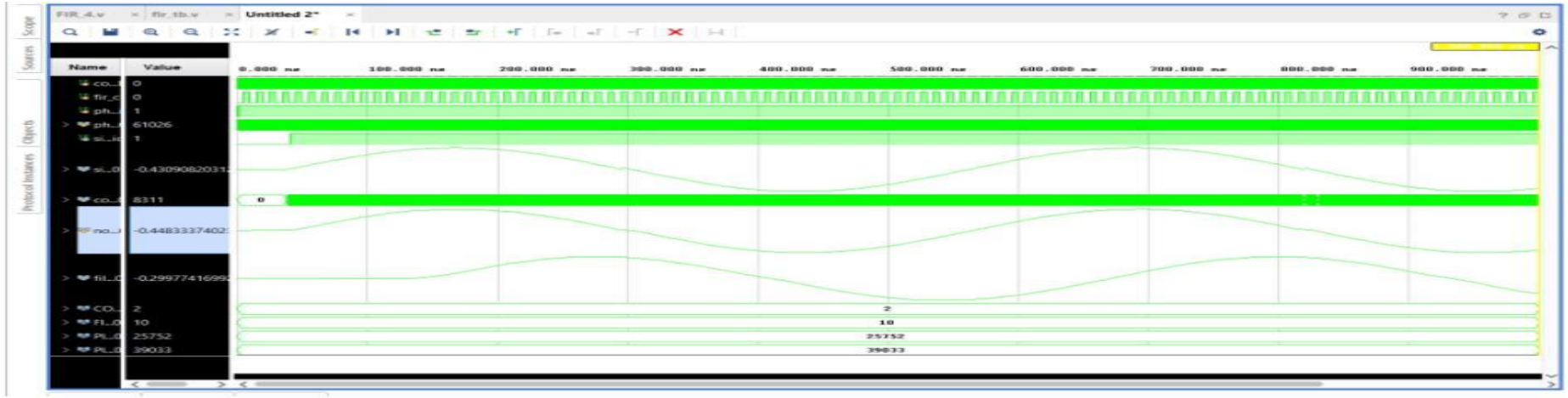
Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	∞	2	1	sum3_reg[15]/C	filtered_signal[0]	5.441	3.055	2.385	∞
Path 2	∞	2	1	sum3_reg[19]/C	filtered_signal[4]	5.430	3.063	2.367	∞
Path 3	∞	2	1	sum3_reg[17]/C	filtered_signal[2]	5.429	3.053	2.376	∞
Path 4	∞	2	1	sum3_reg[16]/C	filtered_signal[1]	5.423	3.050	2.373	∞
Path 5	∞	2	1	sum3_reg[18]/C	filtered_signal[3]	5.409	3.054	2.355	∞
Path 6	∞	2	1	sum3_reg[20]/C	filtered_signal[5]	5.381	3.054	2.327	∞
Path 7	∞	2	1	sum3_reg[23]/C	filtered_signal[8]	5.250	3.070	2.180	∞

timing analysis of pipelined

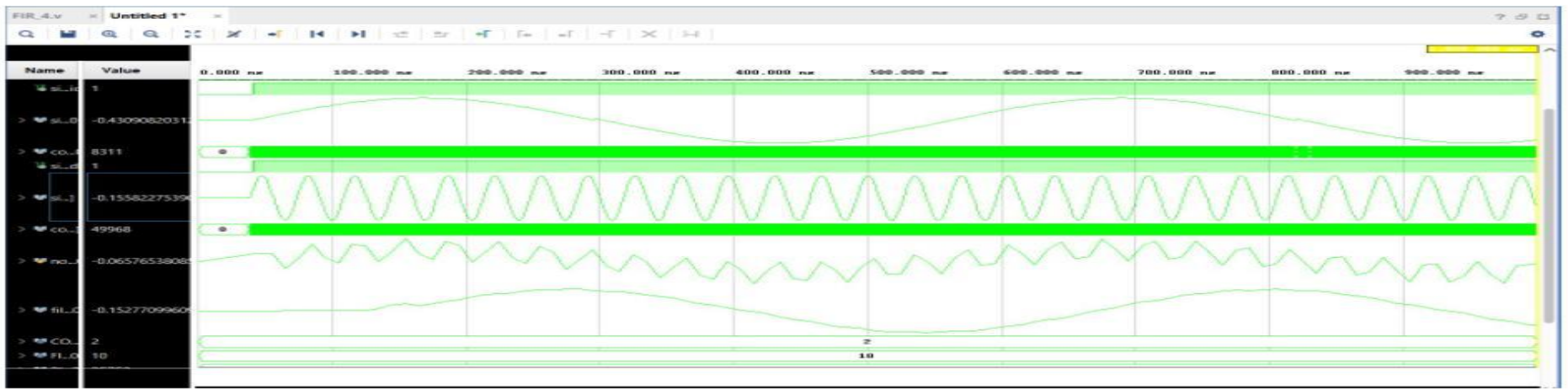




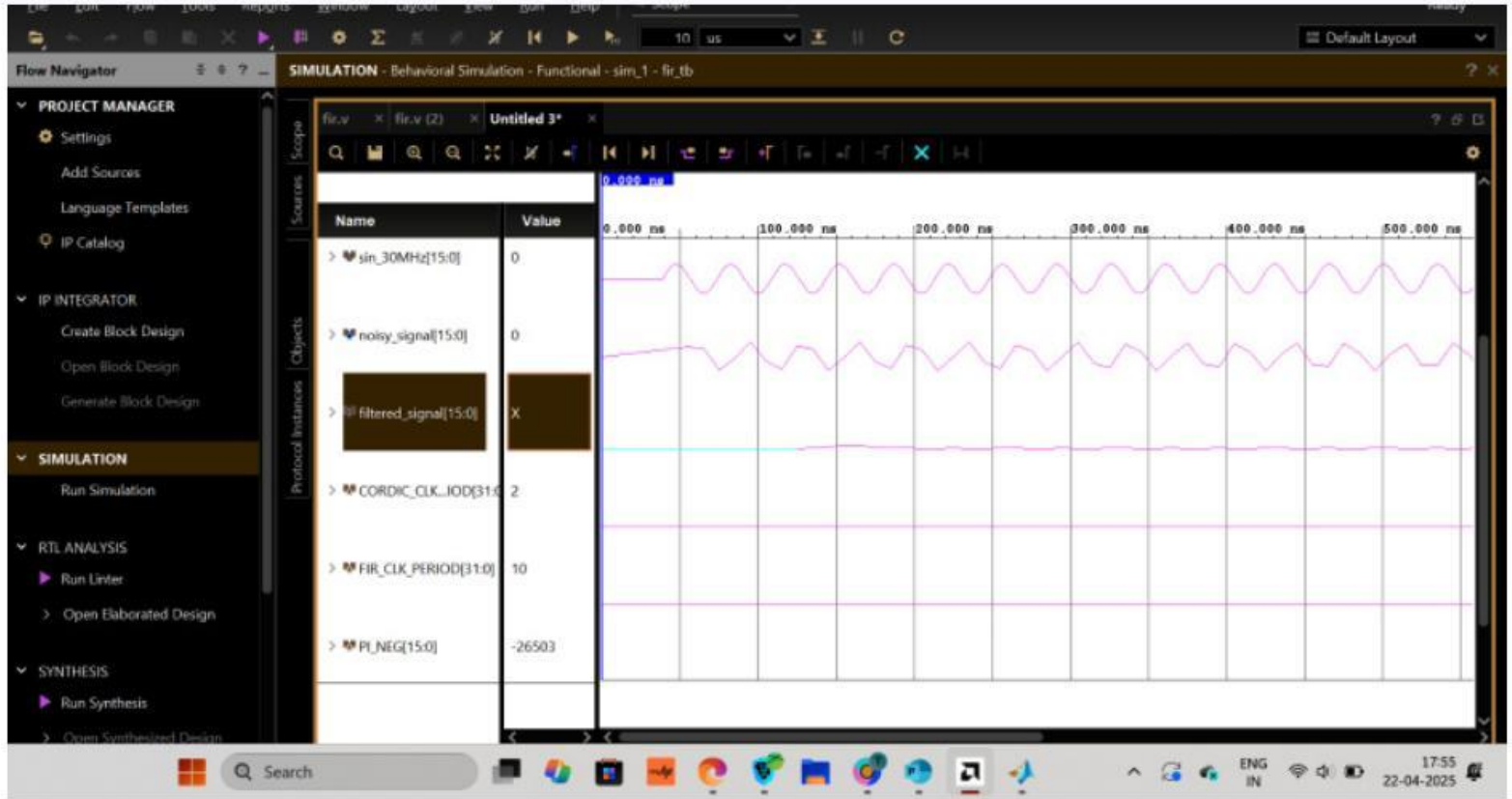
power analysis of pipelined (2)and non pieplined (1)



output when input is f1 = 2MHz



output when f1 =2 MHz and f2 = 30 MHz are given



output when f2 = 30MHz is given