Computer Architecture & Organization

P. Pages : 2

Time : Three Hours

AHK/KW/19/2150

Max. Marks : 80

1197

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Assume suitable data whenever necessary.
9. Illustrate your answers whenever necessary with the help of neat sketches.

1.	a)	Explain straight line sequencing in detail what is the function of MAR, MDR, ALU.	7
	b)	Differentiate between multiprocessor & multicomputers.	6

OR

2.	a)	Explain various address modes with example.	7
	b)	Explain functional units of a basic computer system.	6
3.	a)	Enlist and explain with example the difference addressing modes of 68000 processor.	8
	b)	Explain instruction format of M 68000 machine.	6

OR

4.	a)	Write down the control steps for execution of following instruction. ADD LOC, R1 (where LOC is memory location).	6
	b)	Explain with proper diagram single and three bus structure.	8
5.	a)	Explain Hardwired control unit.	7
	b)	Write a short note on : i) Bit-slices. ii) Emulation. iii) Micro instruction with next address field.	6

OR

6.	a)	Why control signals are needed in a CPU to execute an instruction? Write a control signal generation for ADD R_0, R_1 where result is stored in R_6.	7
	b)	What is horizontal and vertical μ-instruction format? Explain grouping of control signal with suitable example.	6

7. a) Represent 1/32 and −1/16 in IEEE 754 signal precision format. 6

   b) Multiply the following pair of signed 2's complement number using Booths multiplication and bit pair recording techniques. 7
   A = 010111, B = 110110
   where A is multiplicant & B is multiplier.

OR

8. a) Solve the following using non-restoring division method 11/3. 7

   b) Explain the design of carry Look ahead address. 6

9. a) Define virtual memory. Explain address translation in virtual memory. 7

   b) Write advantages of Dynamic RAM cell over static RAM cell. 6

OR

10. a) Explain various mapping techniques in cache memory. 7

    b) Explain in brief about memory interleaving. 6

11. a) Explain DMA in details. 6

    b) Explain the following. 8
    i) Array processors.　　　　　　ii) Online storage.
    iii) Pipelining.　　　　　　　　iv) Memory Interleaving.

OR

12. a) Define Interrupts. Explain in detail different types of interrupts. 6

    b) Write short note on **any three.** 8
    i) Pipelining.
    ii) RISC and CISC processor.
    iii) Array processor.
    iv) Loosly coupled & tightly coupled systems.

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