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B.E. (Computer Science & Engineering) (New) Third Semester (C.B.S.)

Computer Architecture & Organization

P. Pages : 2 **NIR/KW/18/3326**

Time : Three Hours * 1 8 9 3 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.

1. a) Explain various addressing modes with examples which are used in instruction set design. **7**

b) Discuss single and three bus architecture with the help of diagram. **6**

OR

2. a) Differentiate between Hardwired control unit and microprogrammed control unit. **7**

b) Explain zero address, one address and two address instructions with example. Solve $(A*B) + (C*D)$ **6**

3. a) Give the non-restoring integer division algorithm. Also draw the necessary circuit arrangement for the same and solve 10/3. **7**

b) Represent the following number in IEEE single precision and double precision floating point format **7**
a) 0.000138 b) 411.1825

OR

4. a) Describe Booth's algorithm for multiplication of two binary numbers and multiply $20*-4$ **7**

b) Design a carry look ahead adder. **7**

5. a) Find the page hit and page fault ratio for the given page address stream using **6**
i) Least recently used
ii) Optimal page replacement policy.
Assume four page buffers. Page address stream $\rightarrow$ [2,3,2,1,5,2,4,5,3,2,5,2]

b) Write a note on multiple module memory system. **7**

OR

6. a) Draw and explain internal structure of cache. **6**

	b)	Explain the concept of memory hierarchy and characteristics of memory.	**7**
7.	a)	Explain direct memory access in detail.	**7**
	b)	Write a short note on hard disk and floppy disk.	**6**

OR

8.	a)	Differentiate between synchronous & Asynchronous data transfer.	**7**
	b)	Explain I/O mapped I/O and memory mapped I/O. State the advantage of I/O mapped I/O over memory mapped I/O.	**6**
9.	a)	State and explain various hazards in instruction pipelining with proper example of each.	**7**
	b)	Discuss in brief about delayed branching.	**6**

OR

10.	a)	Draw a typical hardware for a four stage instruction pipelining and explain it.	**7**
	b)	Explain data dependency in detail with example.	**6**
11.	a)	Draw and explain the uniform and non-uniform memory access multiprocessor system.	**7**
	b)	Write a short note on array processor.	**7**

OR

12.	a)	Explain vector processor with suitable example.	**7**
	b)	Describe the loosely and tightly coupled multi-computer system.	**7**

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All our dreams can come true if we have the courage to pursue them.

~ Walt Disney