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B.E. (Information Technology) Fourth Semester (C.B.S.)

Computer Architecture & Organization

P. Pages : 2 **NRT/KS/19/3386**

Time : Three Hours * 0 7 8 4 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Assume suitable data whenever necessary.
8. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) Explain the functional units of a basic computer system with suitable example. **6**

b) Explain straight line sequencing in detail. What is the function of MAR, MDR, ALU. **7**

OR

2. a) Differentiate between the big Indian assignment and little Indian assignment. **6**

b) Explain 3-address, 2-Address, 1-address and zero-address instruction format with example. **7**

3. a) Explain the instruction formats of M 68000 machine. **6**

b) Write and explain control sequences for Add (R3) R1. **7**

OR

4. a) Explain single bus organization of a data path of a processor with block diagram. **6**

b) Explain the role of stack in subroutine (all implementations) with example. **7**

5. a) Explain the difference between hardwired and micro programmed control unit. **7**

b) List out the application of micro programming with example. **6**

OR

6. a) What is horizontal and vertical μ - instruction format? **6**

b) Explain grouping of control signals with a suitable example. **7**

7. a) Why 2's complement number representation is used over other methods of negative number representation. **7**

b) Solve 1010 DIV 0101 using non restoring division algorithm. **7**

OR

8.	a)	Multiply the following pair of signed 2's complement number using Booth's multiplication and bit pair recording technique A = 010111, B = 110110 A = Multiple & B = Multiplies.	**8**
	b)	Explain how arithmetic operations are performed in floating point numbers.	**6**
9.	a)	Explain virtual memory also explain how virtual address is translated into physical address.	**7**
	b)	Differentiate between	**6**
		i) RAM and ROM	
		ii) RISC And CISC.	

OR

10.	a)	Explain the various mapping techniques used in cache memory.	**7**
	b)	Explain about static RAM and Dynamic RAM.	**6**
11.	a)	Write in detail about Flynn's classification on parallel structure.	**7**
	b)	What are tightly and loosely coupled systems? Explain.	**7**

OR

12.		Write a short note on **any three.**	**14**
		i) Array processory	
		ii) Pipelining	
		iii) Memory Interleaving	
		iv) Memory mapped I/O.	

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The secret of getting ahead is getting started.

~ Mark Twain