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B.E. (Computer Science & Engineering) (New) Third Semester (C.B.S.)

Digital Circuits & Fundamentals of Microprocessor

P. Pages : 2 **NRT/KS/19/3324**

Time : Three Hours * 0 1 9 0 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) Convert the following **6**

i) $(27.125)_{10} \rightarrow (?)_8 \rightarrow (?)16$

ii) $(101011)_{gray} \rightarrow (?)_{Binary}$

iii) $(10.655)_{10} \rightarrow (?)_2 \rightarrow (?)_{BCD}$

b) Realize X-OR gate using NOR gate **3**

c) Minimize $f_2(A,B,C,D) = \Sigma m\,(0,1,5,9,11,14,15) + \Sigma d\,(10,13)$ using k - map. **4**

OR

2. a) Explain and prove De-Morgan's Theorem. **5**

b) Express the following function in standard sop form **4**

$f(A,B,C,D) = (\overline{A} + BC)(B + \overline{C}D)$

c) Simplify the following expression and implement it with NAND gate circuit **4**

$F = A\overline{B} + ABD + AB\overline{D} + \overline{A}\,\overline{C}\,\overline{D} + \overline{A}\,B\,\overline{C}$

3. a) Design BCD to 7 segment decoder for common cathode configuration. **8**

b) Draw & explain full adder using two half adders and one OR gate. **5**

OR

4. a) Implement the following using 4:1 multiplexer **7**

$F(A,B,C,D) = \Sigma m\,(1,2,3,4,5,8,9,12)$

b) Implement the following using 3:8 decoder circuit **6**

i) $f_1(A,B,C) = \Sigma m(0,3,2,4)$

ii) $f_2(A,B,C) = \pi M(1,2,5,6)$

5. a) Explain the Race - around condition of JK-F/F. Also explain how it can be avoided in master salve JK flip flop **9**

b) Differentiate between combinational circuit and sequential circuit. **5**

OR

6. a) Write notes on:

i) Excitation table for flip flop **3**

ii) Use of preset and clear terminals of flip flop. **3**

b) Explain different methods of triggering in flip-flop. **4**

c) Draw and explain how a Latch can be used as 1 bit memory cell. **4**

7. a) Draw and explain 4 bit parallel input serial output (PISO) shift register. **5**

b) Convert the following **8**
i) JK flip flop to SR flip flop ii) T flip flop to JK flip flop

OR

8. a) Draw and explain 3 bit Down-counter (Synchronous) using JK F/F **6**

b) Draw and explain Johnson counter with state diagram, sequence table and Timing diagram upto 4 bit. **7**

9. a) Draw and explain the architecture of up 8085 **8**

b) Write short note on **6**
i) ROM ii) PLA and PAL

OR

10. a) Give the format of Flag register in 8085. Explain each flag. **7**

b) Explain the classification of memories and their characteristics. **7**

11. a) Draw and explain hardware Interrupt in 8085. **8**

b) Write ALP to find the number of negative elements (most significant bit 1) in a block of data The length of the block is in memory location 2200 H and the block itself begins from location 2201 H, store the number of negative elements in memory location 2300 H **5**

OR

12. a) Explain the following **6**
i) ANA M ii) PCHL iii) JPO address

b) Draw and explain timing diagram of instruction MVI A, 30 H **7**

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The best time to plant a tree was 20 years ago. The second best time is now.

~ Chinese Proverb