B.E. (Information Technology) Third Semester (C.B.S.)

Digital Electronics & Fundamentals of Microprocessor

P. Pages : 2 **NRJ/KW/17/4385**

Time : Three Hours * 0 5 2 3 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) State & prove the De-Morgan's theorem. **6**

b) Convert the following **8**

1) $(675.625)_{10} = (?)_{16}$
2) $(3287.51)_{10} = (?)_{8}$
3) $(11011.010)_{2} = (?)_{G}$
4) $(2A3.AB)_{H} = (?)_{8}$

OR

2. a) Simplify the following **6**

1) $AB + \overline{A}C + BC = AB + \overline{A}C$

2) $AB + A\overline{B}C + B\overline{C} = AC + B\overline{C}$

b) Draw symbol of AND, NOR, Ex – OR & NAND gates & write their truth tables. **8**

3. a) Express the following function in standard SOP form **5**

i) $f(A, B, C) = AB + A\overline{C} + BC$

ii) $f(A, B, C, D) = (\overline{A} + BC)\,(B + \overline{C}\,D)$

b) Simplify following function using k-map & implement using universal gate. **8**

i) $f(A, B, C, D) = \sum M\,(0,1,4,5,6,7,9,11,15) + d(10,14)$

ii) $f(W, X, Y, Z) = \Pi M\,(1,4,6,9,10,11,14,15)$

OR

4. a) Minimize the following expressions using k-map & realize using NAND gates. **8**

$F(A, B, C, D, E) = \sum M\,(0,5,6,8,9,10,11,16,20,24,25,26,27,29,31)$

b) Minimize the following expression using k-map & realize using NOR gates only. **5**

$F(P, Q, R, S) = \Pi\, M\,(1,2,3,5,6,7,9,10,11,13,14,15)$

5. a) Design full subtractor circuit using two half subtractor & one OR gate. Also draw the logic circuit & give it's truth table. **6**

b) Implement the following function using 8:1 MUX. Use W, X, Y as select lines. **7**
$F(W, X, Y, Z) = \Pi M(0,1,4,6,9,10,11,15)$

OR

6. a) Design 3 bit binary to grey code converter. **7**

b) Design & implement 3 input priority encoder. **6**

7. a) Convert the following **8**
1) SR flip flop to JK flip flop
2) JK flip flop to T flip flop

b) What is race around condition in JK flip flop? How it is eliminated by using JK-Master slave flip-flop. **6**

OR

8. a) Design lock free counter to count in following sequence (Use T Flip Flop) **8**

$$\frac{1}{\uparrow} \rightarrow 3 \rightarrow \frac{4}{\downarrow}$$
$$6 \leftarrow 7 \leftarrow 5$$

b) Draw the logic diagram of JK flip-flop using NAND gate & explain its working. **6**

9. a) Define addressing mode. Explain different addressing mode of 8085 microprocessor with one example each. **7**

b) Explain the following instruction **6**
1) XTHL
2) DAA
3) DAD R_p
4) LDAX B

OR

10. a) Draw & explain the architecture of 8085 microprocessor in detail. **8**

b) Draw & Explain the flag register of 8085 microprocessor. **5**

11. a) Draw & explain interrupt structure of 8085 microprocessor in detail. **7**

b) Draw & explain timming diagram of instruction MVI A, 22H. **6**

OR

12. a) Write an assembly language program to add 10 bytes of data. Data is present from 8000H & onwards memory location. Store answer in B register. **6**

b) Draw & explain RIM & SIM instruction of 8085 microprocessor. **7**

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