Implementation of AND-Gate using VHDL

OBJECTIVE:

To implement AND gate using VHDL and verify its waveform in Xilinx.

INTRODUCTION:

VHDL: It is an industry standard hardware description language that is widely used for specifying modeling, designing and simulation digital systems, we can use VHDL to describe system structurally or behaviorally at any of several different level of abstraction.

Library: IEEE is a common library containing predefined data types and operations for standard digital logic.

IEEE.STD_LOGIC_1164.ALL; --Standard logic types
IEEE.STD_LOGIC_ARITH.ALL; --Arithmetic operations
IEEE.STD_LOGIC_UNSIGNED.ALL; --Unsigned operations

Entity: Defines inputs and outputs of a component.

Architecture: It describes the internal implementation of the system. It defines how the system behaves or is structured. There can be multiple architectures for a single entity.

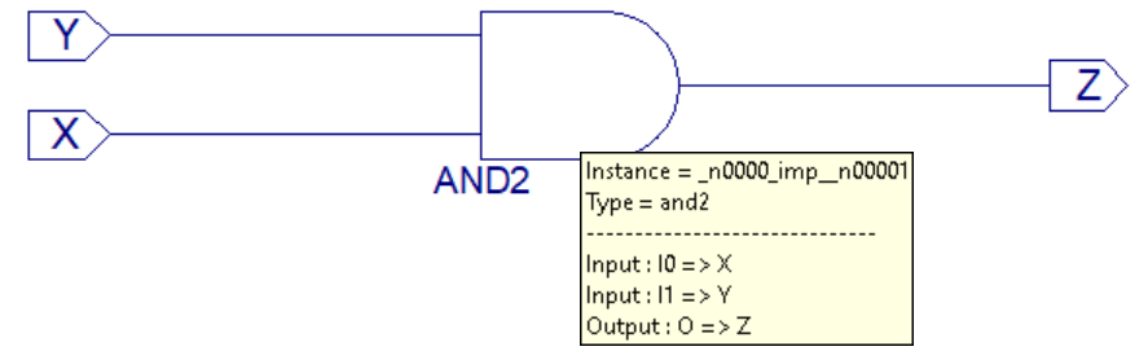
Process: It is a block of code that describe sequential behavior. It is use to model time-dependent behavior such as clocking events or state machines.

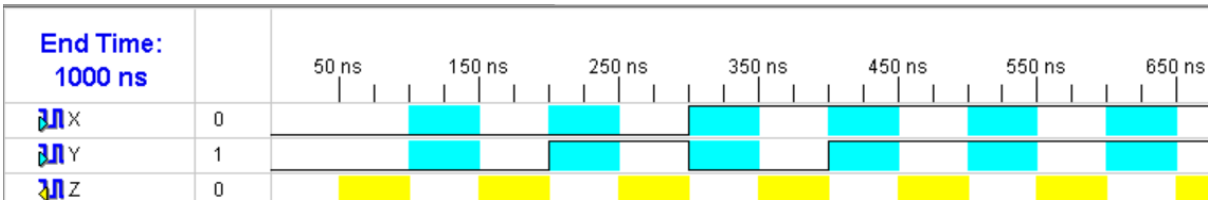
Signal Assignment: Defines how signals are assigned values based on logic.

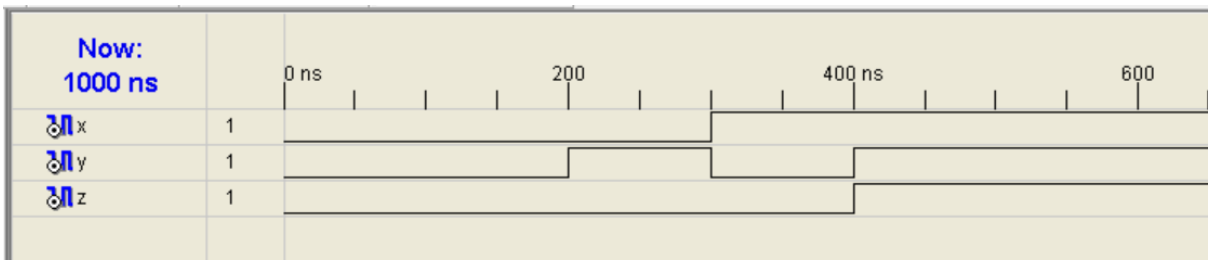
Source Code:

```
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.STD_LOGIC_ARITH.ALL;
23  use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25  ---- Uncomment the following library declaration if instantiating
26  ---- any Xilinx primitives in this code.
27  --library UNISIM;
28  --use UNISIM.VComponents.all;
29
30  entity OHO is
31      Port ( X : in  STD_LOGIC;
32             Y : in  STD_LOGIC;
33             Z : out  STD_LOGIC);
34  end OHO;
35
36  architecture Behavioral of OHO is
37
38  Begin
39     Process (X, Y)
40        Begin
41           If (X = '1' and Y = '1') then
42              Z <= '1';
43           Else
44              Z <= '0';
45        End if;
46     End process;
47  End Behavioral;
```

- **Output:**







- **DISCUSSION:**

In this lab of an Embedded System, we successfully implemented an AND Gate using VHDL. The VHDL code was simple once I understood the syntax. The simulation results matched the expected output, confirming our design was correct. The test bench helped verify all input combinations.

- **CONCLUSION:**

Overall, the lab was a great learning experience. We implemented a basic AND gate and gained valuable insights into VHDL programming and digital logic design. I'm excited to explore more complex circuits in future labs.