CONCORDIA UNIVERSITY

Laboratory Report
COEN - 316

Lab – 2
Register File

Submission Date: October 24, 2019

Prepared by

Salman Rahman	27853815
Name	Student ID

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Figures

- ModelSim Simulation of Register file: (please zoom in the figures if required)

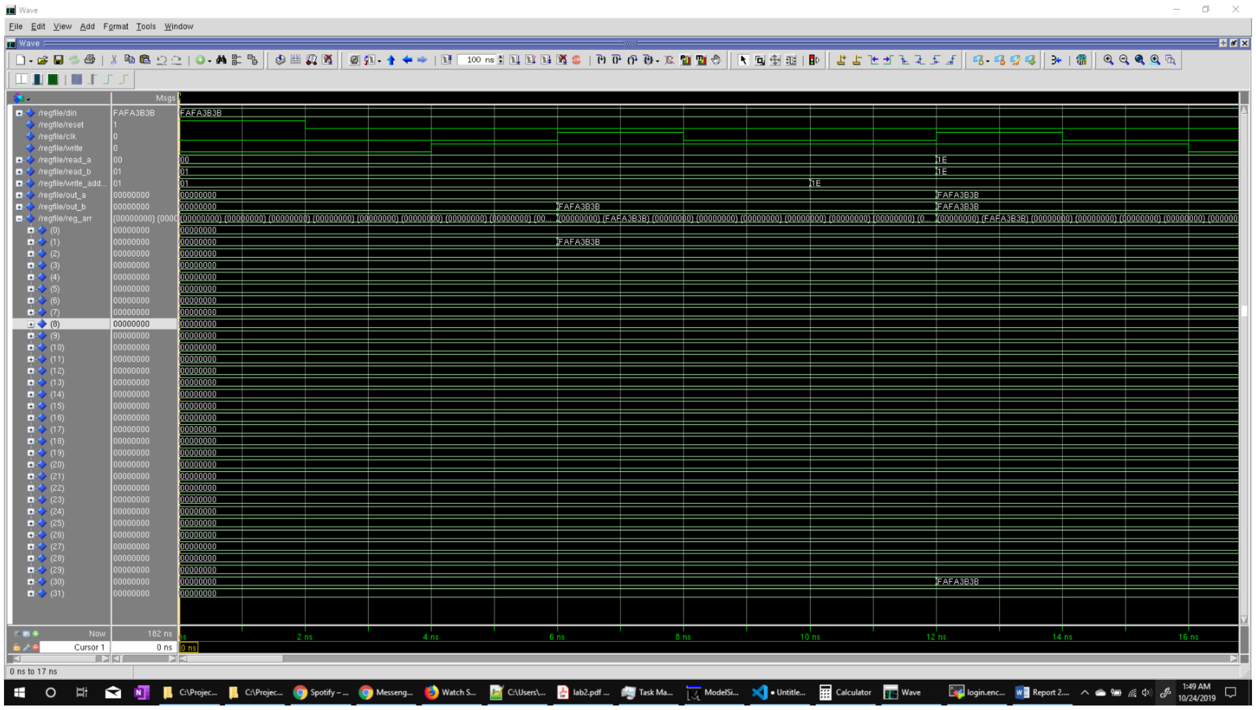


Figure 1 Simulation of register file from 0 to 16 ns according to the given do file in the lab manual, in this case the register file was reset using the asynchronous reset signal and different registers are being loaded with the data from the din input signal

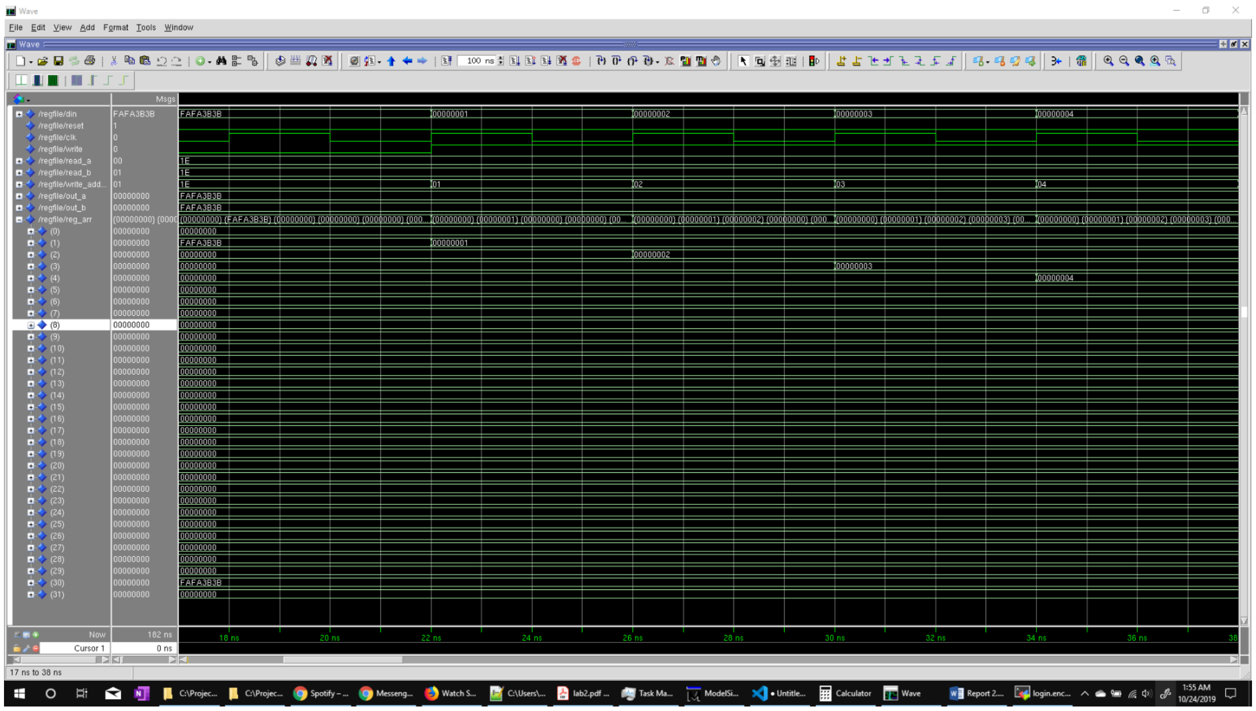


Figure 2 Simulation of register file from 16 to 38 ns, during this time every register is being saved with data at every clock cycle

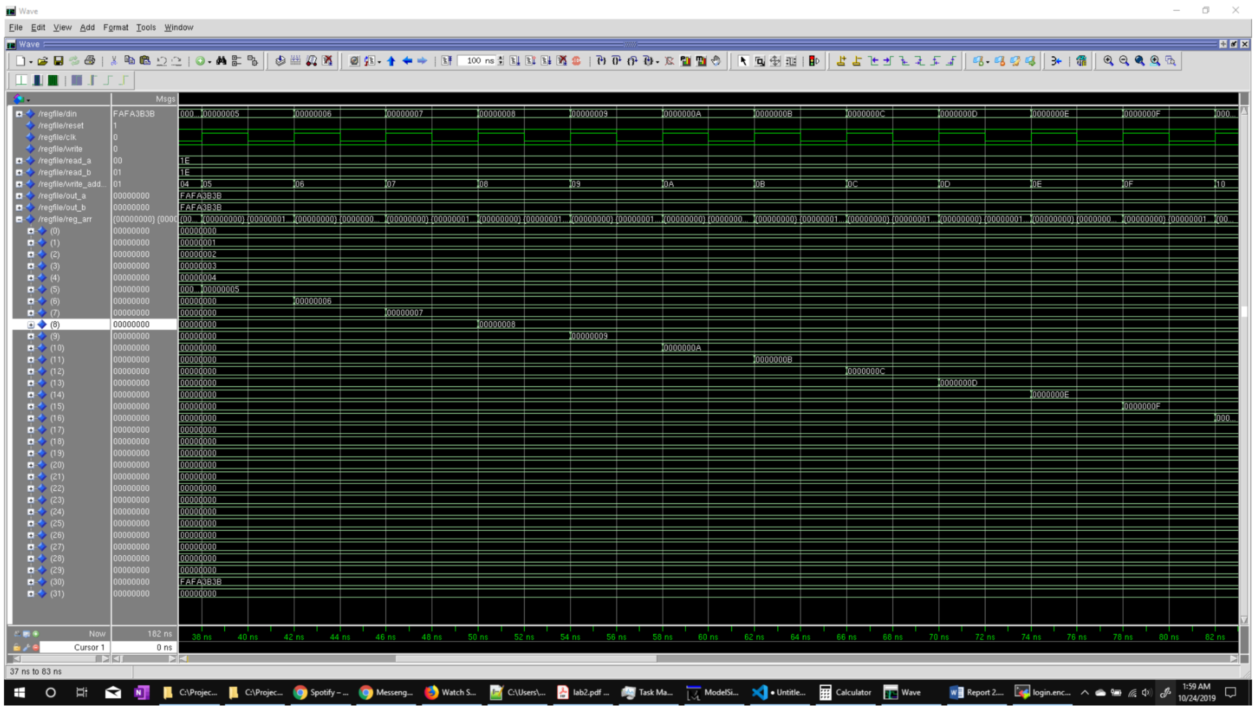


Figure 3 Simulation of register file from 38 to 82ns, during this time registers up to register 16 in the register file was loaded with data from the din input at every rising clock edge

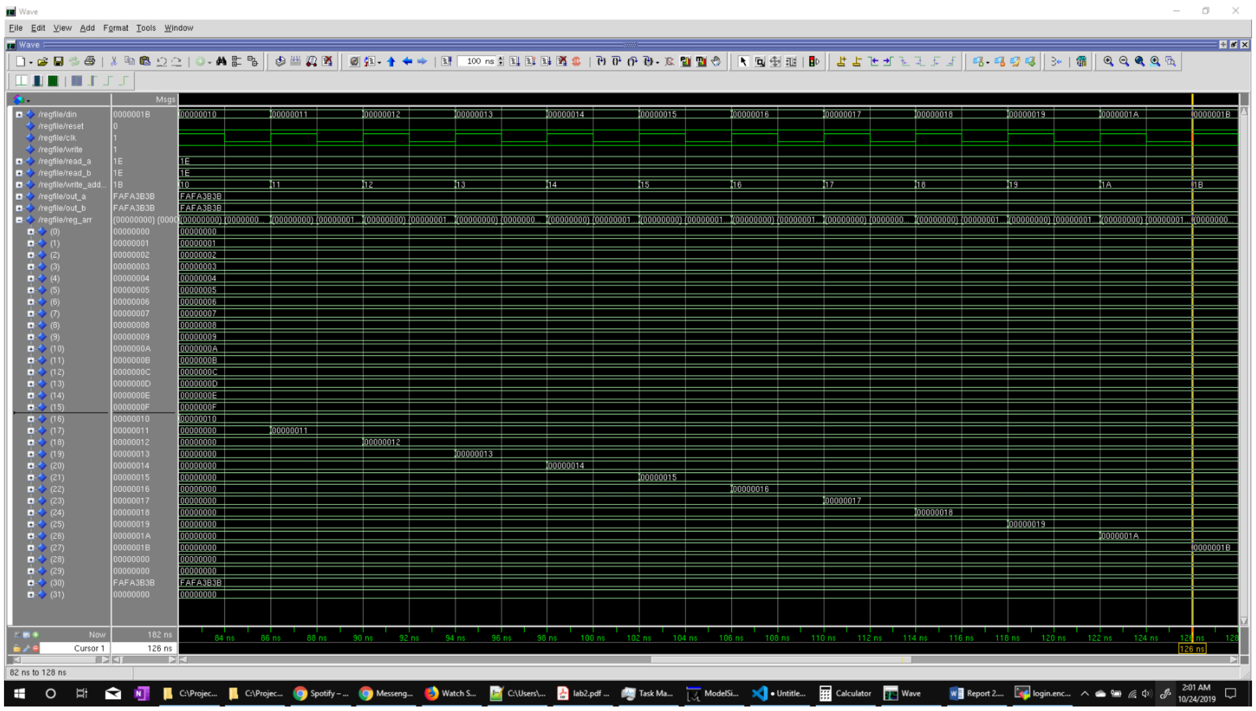
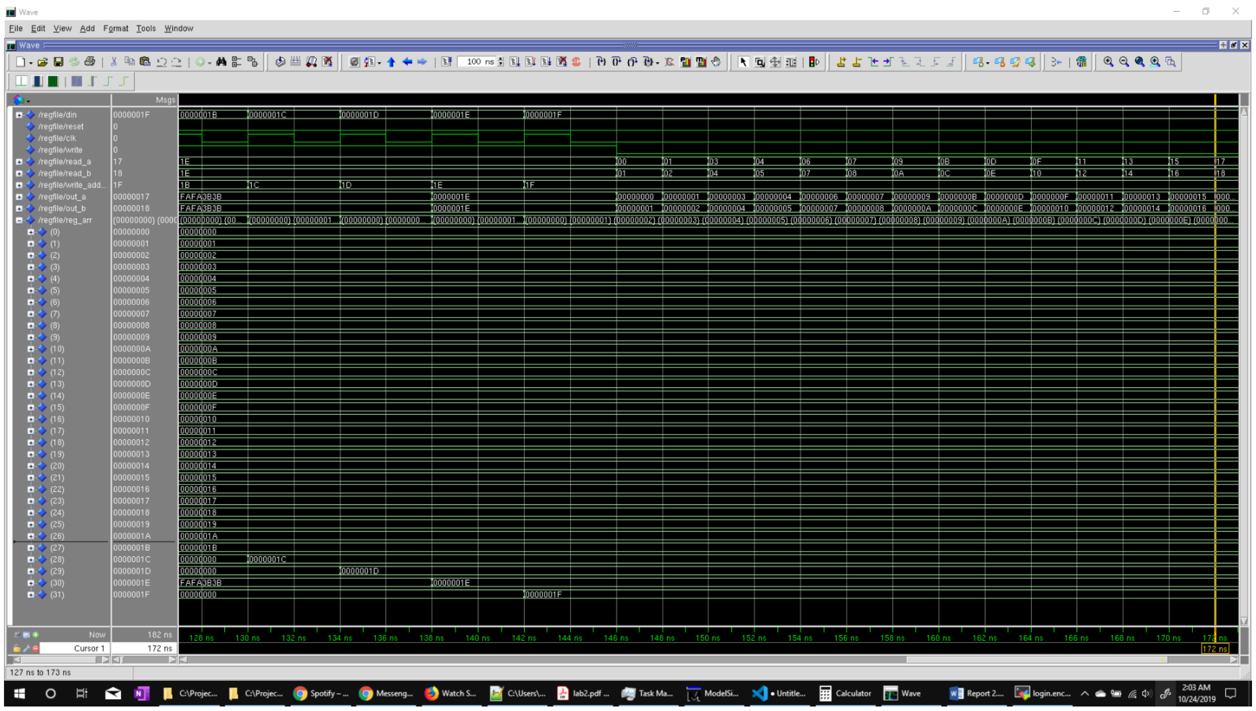


Figure 4 Simulation of register file from 82 to 126ns, during this time registers up to register 27 in the register file was loaded with data from the din input at every rising clock edge



```
/regfile/din          0000001F
/regfile/reset        0
/regfile/clk          0
/regfile/write        0
/regfile/read_a       17
/regfile/read_b       18
/regfile/write_add... 1F
/regfile/out_a        00000017
/regfile/out_b        00000018
/regfile/reg_arr      {00000000} {0000
  (0)                 00000000
  (1)                 00000001
  (2)                 00000002
  (3)                 00000003
  (4)                 00000004
  (5)                 00000005
  (6)                 00000006
  (7)                 00000007
  (8)                 00000008
  (9)                 00000009
  (10)                0000000A
  (11)                0000000B
  (12)                0000000C
  (13)                0000000D
  (14)                0000000E
  (15)                0000000F
  (16)                00000010
  (17)                00000011
  (18)                00000012
  (19)                00000013
  (20)                00000014
  (21)                00000015
  (22)                00000016
  (23)                00000017
  (24)                00000018
  (25)                00000019
  (26)                0000001A
  (27)                0000001B
  (28)                0000001C
  (29)                0000001D
  (30)                0000001E
  (31)                0000001F
Now                   182 ns
Cursor 1              172 ns
127 ns to 173 ns
```

Figure 5 Simulation of 126 to 172ns is shown in the figure. All the 32 registers are loaded with data at 32 clock rising edges. The read_a and read_b values are changed to see the proper output at the out ports.

- Precision log file

```
# Info: [9566]: Logging session transcript to file /nfs/home/s/sal_rahm/316/fpga_adv/lab2/precision.log
//  Precision RTL Synthesis  64-bit 2016.1.0.15 (Production Release) Wed Jun  8 09:35:56 PDT 2016
//
//  Copyright (c) Mentor Graphics Corporation, 1996-2016, All Rights Reserved.
//             Portions copyright 1991-2008 Compuware Corporation
//                       UNPUBLISHED, LICENSED SOFTWARE.
//            CONFIDENTIAL AND PROPRIETARY INFORMATION WHICH IS THE
//          PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS
//
//  Running on Linux sal_rahm@grace.encs.concordia.ca #1 SMP Fri Sep 20 08:24:10 CDT 2019 3.10.0-1062.1.2.el7.x86_64 x86_64
//
//  Start time Thu Oct 24 02:16:52 2019
# --------------------------------------------------
# Info: [9566]: Logging session transcript to file /nfs/home/s/sal_rahm/316/fpga_adv/lab2/precision.log
# COMMAND: new_project -name project_1 -folder /nfs/home/s/sal_rahm/316/fpga_adv/lab2 -createimpl_name lab2
# Info: [9574]: Input directory: /nfs/home/s/sal_rahm/316/fpga_adv/lab2
# Info: [9569]: Moving session transcript to file /nfs/home/s/sal_rahm/316/fpga_adv/lab2/precision.log
# Info: [9555]: Created project /nfs/home/s/sal_rahm/316/fpga_adv/lab2/project_1.psp in folder /nfs/home/s/sal_rahm/316/fpga_adv/lab2.
# Info: [9531]: Created directory: /nfs/home/s/sal_rahm/316/fpga_adv/lab2/lab2.
# Info: [9554]: Created implementation lab2 in project /nfs/home/s/sal_rahm/316/fpga_adv/lab2/project_1.psp.
# Info: [9575]: The Results Directory has been set to: /nfs/home/s/sal_rahm/316/fpga_adv/lab2/lab2/
# Info: [9566]: Logging project transcript to file /nfs/home/s/sal_rahm/316/fpga_adv/lab2/lab2/precision.log
# Info: [9566]: Logging suppressed messages transcript to file /nfs/home/s/sal_rahm/316/fpga_adv/lab2/lab2/precision.log.suppressed
# Info: [9550]: Activated implementation lab2 in project /nfs/home/s/sal_rahm/316/fpga_adv/lab2/project_1.psp.
new_project -name project_1 -folder /nfs/home/s/sal_rahm/316/fpga_adv/lab2 -createimpl_name lab2
# COMMAND: add_input_file {../../32-bit-CPU/32-bit-register.vhd}
add_input_file {../../32-bit-CPU/32-bit-register.vhd}
# COMMAND: setup_design -manufacturer Xilinx -family "VIRTEX-II Pro" -part 2VP30ff896 -speed -7
# Info: [15298]: Setting up the design to use synthesis library "xcv2p.syn"
# Info: [575]: The global max fanout is currently set to 10000 for Xilinx - VIRTEX-II Pro.
# Info: [15324]: Setting Part to: "2VP30ff896".
# Info: [15325]: Setting Process to: "7".
# Info: [7512]: The place and route tool for current technology is ISE.
setup_design -manufacturer Xilinx -family "VIRTEX-II Pro" -part 2VP30ff896 -speed -7
# COMMAND: setup_design -frequency 100 -max_fanout=10000
# Info: [575]: The global max fanout is currently set to 10000 for Xilinx - VIRTEX-II Pro.
setup_design -frequency 100 -max_fanout=10000
# COMMAND: compile
# Info: [3022]: Reading file: /CMC/tools/mentor/precision/Mgc_home/pkgs/psr/techlibs/xcv2p.syn.
# Info: [634]: Loading library initialization file /CMC/tools/mentor/precision/Mgc_home/pkgs/psr/userware/xilinx_rename.tcl
# Info: XILINX
# Info: [40000]: vhdlorder, Release 2016a.7
# Info: [40000]: Files sorted successfully.
# Info: [40000]: hdl-analyze, Release RTLC-Precision 2016a.7
# Info: [42502]: Analyzing input file "/nfs/home/s/sal_rahm/316/fpga_adv/lab2/../../32-bit-CPU/32-bit-register.vhd" ...
# Info: [659]: Top module of the design is set to: regfile.
# Info: [657]: Current working directory: /nfs/home/s/sal_rahm/316/fpga_adv/lab2/lab2.
# Info: [40000]: RTLC-Driver, Release RTLC-Precision 2016a.7
# Info: [40000]: Last compiled on Jun  2 2016 06:11:46
# Info: [44512]: Initializing...
# Info: [44504]: Partitioning design ....
# Info: [40000]: RTLCompiler, Release RTLC-Precision 2016a.7
# Info: [40000]: Last compiled on Jun  2 2016 06:47:43
# Info: [44512]: Initializing...
# Info: [44522]: Root Module work.regfile(register_file_arch): Pre-processing...
# Info: [45251]: Built-in hardware memory core inferred for variable ': regfile.reg_arr depth = 32, width = 32'.
# Info: [44523]: Root Module work.regfile(register_file_arch): Compiling...
# Info: [44842]: Compilation successfully completed.
# Info: [44856]: Total lines of RTL compiled: 42.
# Info: [44835]: Total CPU time for compilation: 0.0 secs.
# Info: [44513]: Overall running time for compilation: 0.0 secs.
# Info: [657]: Current working directory: /nfs/home/s/sal_rahm/316/fpga_adv/lab2/lab2.
# Info: [15330]: Doing rtl optimizations.
# Info: [660]: Finished compiling design.
compile
# COMMAND: synthesize
# Info: [657]: Current working directory: /nfs/home/s/sal_rahm/316/fpga_adv/lab2/lab2.
# Info: [20013]: Precision will use 3 processor(s).
# Info: [15002]: Optimizing design view:.work.regfile.register_file_arch
# Info: [12035]: -- Running timing characterization...
# Info: [8048]: Added global buffer BUFGP for Port port:clk
# Info: [3027]: Writing file: /nfs/home/s/sal_rahm/316/fpga_adv/lab2/lab2/regfile.edf.
# Info: [3027]: Writing file: /nfs/home/s/sal_rahm/316/fpga_adv/lab2/lab2/regfile.ucf.
# Info: [12045]: Starting timing reports generation...
# Info: [12046]: Timing reports generation done.
# Info: [12048]: POST-SYNTHESIS TIMING REPORTS ARE ESTIMATES AND SHOULD NOT BE RELIED ON TO MAKE QoR
DECISIONS. For accurate timing information, please run place-and-route (P&R) and review P&R generated timing reports.
# Info: [660]: Finished synthesizing design.
# Info: [11019]: Total CPU time for synthesis: 1.1 s secs.
# Info: [11020]: Overall running time for synthesis: 2.2 s secs.
synthesize
# COMMAND: save_project
# Info: [9562]: Saved implementation lab2 in project /nfs/home/s/sal_rahm/316/fpga_adv/lab2/project_1.psp.
save_project
# COMMAND: close_project -discard
# Info: [9530]: Closed project: /nfs/home/s/sal_rahm/316/fpga_adv/lab2/project_1.psp.
close_project -discard
# COMMAND: exit
exit
```

- RTL schematic and Tech schematic

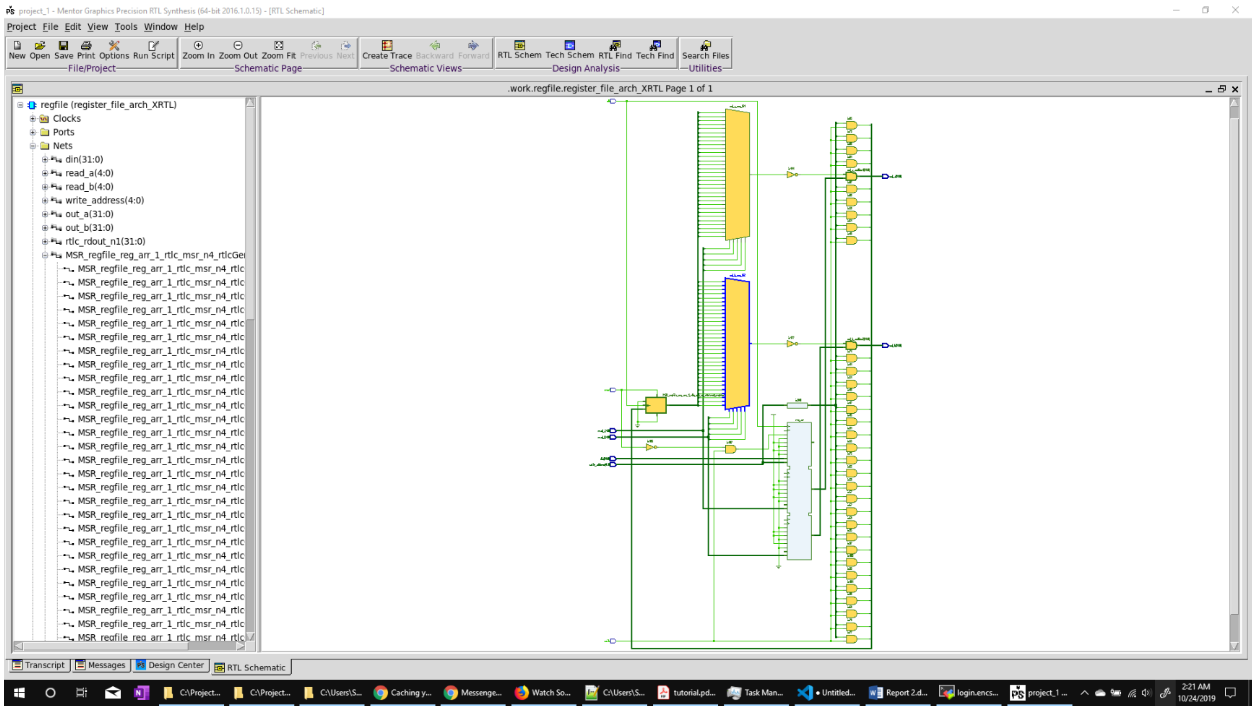

project_1 - Mentor Graphics Precision RTL Synthesis (64-bit 2016.1.0.15) - [RTL Schematic]
Project File Edit View Tools Window Help
New Open Save Print Options Run Script
File/Project
Zoom In Zoom Out Zoom Fit Previous Next
Schematic Page
Create Trace Backward Forward
Schematic Views
RTL Schem Tech Schem RTL Find Tech Find
Design Analysis
Search Files
Utilities
.work.regfile.register_file_arch_XRTL Page 1 of 1
regfile (register_file_arch_XRTL)
Clocks
Ports
Nets
din(31:0)
read_a(4:0)
read_b(4:0)
write_address(4:0)
out_a(31:0)
out_b(31:0)
rtlc_rdout_n1(31:0)
MSR_regfile_reg_arr_1_rtlc_msr_n4_rtlcGe
MSR_regfile_reg_arr_1_rtlc_msr_n4_rtlc
Transcript
Messages
Design Center
RTL Schematic
2:21 AM
10/24/2019

Figure 6 RTL schematic of the VHDL code

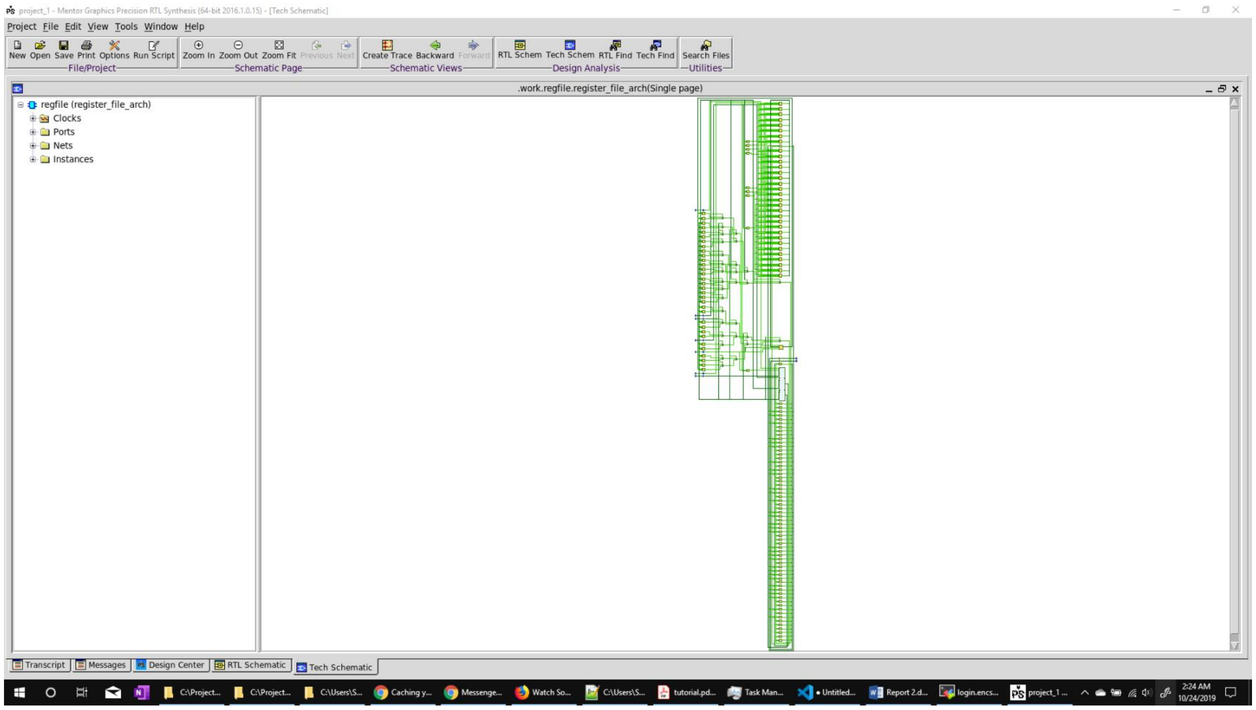

project_1 - Mentor Graphics Precision RTL Synthesis (64-bit 2016.1.0.15) - [Tech Schematic]
Project File Edit View Tools Window Help
New Open Save Print Options Run Script
File/Project
Zoom In Zoom Out Zoom Fit Previous Next
Schematic Page
Create Trace Backward Forward
Schematic Views
RTL Schem Tech Schem RTL Find Tech Find
Design Analysis
Search Files
Utilities
.work.regfile.register_file_arch(Single page)
regfile (register_file_arch)
Clocks
Ports
Nets
Instances
Transcript
Messages
Design Center
RTL Schematic
Tech Schematic
2:24 AM
10/24/2019

Figure 7 Tech schematic of the synthesis

- ALU.UCF file

```
# Precision RTL Synthesis  64-bit 2016.1.0.15 (Production Release) Wed Jun  8 09:35:56 PDT 2016

CONFIG STEPPING="0";
NET out_a (0) LOC = T6;
NET out_a (1) LOC = V1;
NET out_a (2) LOC = R3;
NET out_a (3) LOC = R5;
NET out_a (4) LOC = T2;
NET out_a (5) LOC = P4;
NET out_a (6) LOC = R7;
NET out_a (7) LOC = P2;
```

- VHDL Code

```
-- 32 x 32 register file
-- two read ports, one write port with write enable
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity regfile is
port(
    din : in std_logic_vector(31 downto 0);
    reset : in std_logic;
    clk : in std_logic;
    write : in std_logic;
    read_a : in std_logic_vector(4 downto 0);
    read_b : in std_logic_vector(4 downto 0);
    write_address : in std_logic_vector(4 downto 0);
    out_a : out std_logic_vector(31 downto 0);
    out_b : out std_logic_vector(31 downto 0)
    );
end regfile ;


architecture register_file_arch of regfile is
    -- 32 registers in a register file, thus 0 to 31 in reg_arr
    type register_array is array(0 to 31) of std_logic_vector(din'length-1 downto din'right);
    signal reg_arr : register_array;

begin

    read: process(read_a, read_b, reg_arr)
    begin
            -- converting std vector to integer - to find the appropriate register to access
            out_a <= reg_arr(CONV_INTEGER(read_a));
            out_b <= reg_arr(CONV_INTEGER(read_b));
    end process;

    reg_file_update: process(clk, reset)
    begin

        if(reset = '1') then
            reg_arr <= (others => (others => '0'));

        elsif(clk'event and clk = '1' and write = '1') then
            reg_arr(CONV_INTEGER(write_address)) <= din;
        end if;

    end process;

end register_file_arch ;
```