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Dept. of Electronics and Electrical Communications  
Engineering**

**Third Year – Mainstream  
Analog Integrated Circuits Project 2**

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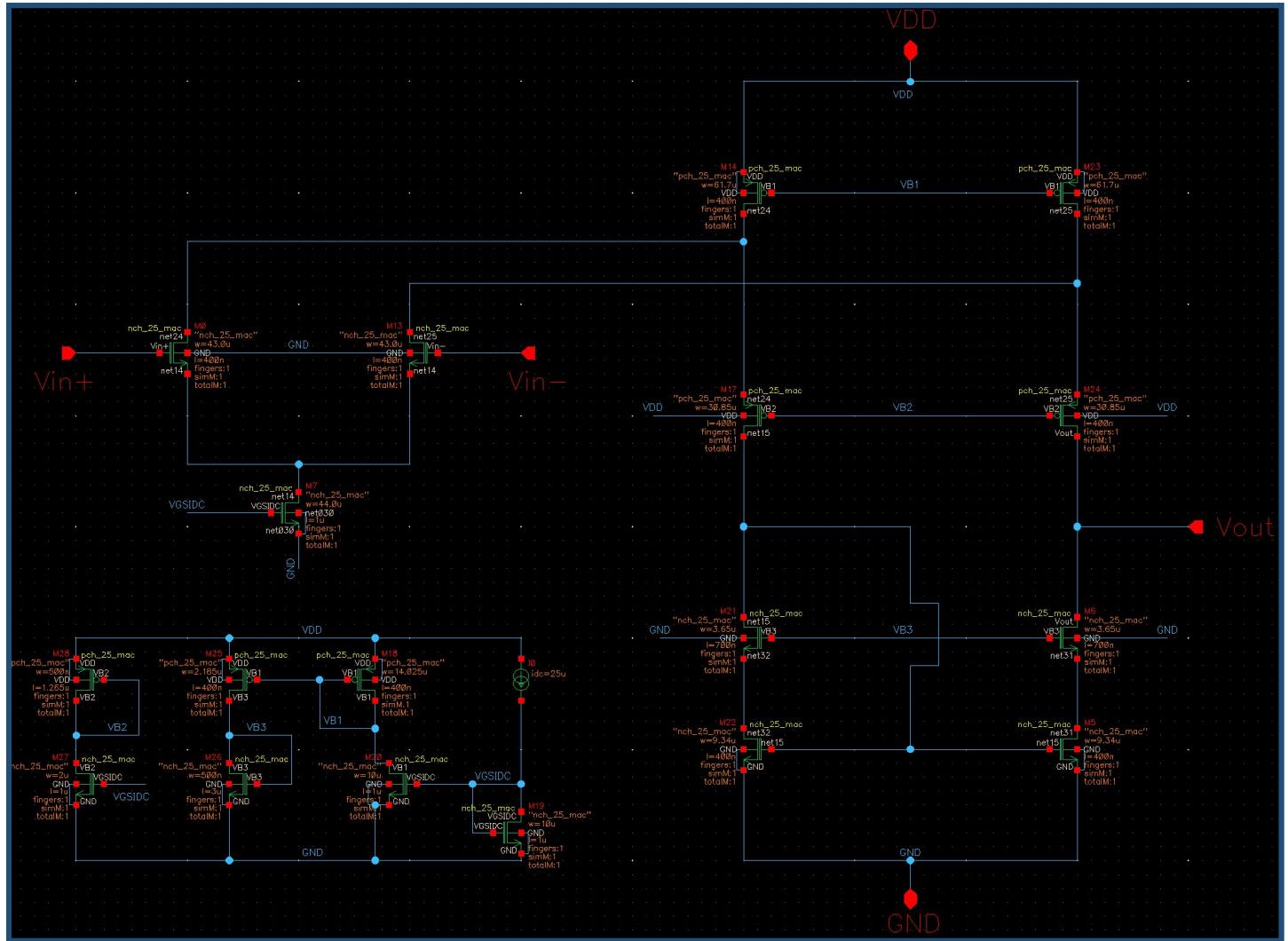
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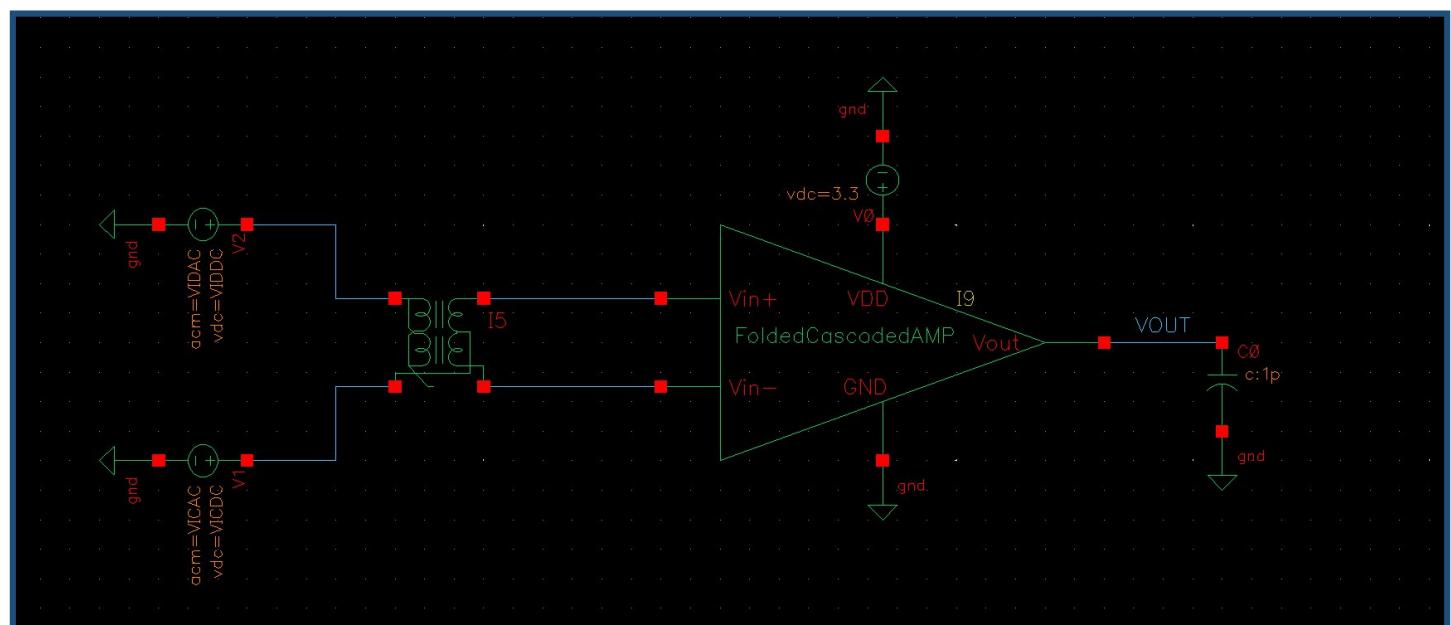
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## **1. Schematic diagrams:**



*Figure 1 Full Circuit Design.*



*Figure 2 Final Circuit Symbol.*

## 2. Design Procedure:

### ▪ Sizing:

GBW spec :

$$\text{GBW} > 150 \text{ MHz} , \quad \text{GBW} = \frac{g_m}{2\pi \cdot C_L} , \quad C_L = 1 \text{ pF}$$

$$g_m > 0.9425 \text{ mS} \quad \text{let } g_m = 0.95 \text{ mS}$$

slew rate spec :

$$\text{SR} > 100 \frac{\text{V}}{\mu\text{Sec}} , \quad \text{SR} = \frac{I_1}{C_L} , \quad C_L = 1 \text{ pF}$$

$$I_1 > 100 \mu\text{A} \quad \text{let } I_1 = 110 \mu\text{A}$$

### ❖ Input pair (M1,M2)

In designing a MOSFET, we must consider numerous constraints. However, for practical design flow in tools like Cadence, we often follow standard heuristics and expert recommendations to streamline the process.

#### 1. Choosing Channel Length (L):

For the input differential pair, we aim for a relatively small channel length (L) to minimize parasitic capacitance, while still satisfying minimum length constraints. **Chosen value: L = 400 nm.**

(This value is selected as a trade-off between performance and layout area.)

#### 2. Use of gm/ID Methodology:

In test bench simulations, absolute values of trans-conductance  $g_m$  are hard to extract accurately. However, the ratio  $\frac{g_m}{I_d}$  provides a reliable metric for sizing. From equations:  $\frac{g_m}{I_d} \approx 17.27$  (targeted = 18).

#### 3. Plotting for Analysis:

We plot the following to extract operating points :

- $\frac{g_m}{I_d}$  vs  $V_{gs}$
- $i_d$  vs  $V_{gs}$  ,  $r_{out}$  vs  $V_{gs}$  ,  $V_{d,sat}$  vs  $V_{gs}$

Reference width used in initial simulations: **W=10 μm.**

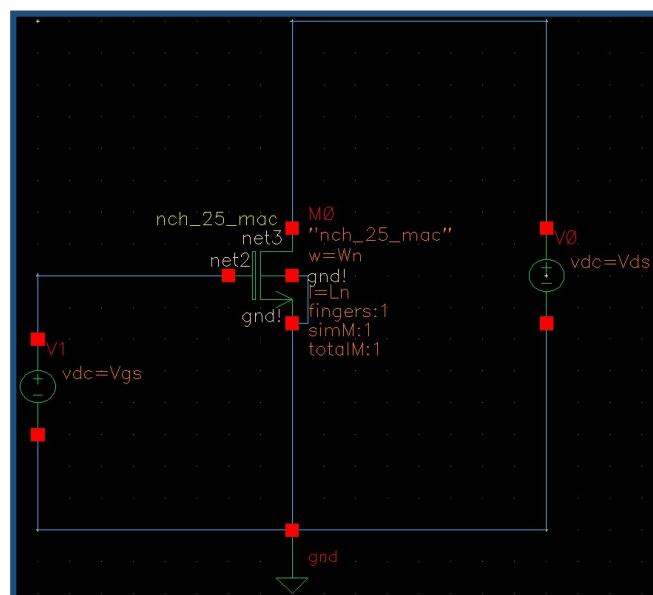


Figure 3 NMOS test-bench.

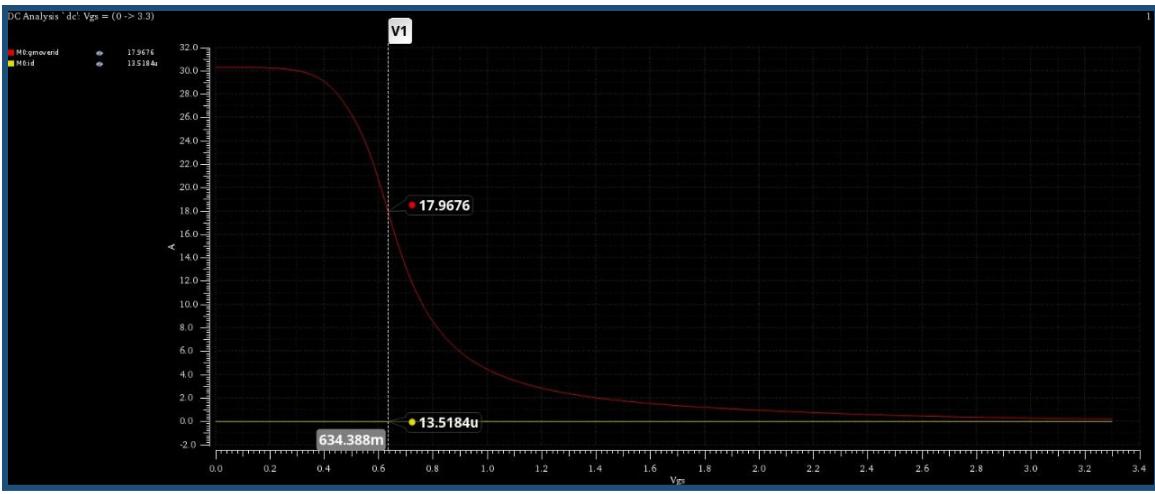


Figure 4 NMOS 1 and 2 before adjusting  $W$ .

#### 4. Initial Operating Point Extraction:

From plots, we determine:

$$V_{gs} = 634 \text{ mV}$$

$$I_d = 13.42 \mu\text{A} \text{ at } W=10 \mu\text{m}.$$

#### 5. Scaling Width ( $W$ ):

Given that our design requires:

$$I_d \text{ target} = 55 \mu\text{A}$$

$$W_{new} = \frac{I_{d, \text{target}}}{\frac{I_d}{W_{old}}} = \frac{55 \mu\text{A}}{\frac{13.42 \mu\text{A}}{10 \mu\text{m}}} = 41 \mu\text{m}$$

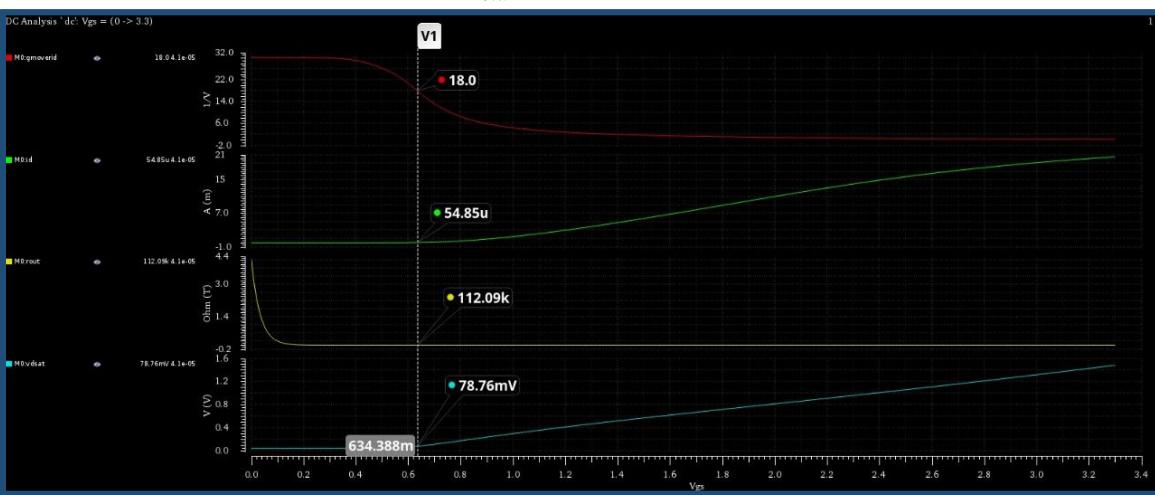


Figure 5 NMOS 1 and 2 after adjusting  $W$  and got the specs.

#### 6. Final Simulation Results (After Scaling):

After adjusting  $W$  and rerunning the simulation:

$$I_d = 54.45 \mu\text{A}, V_{d,sat} = 78.57 \text{ mV}, r_{out} = 112.74 \text{ k}\Omega$$

And to follow instructions we increase the  $V_{d,sat}$  by 100 mV for improving  $r_{out}$  to be  $V_{d,sat} = 178.57 \text{ mV}$ .

## ❖ Upper PMOS current source pair(M3,M4)

### 1. Assumption:

- $r_{o4} = r_{o2} = 112.74\text{k}\Omega$  ,  $I_d = 110 \mu\text{A}$
- However,  $r_o$  varies significantly with VDS , so we instead choose a value of  $g_{m4}$ .  $r_{o4} = 75$
- Which is more stable.
- $L_4 = 400 \text{ nm}$  ,  $V_{d,sat} = (3.3 / 4) \text{ V}$  dividing the VDD for the 4 MOS.

### 2. Simulations:

- $g_m, r_o$  vs  $V_{gs}$  ,  $i_d$  vs  $V_{gs}$
- $i_d$  vs  $V_{gs}$  ,  $r_{out}$  vs  $V_{gs}$  ,  $V_{d,sat}$  vs  $V_{gs}$

Reference width used in initial simulations: **W=10 μm**.

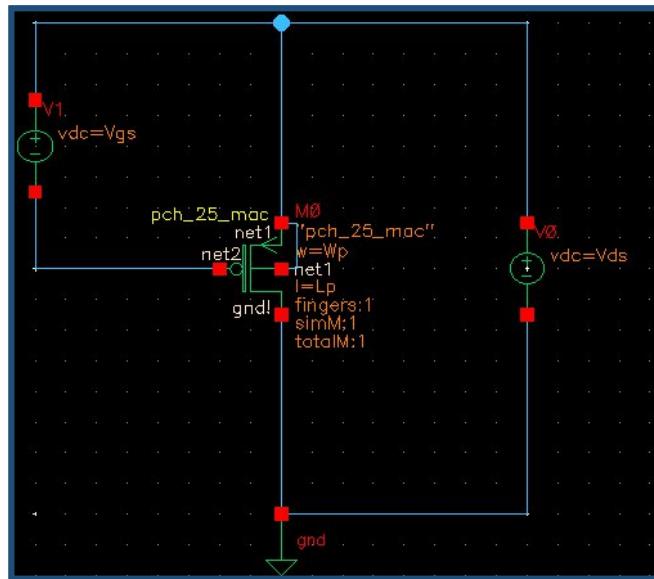


Figure 6 PMOS test-bench.

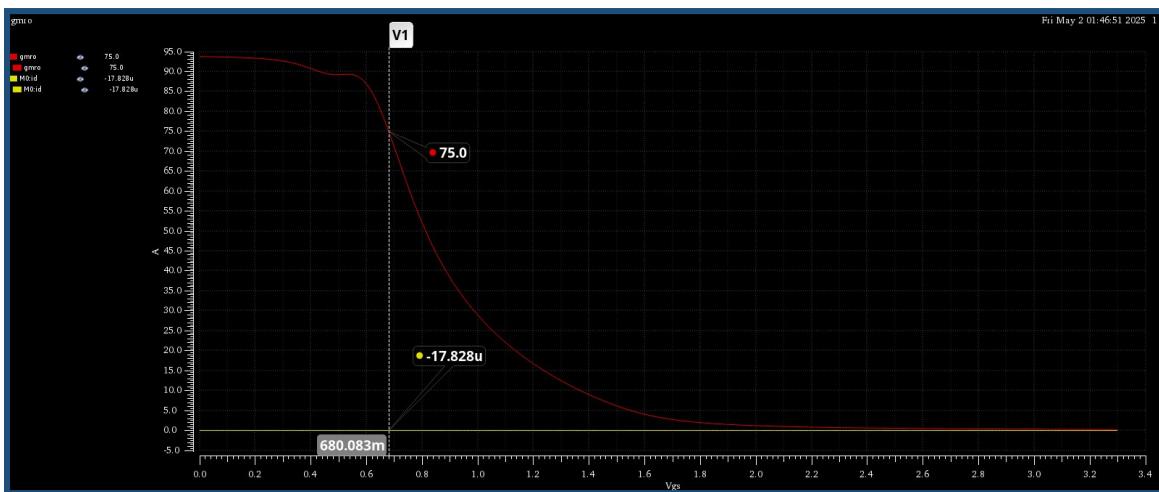


Figure 7 PMOS 3 and 4 before adjusting W.

### 3. From simulation results:

- $g_m \cdot r_o = 80$  ,  $V_{gs} = 680.1 \text{ mV}$  ,  $I_d = 17.83$

$$W_{new} = \frac{\frac{I_d, target}{I_d}}{\frac{W_{old}}{10 \mu\text{m}}} = \frac{\frac{110 \mu\text{A}}{17.83 \mu\text{A}}}{\frac{10 \mu\text{m}}{10 \mu\text{m}}} = 61.7 \mu\text{m}$$

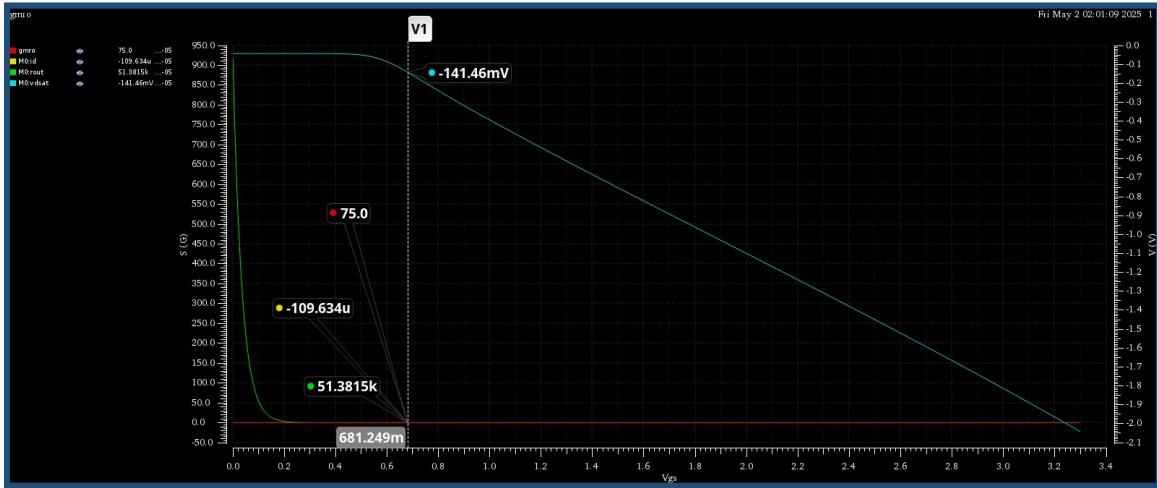


Figure 8 PMOS 3 and 4 after adjusting W.

So final values for PMOS 3 and 4 is:

- $I_d = 109.6 \mu\text{A}$ ,  $V_{d,sat} = 141.5 \text{ mV}$ ,  $r_{out} = 51.83 \text{ k}\Omega$

And increase  $V_{d,sat}$  also to be  $241.5 \text{ mV}$ .

For the rest of the transistors we made the same with small variations but there is no space to put them and maintain 15 pages for raw report, So we have uploaded it here to view the full procedure: [Link](#).

#### Final Table of values and specs for all MOS:

Mos	W	L	$I_d$	$V_{gs}$	$V_{d,sat}$	$r_{out}$
<b>Input pair</b>	41 $\mu\text{m}$	400 nm	54.45 $\mu\text{A}$	634 mV	178.57 mV	112.74 K $\Omega$
<b>Upper PMOS current source pair</b>	61.7 $\mu\text{m}$	400 nm	109.6 $\mu\text{A}$	680.1 mV	241.5 mV	51.38 K $\Omega$
<b>Cascade PMOS pair</b>	30.85 $\mu\text{m}$	400 nm	55 $\mu\text{A}$	681.249 mV	241.649 mV	102.46 K $\Omega$
<b>Cascade NMOS pair</b>	3.65 $\mu\text{m}$	700 nm	54.75 $\mu\text{A}$	931.26 mV	382.45 mV	290.95 K $\Omega$
<b>Lower NMOS pair</b>	9.34 $\mu\text{m}$	400 nm	54.9 $\mu\text{A}$	740.118 mV	236.48 mV	123.37 K $\Omega$

These are the shared values that we have got from the simulation, there is other values like  $g_m$  but it is not always explicitly mentioned directly check the procedure: [Link](#).

We needed  $g_m$  in noise calculations and that where we got them.

## ▪ Biasing:

As for our Biasing circuit we have one ideal current source ( $25\mu A$ ) to bias 4 parts of our design(**I1**, **VB1**, **VB2**, **VB3**):

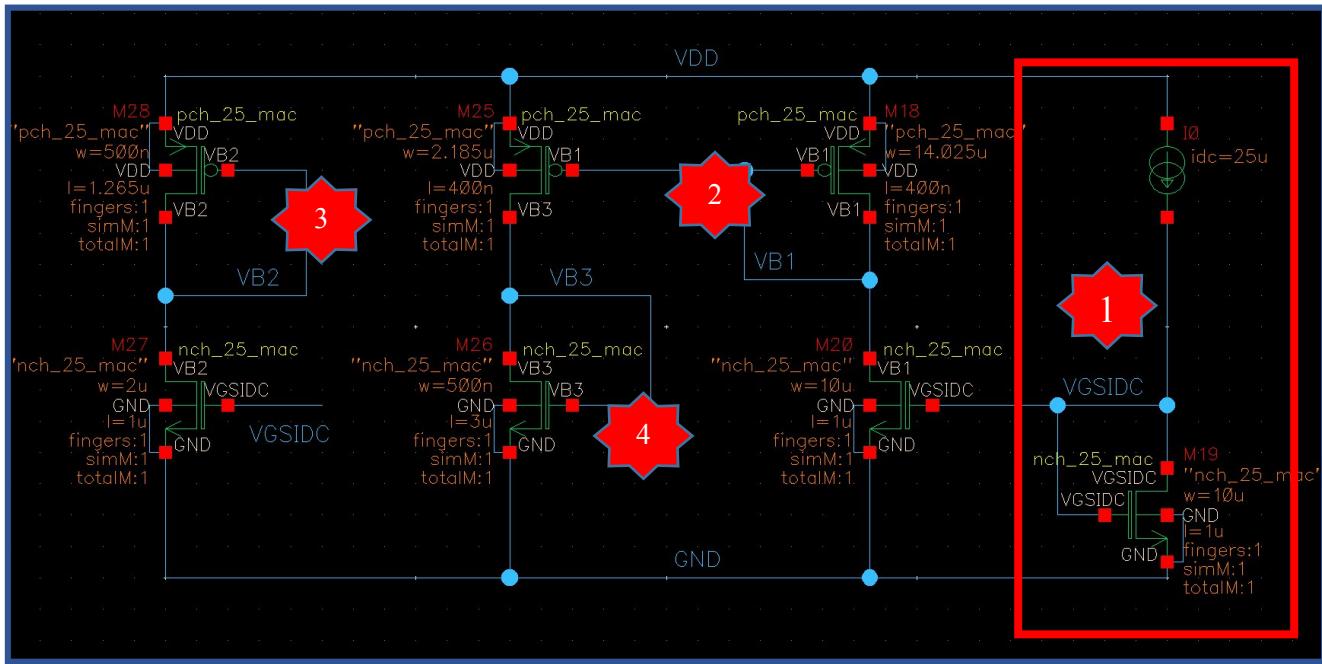


Figure 9 Biasing Circuit highlighting the current source.

From this current source we got **VGSIDC** to generate current by mirroring to different parts of the circuit:

1. The current source under the Input pair used Current mirroring with ratio 4.4 between widths to generate the designed current  $I_1 = 110\mu A$ .

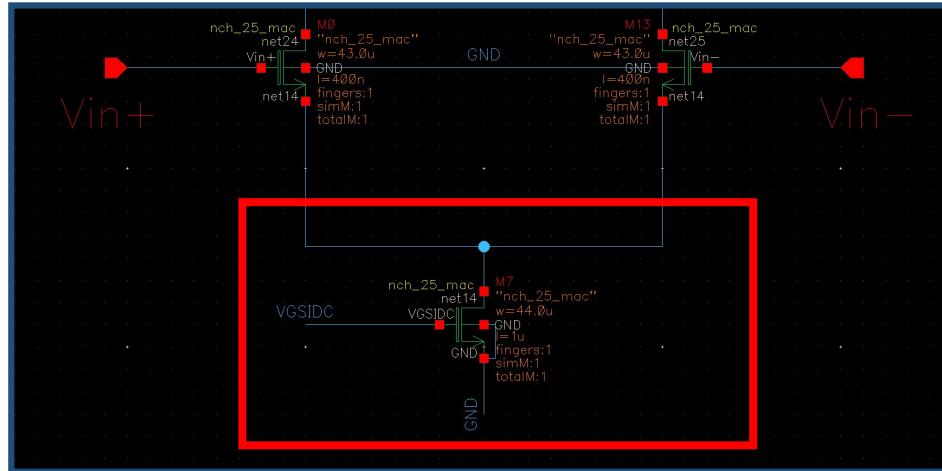


Figure 10 II Biasing.

2. As for **VB1** it is also a simple current mirror but we need PMOS to do so, so we copied the  $25\mu A$  to the next branch and from this branch added a PMOS with a ratio of 4.4 also to generate  $I_3 = 110\mu A$ .
3. **VB2** is different, it needs an absolute voltage of value 2V to correctly bias the cascaded current mirror mosfets meaning 5 and 6. To achieve this value we copied the current to another branch first and then added a diode connected PMOS to generate this voltage so we went to the test bench circuit fixed  $V_{BS} = V_{DS} = 2V$  then swept  $L$  from  $\mu$  to  $\mu$ , and searched where does get a current of the mirrored current to this new branch which happens to be  $5.39\mu A$  after DC run (lowest current possible for lowest Power consumption).

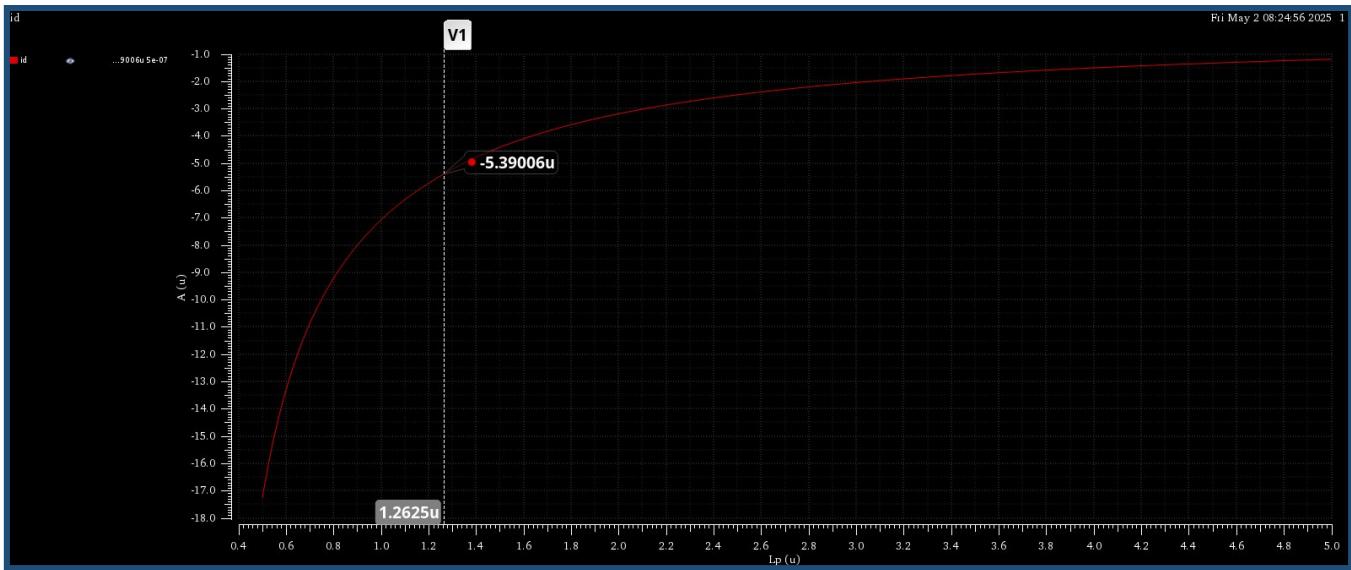


Figure 11 Length Sweep to generate VB2

Found the valid Length =  $1.2625\mu$  for the smallest Width =  $0.5\mu$  for the PMOS to generate the needs **VB2** = 2V. Theoretically, it should be  $VDD - Vdsat4 + Vgs6 = 2.3$  but after running with other variances got the perfect value to be 2V.

4. As for **VB3** it is the same as **VB2** but with NMOS. So, doing the same copying the current to a new branch from any PMOS like the one we just used for **VB1** and adding a diode connected NMOS to generate the absolute voltage needed to bias **VB3** = 1.167 V. Running the test bench fixing the  $VBS = VDS = 1.167V$  and fixing Width to minimum =  $0.5\mu$  and sweeping L.

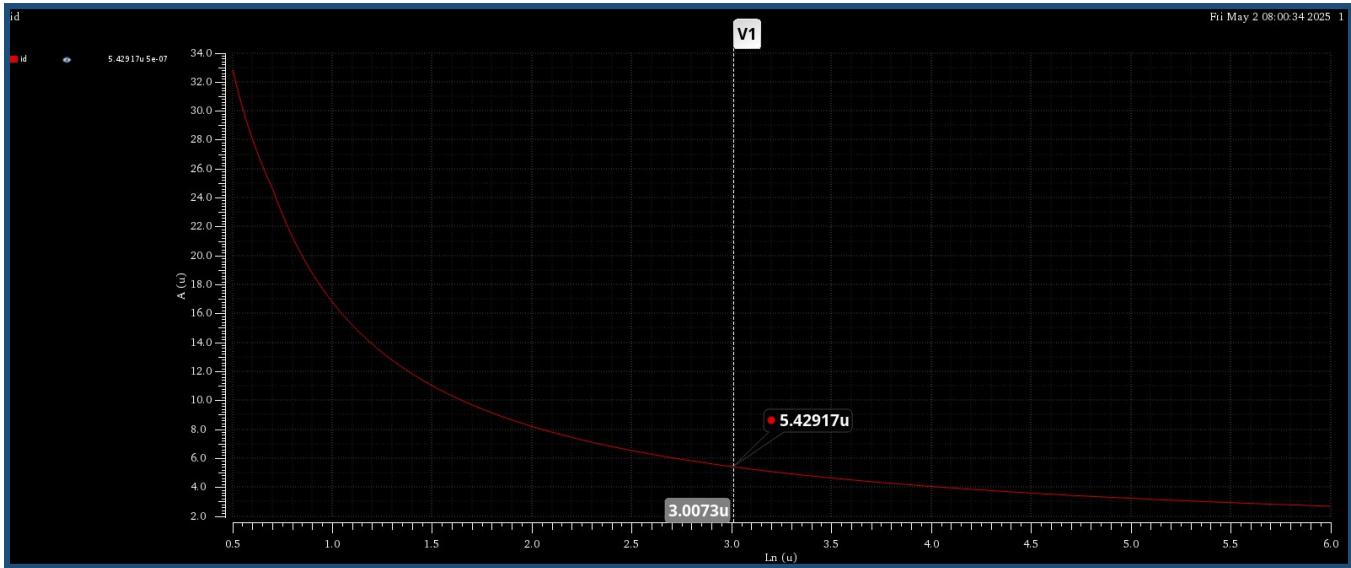


Figure 12 Length Sweep to generate VB3.

Found the valid Length =  $3\mu$  for the smallest Width =  $0.5\mu$  for the NMOS to generate the needs **VB3** = 1.167V which matched the Theoretical Value with good performance.

### 3. Simulations:

- Simulate the circuit (DC analysis - save operating point, AC analysis):
- Print all transistor operating point information (DC):

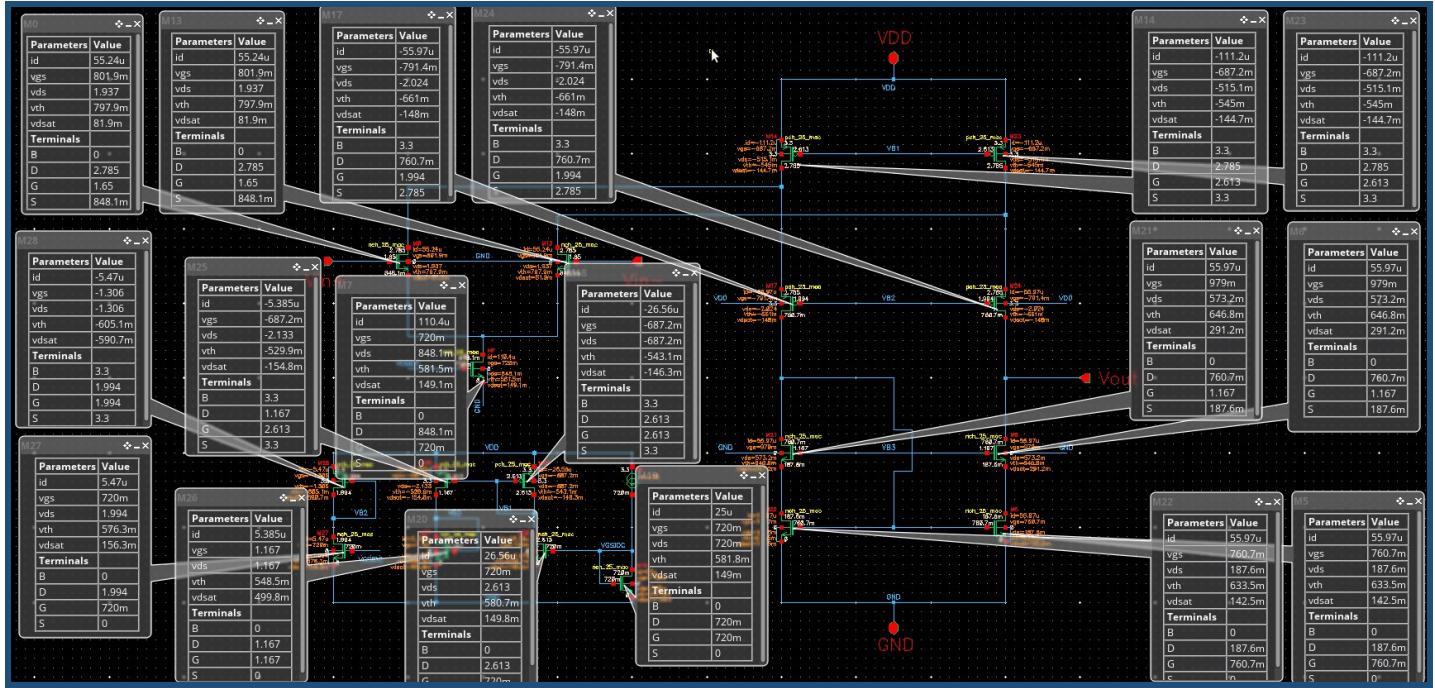


Figure 13 All Transistor Operating Point Information (DC)

- Plot the gain and phase versus frequency (AC). Show GM and PM:

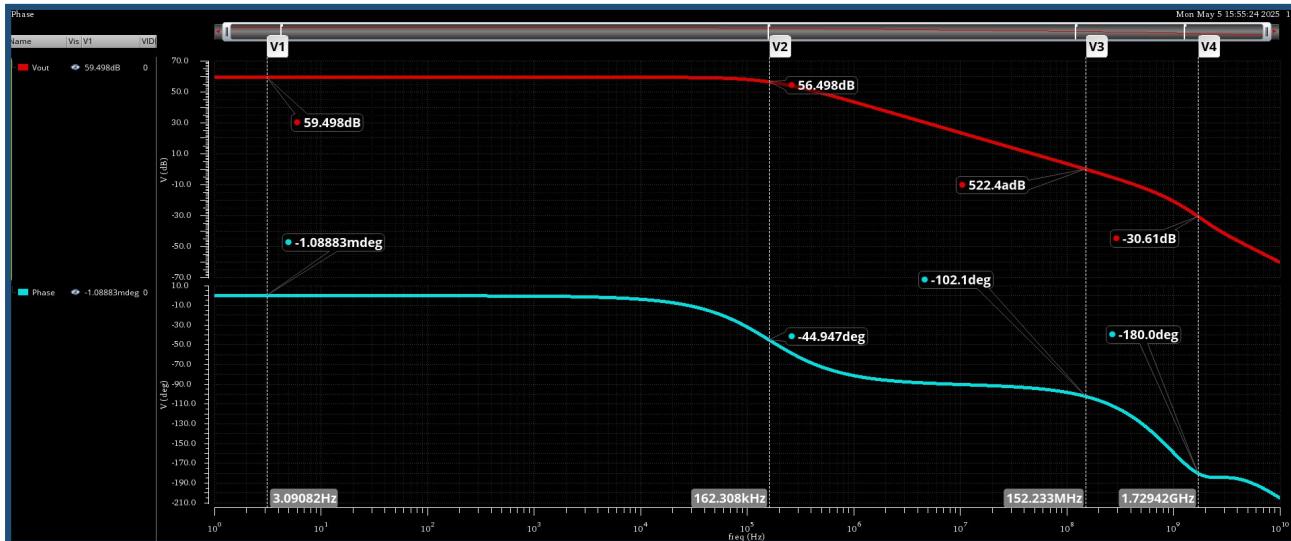


Figure 14 Gain and Phase Versus Frequency (AC).

- From the figure we got  $GM = -(-30.615\text{dB}) = 30.615\text{dB} > 12\text{dB}$ ,  $PM = 180 - (-102) = 78\text{deg} > 60\text{deg}$ . Also the Gain(ADC) =  $59.498\text{dB} > 58\text{dB}$ .
- which all achieved the requirements. The results also matches the values from the simulation direct functions. Also the  $GBW = 153.6\text{M} > 150\text{M}$ .

PM	77.95
GM	30.61
BW	162.3k
GBW	153.6M

## – Plot the common-mode rejection ratio (CMRR):

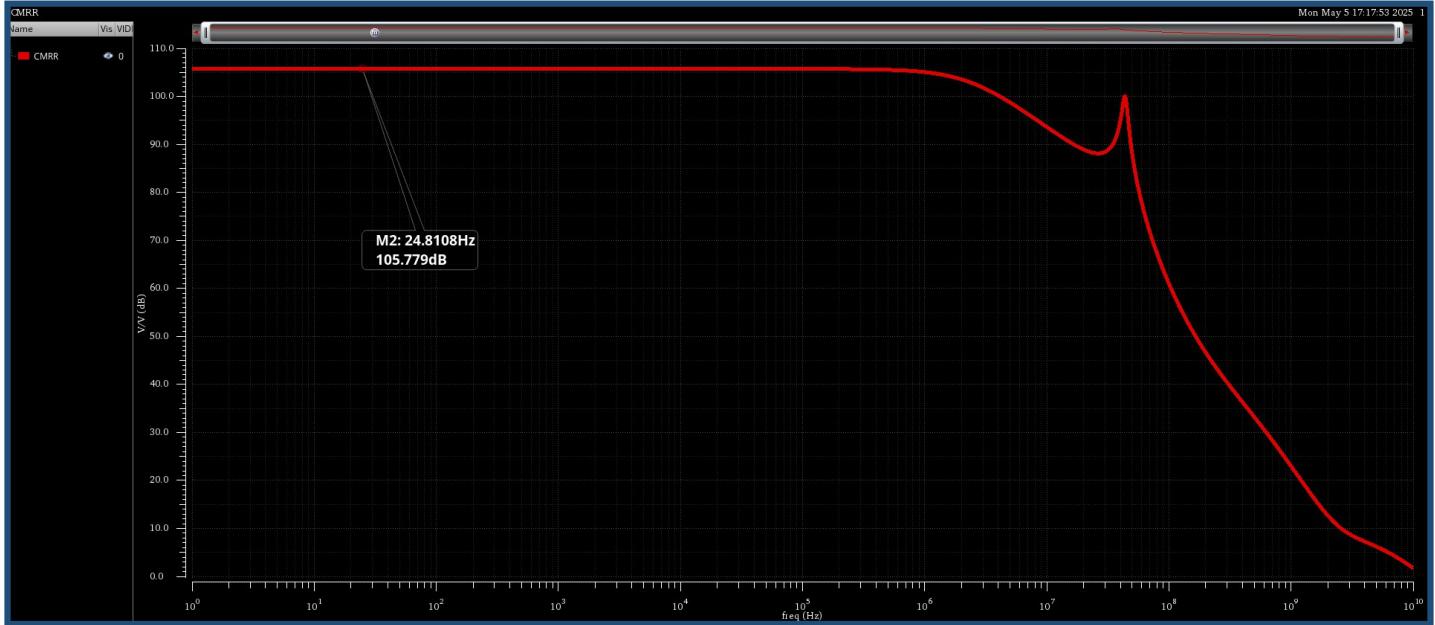


Figure 15 common mode rejection ratio (CMRR)

- Using xf analysis we got CMRR and PSRR.

CMRR represents how well the circuit rejects the common mode variations by dividing the differential gain by the common mode gain. Inside BW, we have a CMRR of **105.78dB** which is great.

## – Plot the power supply rejection ratio (PSRR):

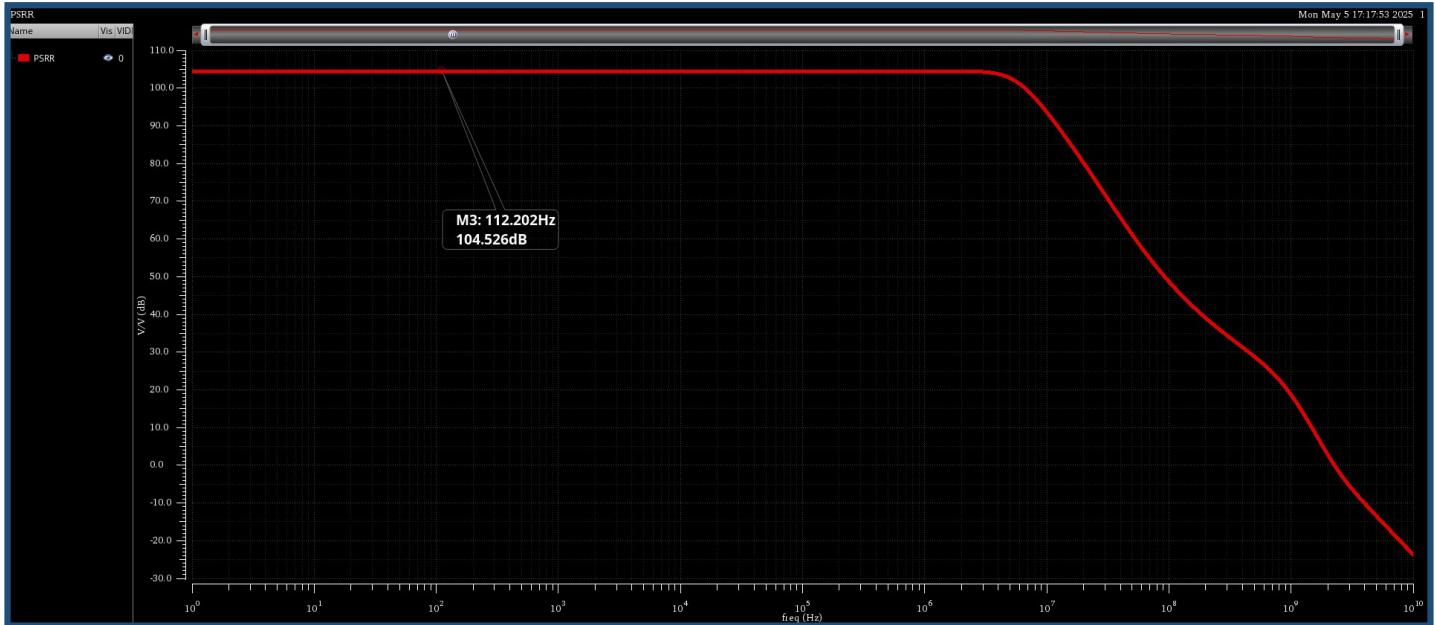


Figure 16 Power Supply Rejection Ratio (PSRR) Due To Differential Input.

PSRR: describes the ability of a circuit to suppress any power supply variations from passing to its output signal. Calculated using the equation  $\text{PSSR}_{\text{linear}} = \frac{\Delta V_{DD}}{\Delta V_i}$ , low PSRR indicates low efficiency. In the simulation we have measured PSSR due to differential input which is our main focus on and got a great value of **104.526dB**.

- Place the op-amp in a unity feedback (Buffer) configuration:

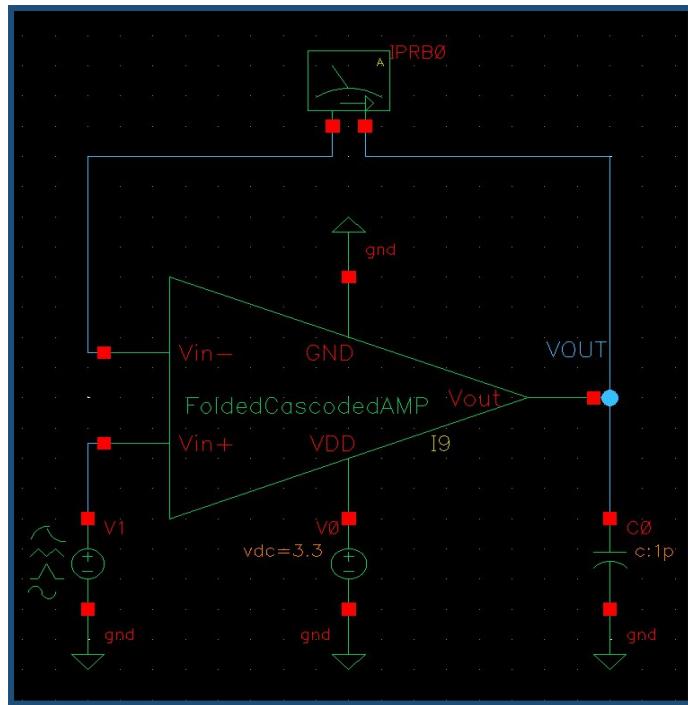


Figure 17 Buffer connection.

- Plot STB gain and phase versus frequency (AC):

and calculate loop gain and PM and compare with previous open loop gain and PM:

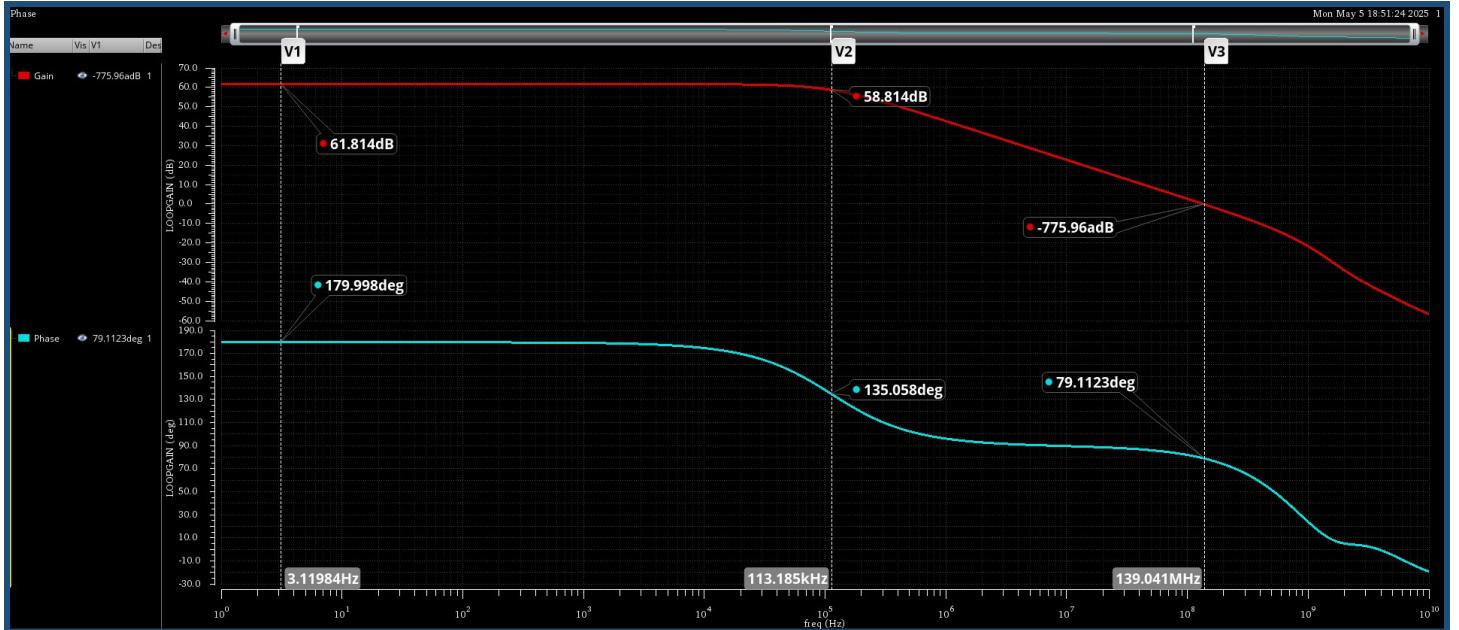


Figure 18 Gain and Phase of Closed Loop buffer.

As shown in figure 12, The Loop gain and PM is almost the same as open loop gain

$$\text{ADC} = 61.81\text{dB}, \text{PM} = 79.1123\text{deg}$$

Which is predictable as the feedback gain ( $H = 1$ ) so no big changes happens and the whole phase graph is increased by 180deg due to negative feedback so no need to add it to get the correct PM.

- Plot the DC-gain versus Vout (report when DC-gain drops by 10dB to verify specifications) | Swing:

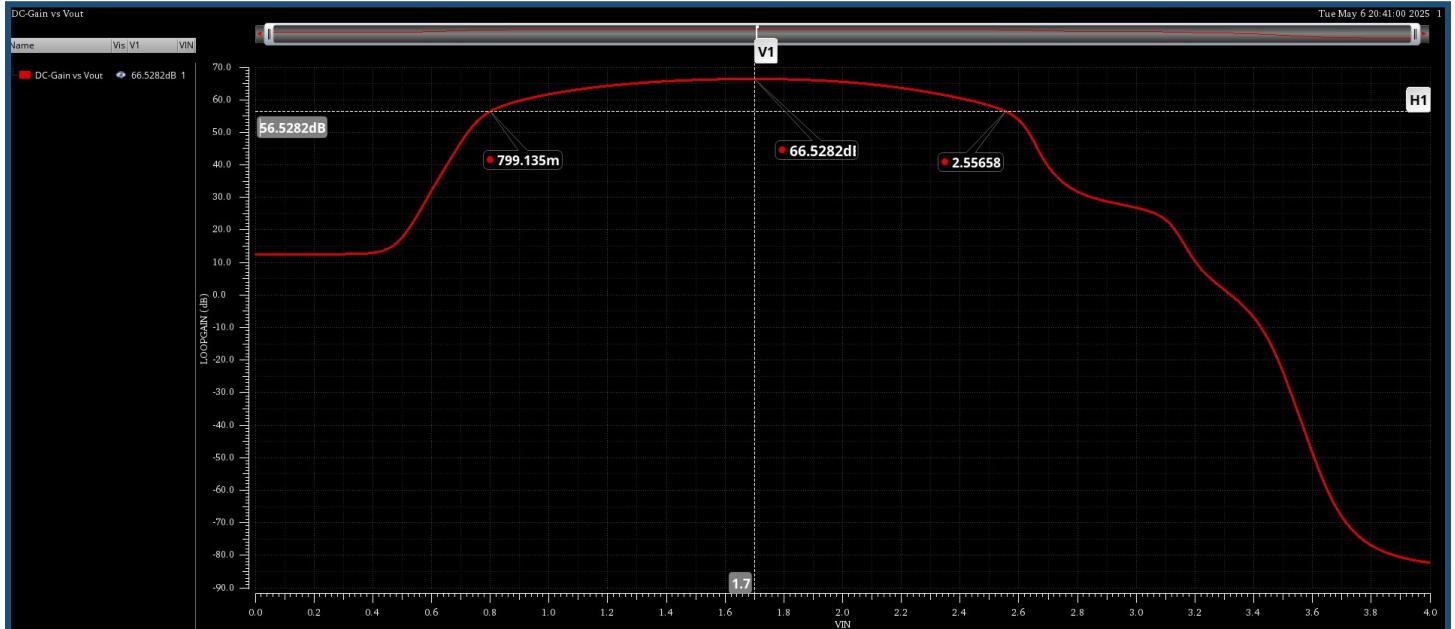


Figure 19 DC-gain versus Vout to show Swing of output.

As shown in the figure the max gain is 66.5282dB so to get the swing with the specifications mentioned to be under the max with 10dB then the swing is:

$$V_1 - V_2 = 2.5565 - 0.799135 = 1.757 \text{ VPP} > 1.5 \text{ VPP}$$

So as shown the value meets the requirements.

- Plot closed-loop (CL) frequency response. What is the ACL and BWCL?

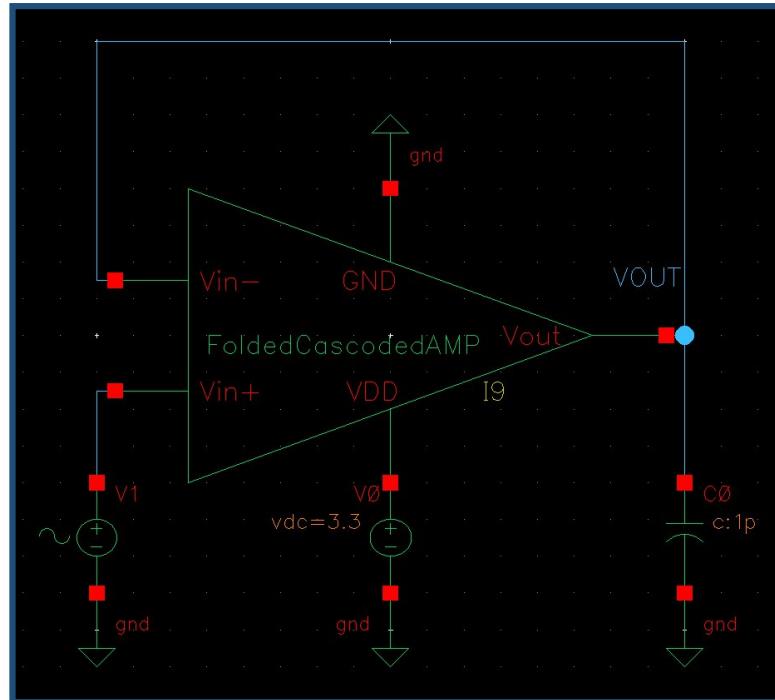


Figure 20 Closed loop circuit without the probe.

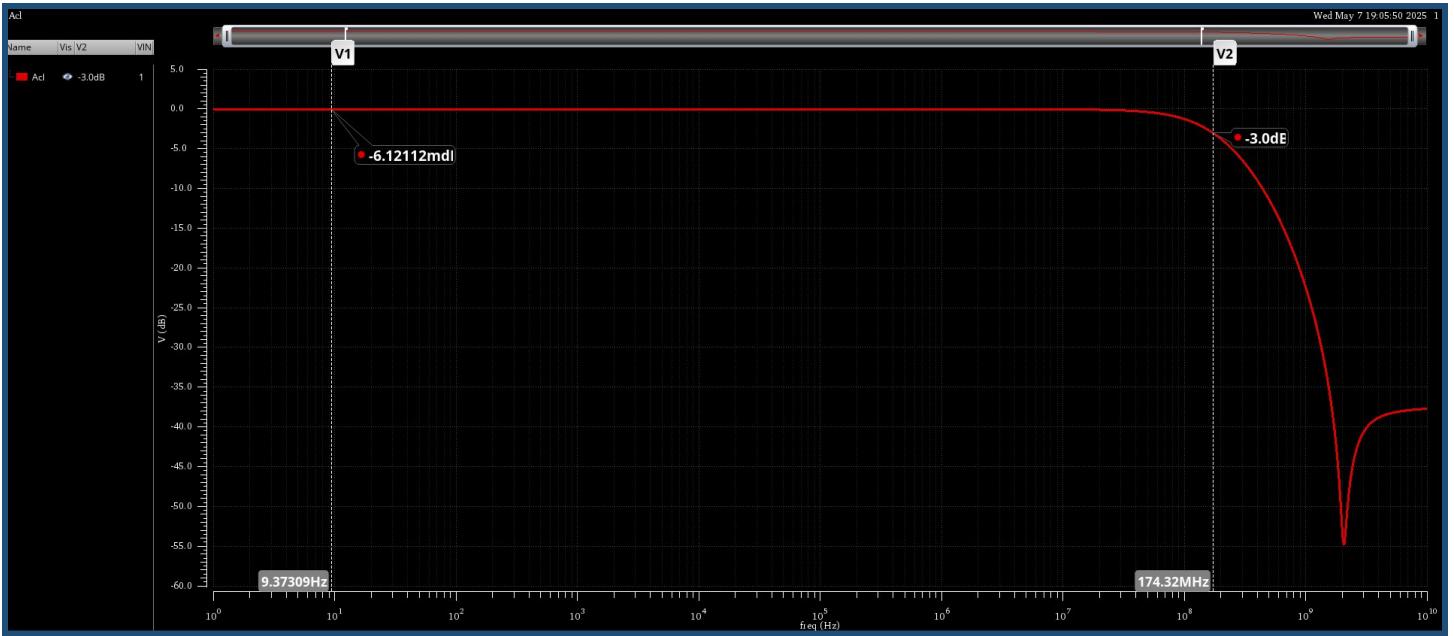


Figure 21 Gain and Band Width of Closed Loop.

As shown in the circuit and as expected the gain is 0dB which is 1 in linear as it is a buffer as the new gain is  $\frac{A}{1+HA}$  where A is the open loop gain and H is the unity feedback so nearly equals 1, and the band width is increased to maintain the relation between gain and bandwidth:

$$A_{cl} = 0\text{dB}, \quad BW_{cl} = 174.32\text{MHz}$$

- Simulate input-referred noise and tabulate top 4(pairs) contributors @10MHz:

Device	Param	Noise Contribution	% Of Total
/I9/M14	id	4.67219e-09	26.61
/I9/M23	id	4.63738e-09	26.22
/I9/M13	id	3.36368e-09	13.79
/I9/M0	id	3.35931e-09	13.76
/I9/M22	id	2.60581e-09	8.28
/I9/M5	id	2.60225e-09	8.26
/I9/M5	fn	7.71148e-10	0.73
/I9/M22	fn	7.67152e-10	0.72

Spot Noise Summary (in V/sqrt(Hz)) at 10M Hz Sorted By Noise Contributors  
 Total Summarized Noise = 9.05661e-09  
 Total Input Referred Noise = 9.07788e-09  
 The above noise summary info is for noise data with VIN = 1.0

Figure 22 Noise analysis showing top 4 contributors.

As shown in the Noise figure we have got a total noise =  $9.1 \text{ nV}/\sqrt{\text{Hz}}$  which meets the requirements  $< 30 \text{ nV}/\sqrt{\text{Hz}}$ . As for the top contributors they are the input pair and the top PMOS current source and the cascade bottom NMOS. We can minimize the input referred noise by designing the input pair with higher  $g_m$  but not needed as it meets the requirements. To calculate the thermal noise theoretically –as it is the most contributor- knowing the top contributors:

$$V_n^2 = 8KT * \frac{2}{3} \left( \frac{1}{g_{m-\text{input}}} + \frac{g_{m-p-\text{upper}}}{(g_{m-\text{input}})^2} + \frac{g_{m-n-\text{lower}}}{(g_{m-\text{input}})^2} \right) = 7333.549 * 10^{-20} \text{ V}^2/\text{Hz}$$

$$V_n = 8.56 \text{ nV}/\sqrt{\text{Hz}}$$

Which is very near the actual, not exact due to neglecting other components.

## – Simulate the slew rate and verify the specifications:

To simulate slew rate we should apply pulse input with effective voltages, chose the limits of the Vout swing 0.8 to 2.5 V.

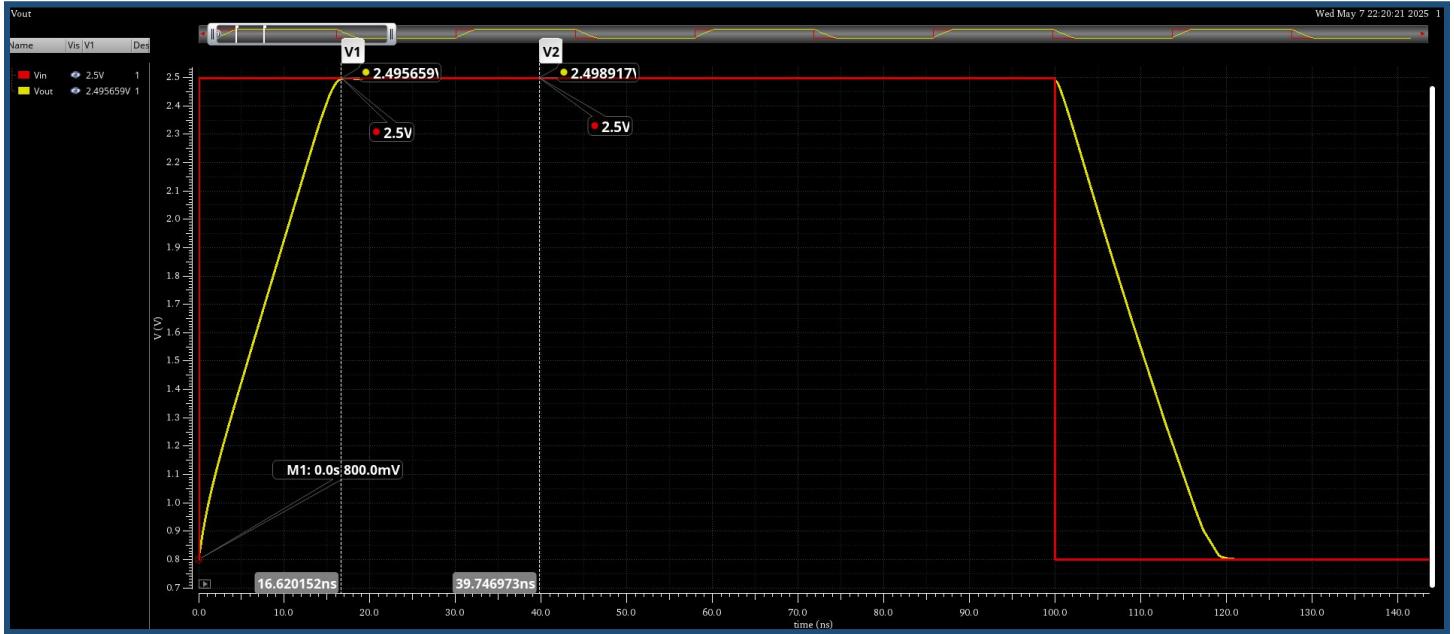


Figure 23 Slew Rate of the Amplifier.

As shown the values we now that  $SR = \frac{\Delta V}{\Delta t} = \frac{2.495649 - 0.8}{16.62ns - 0} = 102.025 \text{ V}/\mu\text{s} > 100 \text{ V}/\mu\text{s}$ . Achieved the Requirement.

## – Sine input signal of 1Vpp @ 10 MHz and plot Vout (Add proper input DC value):

A proper DC input should pass the full sin wave without clipping, and we have a range of swing of 1.7VPP which is much greater than needed, so ideally we get the middle point to achieve symmetry so  $DC = \frac{2.5 + 0.8}{2} = 1.65V$ .

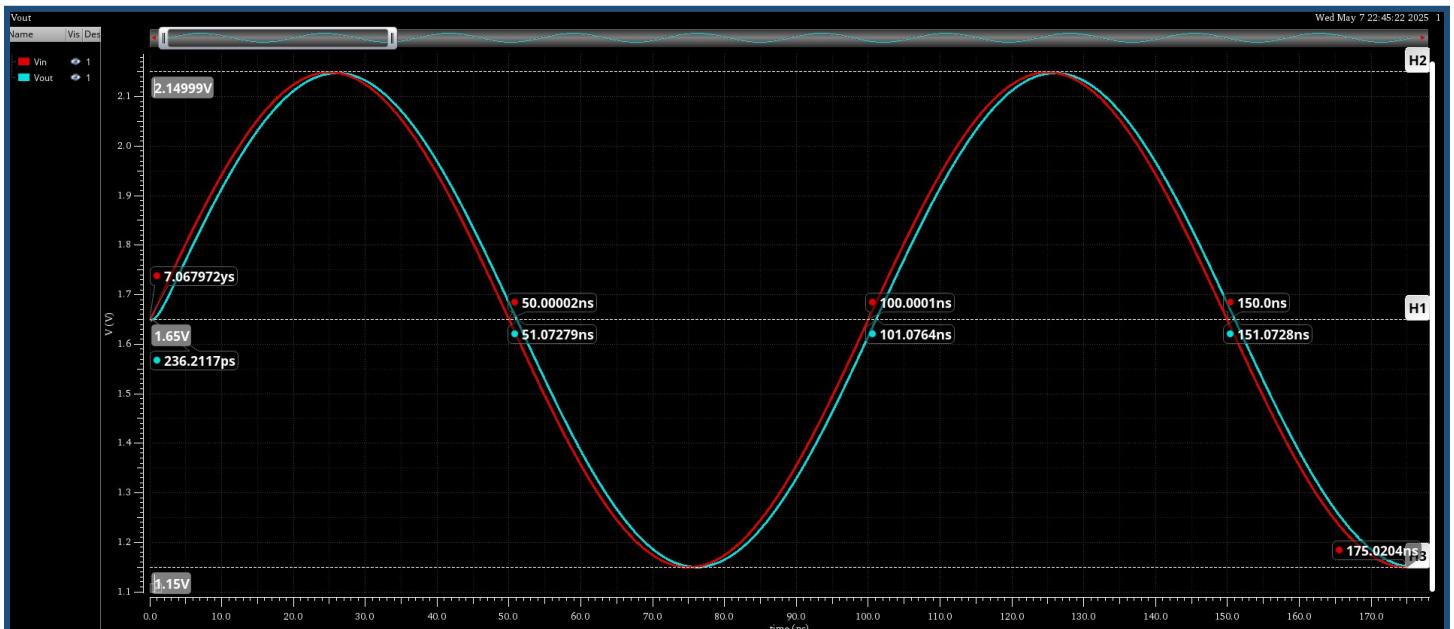


Figure 24 Sin input response.

- Plot DFT (in dB) and calculate harmonic distortion (HD<sub>2</sub>, HD<sub>3</sub>, and THD) in dB:



Figure 25 DFT of the sin signal output.

From DFT figure, knowing that 10MHz represents the fundamental frequency, **HD<sub>2</sub> @ 20MHz = -64.232dB, HD<sub>3</sub> @ 30MHz = -73.239dB**, And the fundamental one is **-6.04dB**.

$$THD = \sqrt{\frac{HD_2^2 + HD_3^2}{fundmental^2}} = -57.6778 \text{ dB}$$

– Plot Vout for a small step input of 100mV, Calc (FGE and settling time):

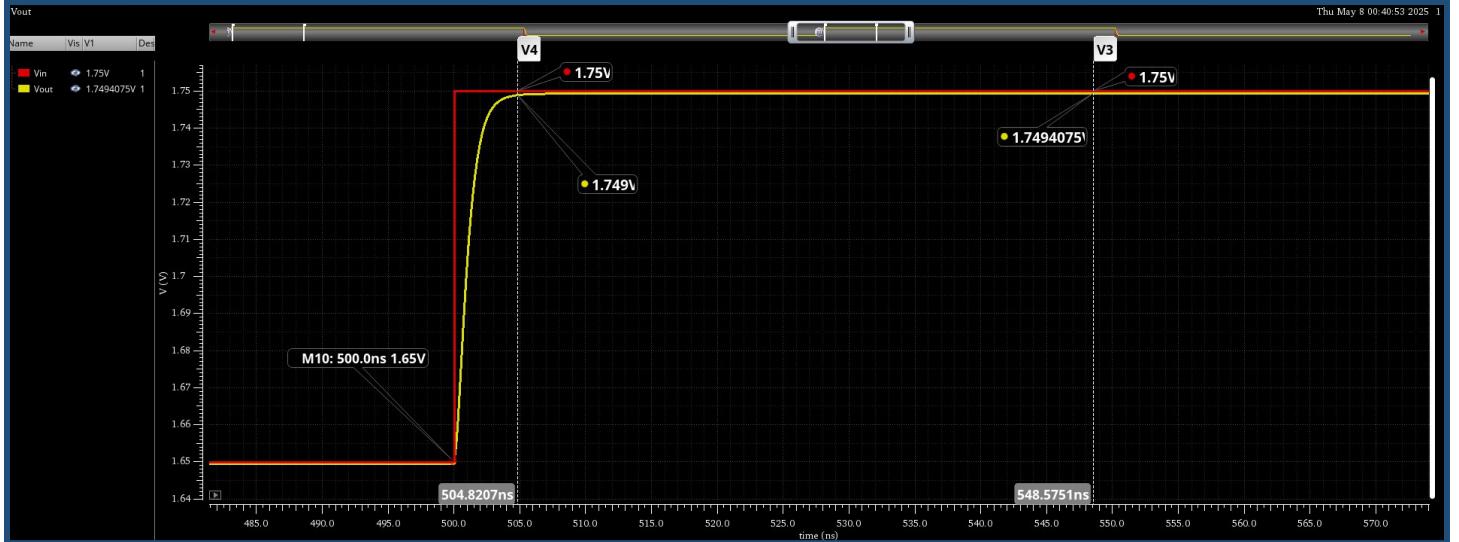


Figure 26 Small step input response.

From vertical line V3 get the  $FGE = \frac{1.75 - 1.7494075}{1.75} = 0.0338\%$ , and theoretically we can get it by the loop gain from the stability response  $LG = 61.81\text{dB}$  and  $FGE = \frac{1}{LG} = 0.081\%$ . well, this is a big error of 62.5% but still both FGE are small.

As for the settling time we can get it from the graph using the time points at 99% of change which is  $504.8207\text{ns} - 500\text{ns} = 4.8207\text{ns}$ , And theoretically we can get it using the equation  $\frac{4.6}{2\pi\beta GBW} = 5.25\text{ns}$ .

which is very close with the error 8.17% only.

## 4. Specs Table Verification

SPEC	REQUIRED	ACHIEVED
ADC	>58dB	<b>59.498dB</b>
GBW	>150M	<b>153.6M</b>
Slew Rate	>100V/ $\mu\text{s}$	<b>102.025V/<math>\mu\text{s}</math></b>
Output Swing	>1.5VPP	<b>1.757VPP</b>
Noise	<30nV/ $\sqrt{\text{Hz}}$	<b>9.1nV/<math>\sqrt{\text{Hz}}</math></b>
PM	>60deg	<b>78deg</b>
GM	>12dB	<b>30.165dB</b>