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Digital Design and Computer Architecture (CIE 239)

Assignment 3

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1. If all the inputs P, Q, R, S and T are applied simultaneously and held constant. Determine the propagation delay and contamination delay of the following circuit. Use the gate delays given. the XOR gate, AND gate and multiplexer (MUX) are 4 ns, 2 ns and 1 ns, respectively.

   Solution.

$$Pd = Pd_{\text{XOR}} + Pd_{\text{MUX}} + Pd_{\text{AND}} + Pd_{\text{MUX}} = 4 + 1 + 2 + 1 = 8 \text{ ns} \tag{1}$$
$$Cd = Cd_{\text{AND}} + Cd_{\text{MUX}} = 2 + 1 = 3 \text{ ns}. \tag{2}$$

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2. Write a minimized Boolean equation for the function performed by the circuit and Implement the function using a 2:1 multiplexer and other logic gates.

   Solution.

s_1	s_0	out
0	0	i_0
0	1	i_1
1	0	i_2
1	1	i_3

Table 1

$$\text{out} = \overline{s_1 s_0} i_0 + \overline{s_1} s_0 i_1 + s_1 \overline{s_0} i_2 + s_1 s_0 i_3. \tag{3}$$

   $\implies$ when $s_1 = 0$, the output of m_1 is selected. When $s_1 = 1$, the output of m_2 is selected.

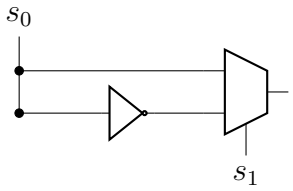

Figure 1

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3. Given the input waveforms shown in figure below, sketch the output Q of an SR latch.

Solution.

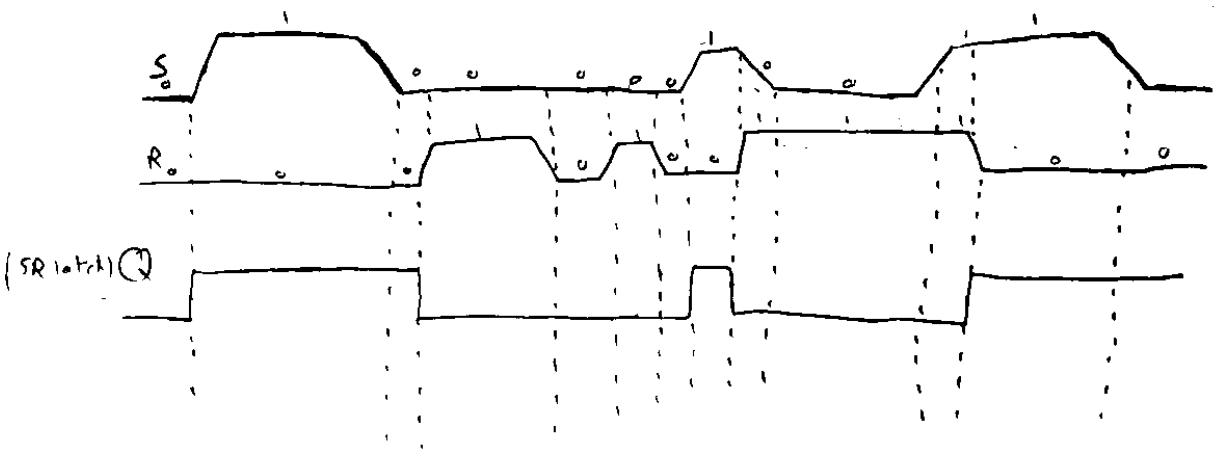

Figure 2

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4. Given the input waveforms shown in figure below, sketch the output, Q, of D latch and D flip-flop.

Solution.

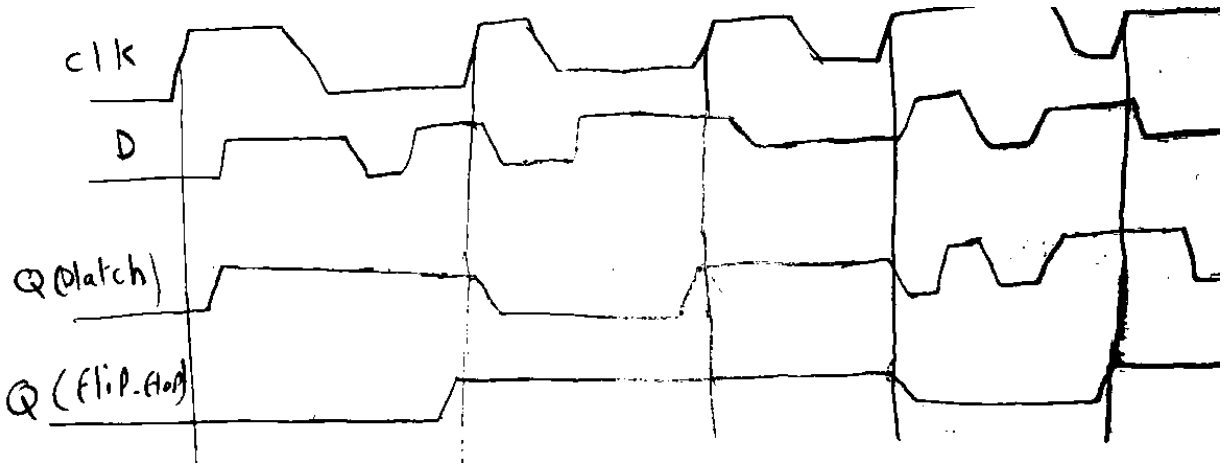

Figure 3

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5. The following characteristic table describes a storage element A–B

(a) Write the characteristic equation for the storage element A–B.

Solution.

$$Q_{n+1} = aL\overline{Q}_n + \overline{L}Q_n \tag{4}$$
$$S = aL\overline{Q} \tag{5}$$
$$R = LQ. \tag{6}$$

■

(b) Implement the A–B storage element using additional gates and an S–R Latch. Show your schematic diagram and derivation process.

Solution.

a	L	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	0	0	X
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

Table 2

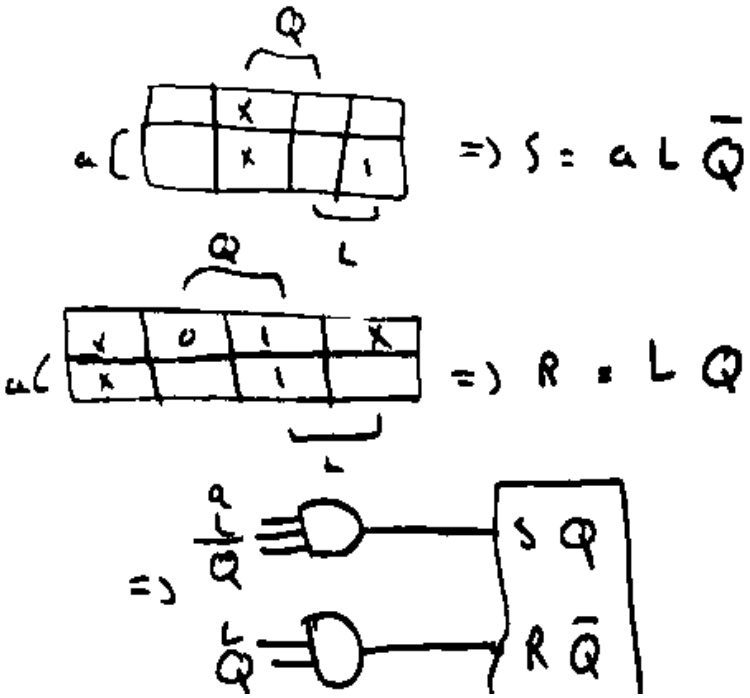

Figure 4

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6. Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter.

Solution.

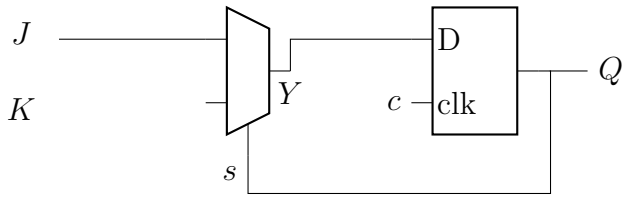

Figure 5

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7. Design and Simulate a HDL Code for D-flip flop with an active-high enable signal.

```
module d_flip_flop (
  input wire D,
  input wire EN,
  input wire CLK,
  output reg Q
);

always @(posedge CLK) begin
  if (EN) begin
    Q <= D;
  end
end
endmodule

module tb;
  reg D, CLK, EN;
  wire Q;

  DFlipFlop UUT (
    .D(D),
    .CLK(CLK),
    .EN(EN),
    .Q(Q)
  );

  initial begin
    D = 0;
    CLK = 0;
    EN = 0;
    #10
    D = 1;
    EN = 1;
    #10
    CLK = 1;
    #10
    CLK = 0;
```

```
37      #10
38      $finish;
39    end
40 endmodule
```

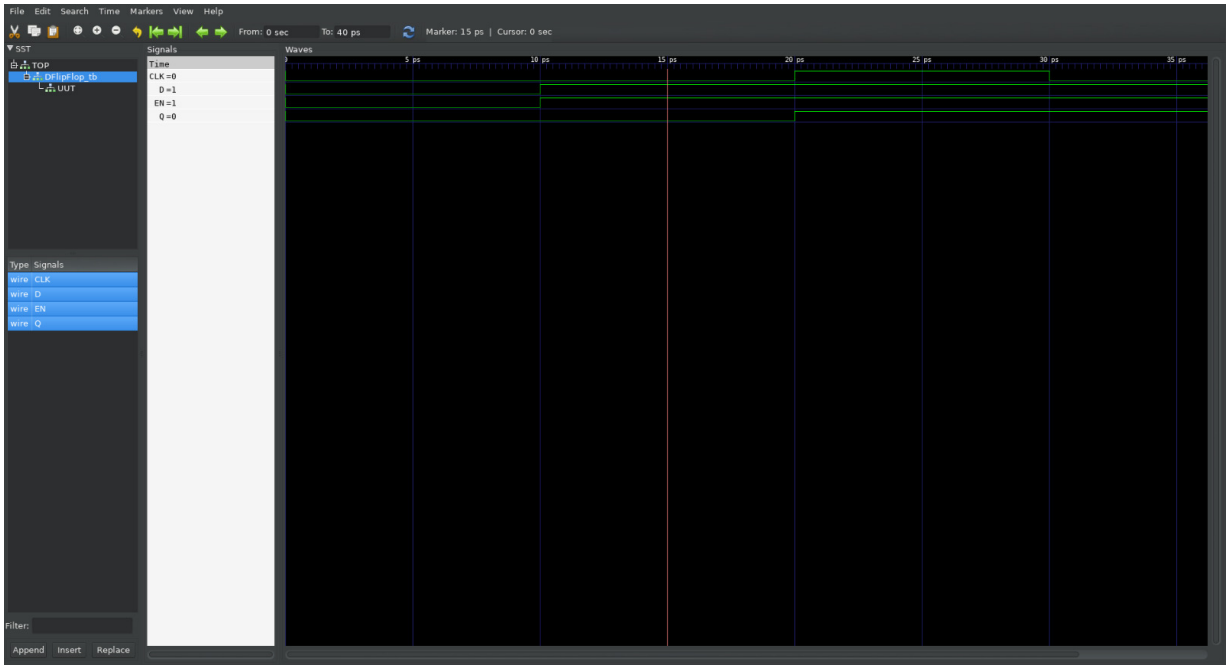

Figure 6

8. A sequential circuit has one flip-flop Q, two inputs x and y, and one output S . It consists of a full-adder circuit connected to a D flip-flop, as shown in Figure. Write a HDL code for the circuit.

```
module FullAdderWithFlipFlop (
  input logic x,         // Input x
  input logic y,         // Input y
  input logic clk,       // Clock input
  output logic S         // Output S
);

  logic sum, carry, dff_input;

  always @(posedge clk)
    begin
      // Full Adder logic
      sum = x + y + dff_input;
      carry = (x & y) | ((x ^ y) & dff_input);

      // D Flip-Flop
      dff_input <= carry; // D input is the carry-out from the
         full-adder
    end

  // Output
  assign S = sum;

endmodule


module FullAdderWithFlipFlop_tb;

  // Inputs
  reg x;
  reg y;
  reg clk;

  // Outputs
  wire S;

  // Instantiate the module under test
  FullAdderWithFlipFlop dut (
    .x(x),
    .y(y),
    .clk(clk),
    .S(S)
  );

  // Clock generation
  always #5 clk = ~clk;

  // Stimulus
  initial begin
    x = 0;
```

```
    y = 0;
    clk = 0;

    #10 x = 1;
    #10 y = 1;
    #10 x = 0;
    #10 y = 1;
    #10 x = 1;
    #10 y = 0;
    #10 x = 0;
    #10 y = 0;

    #10 $finish;
  end

  // Monitor
  always @(posedge clk) begin
    $display("x = %b, y = %b, S = %b", x, y, S);
  end

endmodule
```

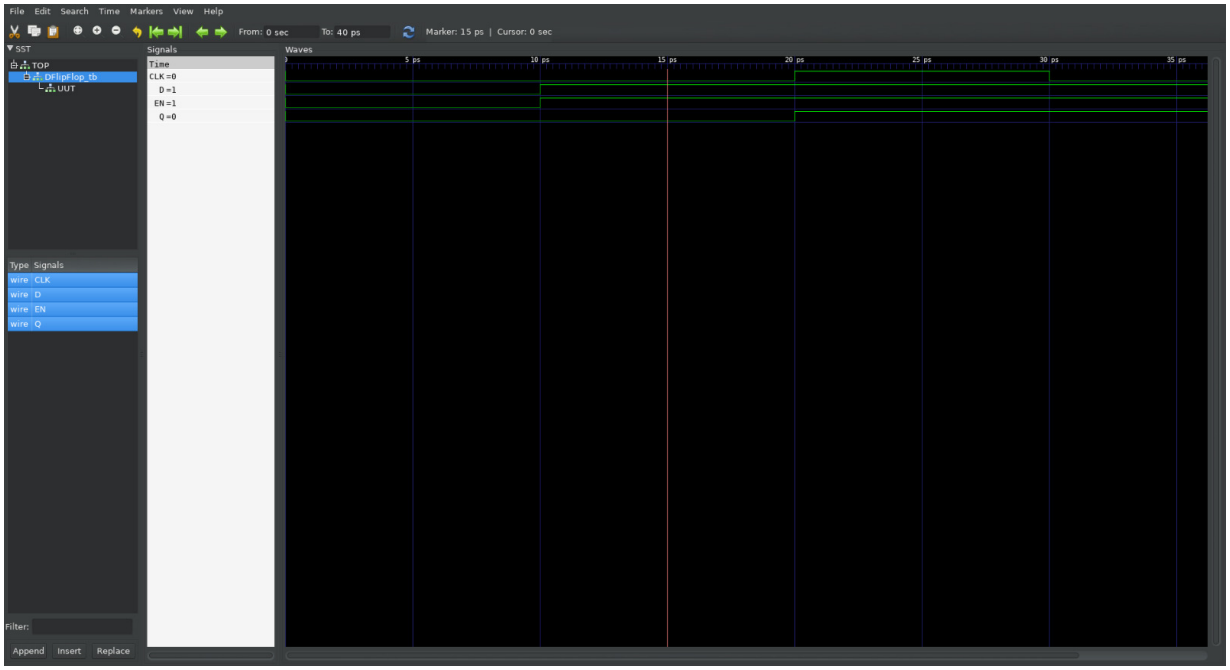

Figure 7