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Digital Design and Computer Architecture (CIE 239)

Assignment 4

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1. Assume that registers R_1 and R_2 in the Figure hold two unsigned numbers. When select input X is equal to 1, the adder–subtractor circuit performs the arithmetic operation "R_1 + 2's complement of R_2." This sum and the output carry C_n are transferred into R_1 and C when $K_1 = 1$ and a positive edge occurs on the clock.

   Solution.

   - Assume $C = 1$.
     Perform $R_1 - R_2$ and $X = 1$
     $\therefore R_1 = 1111$, suppose $R_2 = 1010$ 2's complement of R_2 is 0110
     $R_1 - R_2 = 10101$
     $\therefore R_1 = 0101$ and $C = 1$
     So if $C = 1$ then the value transferred to R_1 is equal to $R_2 - R_1$
   - Assume $C = 0$. Perform $R_2 - R_1$
     2's complement of R_1 is 1010
     $R_2 - R_1 = 1101$
     2's complement of $R_2 - R_1$ is 0011
     So if $C = 0$ then the 2's complement of $R_2 - R_1$ is equal to R_1

   ■

2. The outputs of registers R_0, R_1, R_2, and R_3 are connected through 4-to-1 multiplexers to the inputs of a fifth register, R_4. Each register is 8 bits long. The required transfers, as dictated by four control variables, are

$$C_0 : R_4 \leftarrow R_0,$$
$$C_1 : R_4 \leftarrow R_1,$$
$$C_2 : R_4 \leftarrow R_2,$$
$$C_3 : R_4 \leftarrow R_3.$$

The control variables are mutually exclusive (i.e., only one variable can be equal to 1 at any time) while the other three are equal to 0. Also, no transfer into R_4 is to occur for all control variables equal to 0.

(a) Using registers and a multiplexer, draw a detailed logic diagram of the hardware that implements a single bit of these register transfers.

Solution. ■

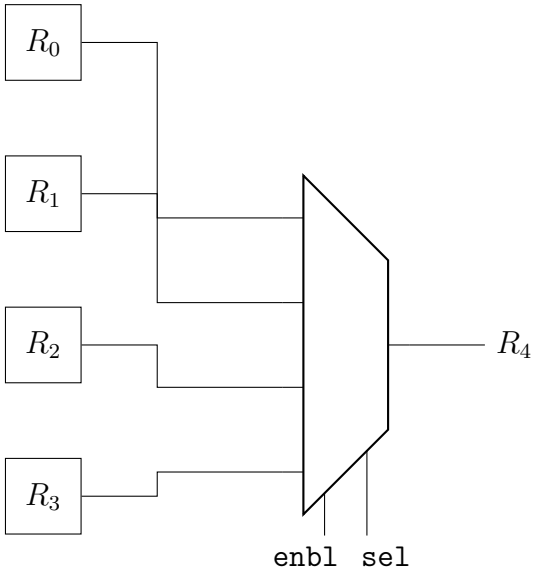

Figure 1

(b) Write HDL code for the design.

Solution.

```
module Q_2 (clk, reset, C[0:3], R[0:4]);
  input clk, reset;
  input [3:0] C;
  input [7:0] R[0:3];
  output [7:0] R[4];
  reg [7:0] R[0:4];
  always @(posedge clk, posedge reset)
    if (reset)
      R[0:4] <= 0;
    else
      case (C)
        4'b0001: R[4] <= R[0];
        4'b0010: R[4] <= R[1];
        4'b0100: R[4] <= R[2];
        4'b1000: R[4] <= R[3];
        default: R[4] <= 0;
      endcase
endmodule
```

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3. You are designing an FSM to keep track of the mood of four students working in the digital design lab. Each student's mood is either HAPPY (the circuit works), SAD (the circuit

blew up), BUSY (working on the circuit), CLUELESS (confused about the circuit), or ASLEEP (face down on the circuit board). How many states does the FSM have? What is the minimum number of bits necessary to represent these states?

Solution.

- The FSM has $5^4 = 625$ states.
- The minimum number of bits necessary to represent these states is $\lceil \log_2 625 = \lceil 9.28 = 10$ bits.

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4. You have been enlisted to design a soda machine dispenser for your department lounge. Sodas are partially subsidized by the student chapter of the IEEE, so they cost only 25 cents. The machine accepts nickels, dimes, and quarters. When enough coins have been inserted, it dispenses the soda and returns any necessary change. Design an FSM controller for the soda machine. The FSM inputs are Nickel, Dime, and Quarter, indicating which coin was inserted. Assume that exactly one coin is inserted on each cycle. The outputs are Dispense, ReturnNickel, ReturnDime, and ReturnTwoDimes. When the FSM reaches 25 cents, it asserts Dispense and the necessary Return outputs required to deliver the appropriate change. Then it should be ready to start accepting coins for another soda.

Solution. ■

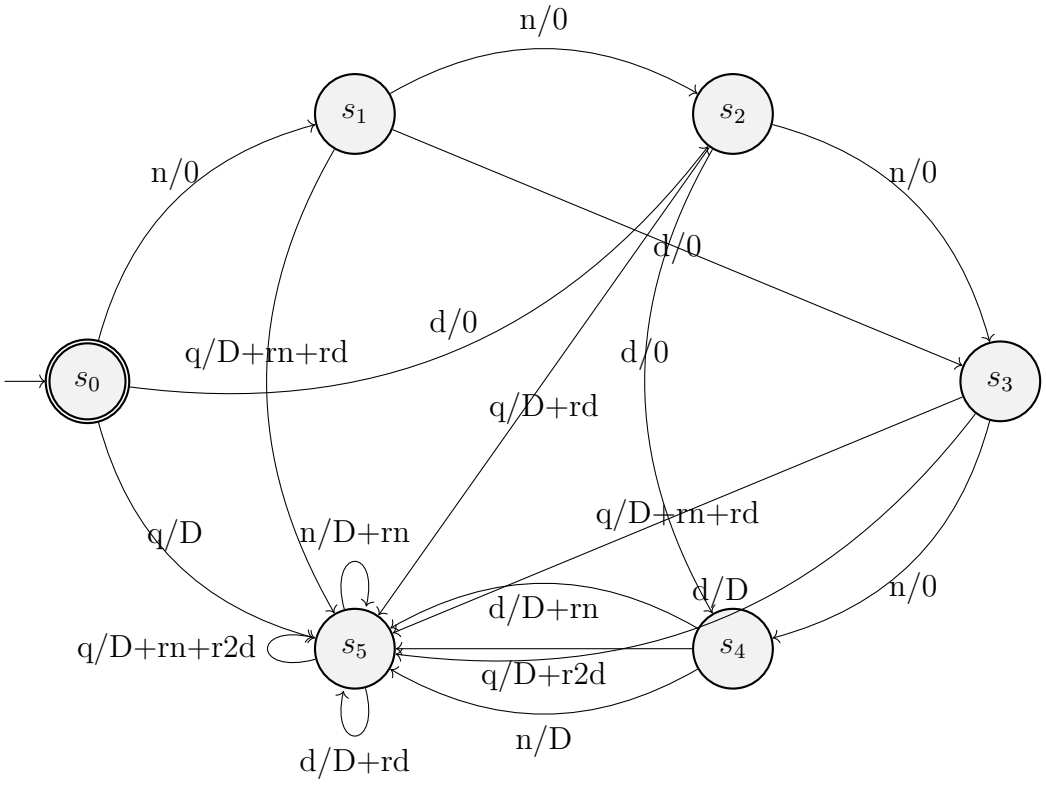

Figure 2

5. Analyze the FSM shown in the figure. Write the state transition and output tables and sketch the state transition diagram. Describe in words what the FSM does. Recall that the s and r register inputs indicate set and reset, respectively.

Solution.

$$D_0 = \overline{A}, \quad D_1 = Q_0 A, \quad D_2 = (Q_1 + Q_2)A, \quad Q = Q_2 \tag{1}$$

■

Q_0	Q_1	Q_2	A	Q_0'	Q_1'	Q_2'	D_0	D_1	D_2	Q
0	0	0	0	0	0	0	0	0	0	0

Table 1