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Digital Design and Computer Architecture (CIE 239)

Assignment 2

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1. a. Write a Boolean equation in sum-of-products canonical form and product-of-sum canonical form for following truth table.

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

Table 1

Solution.

$$Y = A'B'C'D' + A'B'C'D + A'B'CD' + A'B'CD + AB'C'D' + AB'CD' + ABCD' \quad (1)$$
$$= \Sigma(0, 1, 2, 3, 8, 10, 14). \quad (2)$$

$$Y = \begin{array}{l}(A + B' + C + D)(A + B' + C + D')(A + B' + C + D')(A + B' + C' + D) \\ (A + B' + C' + D')(A' + B + C + D')(A' + B + C' + D')(A' + B' + C + D) \\ (A' + B' + C + D')(A' + B' + C' + D')\end{array} \quad (3)$$
$$= \Pi(4, 5, 6, 7, 9, 11, 12, 13, 15). \quad (4)$$

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b. Minimize each of the Boolean equations of the sum-of products (use Boolean algebra) and implement the simplified equation using basic logic gates (AND, OR and NOT gate).

Solution.

$$
\begin{aligned}
Y &= A'B'C'D' + A'B'C'D + A'B'CD' + A'B'CD + AB'C'D' + AB'CD' + ABCD' && (5)\\
&= A'B'C'(D' + D) + A'B'CD' + A'B'CD + AB'D'(C' + C) + ABCD' && (6)\\
&= A'B'C' + A'B'CD' + A'B'CD + AB'D' + ABCD' && (7)\\
&= A'B'(C' + CD') + A'B'CD + AB'D' + ABCD' && (8)\\
&= A'B'(C' + D') + A'B'CD + AB'D' + ABCD' && (9)\\
&= A'B'(C' + D' + CD) + AB'D' + ABCD' && (10)\\
&= A'B'(C' + CD + D') + AB'D' + ABCD' && (11)\\
&= A'B'(C' + D + D') + AB'D' + ABCD' && (12)\\
&= A'B'(C' + 1) + AB'D' + ABCD' && (13)\\
&= A'B' + AB'D' + ABCD' && (14)\\
&= B'(A' + AD') + ABCD' && (15)\\
&= B'(A' + D') + ABCD' && (16)\\
&= A'B' + B'D' + ABCD' && (17)\\
&= A'B' + D'(B' + ABC) && (18)\\
&= A'B' + D'(B' + BAC) && (19)\\
&= A'B' + D'(B' + AC) && (20)\\
&= A'B' + B'D' + ACD'. && (21)
\end{aligned}
$$

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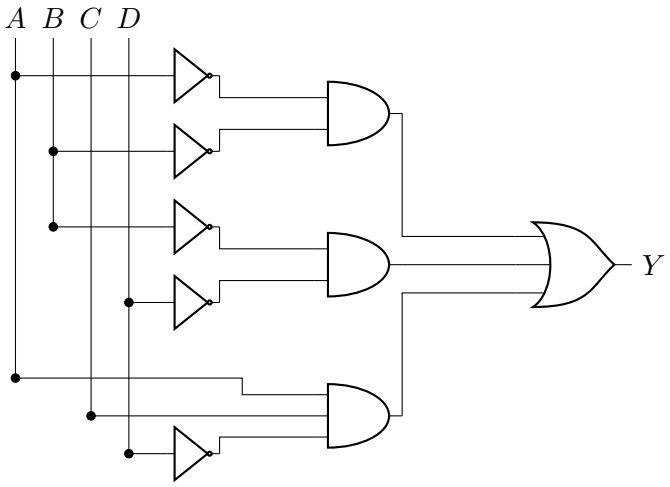

Figure 1

c. Implement the minimized function again using only using only NOT gates and NAND and NOR gates.

Solution.

$$Y = \overline{\overline{A'B' + B'D' + ACD'}} \tag{22}$$
$$= \overline{\overline{A'B'} \cdot \overline{B'D'} \cdot \overline{ACD'}}. \tag{23}$$

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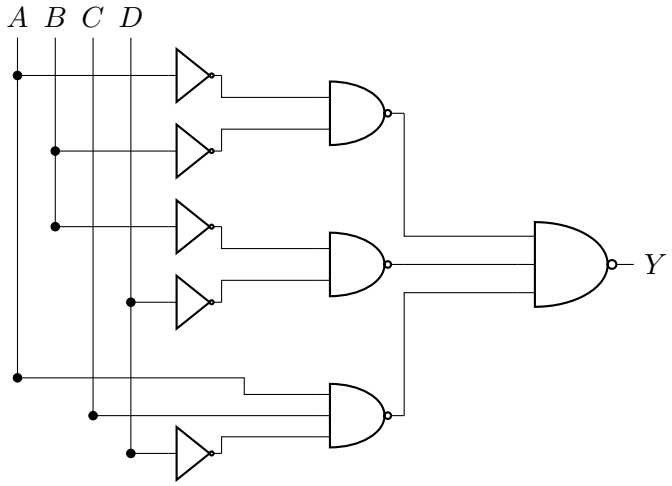

Figure 2

2. Simplify the following Boolean equations using Boolean theorems. Check for correctness using K-map.

a. $F(x, y, z) = x'y' + xyz + x'y$

Solution.

$$F(x, y, z) = x'y' + xyz + x'y \tag{24}$$
$$= x'(y' + y) + xyz \tag{25}$$
$$= x' + xyz \tag{26}$$
$$= x' + yz. \tag{27}$$

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x \ yz	00	01	11	10
0	1	1	1	1
1	0	0	1	0

K-Map 1

b. $F(w,x,y,z) = w'x(z' + yz) + x(w + w'yz)$

Solution.

$$\begin{aligned}
F(w,x,y,z) &= w'x(z' + yz) + x(w + w'yz) && (28)\\
&= w'x(z' + zy) + x(w + w'yz) && (29)\\
&= w'x(z' + y) + x(w + yz) && (30)\\
&= w'xz' + w'xy + xw + xyz && (31)\\
&= x(w + w'z') + w'xy + xyz && (32)\\
&= x(w + z') + w'xy + xyz && (33)\\
&= xw + xz' + w'xy + xyz && (34)\\
&= xz' + x(w + w'y) + xyz && (35)\\
&= xz' + x(w + y) + xyz && (36)\\
&= xz' + xw + xy + xyz && (37)\\
&= xz' + xw + xy(1 + z) && (38)\\
&= xz' + xw + xy. && (39)
\end{aligned}$$

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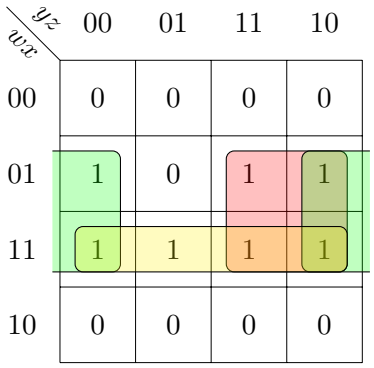
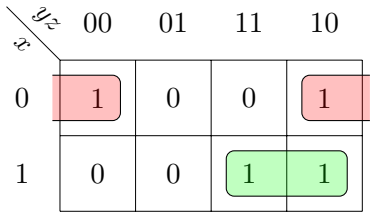


K-Map 2

3. Simplify the following using Kmap and implement using logic gates

(a) $F(x, y, z) = \Sigma m(0, 2, 6, 7)$



K-Map 3

Solution.

$$F(x, y, z) = x'z' + xy. \tag{40}$$

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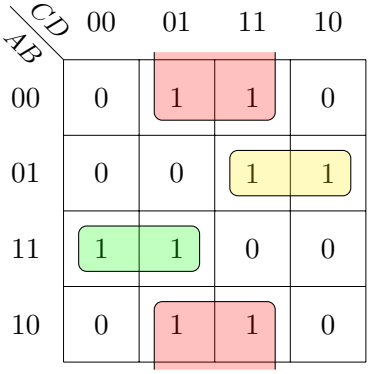
(b) $F(A, B, C, D) = \Sigma m(1, 3, 6, 7, 9, 11, 12, 13)$



K-Map 4

Solution.

$$F(A, B, C, D) = ABC' + A'BC + B'D. \tag{41}$$

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4. Using De Morgan equivalent gates and bubble pushing methods, redraw the circuit so that you can find the Boolean equation by inspection. Write the Boolean equation.

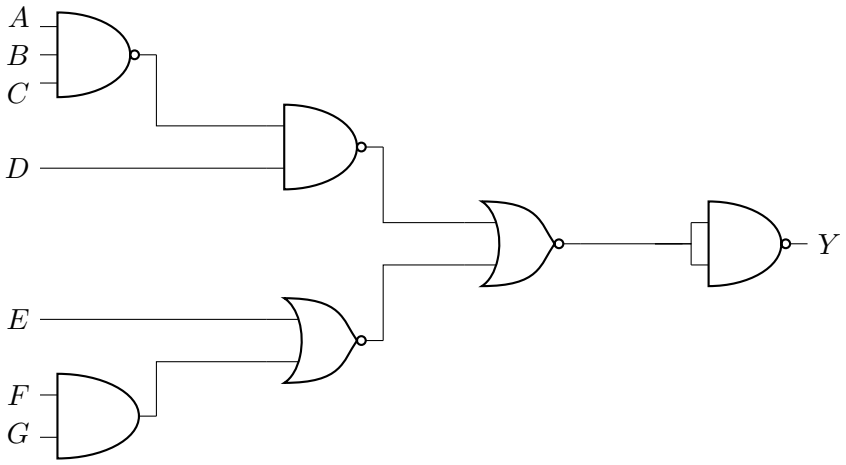

Figure 3

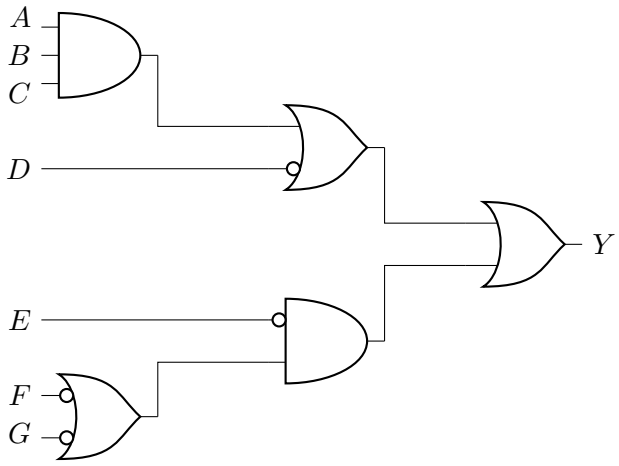

Figure 4

Solution.

$$Y = ABC + D' + E'(F' + G') \tag{42}$$
$$= ABC + D' + E'F' + E'G'. \tag{43}$$

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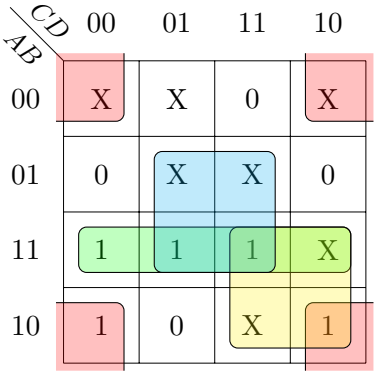
5. Find a minimal Boolean equation for the function. Remember to take advantage of the don't care entries. (use k-map)

A	B	C	D	Y
0	0	0	0	X
0	0	0	1	X
0	0	1	0	X
0	0	1	1	0
0	1	0	0	0
0	1	0	1	X
0	1	1	0	0
0	1	1	1	X
1	0	0	0	1
1	0	0	1	0
1	0	1	0	X
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	X
1	1	1	1	1

Table 2



K-Map 5

Solution.

$$F(A,B,C,D) = AD + AB + B'D'. \tag{44}$$

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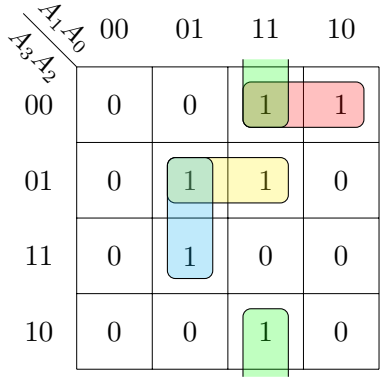
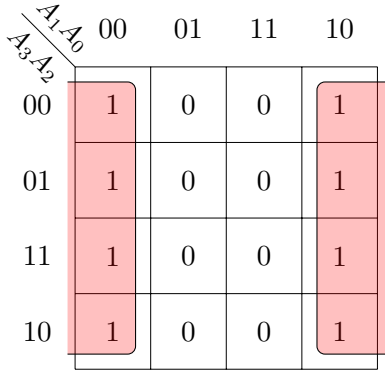
6. A circuit has four inputs and two outputs. The inputs, $A_{3:0}$, represent a number from 0 to 15. Output P should be `TRUE` if the number is prime (0 and 1 are not prime, but 2, 3, 5, and so on, are prime). Output D should be `TRUE` if the number an even number Give simplified Boolean equations for each output and sketch a circuit (use k-map)

Dec	A_3	A_2	A_1	A_0	P	D
0	0	0	0	0	0	1
1	0	0	0	1	0	0
2	0	0	1	0	1	1
3	0	0	1	1	1	0
4	0	1	0	0	0	1
5	0	1	0	1	1	0
6	0	1	1	0	0	1
7	0	1	1	1	1	0
8	1	0	0	0	0	1
9	1	0	0	1	0	0
10	1	0	1	0	0	1
11	1	0	1	1	1	0
12	1	1	0	0	0	1
13	1	1	0	1	1	0
14	1	1	1	0	0	1
15	1	1	1	1	0	0

Table 3



(a) P



(b) D

K-Map 6

Solution.

$$D(A_3, A_2, A_1, A_0) = A_0'. \tag{45}$$

$$P(A_3, A_2, A_1, A_0) = A_3'A_2'A_1 + A_3'A_2A_0 + A_2A_1'A_0 + A_2'A_1A_0. \tag{46}$$

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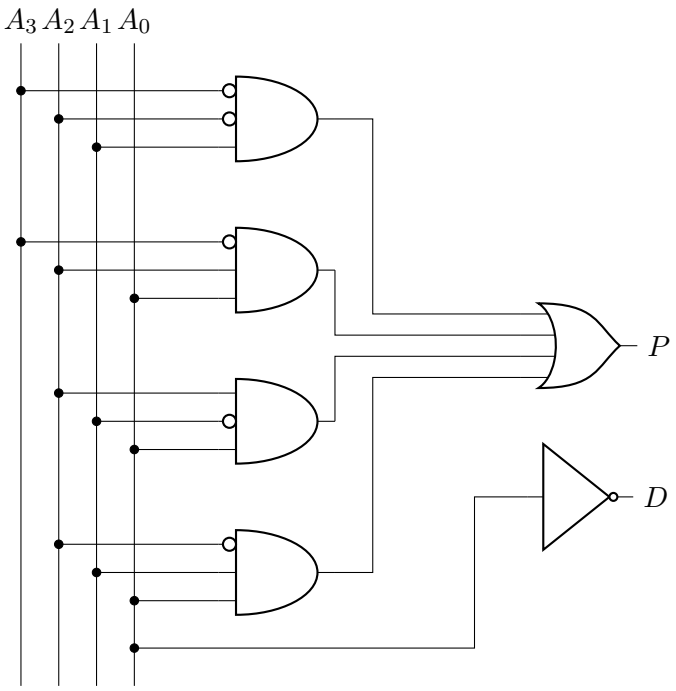

Figure 5

7. Write the HDL code for question number 6 (Your answer should include the HDL code and the input and output signal screenshot from modelsim)

SystemVerilog

```
module prime_even(
  input logic [3:0] A,
  output logic P, D
);

  assign P = ~A[3] & ~A[2] & A[1] | ~A[3] & A[2] & A[0] | A[2] & ~A[1] & A[0]
    | ~A[2] & A[1] & A[0];
  assign D = ~A[0];

endmodule
```

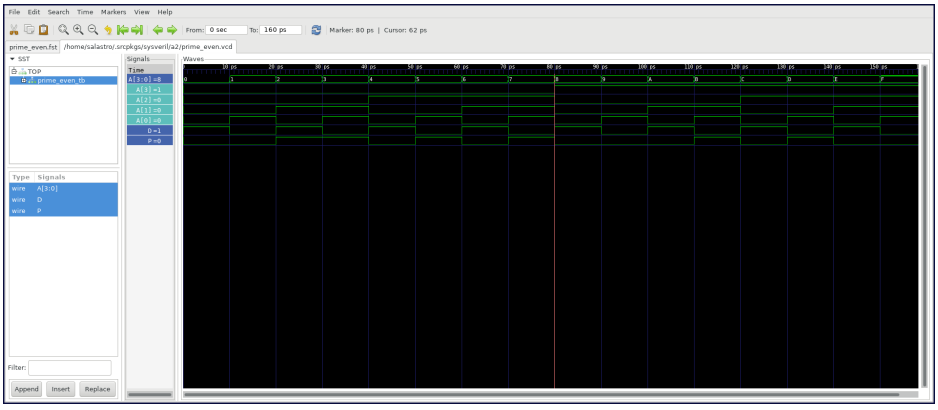

Figure 6: Waveform of `prime_even` using GTKWave