Characteristic description

TM1814 is four channels LED constant current adjustable driver IC with function of internal control synchronizing, which can achieve a wide range of display as MCU inputs one group of data set by constant current and PWM to TM1814. When input signal is disconnected, it can realize synchronized fixation of colorful pattern change and prevent in-operation of subsequent cascade chip caused by chip damage. Internal chip is integrated with MCU solidification program and single wire digital interface, data flip-latch, LED constant current driver, circuit, etc. Internal VDD pin is integrated with 5V regulator with less peripheral devices, which applies to guardrail tube, point source and LED decorative products. This product has excellent performance and reliable quality.

Features

- Adopt power CMOS technology
- Withstand voltage of OUT output port is 32V
- 5 V voltage-regulator tube is built into VDD, and the voltage supports 6-24 V after cascading the resistor
- Constant current can achieve level 64 adjustment (6.5 mA-38mA)
- PWM brightness controls circuit, and 256 brightness is adjustable
- Accurate current output value
  Maximum error (between channels): ±3%
  Maximum error (between chips): ±5%
- Single line serial concatenated port
- Oscillation mode: build in RC vibration and conduct clock synchronization according to signals on data line. After receiving the data from this unit, it can reproduce follow-up data and send it to lower level through data output end, and signals will not be distorted and reduced along with cascade
- Build in power on reset circuit, and after powering on reset, all registers are initialized to zero
- External control mode data transmission rate is 800 KHZ
- Internal control mode data transmission rate is 500 KHZ
- Internal control mode chip sends 2048 points of data
- Encapsulation mode: SOP8

Internal structure diagram

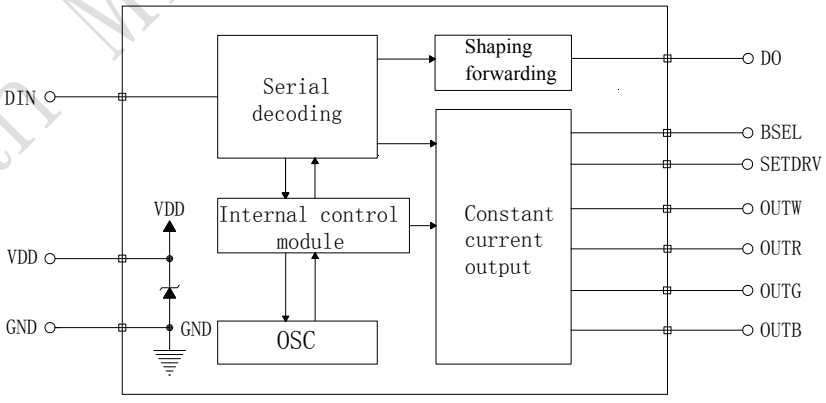


Figure1

Pin configuration

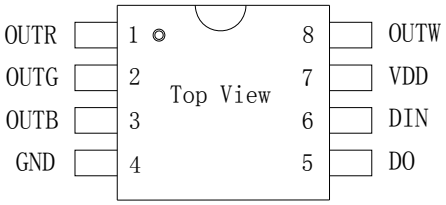


Figure 2

Pin function

Pin name	Pin SN	I/O	Function description
DIN	6	I	Data input
DO	5	O	Data output
VDD	7	--	Positive power supply
OUTR	1	O	Open-drain of N tube and constant current output
OUTG	2	O	Open-drain of N tube and constant current output
OUTB	3	O	Open-drain of N tube and constant current output
OUTW	8	O	Open-drain of N tube and constant current output
GND	4	--	Power ground

Input and output equivalent circuit

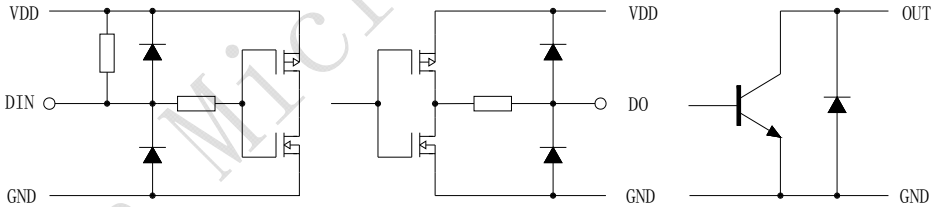


Figure 3

Integrated circuit is an electrostatic sensitive device, which is easy to generate a large amount of static electricity in the dry season or dry environments. Electrostatic discharge may damage integrated circuits. Titan Micro Electronics suggests that all preventive measures of appropriate integrated circuit shall be taken. Improper handling and welding may result in ESD damaged, or performance degradation. In addition, the chip fails to work.

Limit parameter

Parameter name	Symbols for parameters	Limiting value	Unit
Logic supply voltage	VDD	-0.4～+7.0	V
Din port voltage	Vin	-0.4～VDD+0.7	V
Out port voltage	Vout	-0.4～+32.0	V
Operating temperature range	Topr	-40～+85	℃
Storage temperature range	Tstg	-50～+150	℃
Static electricity ESD	Human Body Mode (HBM)	3000	V
	Machine Mode (MM)	200	V

(1) For these levels in the above table, it may cause permanent damage to the device and reduce device reliability under the condition of prolonged using of the chip. We do not suggest that chips operate beyond these limit parameters under any other conditions;
(2) All voltage values are tested systematically.

Recommended operating conditions

It shall be tested under at-40～+85℃, unless otherwise stated			TM1814			Unit
Parameter name	Symbols for parameters	Test condition	Minimum value	Typical value	Maximum value	
Voltage Drain Drain	VDD		4.5	5.0	6.5	V
DIN port voltage	Vin	VDD=5V，DIN cascades 1KΩ resistor			VDD+0.4	V
DO port voltage	Vdo	VDD=5V，DO cascades 1KΩ resistor			VDD+0.4	V
OUT port voltage	Vout	OUT＝OFF			24.0	V

Electrical characteristics

It shall be tested when VDD=3.0～5.5V and operating temperature is -40～+85℃, unless otherwise stated			TM1814			Unit
Parameter name	Symbols for parameters	Test condition	Minimum value	Typical value	Maximum value	
High level output voltage	Voh	Ioh=3mA	VDD-0.5			V
Low level output voltage	Vol	Iol=10mA			0.4	V
High level input voltage	Vih	VDD=5.0V	3.5		VDD	V
Low level input voltage	Vil	VDD=5.0V	0		1.5	V
High level output current	Ioh	VDD=5.0V，Vdo=4.9V		1		mA
Low level output current	Iol	VDD=5.0V，Vdo=0.4V		10		mA
Input current	Iin	DIN connects VDD		1		μA
Quiescent current	IDD	VDD=4.0V，GND=0V，other ports are hanging	0.5	2.8	3.5	mA
OUT output constant current	Iout	OUTRW,OUTR,OUTG,OUTB=ON，Vout=3.0V	6.5		38	mA
OUT output leakage current	Iolkg	OUTRW,OUTR,OUTG,OUTB=OFF，Vout=12.0V			0.5	μA
Constant current error between channels	ΔIolc0	OUTRW,OUTR,OUTG,OUTB =ON，Vout=3.0V			±3	%
Constant current error between chips	ΔIolc1	OUTRW,OUTR,OUTG,OUTB =ON，Vout=3.0V			±5	%
Power consumption	Pd	Ta=25℃			250	mW

Switching characteristic

It shall be tested when VDD=3.0～5.5V and operating temperature is -40～+85℃, typical value VDD=5.0V and TA=+25℃, unless otherwise stated			TM1814			Unit
Parameter name	**Symbols for parameters**	**Test condition**	**Minimum value**	**Typical value**	**Maximum value**	
Data rate	Fin			800		KHz
OUT PWM output frequency	Fout	OUTR，OUTG，OUTB	900	1000	1100	Hz
Time when external control is switched to internal control	Tos	DIN is input without pulse	450	500	550	ms
Transmission delay time	Tplz	DIN → DO		178		ns
Input capacitance	Ci				15	pF

Temporal characteristic

Parameter name	Symbols for parameters	Test condition	Minimum value	Typical value	Maximum value	Unit
Input 0 code, low level time	T0l	VDD=5.0V GND=0V	310	360	410	ns
Input 1 code, low level time	T1l		650	720	1000	ns
Output 0 code, low level time	T0l’			350		ns
Output 1 code, low level time	T1l’			700		ns
Cycle of o code or 1 code	T0/T1			1.25		μs
Reset code, high level time	Treset		200		20000	μs

(1) Cycle of 0 code or 1 code is within 1.25 μs, and chip can work normally, but the low level time of 0 code and 1 code must comply with corresponding numerical range in above table;
(2) When it doesn't need to reset, high level time between bytes should not exceed 126μs. Otherwise, the chip may reset. After reset, it receives data again and cannot realize normal transmission of data.

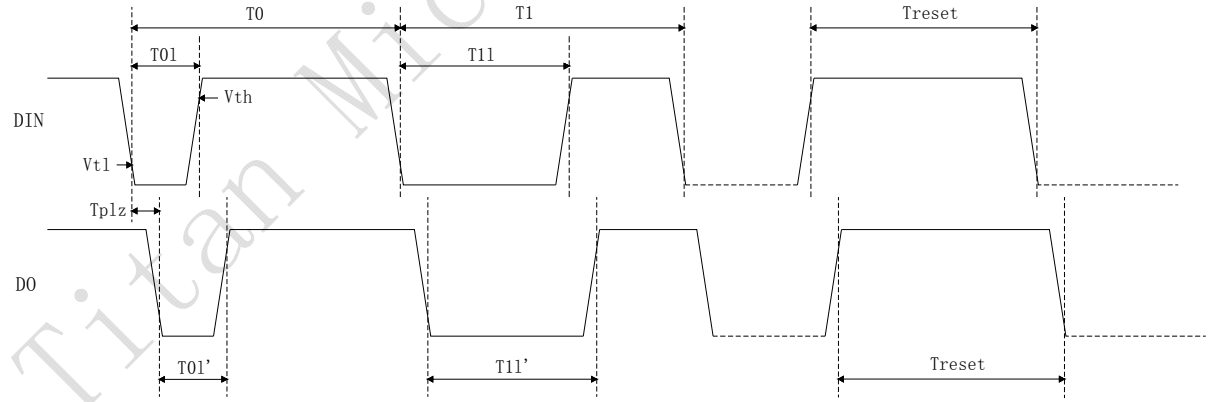


Figure 4

Function declaration

This chip adopts single line communication mode, and sends signal by way of normalizing code. After being powered on and reset, it will receive data from DIN end. After receiving 32 bit, DO ports will start to forward data from DIN end and provide input data for next cascade chip. Before forwarding data, DO port is high level. If the DIN inputs RESET signals, the chip will set constant current value according to the received 32 bit data after the chip is successfully reset, and output duty cycle waveform corresponding to the PWM. The chip waits again to receive new data. After receiving 32 bit data, it will transmit data through DO port. Before the chip does not receive RESET signal, the original output of OUTW, OUTR, OUTG and OUTB pin remains unchanged.

Chip adopts automatic shaping forwarding technology, and signal will not be distorted and reduced to ensure cascade number of the chip is not restricted by signal transmission and only limited by screen refresh rate requirements.

1. One frame of complete data structure

C1	C2	D1	D2	D3	D4	…	Dn	Reset

C1 and C2 are constant current value set commands, and every chip can receive and transmit C1 and C2.
D1, D2, D3, D4... and Dn are PWM set commands of each chip.
Reset represents reset signal, and is valid under high level.

2. Data format of C1

W7	W6	W5	W4	W3	W2	W1	W0	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

C1 command contains 8 × 4bit data bits, and high order position starts firstly. W7, W6, R7, R6, G7, G6, B7 and B6 are set to fixed 0.

W [5:0]: being used for setting OUTW output constant current value. All 0 codes are 6.5mA; all 1 codes are 38mA; level 64 is adjustable.

R [5:0]: being used for setting OUTR output constant current value. All 0 codes are 6.5mA; all 1 codes are 38mA; level 64 is adjustable.

G [5:0]: being used for setting OUTG output constant current value. All 0 codes are 6.5mA; all 1 codes are 38mA; level 64 is adjustable.

B [5:0]: being used for setting OUTB output constant current value. All 0 codes are 6.5mA; all 1 codes are 38mA; level 64 is adjustable.

3. Data format of C2

$\overline{W7}$	$\overline{W6}$	$\overline{W5}$	$\overline{W4}$	$\overline{W3}$	$\overline{W2}$	$\overline{W1}$	$\overline{W0}$	$\overline{R7}$	$\overline{R6}$	$\overline{R5}$	$\overline{R4}$	$\overline{R3}$	$\overline{R2}$	$\overline{R1}$	$\overline{R0}$	$\overline{G7}$	$\overline{G6}$	$\overline{G5}$	$\overline{G4}$	$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{B7}$	$\overline{B6}$	$\overline{B5}$	$\overline{B4}$	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$	$\overline{B0}$

C2 command is bit compl corresponding to C1 command, or chips will not decode data properly.

4. Data format of Dn

W7	W6	W5	W4	W3	W2	W1	W0	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

Each group of PWM locate command contains 8 × 4bit data bits, and high order position starts firstly.

W [7:0]: being used for setting PWM duty cycle from output of OUTW. All 0 codes are shut off; all 1 codes have maximum duty cycle; level 256 is adjustable.

R [7:0]: being used for setting PWM duty cycle from output of OUTR. All 0 codes are shut off; all 1 codes have maximum duty cycle; level 256 is adjustable.

G [7:0]: being used for setting PWM duty cycle from output of OUTG. All 0 codes are shut off; all 1 codes have maximum duty cycle; level 256 is adjustable.

B [7:0]: being used for setting PWM duty cycle from output of OUTB. All 0 codes are shut off; all 1 codes have maximum duty cycle; level 256 is adjustable.

5. Data receiving and forwarding

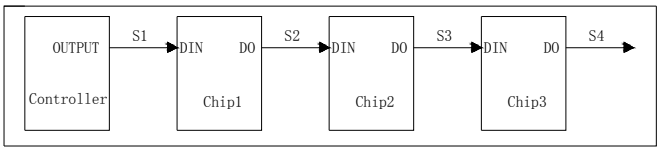


Figure 5

Among which S1 is data sent by controller Di port; S2, S3 and S4 are data forwarded by cascade TM1814.

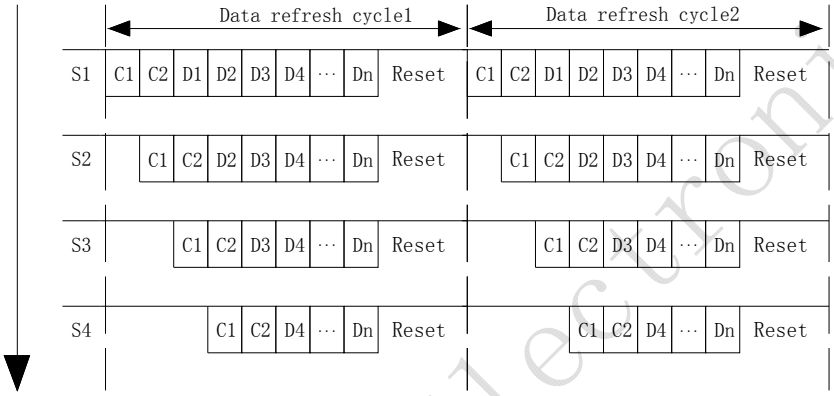


Figure 6

Data transmission and forwarding process: chip 1 is not forwarded when receiving data of C1. When starting to receive C2, chip 1 will forward data of C1. After C2 is received by chip 1, chip 1 will finish forwarding of C1; since then the controller will send D1 to chip 1, and chip 1 will begin to forward C2. When chip 1 completes the forwarding of C2, it just finishes receiving D1. After this, for D2, D3, D4... Dn sent by controller, chip 1 will forward them. The cycle of forwarding data by chip 1 and the cycle of sending data to chip 1 by controller are the same. There are always difference value of 32 bit in the data forwarded by chip1 and the data sent by controller. When the controller sends a reset signal, chip 1 will check C1 and C2. If it is rightful, current value is set to the port, and D1 will be translated into actual PWM control. For subsequent cascade chip2, chip 3… and chip n, functions of data reception and forwarding are the same with chip 1, both of them will retain data (8×4 bit) controlled by the first group of PWM after C1 and C2, and forward other PWM control data.

Application information

1. Typical application circuit

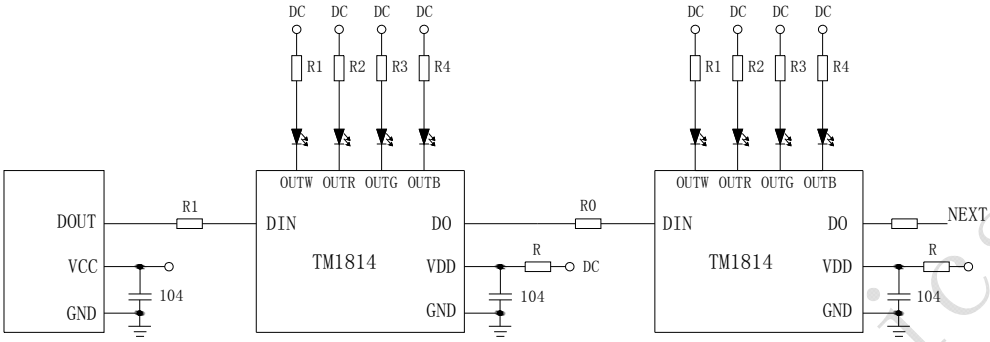


Figure 7

To avoid that instantaneous high pressure resulting from hot plugging during testing results in damage of chip signal input and output pin, protective resistance of 100Ω shall be concatenated in signal input and output pin. In addition, 104 decoupling capacitors of chips in the figure are indispensable, and VDD and GND pin from routing to chips shall be shorter in order to achieve optimal decoupling effect and stabilize chip operation.

2. Power configuration

TM1814 can be configured to DC6 ~ 24 V voltage for power supply, but according to different input voltage, different source resistances should be configured. Resistance calculation method: VDD port current is calculated according to 10 mA, and VDD concatenated resistance R = (DC - 5.5 V) ÷10 mA (DC is power supply voltage).

Typical values of configured resistance are listed as follows:

Power voltage (DC)	The resistance value of the resistance suggested to concatenate between power port and VDD
5V	The internal voltage regulator tube does not work without needing to connect resistor
6V	50Ω
9V	350Ω
12V	650Ω
24V	1.8KΩ

3. Internal control pattern

When chip power supply is normal, and DIN is detected that there is no signal input, or the original signal is normal, then after suddenly losing about 500 ms, chip enters into internal control mode, and conduct following circulation flashing:

	OUT port state			
State SN	OUTW	OUTR	OUTG	OUTB
0	0	1	0	0
1	0	0	1	0
2	0	0	0	1
3	1	0	0	0
4	0	1	1	0
5	0	0	1	1
6	0	1	0	0
7	1	1	0	0
8	1	0	1	0
9	1	0	0	1

Note: '0' represents that the channel is OFF and '1' represents that the channel is ON.

In the following figure, after powering on, chip 1 is detected that there is no signal input, and it will enter into internal control mode. There will be an internal control pattern change in WRGB. At the same time, DO ports will automatically send data to backward stage chip and realize synchronous display function.
After the chip enters into internal control mode, it will send 2,048 points of data.

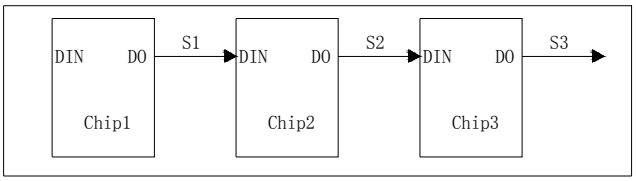


Figure 8

4. How to calculate data refreshing rate

The data refreshing time is calculated according to how many pixel points are connected in a system. One group of WRGB is usually a pixel (or one section), and a TM1814 chip can control a group of WRGB.
Calculate according to normal mode:

1 bit data cycle is 1.25μs (the frequency is 800 KHZ). One pixel data includes PWM data transmission time: W (8 bit), R (8 bit), G (8 bit) and B (8 bit), totaling 32bit; transmission time is 1.25μs×32=40μs, and coupled with transmission time of C1 and C2 is 120μs. If there are 1000 pixels in a system, all display time for one-off refreshing is 40 μs × 1000=40 ms (ignoring C1, C2 and Reset signal time), namely the refreshing rate of one second: 1÷40ms=25Hz.

The following is the refreshing rate table of cascade points corresponding to highest data:

	Normal mode	
Pixels	**Fastest data refreshing time (ms)**	**Highest data refreshing rate (Hz)**
1～400	16	62.5
1～800	32	32.2
1～1000	40	25

5. How to make TM1814 work in optimum constant current state

TM1814 is a constant current adjustable drive. According to the constant current curve, it shows that it will enter constant current state when the OUT port voltage reaches 0.8 V. Higher voltages are not always better. Higher voltages lead to larger power consumption of the chip and more serious heat emitting, which will reduce reliability of the whole system. It is recommended that voltages shall be between 1.2 ~ 3 V when OUT port is on. Too high voltage in OUT port can be reduced by way of series resistance.

6. How to use TM1814 to expand current

For each OUT port of TM1814, if the user needs to expand the drive current, it can be used after shorts of three OUT ports of WRGB. For each short of OUT port, maximum constant current value will increase 38mA. After shorts of three OUT ports, maximum constant current value can reach 152mA. This method needs software to cooperate and control. Writing three groups of register value respectively can realize accurate current control and larger drive current.

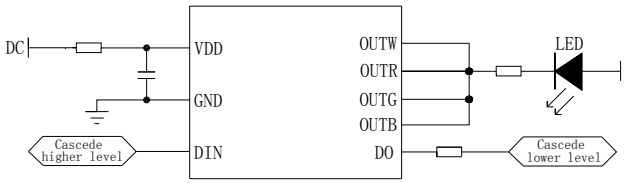


Figure 9

Constant current curve

When applying TM1814 in LED product design, and when constant current is set to the same value, current differences between channels even chips are very small. When there is a change in load terminal voltage, the stability of output current will not be affected. Constant current curve is shown in the following figure:

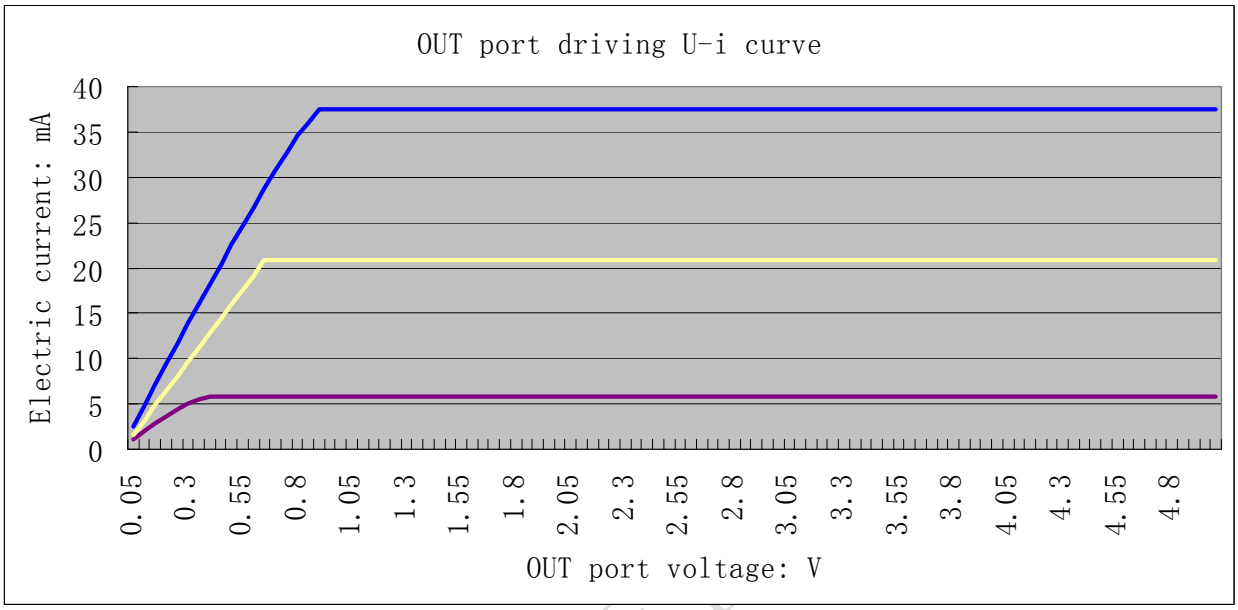
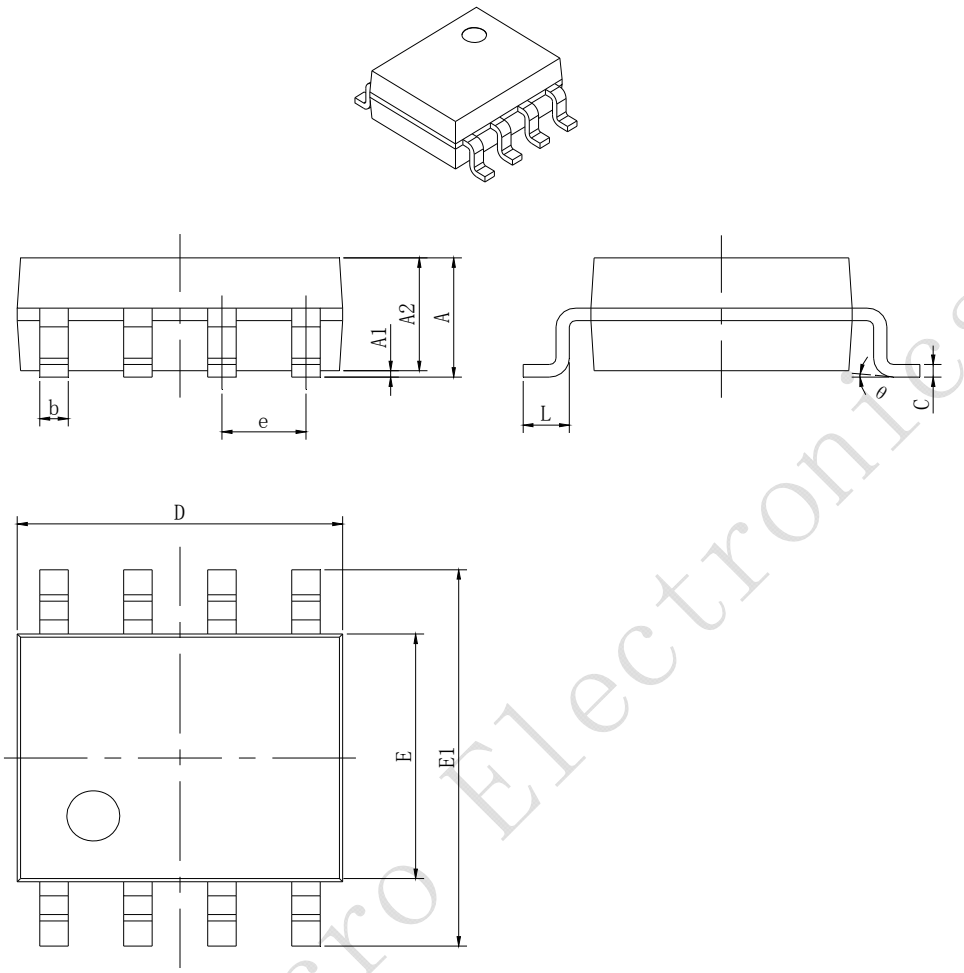


Figure 10

Legend: blue, yellow and purple is respectively curve chart when constant current value is set to 38mA, 21mA and 6mA respectively.

Package diagram（SOP8）



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

All specs and applications shown above are subject to change without prior notice.