

# LAB 01: Introduction to MARS

Saleh AlSaleh  
*salehs@kfupm.edu.sa*

King Fahd University of Petroleum and Minerals  
College of Computing and Mathematics  
Computer Engineering Department

COE301: Computer Architecture  
Term 222

# Agenda

① Personal Information

② Introduction

③ MARS Simulator

④ Demo

⑤ Grade Distribution

# Personal Information

- Name : Saleh AlSaleh
- Office Phone : +966-13-860-7035
- Office Location : Building 23 Room 10-4
- Office Hours : Tuesday and Wednesday 12:30-01:30 PM or by appointment.

# Introduction

- In this lab we will learn about 32-bit MIPS RISC (Reduced Instruction Set Computer) CPU.
- Popular Systems with MIPS CPU: Nintendo 64, Sony Playstation (Original), Sony PlayStation 2, and Sony PlayStation Portable (PSP).
- Common Uses for MIPS CPU: Embedded Systems, routers, and switches.



Sony Playstation 1



Sony Playstation 2

# Introduction

- Assembly Language is the lowest level of programming for CPUs.
- In most cases, each assembly instruction maps to one specific operation.
- An Assembler is needed to convert the assembly code to binary (0 and 1).
- MIPS has 32 General Purpose Registers: \$ 0 to \$ 31.
- Some of these registers have specific functionality (e.g. \$ sp stack pointer).

```
loop: lw    $t3, 0($t0)
      lw    $t4, 4($t0)
      add   $t2, $t3, $t4
      sw    $t2, 8($t0)
      addi  $t0, $t0, 4
      addi  $t1, $t1, -1
      bgtz  $t1, loop
```

MIPS Sample Code

# MARS Simulator

- MARS is a MIPS Assembly and Runtime Simulator.
- MARS is an integrated development environment (IDE) for programming in MIPS assembly language.
- MARS allows editing, assembling, debugging and simulating the execution of MIPS assembly language programs.
- MARS is written in Java, so it can be run on Windows, macOS, and Linux.
- There are two main windows in MARS: **Edit** Window and **Execute** Window.

# Demo

# Grade Distribution

Activity	Weight
Lab Tasks (8 Experiments)	12
Lab Quizzes (Best 3 out of 4)	3
Total	15

## Lab Work Grade Distribution

Activity	Weight
Single Cycle CPU Design	8
Pipelined CPU Design	5
Report	2
Total	15

## Lab Project Grade Distribution