## <u>Manual</u>

## **Digital Logic Design**

## IN LAB TASKS.

- 1.Implement a synchronous up down counter using D FF
- 2.Implement Asychornous ripple counter using jK FF.

## POST LAB submission.

Show that a BCD ripple counter can be constructed from a 4 bit binary ripple counter with asynchronous clear and a NAND gate that detects occurance of count 1010.