DLD LAB 6

OBJECTIVES:

- Understanding the design procedures for multiple output combinational circuit.
- Understanding the working of 2 bit binary comparator.
- Learning about the working of XNOR gate.
- To learn and understand the working of different types of decoders.
- Understanding how to design a multiple output combinational circuit using decoders.
- Function implementation by using decoders.

EQUIPMENT: Logic trainer, Logic probe

COMPONENTS: ICs 74LS08, 74LS32, 74LS04, 74LS139

THEORY:

BINARY COMPARATOR:

A combinational circuit that compares the magnitude of two binary data signals A & B and generates the results of comparison in the form of three output signals A>B, A=B, A<B is called a binary comparator. It is a multiple input and multiple output combinational circuit. When a combinational circuit has two or more than two outputs, then each output is expressed separately as a function of all inputs by using separate K-map for each output. Onebit comparator compares the magnitude of two numbers A and B, 1 bit each, and generates the comparison result. The result consists of three outputs as shown below:

L =1 if A<B

E=1 if A=B

G=1 if A>B The truth table for one bit comparator is given below.

A	B	L	E	G
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

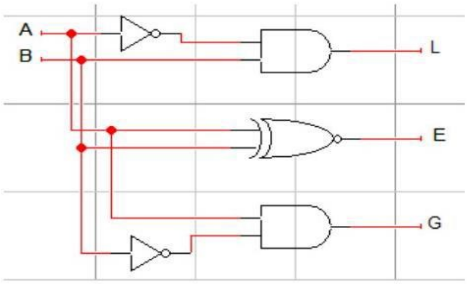
Boolean Expression for Outputs (using separate K-map for each output):

L=A'B

E=AB+A'B' (XNOR gate Boolean expression)

G=AB'

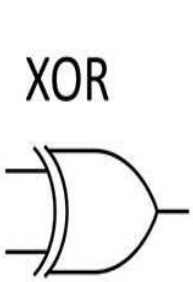
Circuit for 1 bit comparator:



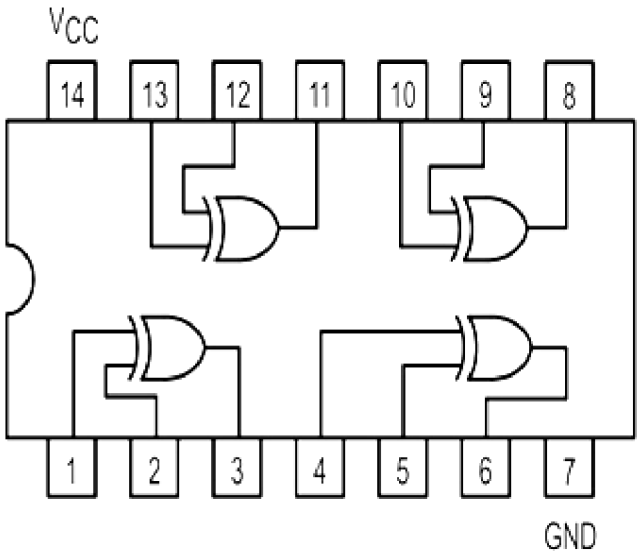
XOR gate Connection Diagram:

The IC used for XOR gate is 74LS86.

XOR



A	B	Output
0	0	0
1	0	1
0	1	1
1	1	0



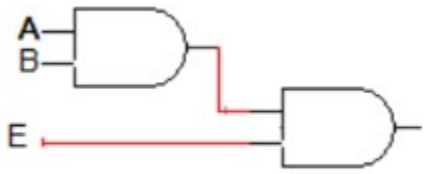
ENABLING:

Enabling is either permitting an input signal to pass through or blocking it completely. The enable bit is used to enable or disable the normal functioning of a logic circuit. A logic circuit can be enabled or disabled using a single enable bit. This enable bit can be either active low or active high. Let us have an example of an AND gate with an enable bit. If the enable bit is **active high** then the AND gate will perform its normal operation if the enable bit is one, else the output of AND gate is forced to be zero.

Truth Table:

Inputs			Output
E	A	B	$F = \begin{cases} AB & if\ E = 1 \\ 0 & otherwise \end{cases}$
0	X	X	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Circuit Diagram:

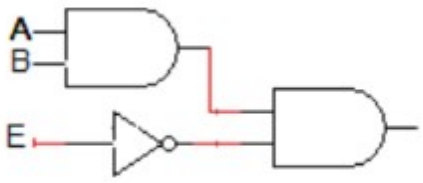


Similarly, If the enable bit is **active low** then it means that the AND gate performs normal operation if the enable bit is zero, else the output of AND gate is forced to be zero.

Truth Table:

Inputs			Output
E	A	B	$F = \begin{cases} AB & if\ E = 0 \\ 0 & otherwise \end{cases}$
1	X	X	0
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

Circuit Diagram:



Decoder:

A decoder is a combinational circuit that decodes the encoded inputs. A binary decoder has n inputs and a maximum of 2n outputs. An n-bit binary number provides 2^nminterms or maxterms. The decoder indicates one of the 2^nminterms or maxterms at the outputs based on the input combinations. The decoder that produces 2^nminterms as its outputs is said to be a decoder with active high outputs, whereas, the decoder that produces 2^nmaxterms as its outputs is said to be a decoder with active low output.

2-to-4-line decoders:

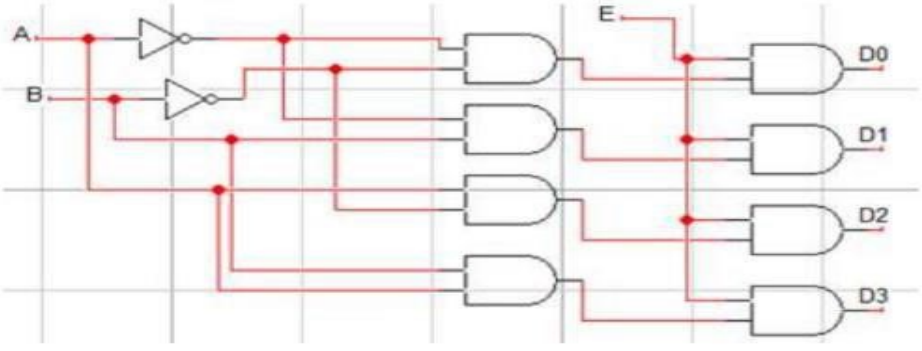
Let us take n=2 as an example, so that we obtain the 2-to-4 line decoder with active high outputs.

Truth Table:

Inputs		Outputs			
A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

The Boolean Expressions for output and the circuit diagram with **active high outputs are** as follows:

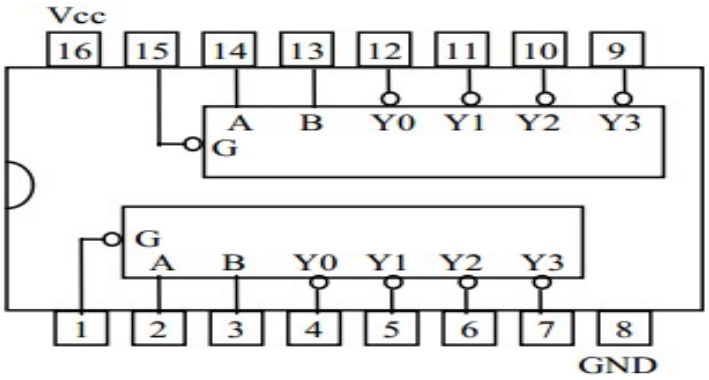
Circuit diagram for 2x4 decoder with active high outputs and active high enable:



2-to-4-line decoders with active low enables:

74LS139 IC contains two fully independent 2-to-4-line decoders with active low enables. The connection diagram for this IC is shown below:

Connection Diagram:



3-to-8 line decoders:

74LS138 IC contains 3-to-8-line decoder. The function table and connection diagram for this IC are shown below:

LAB TASKS:

IN LAB TASKS

Tasks#1:

Implement 3x8 decoder using two 2x4 and NOT gate [use decoder IC; Implement on LW, LT

Task#2

POS function using 3 to 8 decoder. Implement the combined F output only. Do on trainer.

F =ΠM(1,2,3,7)

POST LAB TASKS(ONLINE SUBMISSION)

Task #3

Implement a parity checker using decoder and OR gates

Task#4

A circuit that receives 4-bit message and output Error (E = 0) if its parity is ODD. Implement on LW

Design a combinational circuit that compares two 2-bit numbers and generates the comparison result. The result will consist of three outputs. a) Draw a truth table.

b) Find the minimal SOP expression for each of the three outputs using K-maps.

c) Implement the optimal solution in Logic works.