DLD LAB 10

FLIP FLOPS AND LATCHES

Objectives:

To learn and understand the working of Flip-Flops and Latches

Theory:

Flip Flops:

A flip-flop is a memory device that samples and acts upon its input lines only when it is told to do so with a special timing signal called the clock. This may be in the form of a level or an edge. The student should understand how a latch or flip-flop works to hold the data set and reset states.

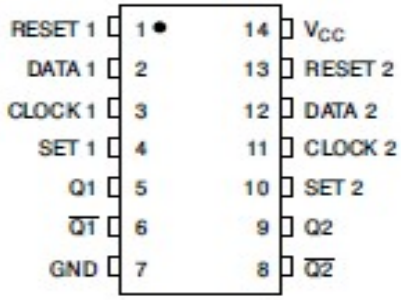
D Flip Flop:

D flip flops are considered as one bit memory. The D stands for data. This flip flop stores the value that is on the data line.

Pin Configuration:

This device contains two independent positive-edge-triggered D-type flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. Low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

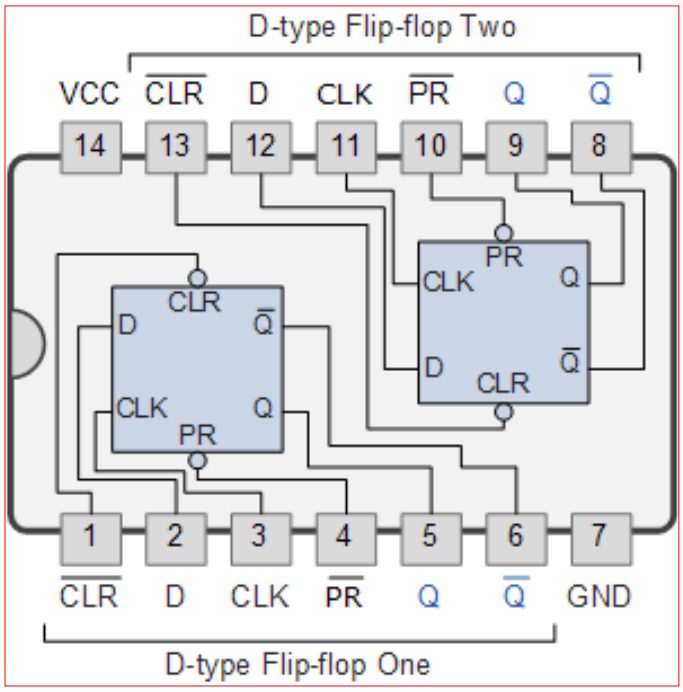
PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↓	H	H	L
H	H	↓	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↑	X	No Change	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

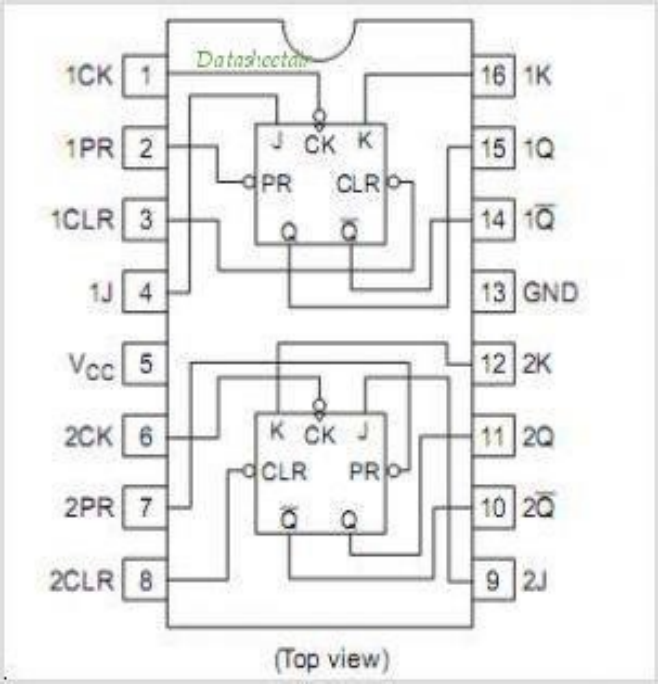


JK Flip Flop:

This device contains two independent negative-edge-triggered JK-type flip-flops with complementary outputs. The information on the J and K is accepted by the flip-flops on the negative going edge of the clock pulse. Low

logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Pin Configuration:



Function Table:

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FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

LAB TASKS:

Task #1: Construct a T flip flop from D flip flop.

a) Draw a truth table.
b) Draw the logic diagram.
c) Implement on Hardware and Software.

Task #2: Implement an SR latch using NAND gates on Logic Works with control input as follows:

C	S	R	Q(t+1)
0	X	X	No Change
1	0	0	No Change
1	0	1	Q=0 ,Reset State
1	1	0	Q=1, Set State
1	1	1	Undefined

Task 3 : USE a D FF to build JK flipflop

TASK 4 : IMPLEMENT A + VE EDGE TRIGGERED MASTER SLAVE Dtype FF.