Digital Logic Design

Lecture 17

Selecting

- **Selecting of data or information is a critical function in digital systems and computers**
- **Circuits that perform selecting have:**
  - **A set of information inputs from which the selection is made**
  - **A single output**
  - **A set of control lines for making the selection**
- **Logic circuits that perform selecting are called *multiplexers***
- **Selecting can also be done by three-state logic or transmission gates**

Multiplexers

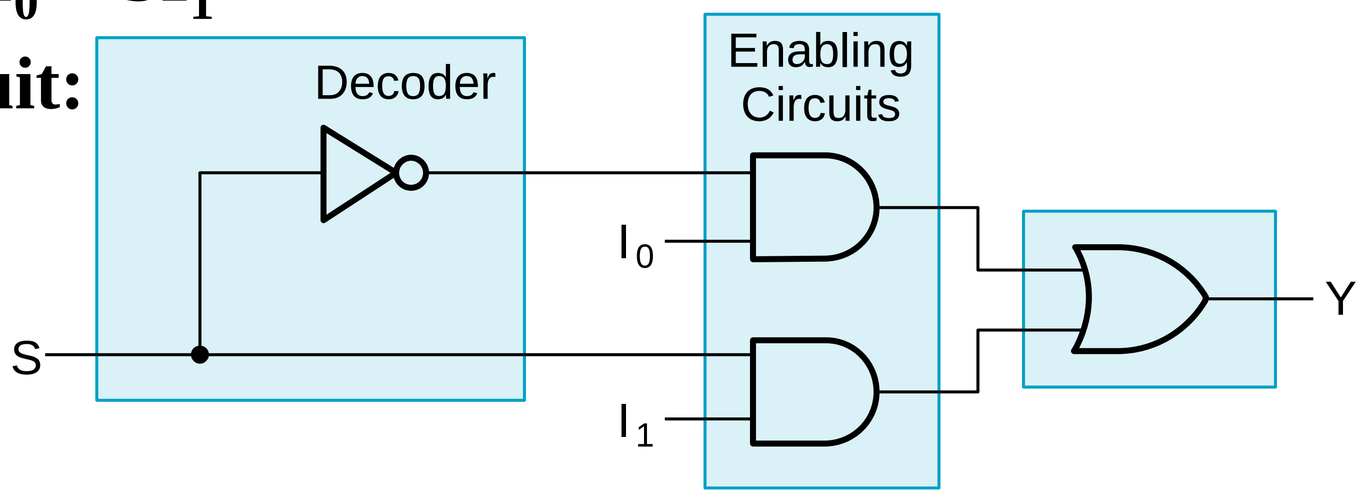
- **A multiplexer selects information from an input line and directs the information to an output line**
- **A typical multiplexer has *n* control inputs (S_{n-1}, … S_0) called *selection inputs*, 2^n information inputs (I_{2^n-1}, … I_0), and one output Y**
- **A multiplexer can be designed to have *m* information inputs with $m < 2^n$ as well as *n* selection inputs**

2-to-1-Line Multiplexer

- Since $2 = 2^1$, $n = 1$
- The single selection variable S has two values:
  - ⓾ $S = 0$ selects input I_0
  - ⓾ $S = 1$ selects input I_1
- The equation:

$$Y = \overline{S}I_0 + SI_1$$

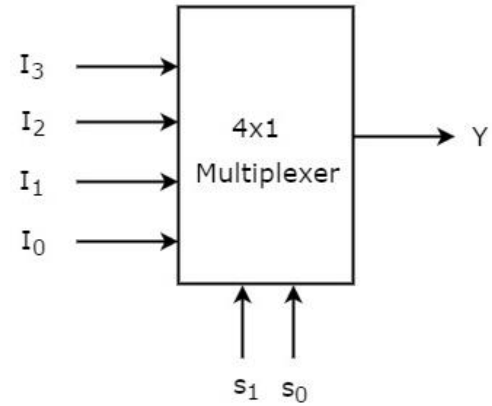
- The circuit:



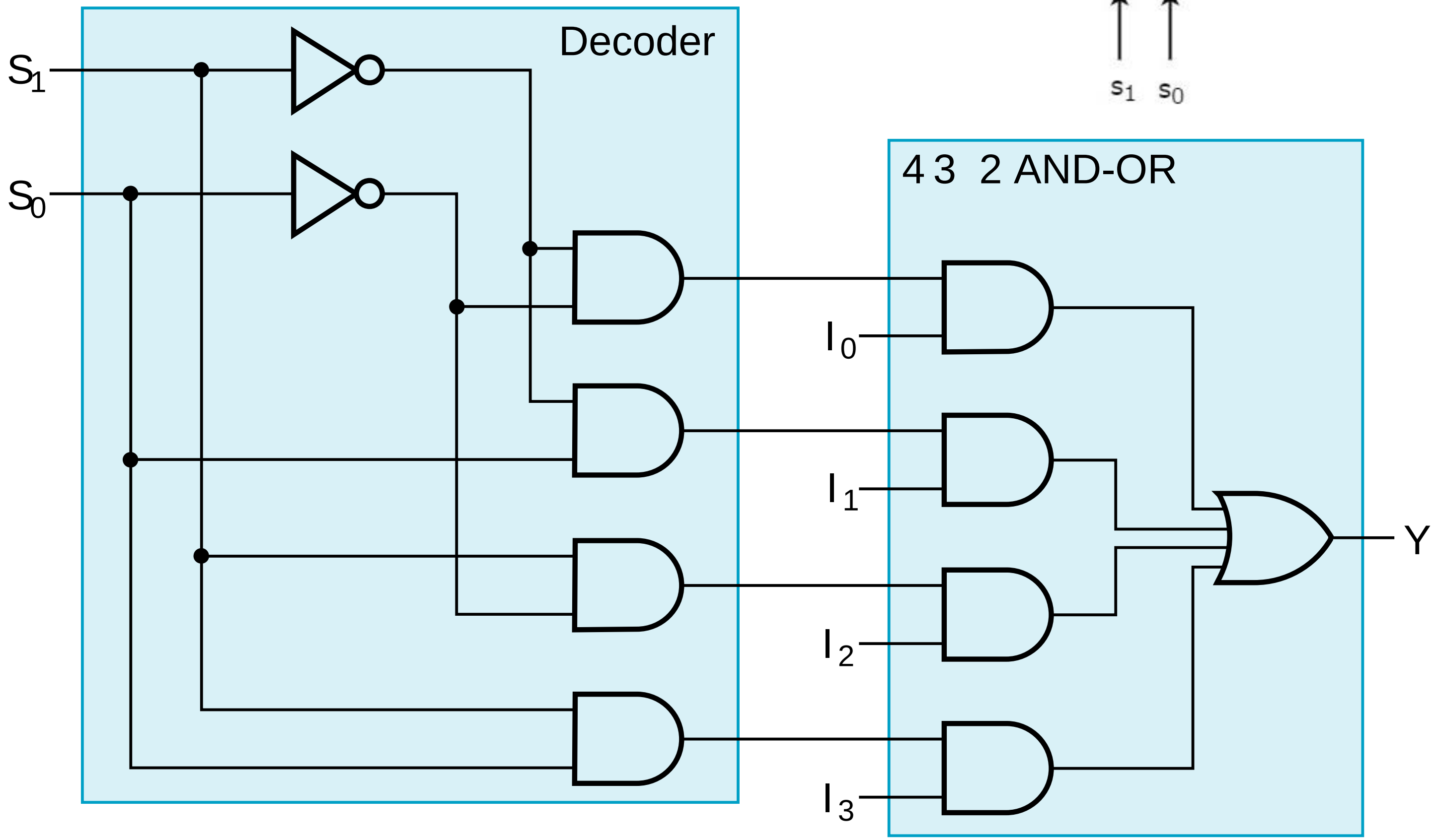
2-to-1-Line Multiplexer (continued)

- **Note the regions of the multiplexer circuit shown:**
  - **1-to-2-line Decoder**
  - **2 Enabling circuits**
  - **2-input OR gate**
- **To obtain a basis for multiplexer expansion, we combine the Enabling circuits and OR gate into a 2 × 2 AND-OR circuit:**
  - **1-to-2-line decoder**
  - **2 × 2 AND-OR**
- **In general, for an 2^n-to-1-line multiplexer:**
  - **n-to-2^n-line decoder**
  - **$2^n \times 2$ AND-OR**

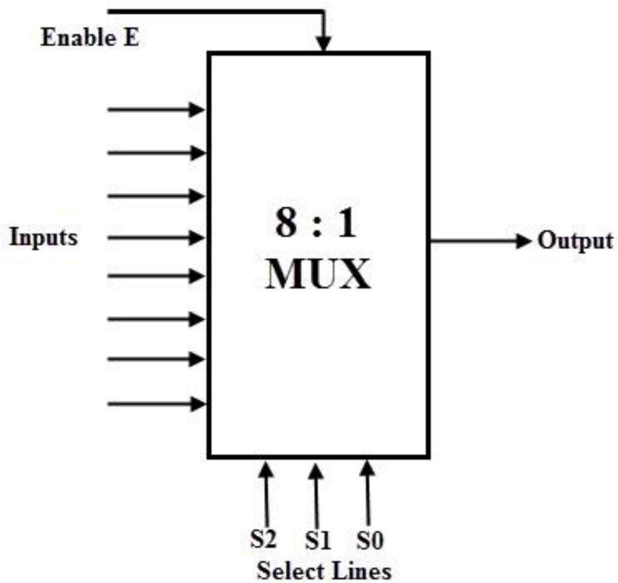
Example: 4-to-1-line Multiplexer



- 2-to-2^2-line decoder
- $2^2 \times$ 2 AND-OR

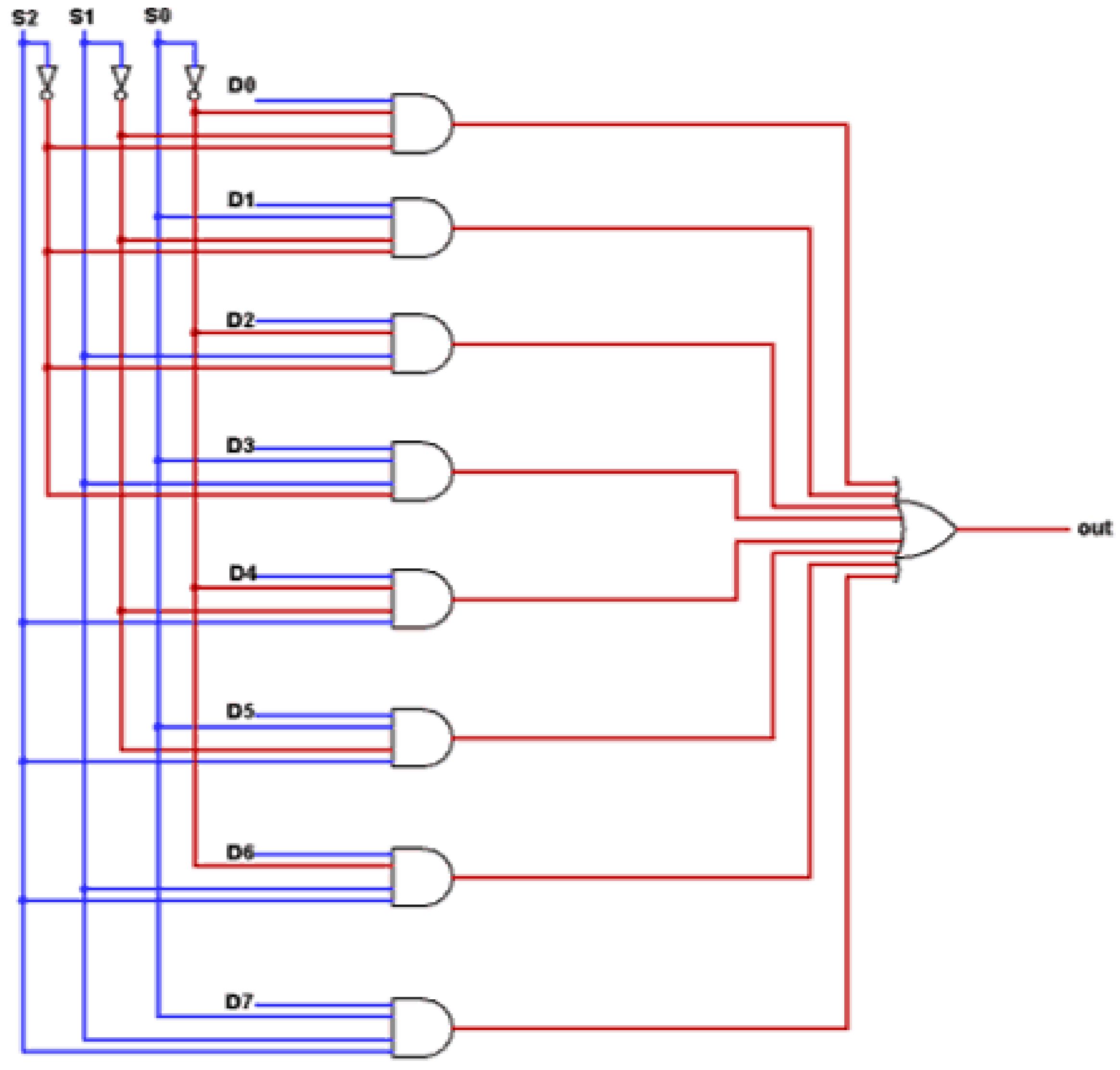


Example: 8-to-1-line Multiplexer



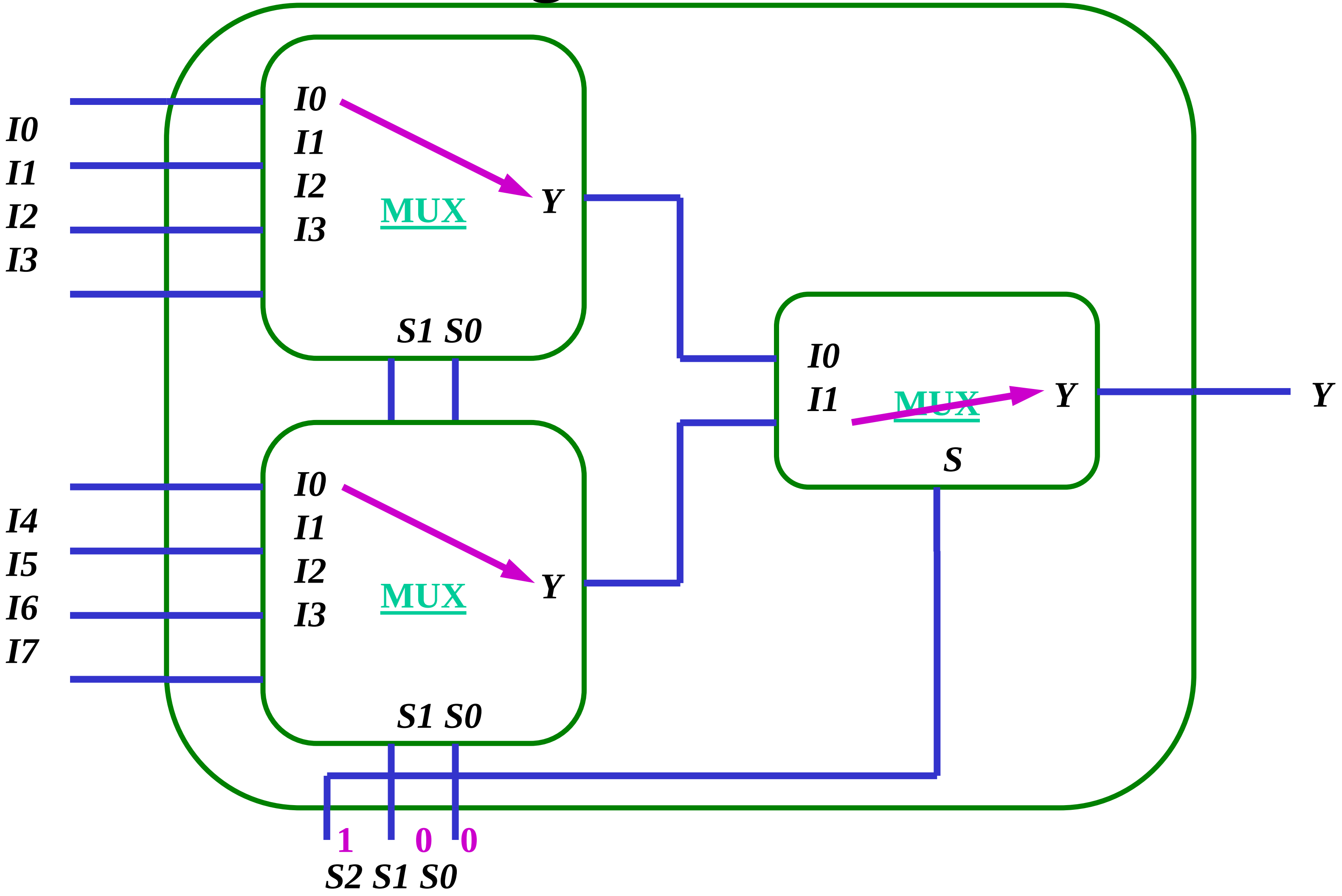
Select Data Inputs			Output
S_2	S_1	S_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

Example: 8-to-1-line Multiplexer



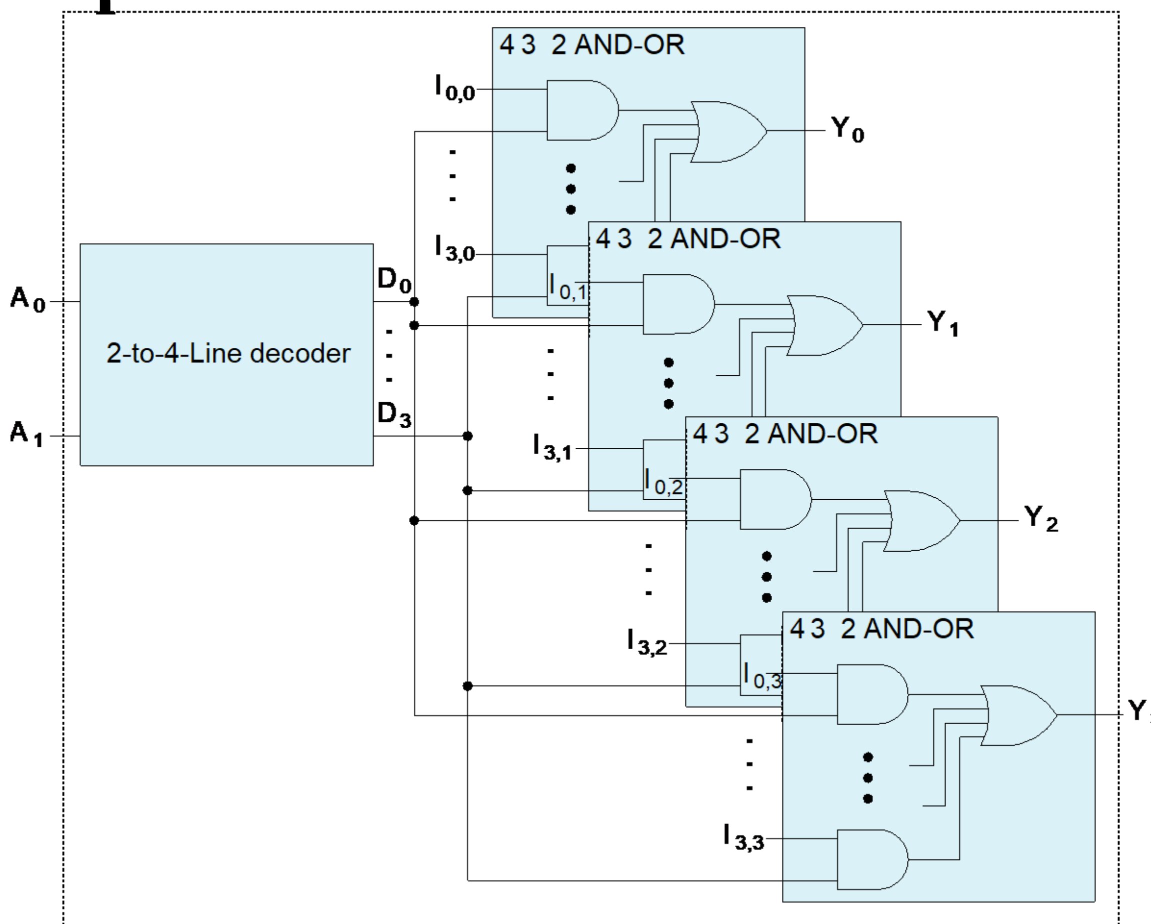
Multiplexer Expansion

- **8-to-1 MUX using Dual 4-to-1 MUX**



Multiplexer Width Expansion

- Select "vectors of bits" instead of "bits"
- Use multiple copies of $2^n \times 2$ AND-OR in parallel
- Example: 4-to-1-line quad multi-plexer



Combinational Circuits using Multiplexer

Approach 1: Using n number of selection lines

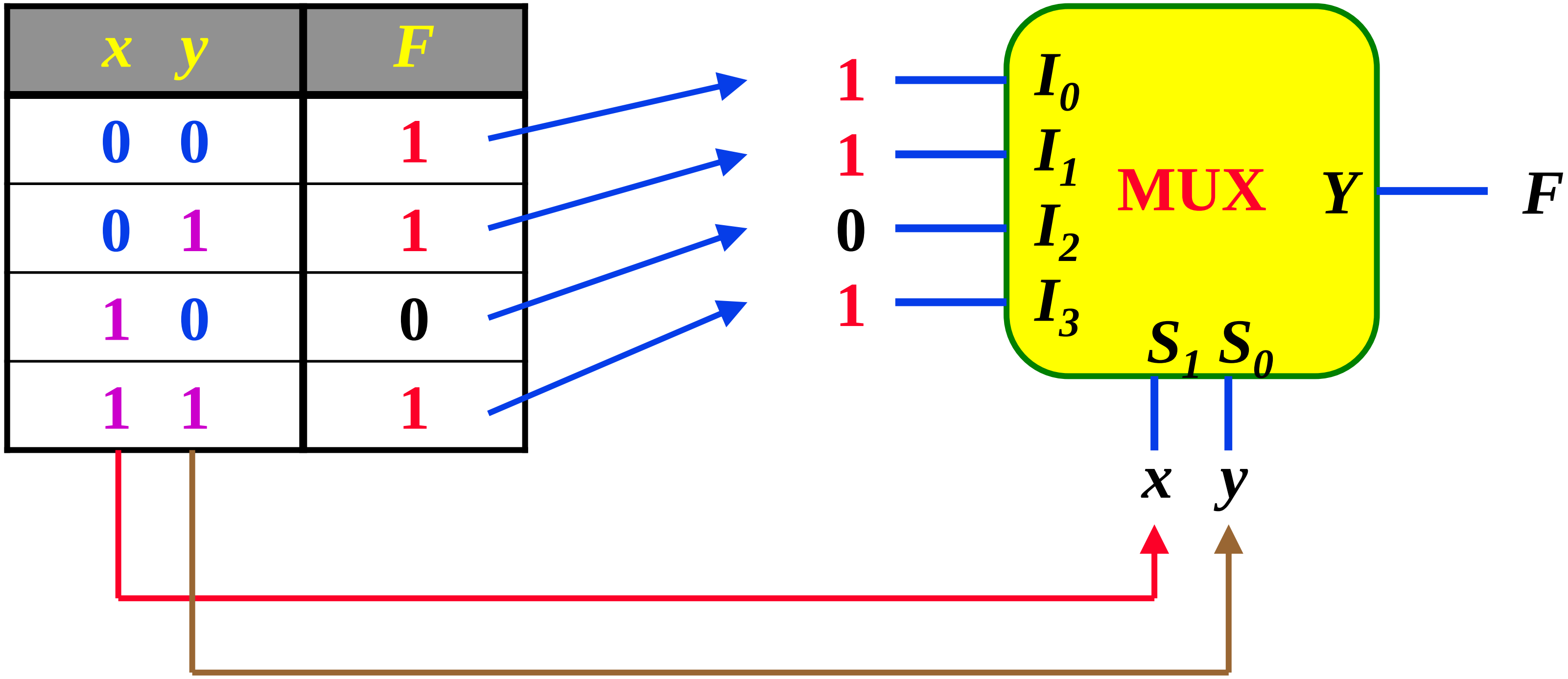
Approach 2: Using n-1 number of selection lines

Implementation Using Multiplexers

★ **Example**

$$F(x, y) = \sum(0, 1, 3)$$

x	y	F
0	0	1
0	1	1
1	0	0
1	1	1

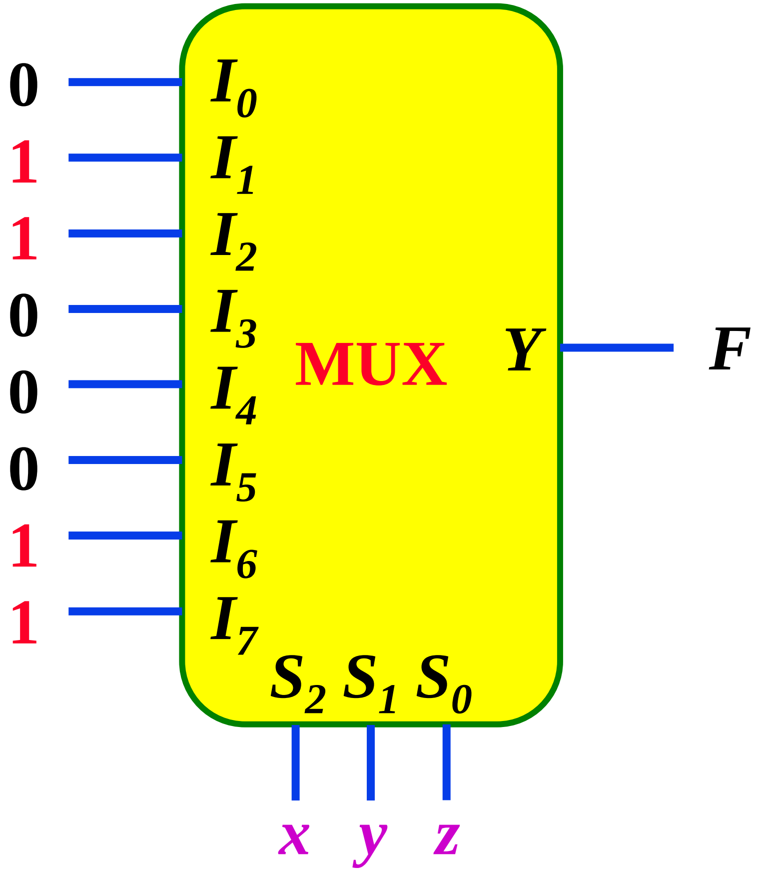


Implementation Using Multiplexers

★ **Example**

$F(x, y, z) = \sum(1, 2, 6, 7)$

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

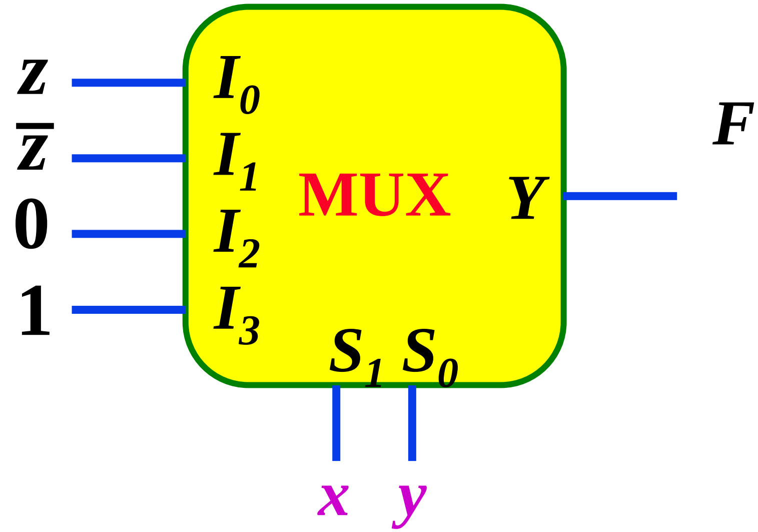


Implementation Using Multiplexers

★ **Example**

$F(x, y, z) = \sum(1, 2, 6, 7)$

x	y	z	F	
0	0	0	0	$F = z$
0	0	1	1	
0	1	0	1	$F = \overline{z}$
0	1	1	0	
1	0	0	0	$F = 0$
1	0	1	0	
1	1	0	1	$F = 1$
1	1	1	1	

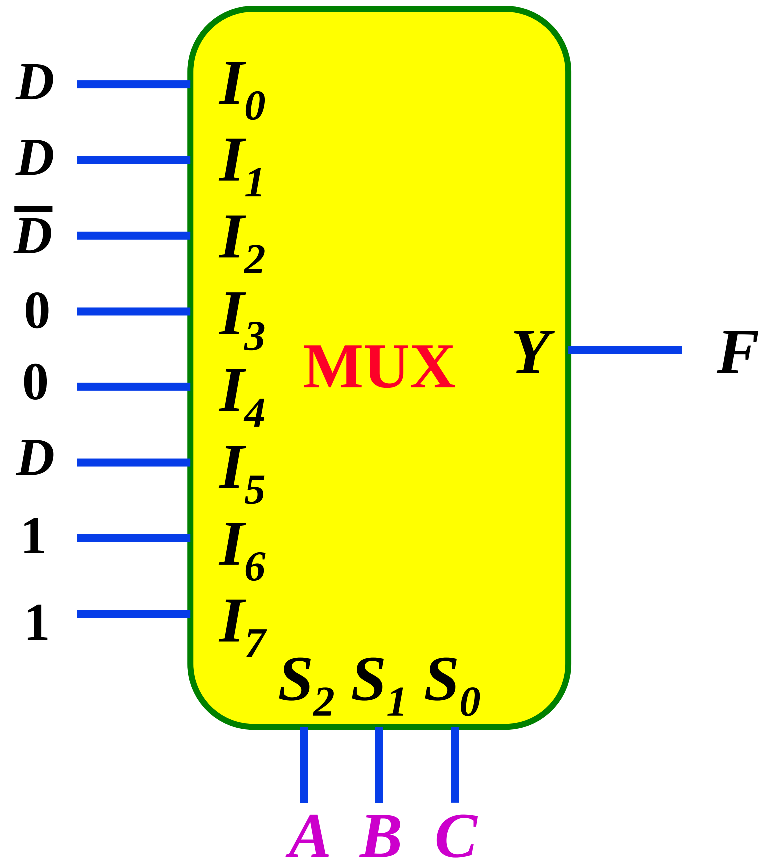


Implementation Using Multiplexers

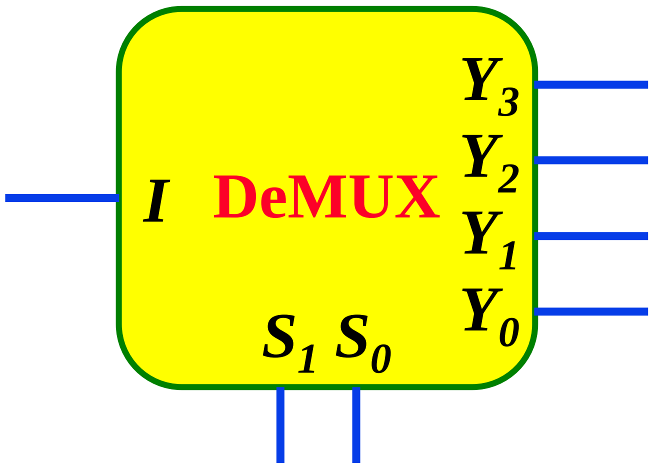
★ **Example**

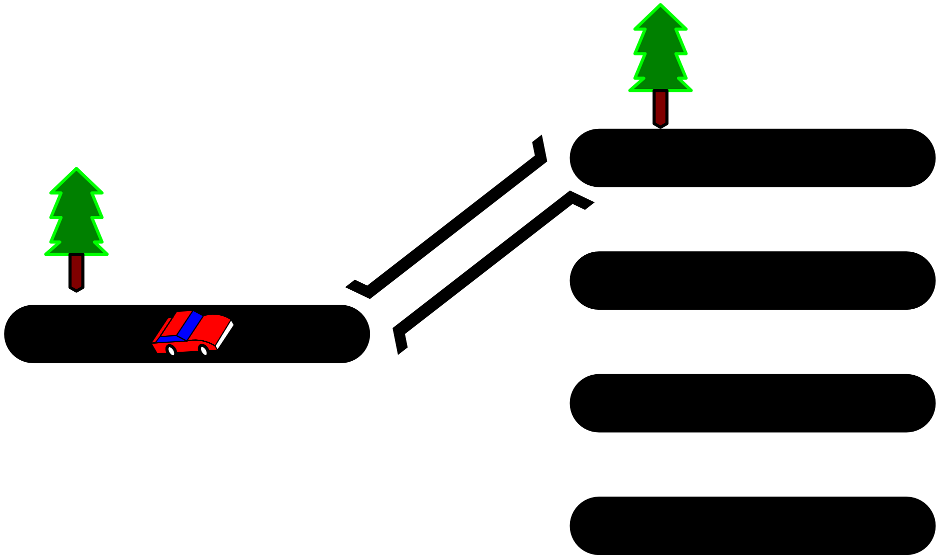
$F(A, B, C, D) = \sum(1, 3, 4, 11, 12, 13, 14, 15)$

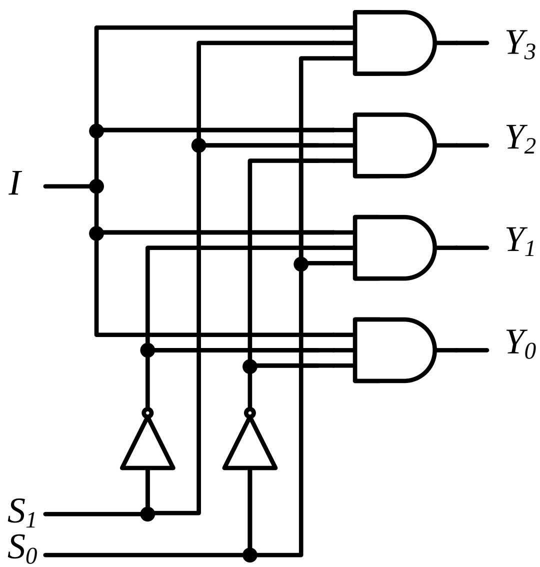
A B C D				F	
0	0	0	0	0	$F = D$
0	0	0	1	1	
0	0	1	0	0	$F = D$
0	0	1	1	1	
0	1	0	0	1	$F = \overline{D}$
0	1	0	1	0	
0	1	1	0	0	$F = 0$
0	1	1	1	0	
1	0	0	0	0	$F = 0$
1	0	0	1	0	
1	0	1	0	0	$F = D$
1	0	1	1	1	
1	1	0	0	1	$F = 1$
1	1	0	1	1	
1	1	1	0	1	$F = 1$
1	1	1	1	1	



DeMultiplexers

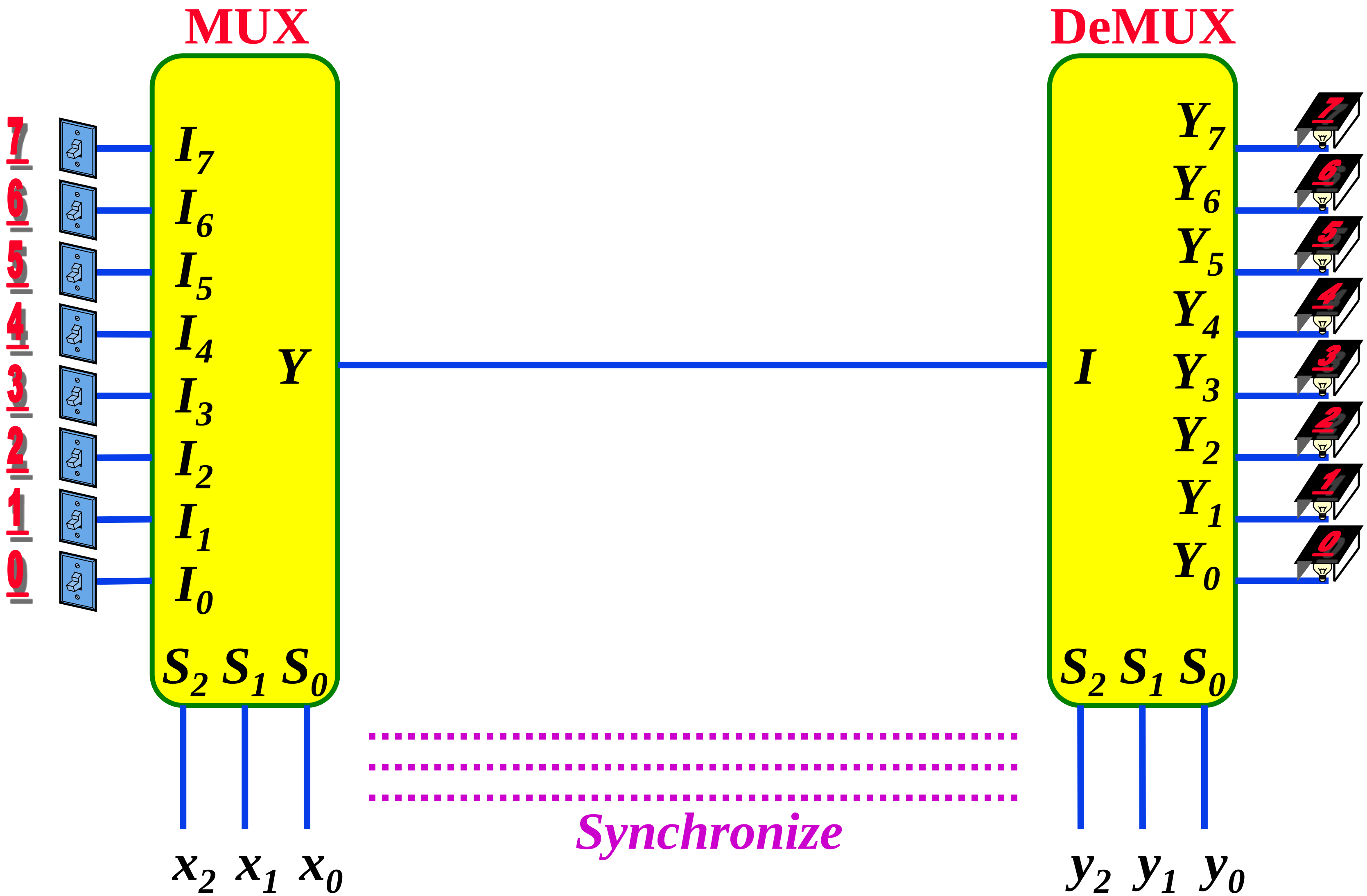




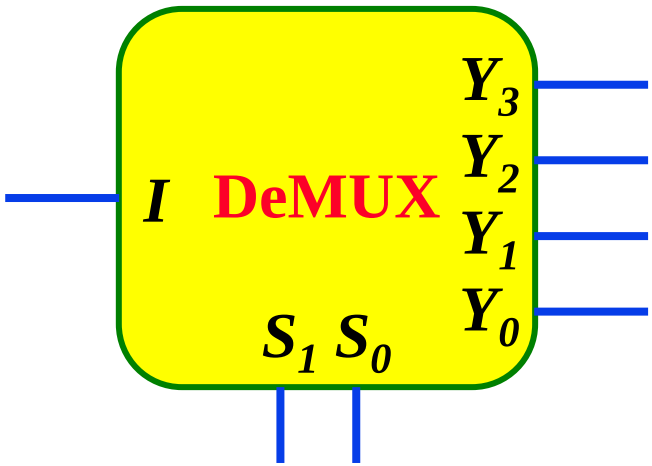


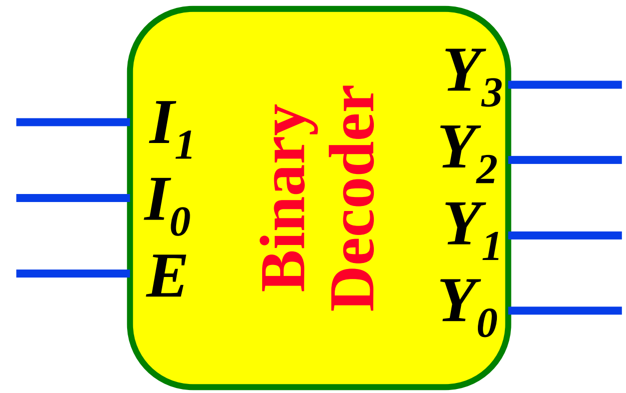
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

Multiplexer / DeMultiplexer Pairs



DeMultiplexers / Decoders





S_1 S_0	Y_3	Y_2	Y_1	Y_0
0 0	0	0	0	I
0 1	0	0	I	0
1 0	0	I	0	0
1 1	I	0	0	0

E	I_1 I_0	Y_3 Y_2 Y_1 Y_0
0	x x	0 0 0 0
1	0 0	0 0 0 1
1	0 1	0 0 1 0
1	1 0	0 1 0 0
1	1 1	1 0 0 0

Half Adder

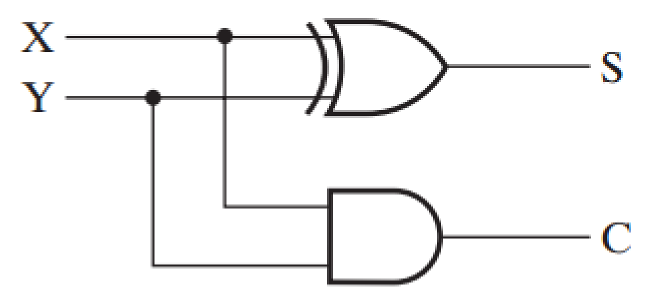
- **A half adder is an arithmetic circuit that generates the sum of two binary digits.**
- **The circuit has two inputs and two outputs.**

Truth Table of Half Adder

Inputs		Outputs	
X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$$S = \overline{X}Y + X\overline{Y} = X \oplus Y$$

$$C = XY$$



Full Adder

- **A full adder is a combinational circuit that forms the arithmetic sum of three input bits.**
- **Besides the three inputs, it has two outputs.**

Truth Table of Full Adder

Inputs			Outputs	
X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$S = \overline{X}\,\overline{Y}Z + \overline{X}Y\overline{Z} + X\overline{Y}\,\overline{Z} + XYZ$$

$$C = XY + XZ + YZ$$

K-map: For sum

X \ YZ	00	01	11	10
0		1		1
1	1		1	

$$S = \overline{X}\,\overline{Y}Z + \overline{X}Y\overline{Z} + X\overline{Y}\,\overline{Z} + XYZ$$

$$= \overline{X}(\overline{Y}Z + Y\overline{Z}) + X(\overline{Y}\,\overline{Z} + Y Z)$$

$$= \overline{X}(Y \oplus Z) + X\,(Y \odot Z)$$

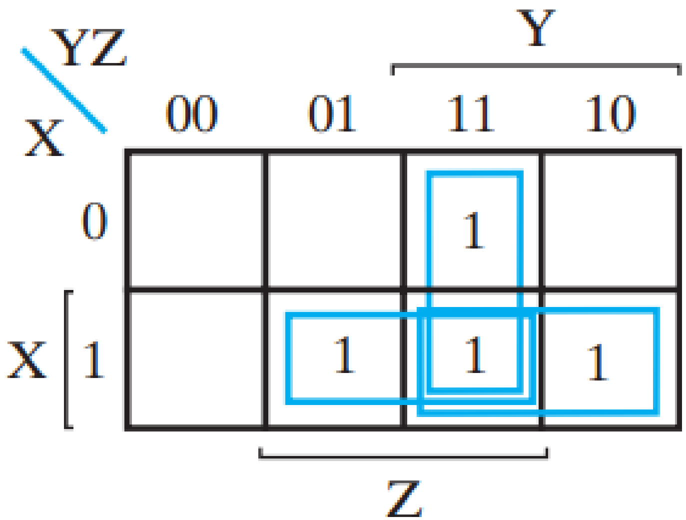
Lets say $Y \oplus Z = A$, $Y \odot Z = \overline{A}$

$$= \overline{X}A + X\overline{A}$$

$$= X \oplus A$$

$$= X \oplus Y \oplus Z$$

K-map: For Carry



$$
\begin{aligned}
C &= XY + XZ + YZ \\
&= XY + Z(X\overline{Y} + \overline{X}Y) \\
&= XY + Z(X \oplus Y)
\end{aligned}
$$

$$
\begin{aligned}
C &= XY + XZ + YZ \\
&= XY + XZ + YZ\,(X + X') \\
&= XYZ + XY + XZ + X'YZ \\
&= XY(Z+1) + XZ + X'YZ \\
&= XY + XZ + X'YZ \\
&= XY + XZ\,(Y + Y') + X'YZ \\
&= XY + XYZ + XY'Z + X'YZ \\
&= XY\,(1 + Z) + XY'Z + X'YZ \\
&= XY + XY'Z + X'YZ \\
&= XY + Z\,(XY' + X'Y) \\
&= XY + Z\,(X \oplus Y)
\end{aligned}
$$