KHULNA UNIVERSITY OF ENGINEERING & TECHNOLOGY

Course Name: Digital Logic Design Laboratory

Course No: CSE1204

Digital Clock with Exclusion of 44 in Display

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OBJECTIVES:

1. The primary objective of this project was to design and implement a digital clock using flip flops and logic gates.
2. The clock actually operates on a unique timekeeping mechanism where 1 minute is equivalent to 59 seconds, and 1 hour is equivalent to 59 minutes
3. Additionally, the clock was designed to exclude the number '44' from both the minute's and second's display.

INTRODUCTION:

Logisim is a powerful and user-friendly digital circuit design simulation tool. It allows user to create , edit and simulate digital logic circuits, making it an excellent platform for learning digital electronics and designing various digital systems. In this project, we tried to make a clock that has 59 seconds in a minute and 59 minutes in an hour, the 44^{th} number was skipped in the process. Skipping a certain number from a regular clock circuit was a bit difficult to implement. Though we successfully designed and implemented the circuit as per requirements.

COMPONENTS:

Serial No.	Component
1	AND Gates
2	OR Gates
3	NOT Gates
4	XNOR Gates
5	D FlipFlops
6	T FlipFlops
7	7 Segment Display
8	Logisim Software

TRUTHTABLES & EQUATIONS:

1. Truth-table for Mod-6 counter:

	Current States			Next States			D Flipflop		
	QA	QB	QC	QA+	QB+	QC+	D_{QA}	D_{QB}	D_{QC}
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	0
2	0	1	0	0	1	1	0	1	1
3	0	1	1	1	0	0	1	0	0
4	1	0	0	1	0	1	1	0	1
5	1	0	1	0	0	0	0	0	0

D_{QA} = QAQC'+QBQC

D_{QB} = QBQC'+QA'QB'QC

D_{QC} = QC'

2. Truth-table for Mod-10 counter:

	Current States				Next States				D Flipflop			
	QA	QB	QC	QD	QA+	QB+	QC+	QD+	D_{QA}	D_{QB}	D_{QC}	D_{QD}
0	0	0	0	0	0	0	0	1	0	0	0	1
1	0	0	0	1	0	0	1	0	0	0	1	0
2	0	0	1	0	0	0	1	1	0	0	1	1
3	0	0	1	1	0	1	0	0	0	1	0	0
4	0	1	0	0	0	1	0	1	0	1	0	1
5	0	1	0	1	0	1	1	0	0	1	1	0
6	0	1	1	0	0	1	1	1	0	1	1	1
7	0	1	1	1	1	0	0	0	1	0	0	0
8	1	0	0	0	1	0	0	1	1	0	0	1
9	1	0	0	1	0	0	0	0	0	0	0	0

D_{QA} = QA+QBQCQD

D_{QB} =QCQD'+QA'QC'QD

D_{QC} = QBQC'+QBQD'+QB'QCQD

D_{QD} = QD'

3. Truth-table for Mod-10(4 skip) counter:

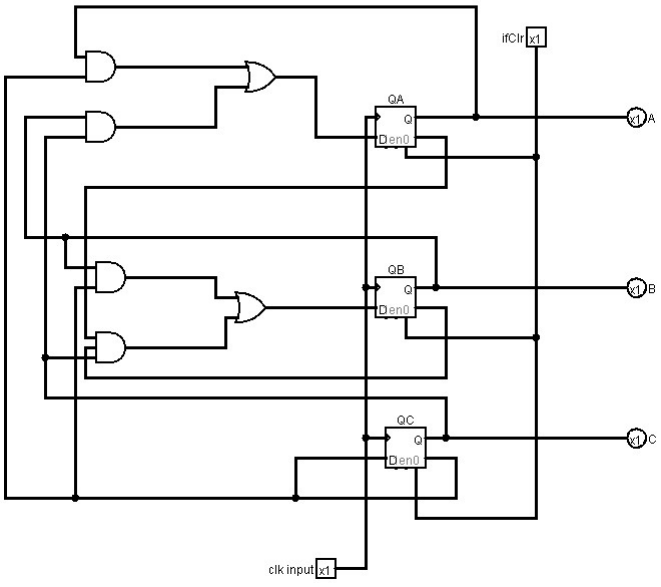
	Current States				Next States				T Flipflop			
	QA	QB	QC	QD	QA+	QB+	QC+	QD+	T_{QA}	T_{QB}	T_{QC}	T_{QD}
0	0	0	0	0	0	0	0	1	0	0	0	1
1	0	0	0	1	0	0	1	0	0	0	1	1
2	0	0	1	0	0	0	1	1	0	0	0	1
3	0	0	1	1	0	1	0	0	0	1	1	0
4	0	1	0	1	0	1	1	0	0	0	1	1
5	0	1	1	0	0	1	1	1	0	0	0	1
6	0	1	1	1	1	0	0	0	1	1	1	1
7	1	0	0	0	1	0	0	1	0	0	0	1
8	1	0	0	1	0	0	0	0	1	0	0	1

T_{QA} = QD'+QB+QC'
T_{QB} = QBQCQD'+QB'QCQD
T_{QC} = QBQD'+QB'QD
T_{QD} = QA+QBQCQD'

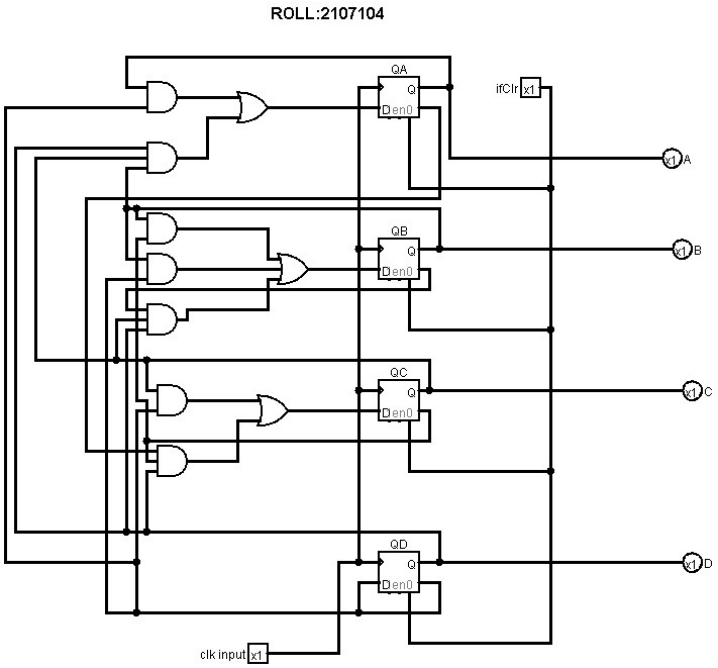
CIRCUIT DIAGRAMS:

1. Mod-6 Counter: Here we used 3 D flip-flops and 2 inputs. Clock input used for getting synchronous pulse and ifclr used for getting the reset state.

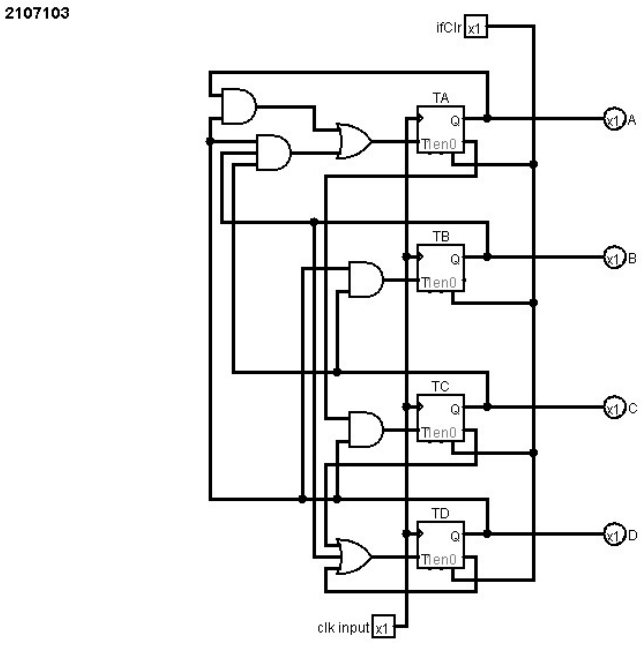
Roll:2107104



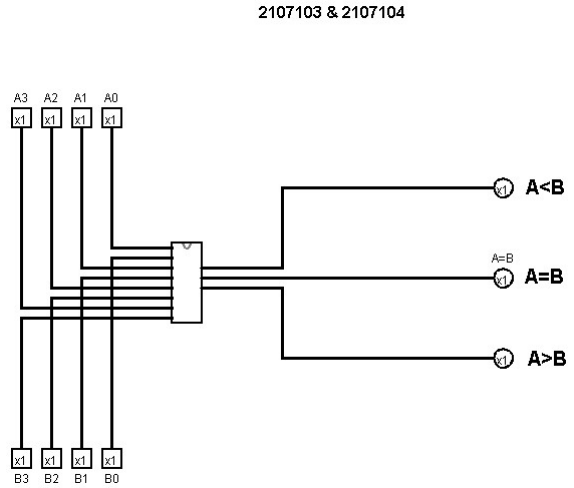
2. Mod-10 Counter: Here we used 4 D flip-flops and 2 inputs. Clock input used for getting synchronous pulse and ifclr used for getting the reset state.



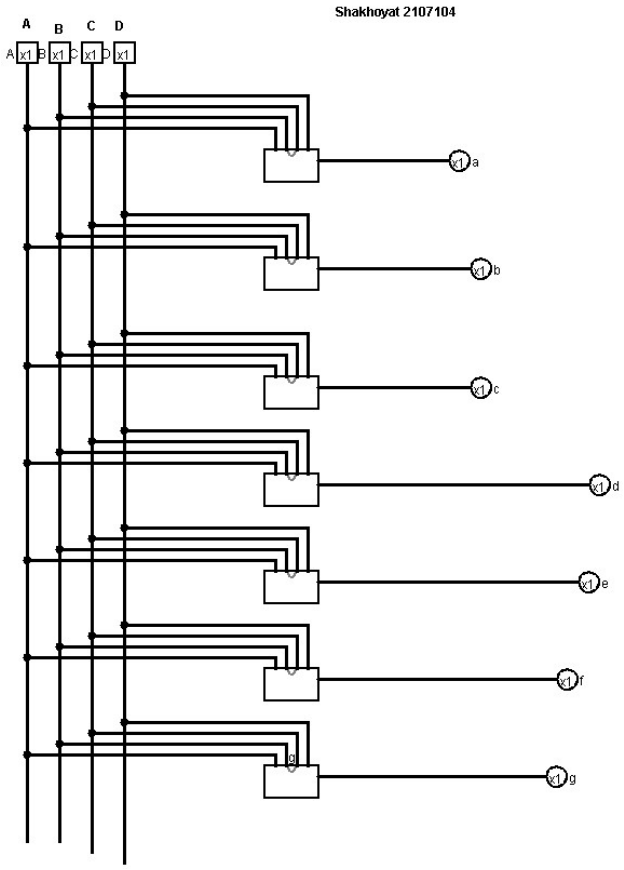
3. Mod-10 Counter(skips 4): Here we used 4 D flip-flops and 2 inputs. Clock input used for getting synchronous pulse and ifclr used for getting the reset state. The basic difference is its skipping the digit 4.



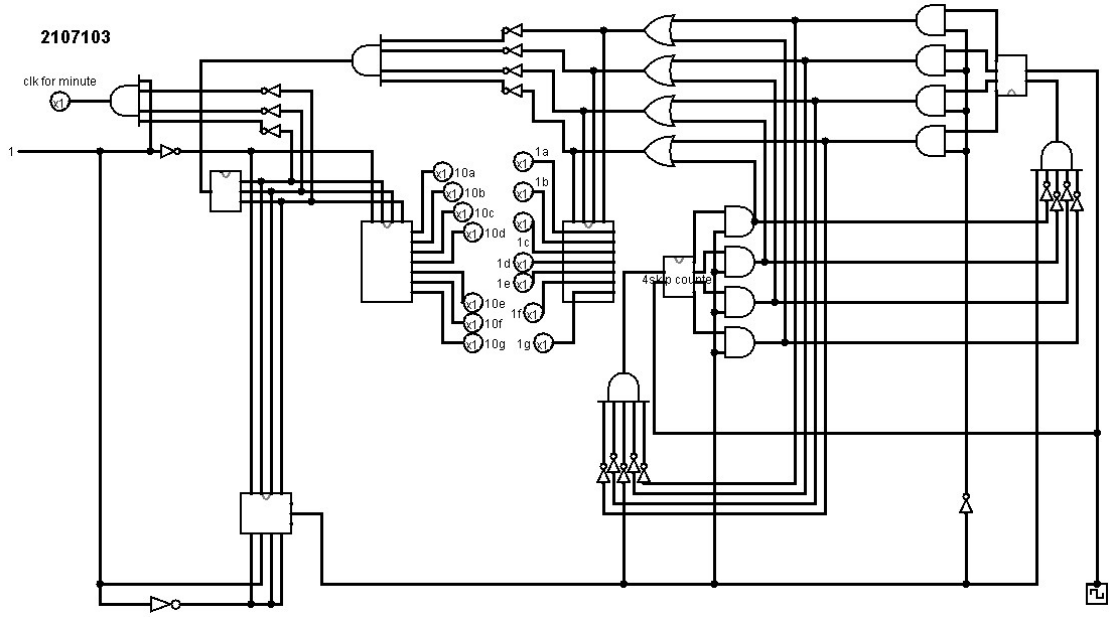
4. 4 Bit Comparator:



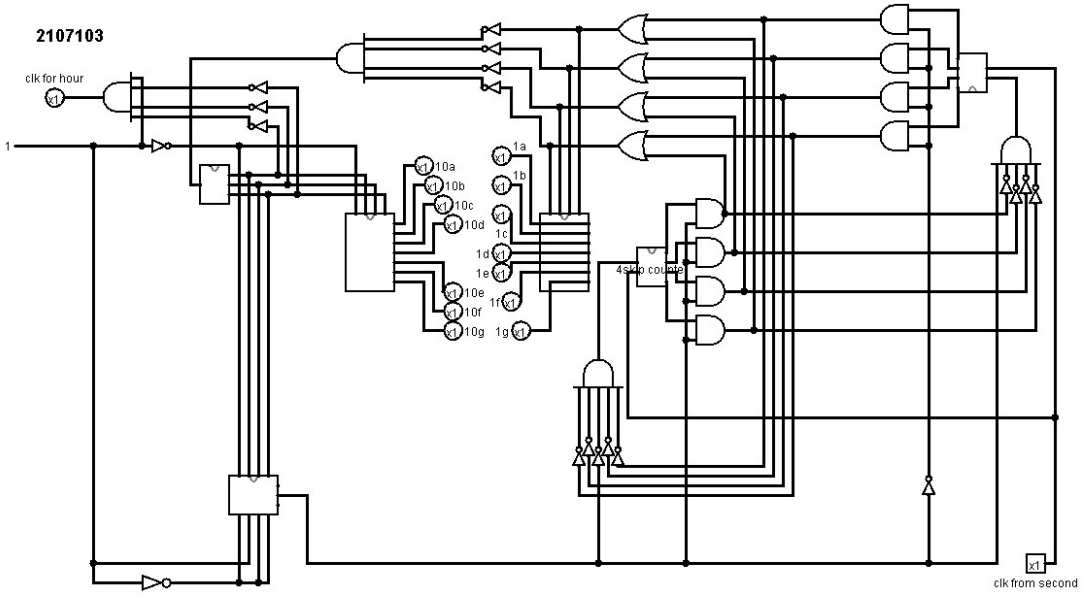
5. BCD to 7 Segment Decoder:



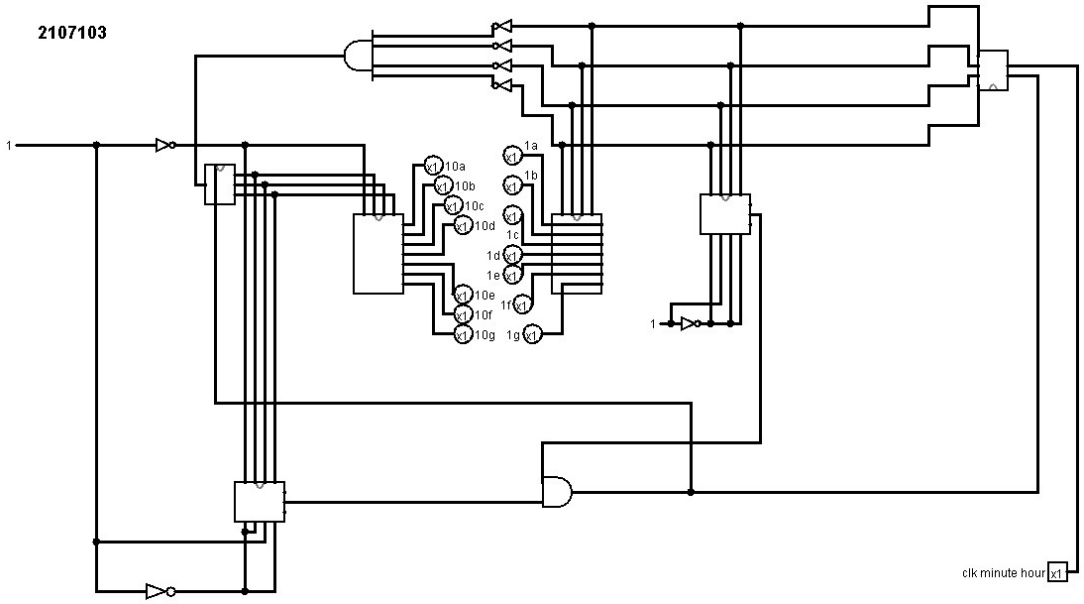
6. Second Circuit:



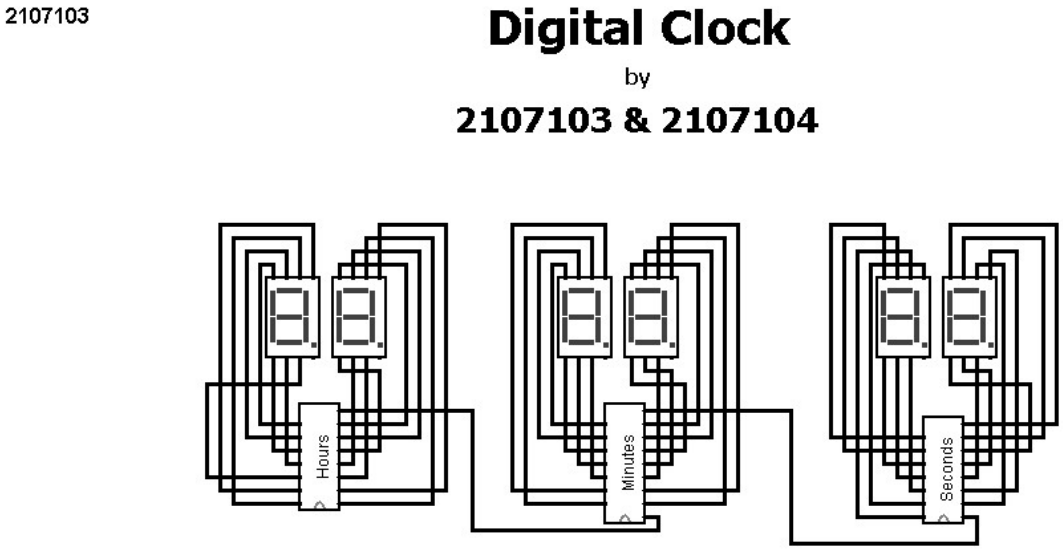
7. Minute Circuit:



8. Hour Circuit:



9. Final Clock:



WORK FLOW:

1. Second/Minute Circuit: At the beginning, the clock pulse goes to the Mod-10 counter, whenever the mod 10 counter hits 0 it passes a pulse to Mod-6 counter. When the Mod-6 counter hits 4, the output of Mod-10 counter is ignored and the output of Mod-10(4 skip) counter is used. And when both the counters hits 0, one pulse goes to Minute/Hour circuit.

2. Hour Circuit: At the beginning, the pulse from the minute circuit goes to the Mod-10 counter, whenever the Mod-10 counter hits zero it passes a pulse to Mod-6 counter. And when the Mod-6 counter hits 2 and Mod-10 counter hits 4 a pulse goes to the ifClr input of the counters which sets the both counters to reset states.

DISCUSSION & CONCLUSION:

Through the project, we learned how we can design and implement a critical circuits by ourselves. As the circuits are quite complex, there are too many logic gates used. Which may occur some unexpected time delay in the output. If implementation on the circuit level could be more optimized then it could be far better minimizing the time delay. So we could have been more cautious while implementing and choosing the circuits we chose for the project to avoid this unexpected time delay that we are having.