



Design of a Phase Locked Loop (PLL) Circuit

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-

Outlines



PLL Introduction
[Pages: 3 to 12]



**Condition for the
locked/steady state**
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**Discussion on the PLL
Design (Mostly
Theoretical)**
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Phase Frequency Detector
Charge Pump and Loop Filter
Voltage Controlled Oscillator
Divider Circuits
Whole Circuit Schematic and
Layout example
Results



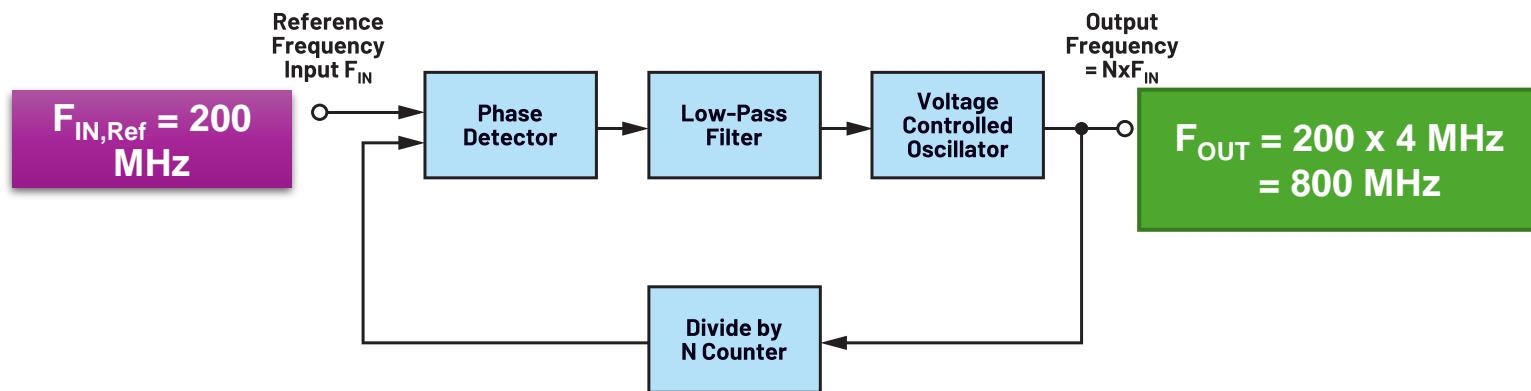
**Step by Step Design
Guide of PLL in
Cadence**
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References
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INTRODUCTION

- ❖ Feedback Control Circuit
- ❖ Frequency and Phase of
→ output signal \propto Input Signal

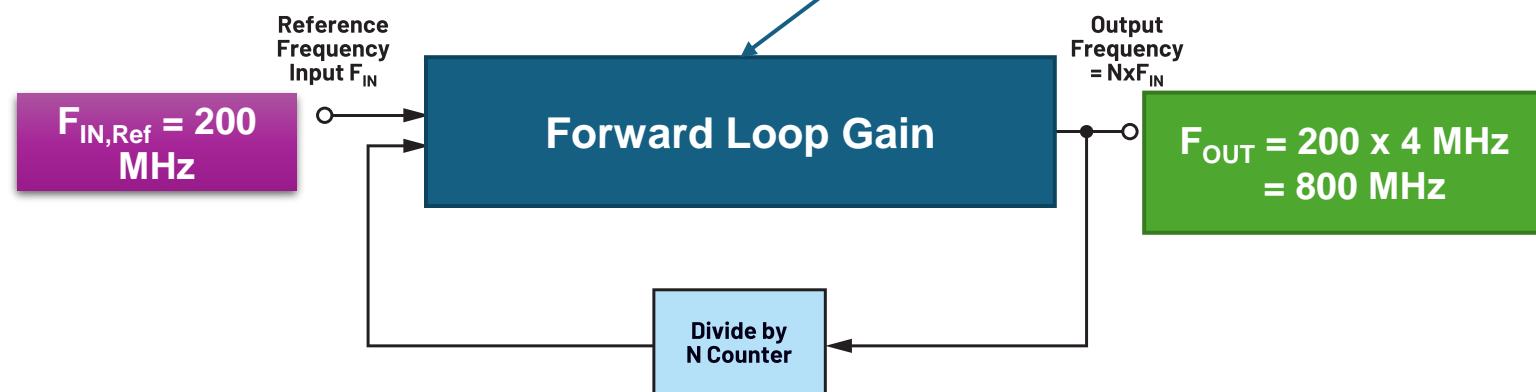


INTRODUCTION

- ❖ Feedback Control Circuit
- ❖ Frequency and Phase of

→ output signal \propto Input Signal

Simplify and let's call it
“Forwards Loop Gain”

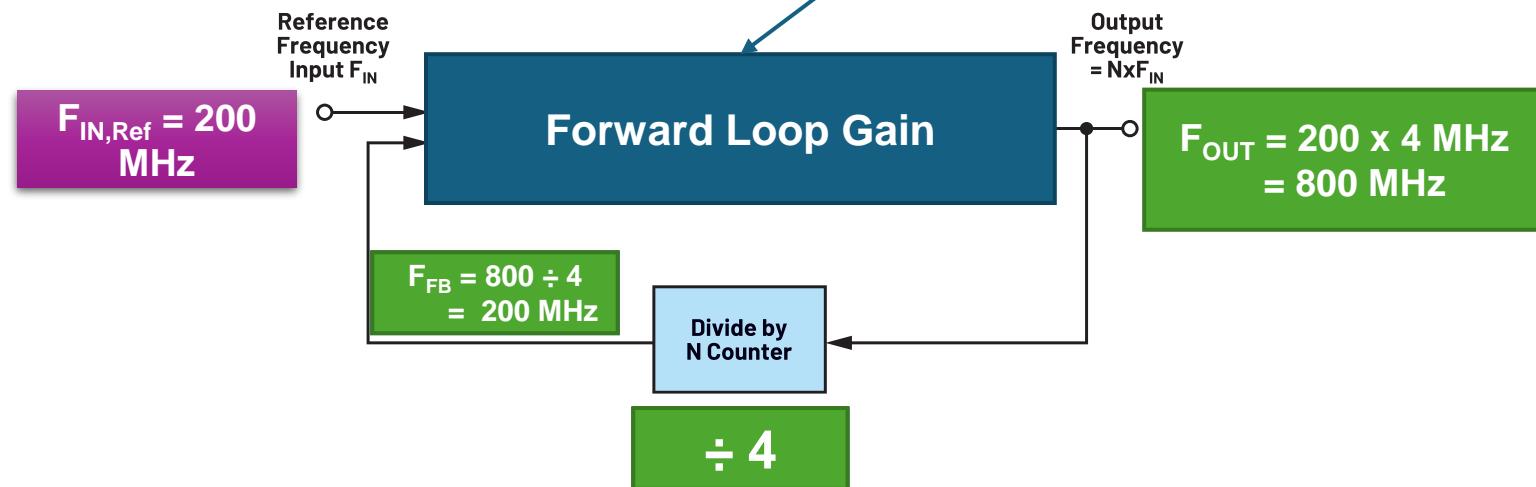


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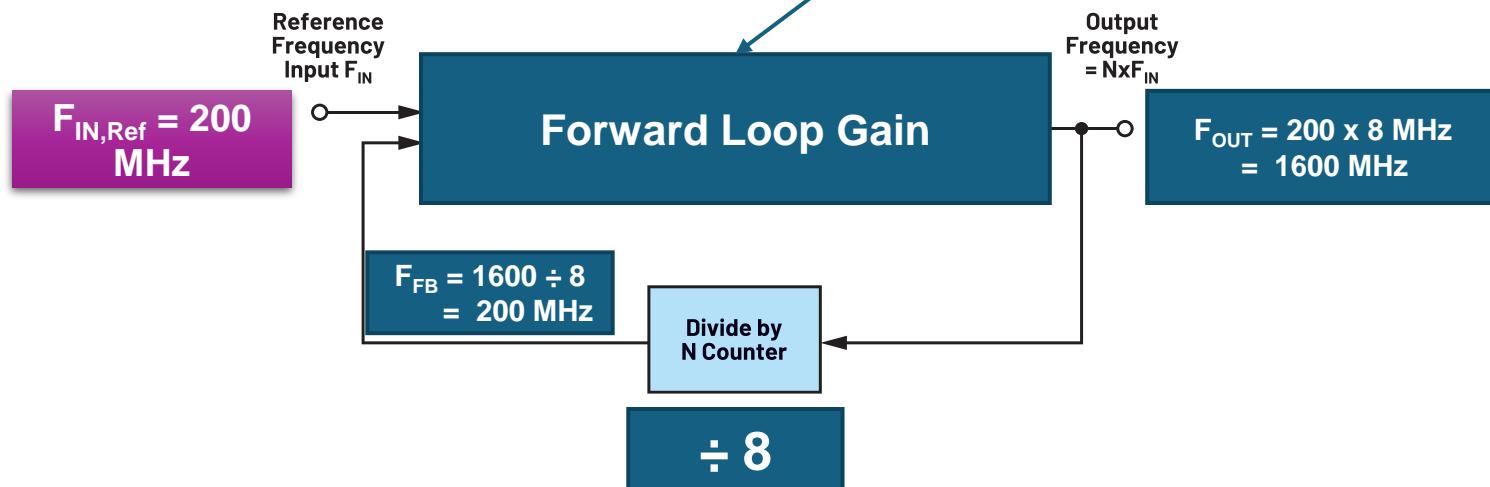


INTRODUCTION

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- ❖ Frequency and Phase of

→ output signal \propto Input Signal

Simplify and let's call it
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Why Do We Need PLL?

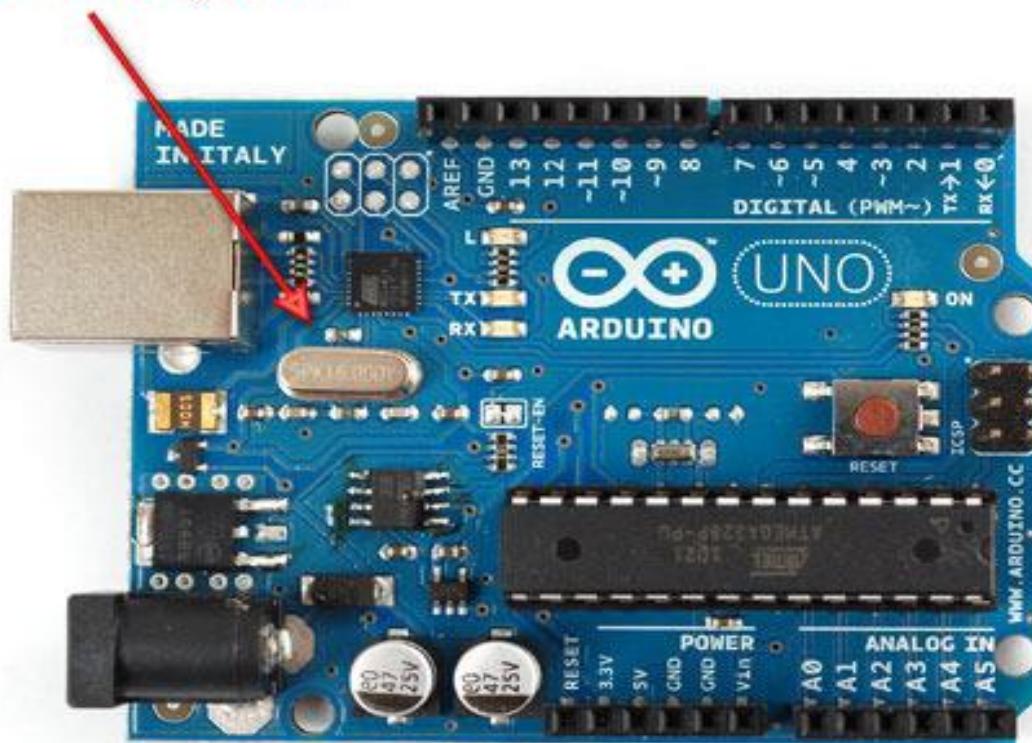
- ❖ To **Synthesize** Frequency from a **Master Clock**

Master Clock

- LC Circuit
- Crystal Oscillator

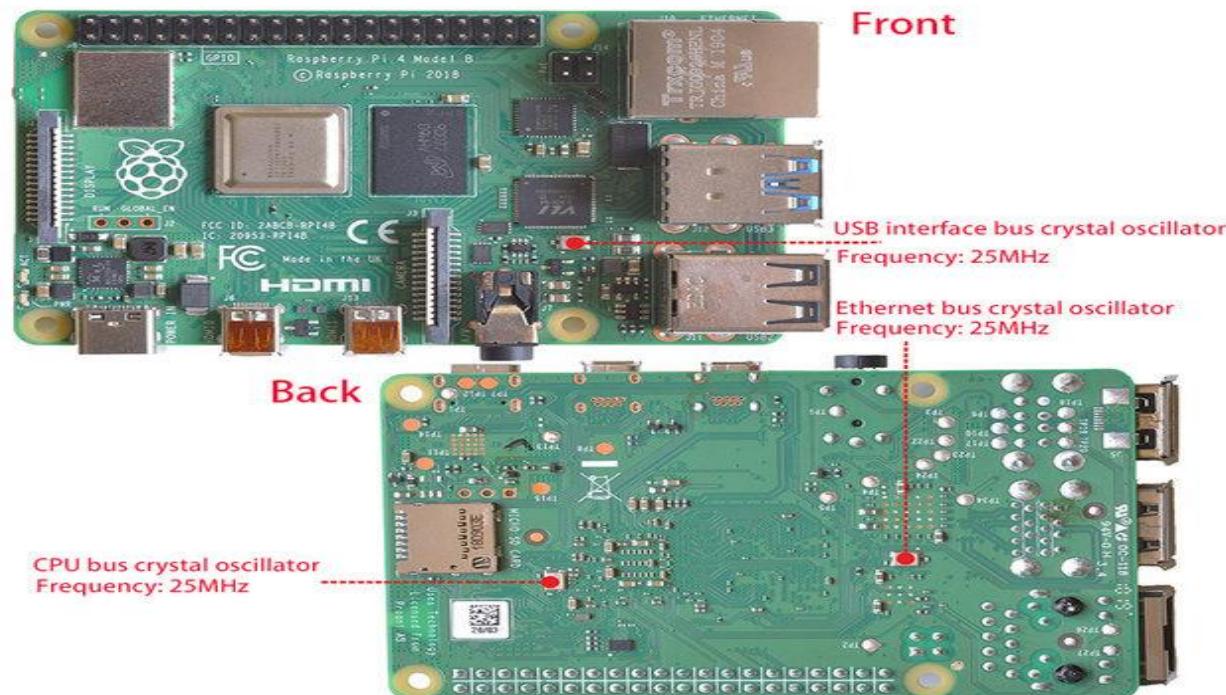
Why Do We Need PLL?

16MHz Crystal

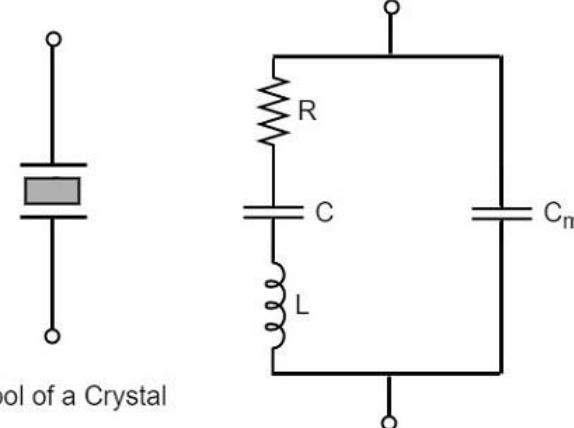
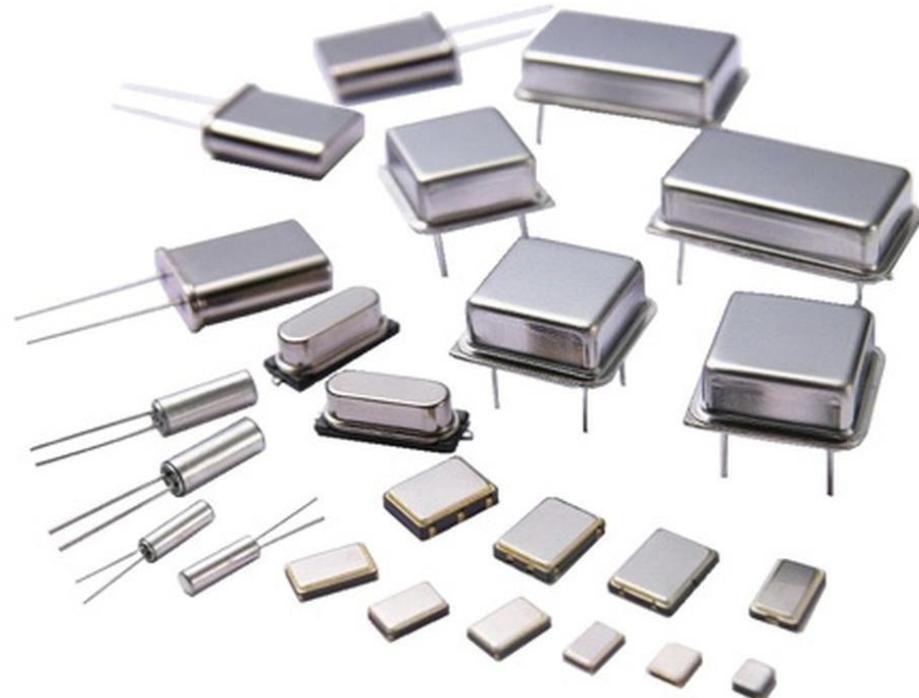


Why Do We Need PLL?

Raspberry Pi 4 crystal location distribution



Crystal Oscillator



Symbol of a Crystal

Equivalent circuit of a crystal

Limitations:

- Output frequency is low
- Very limited tunability after fabrication
- Large area

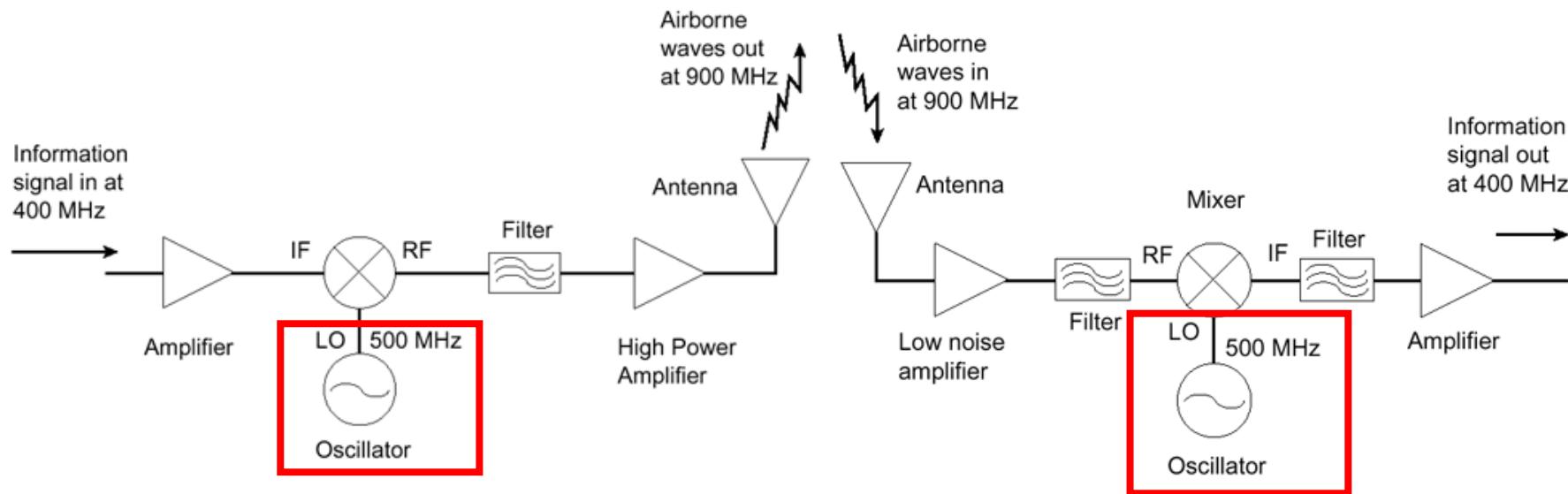
OUR REQUIREMENTS!

- Tunable
- High Frequency
- Periodic Signal Generator

Why Do We Need PLL?

➤ Wireless System

- Generation of carrier frequency, F_{LO} to
- To upconvert baseband signal into passband signal in TX
- To downconvert passband signal into baseband signal in RX

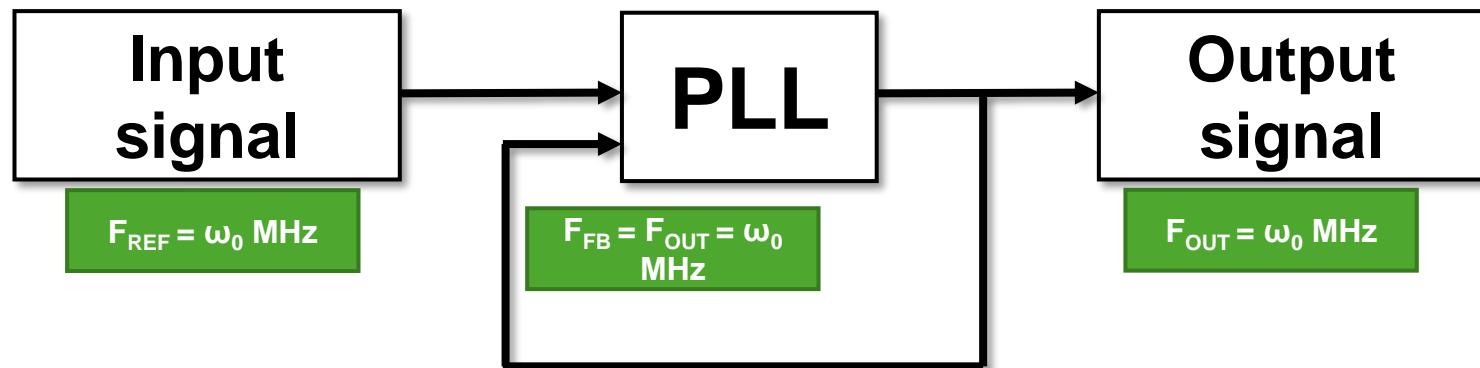


Why Do We Need PLL?

- Wireless System
 - Generation of carrier frequency, F_{LO} to
 - To upconvert baseband signal into passband signal in TX
 - To downconvert passband signal into baseband signal in RX
- Wireline Application
 - Transmit bits every clock period
 - Fast data transfer rate
- Analog Systems
 - Sampling the analog signals in ADCs
 - Tunable digital filter using switch capacitor

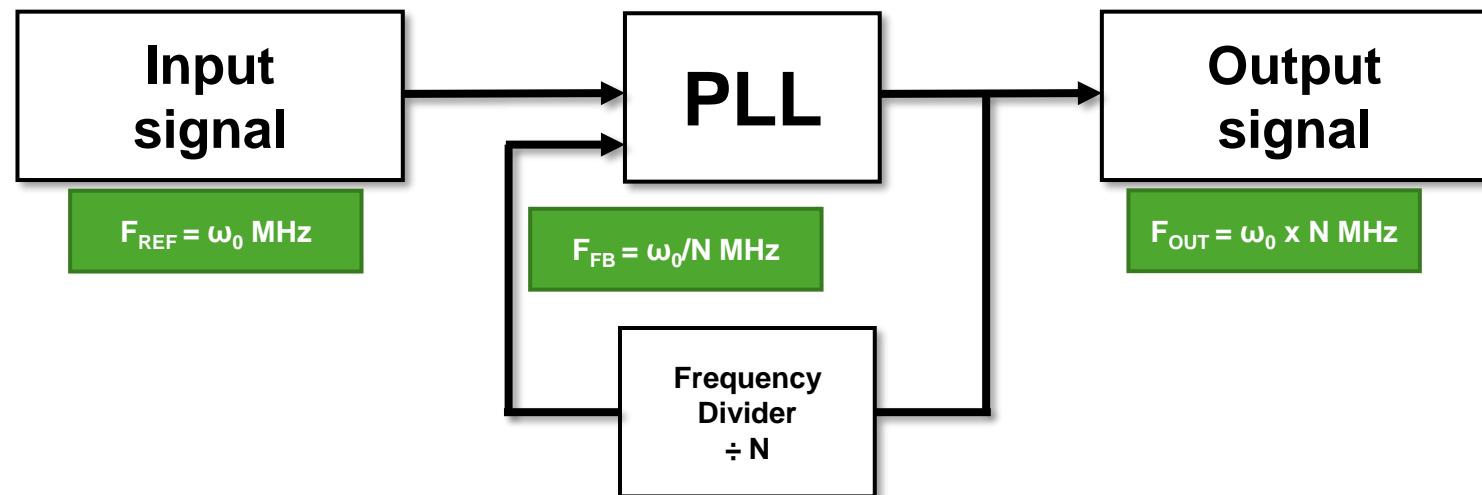
BLOCK DIAGRAM

- ❖ Basic block diagram of PLL :



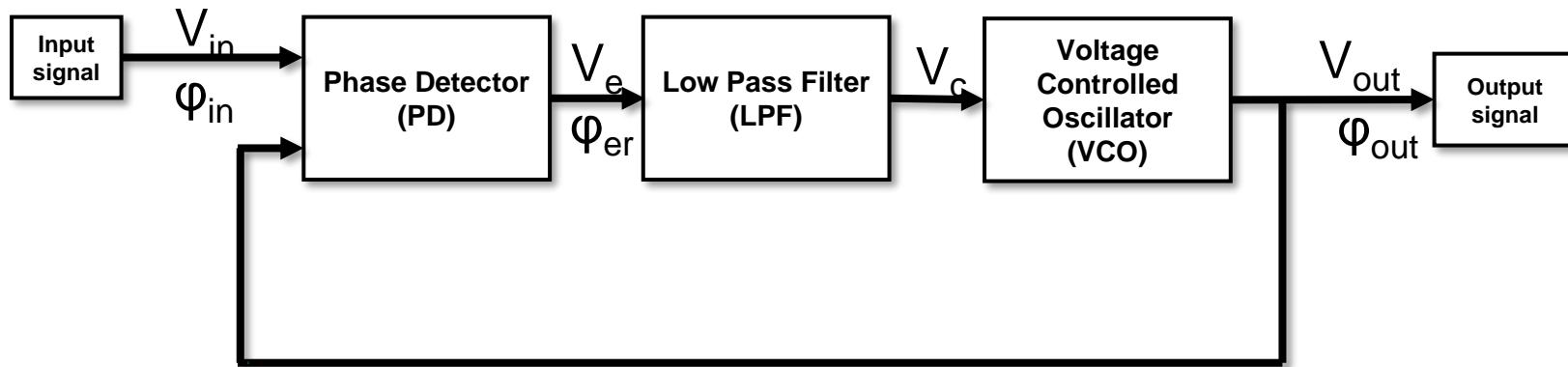
BLOCK DIAGRAM

- ❖ Basic block diagram of PLL :



BLOCK DIAGRAM

- ❖ Basic block diagram of PLL :



$$V_{in} = A_{in} \sin (\omega_{in} t); \Phi_{in} = \omega_{in} t$$

$$V_{out} = A_{out} \cos (\omega_{out} t); \Phi_{out} = \omega_{out} t$$

$$\Phi_{er}(t) = \Phi_{in}(t) - \Phi_{out}(t)$$

$$V_e \propto \Phi_{er}(t)$$

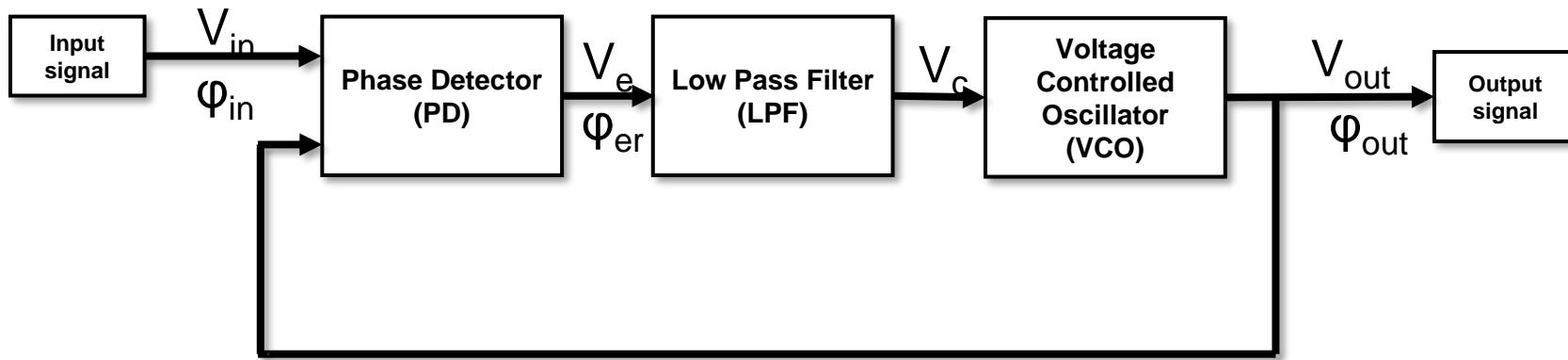
□ Output of PD, $V_e \propto \Phi_{er}$

□ $V_e \xrightarrow[\text{Filtered}]{\text{Loop Filter}} V_c$ (Low f components)

□ $\omega_{out} \propto V_c$

Condition for the locked/steady state

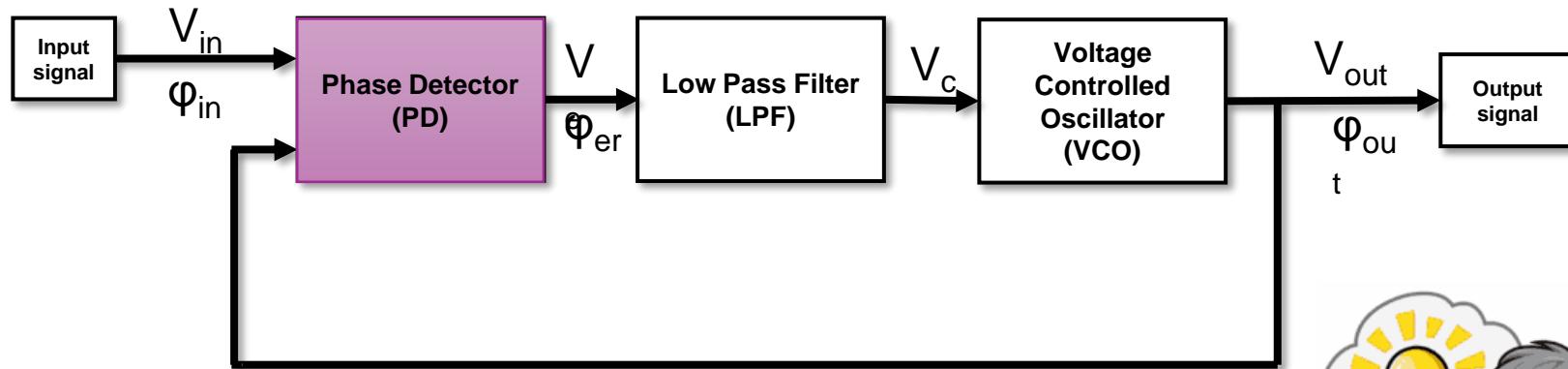
- ❖ Basic block diagram of PLL :



- $\omega_{in} = \omega_{out}$
- $\frac{\delta\phi_{er}}{\delta t} = 0$
- $\frac{\delta(\phi_{in} - \phi_{out})}{\delta t} = 0$ i.e. constant

Simple Implementation of a PLL

- ❖ Phase (Error) Detector: PD



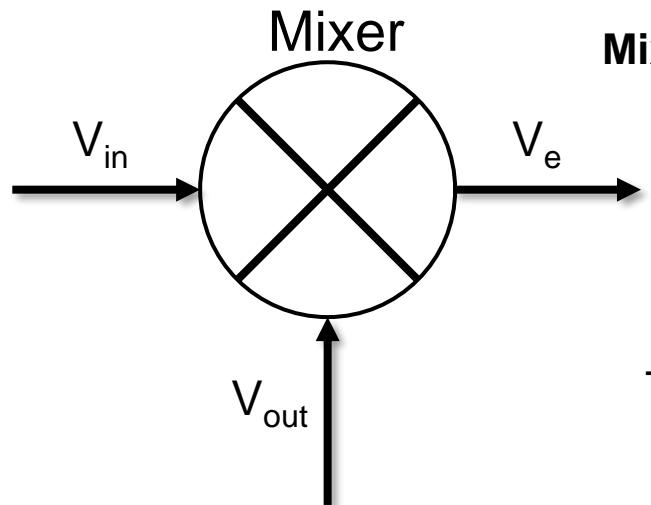
Recall: We want to find the phase error, $\varphi_{\text{er}}(t) = \varphi_{\text{in}}(t) - \varphi_{\text{out}}(t)$

But How?

Trigonometry
→ Product to Sum Identities



Phase (Error) Detector: PD



Mixer:

- Combines two or more input signals, V_{in} and V_{out}
 - Produces an output signal
 - Contains the sum and difference frequencies of the input signals
- $$V_e \propto V_{in} + V_{out} \quad \text{OR}$$
- $$V_e \propto V_{in} - V_{out}$$

Trigonometry

- Product to Sum Identities
- $$\sin A \cos B = \frac{1}{2} \sin (A+B) + \sin (A-B)$$

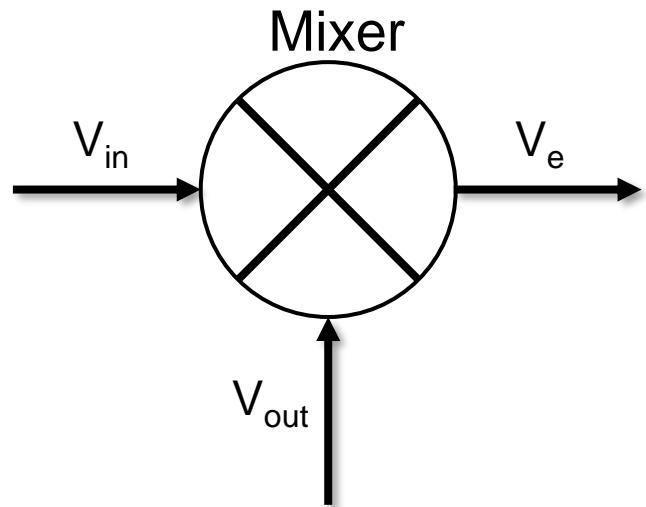
$$V_{in} = A_{in} \sin (\omega_{in} t)$$

$$V_{in} V_{out} = A_{in} \sin (\omega_{in} t) \times A_{out} \cos (\omega_{out} t)$$

$$V_{out} = A_{out} \cos (\omega_{out} t)$$

$$= \frac{1}{2} A_{in} A_{out} \sin (\omega_{in} + \omega_{out}) t + \sin (\omega_{in} - \omega_{out}) t$$

Phase (Error) Detector: PD



Cases:

#1: Freq = No error and φ = No error

$$\begin{aligned}\rightarrow \Delta\omega &= \omega_{in} - \omega_{out} = 0 \\ \rightarrow \omega_{in} &= \omega_{out} = \omega \\ \rightarrow \varphi_{er} &= 0\end{aligned}$$

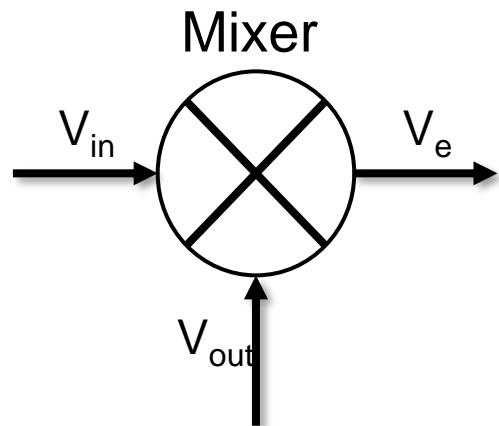
#2: Freq = error and φ = No error

$$\begin{aligned}\rightarrow \omega_{in} &= \omega \\ \rightarrow \omega_{out} &= \omega - \Delta\omega \\ \rightarrow \varphi_{er} &= 0\end{aligned}$$

#3: Freq = No error and φ = error

$$\begin{aligned}\rightarrow \Delta\omega &= \omega_{in} - \omega_{out} = 0 \\ \rightarrow \omega_{in} &= \omega_{out} = \omega \\ \rightarrow \varphi_{er} &\neq 0\end{aligned}$$

Phase (Error) Detector: PD



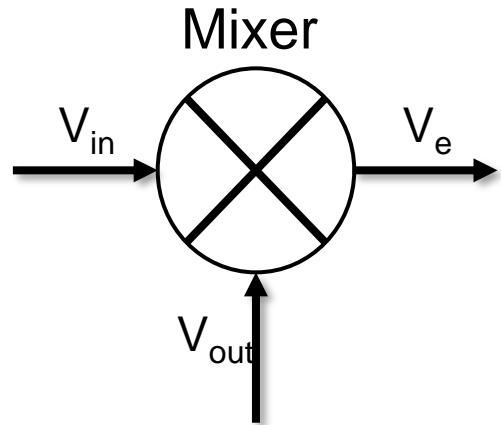
Case #1: Freq = No error and φ = No error

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$$\begin{aligned}V_e &= V_{in} V_{out} = \frac{1}{2} A_{in} A_{out} \sin(\omega_{in} + \omega_{out}) t + \sin(\omega_{in} - \omega_{out}) t \\ &= \frac{1}{2} A_{in} A_{out} \sin(\omega + \omega) t + \sin(\omega - \omega) t \\ &= \frac{1}{2} A_{in} A_{out} \sin 2\omega t + \sin(0) \\ &= \frac{1}{2} A_{in} A_{out} \sin 2\omega t\end{aligned}$$

We only have the high-frequency component

Phase (Error) Detector: PD



Case #2: Freq = error and φ = No error

$$\rightarrow \omega_{in} = \omega$$

$$\rightarrow \omega_{out} = \omega - \Delta\omega$$

$$\rightarrow \varphi_{er} = 0$$

$$\begin{aligned} V_e &= V_{in} V_{out} = \frac{1}{2} A_{in} A_{out} \sin(\omega_{in} + \omega_{out}) t + \sin(\omega_{in} - \omega_{out}) t \\ &= \frac{1}{2} A_{in} A_{out} \sin(\omega + \omega - \Delta\omega) t + \sin(\omega - \omega + \Delta\omega) t \\ &= \frac{1}{2} A_{in} A_{out} \sin(2\omega - \Delta\omega) t + \sin(\Delta\omega) t \end{aligned}$$

High frequency component

$V_e \propto$ frequency error, $\Delta\omega$

Phase (Error) Detector: PD

Case #3: Freq = No error and φ = error

$$\rightarrow \Delta\omega = \omega_{in} - \omega_{out} = 0$$

$$\rightarrow \omega_{in} = \omega_{out} = \omega$$

$$\rightarrow \varphi_{er} \neq 0$$

$$\rightarrow \varphi_{er}(0) = \varphi_{in}(0) - \varphi_{out}(0)$$

$$V_{in} = A_{in} \sin(\omega_{in} t + \varphi_{in}(0))$$

$$V_{out} = A_{out} \cos(\omega_{out} t + \varphi_{out}(0))$$

$$\begin{aligned} V_e &= V_{in} V_{out} = \frac{1}{2} A_{in} A_{out} \sin(\omega_{in} + \omega_{out}) t + \sin(\omega_{in} - \omega_{out}) t \\ &= \frac{1}{2} A_{in} A_{out} \sin(\omega + \varphi_{in}(0) + \omega + \varphi_{out}(0)) t + \sin(\varphi_{er}(0)) t \\ &= \frac{1}{2} A_{in} A_{out} \sin(2\omega + \varphi_{in}(0) + \varphi_{out}(0)) t + \sin(\varphi_{er}(0)) t \end{aligned}$$

V_e has two components:

\rightarrow @ 2ω frequency

\rightarrow @ DC



Phase (Error) Detector: PD Summary

Cases:

#1: Freq = No error and φ = No error

#2: Freq = error and φ = No error

#3: Freq = No error and φ = error

$$V_e = V_{in} V_{out} = \frac{1}{2} A_{in} A_{out} \sin 2\omega t \leftarrow \text{We only have the high-frequency component}$$

$$V_e = V_{in} V_{out} = \frac{1}{2} A_{in} A_{out} \sin (2\omega - \Delta\omega) t + \sin(\Delta\omega)t \leftarrow V_e \propto \text{frequency error, } \Delta\omega$$

$$V_e = V_{in} V_{out} = \frac{1}{2} A_{in} A_{out} \sin (2\omega + \varphi_{in}(0) + \varphi_{out}(0)) t + \sin(\varphi_{er}(0)) t$$

V_e has two components:

→ @ 2ω frequency

→ @ DC

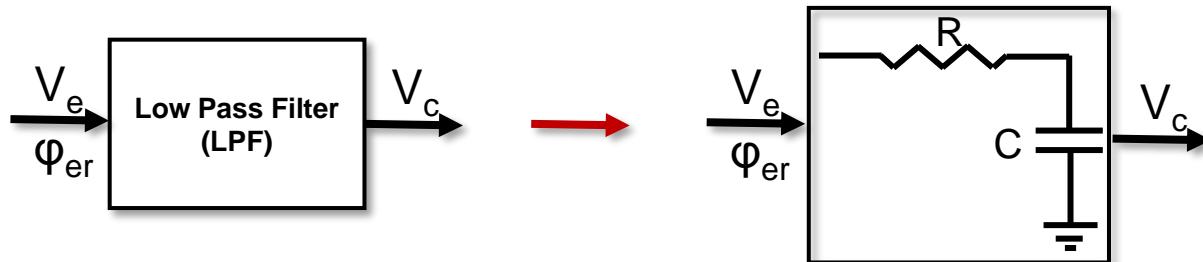


Phase (Error) Detector: PD Summary

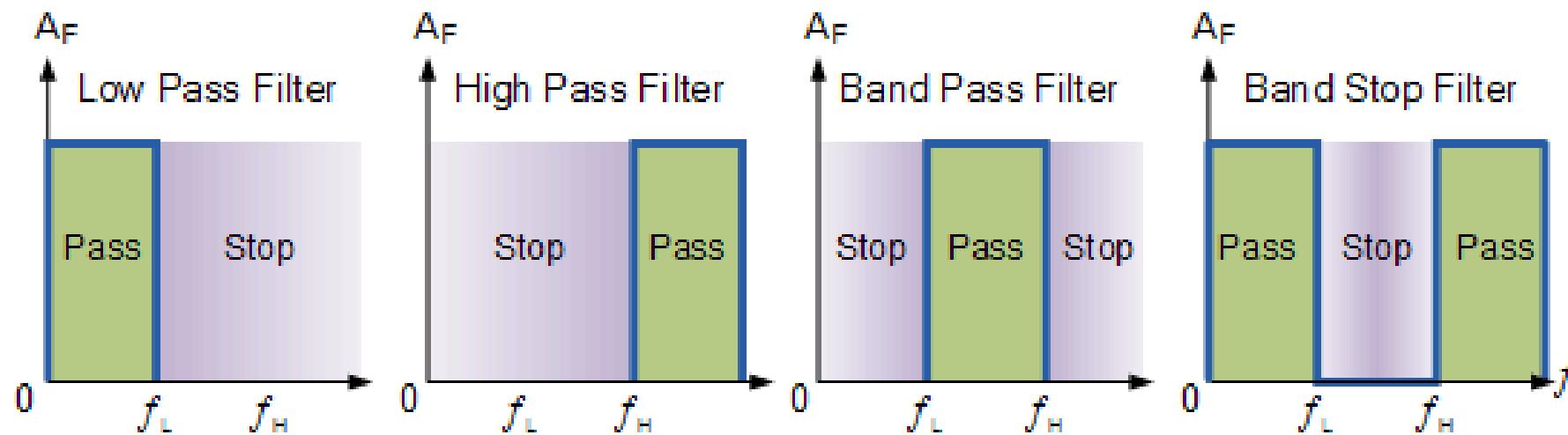
$$V_e = V_{in} \quad V_{out} = \frac{1}{2} A_{in} A_{out} \sin 2\omega t$$

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$$V_e = V_{in} \quad V_{out} = \frac{1}{2} A_{in} A_{out} \sin (2\omega + \varphi_{in}(0) + \varphi_{out}(0)) t + \sin (\varphi_{er}(0)) t$$



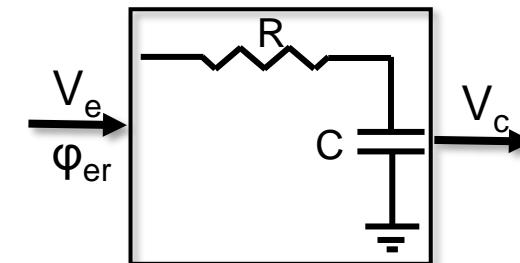
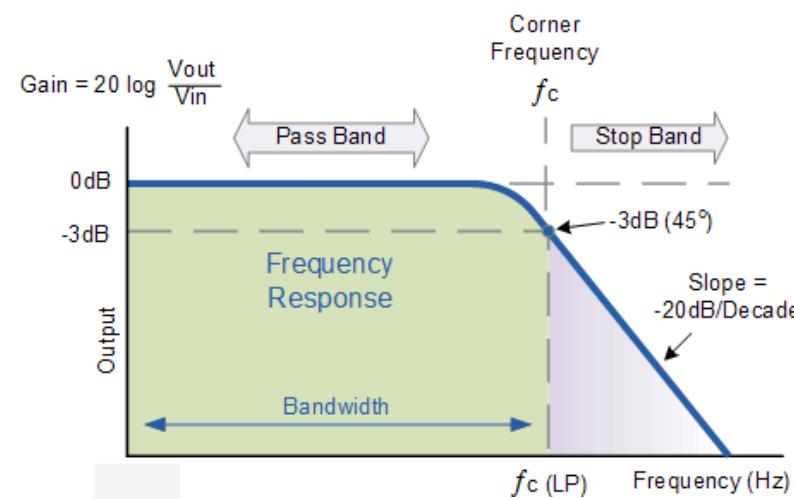
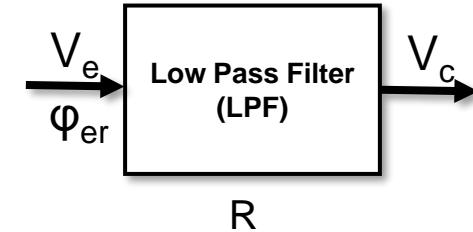
Filters



Frequency Spectrum of the V_e signal

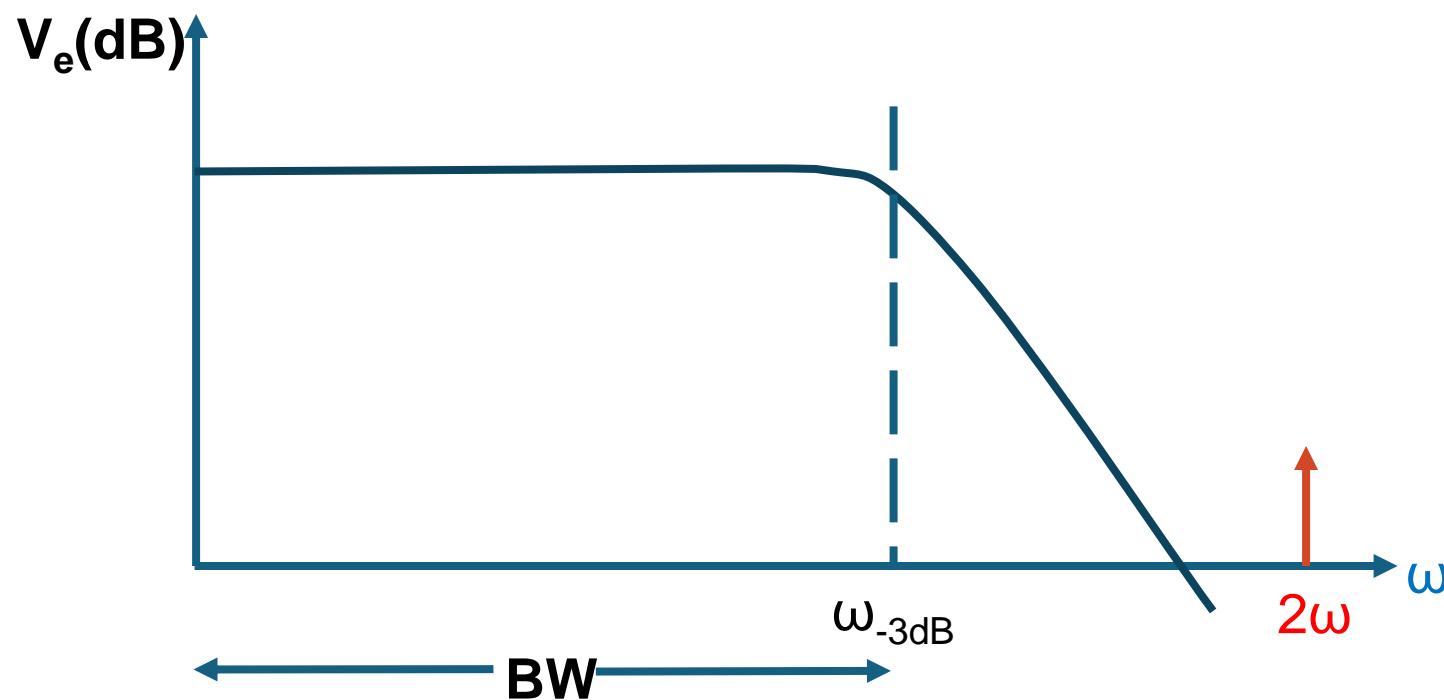
$$\omega_c = \frac{1}{RC}$$

$$f_c = \frac{1}{2\pi RC}$$



Frequency Spectrum of the V_e signal

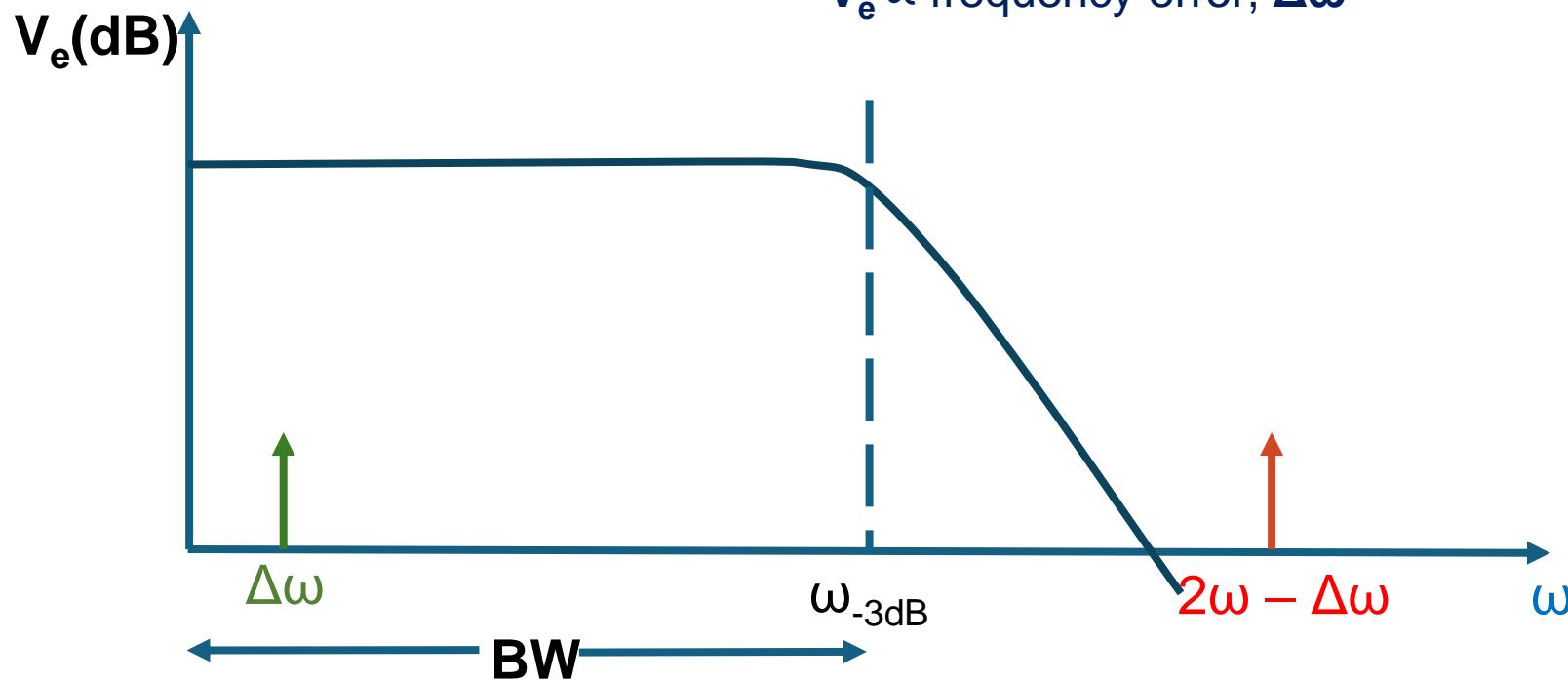
Case #1: $V_e = V_{in}$ $V_{out} = \frac{1}{2} A_{in} A_{out} \sin 2\omega t$ ← **We only have the high-frequency component**



Frequency Spectrum of the V_e signal

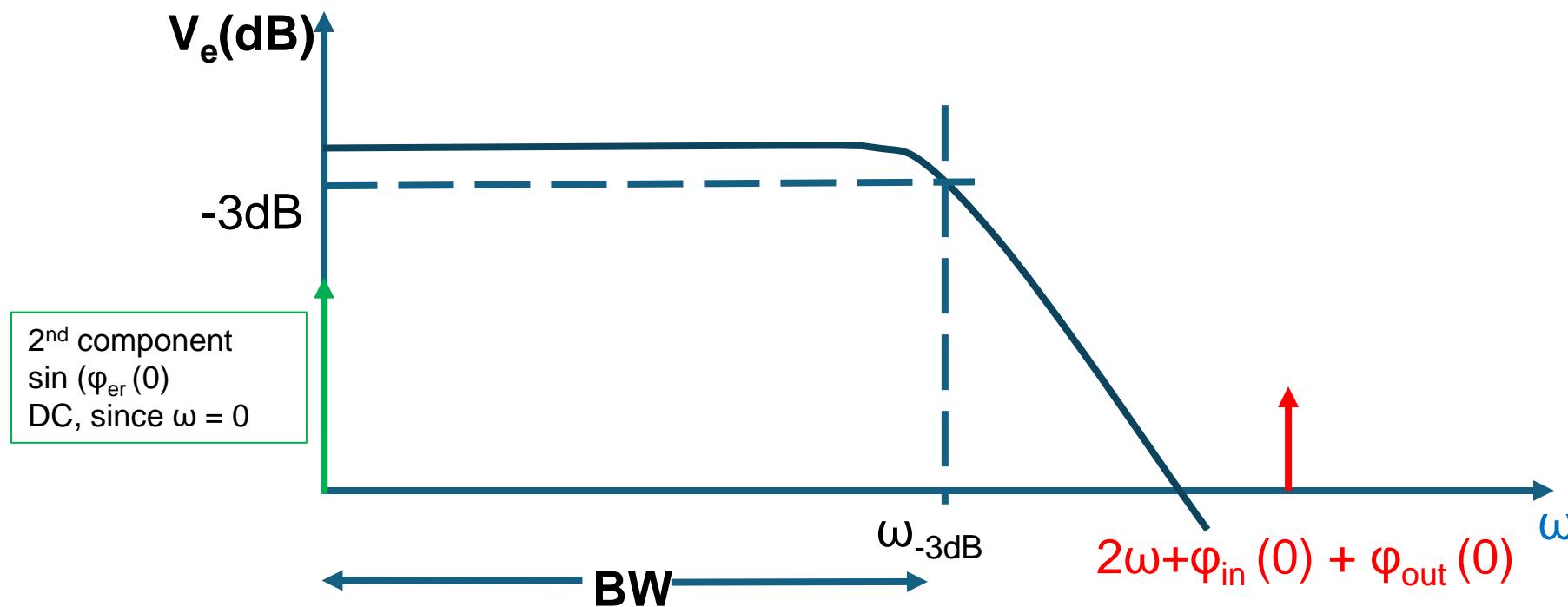
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$V_e \propto$ frequency error, $\Delta\omega$



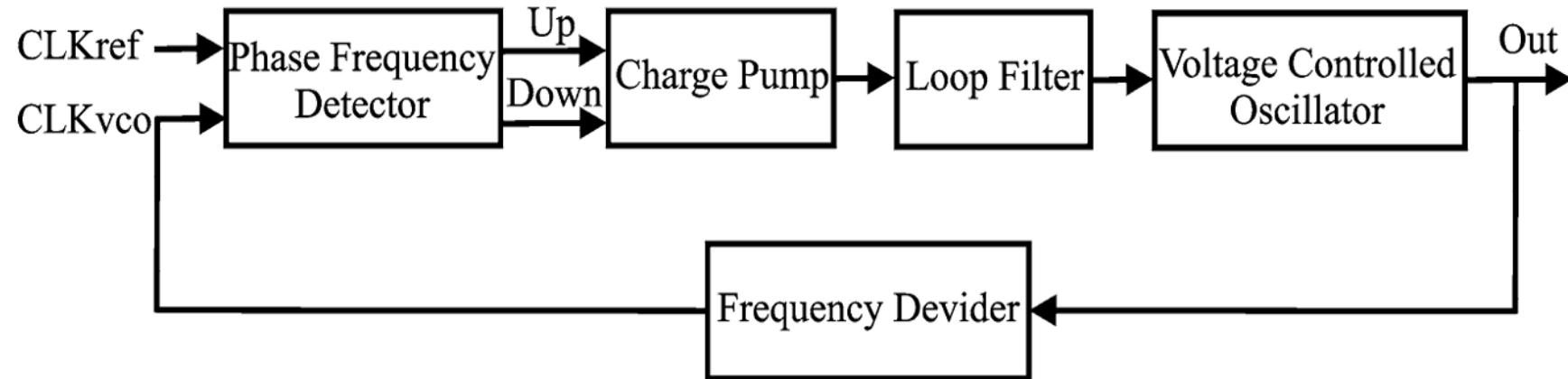
Frequency Spectrum of the V_e signal

Case #3: $V_e = \frac{1}{2} A_{in} A_{out} \sin(2\omega + \varphi_{in}(0) + \varphi_{out}(0)) t + \sin(\varphi_{er}(0)) t$



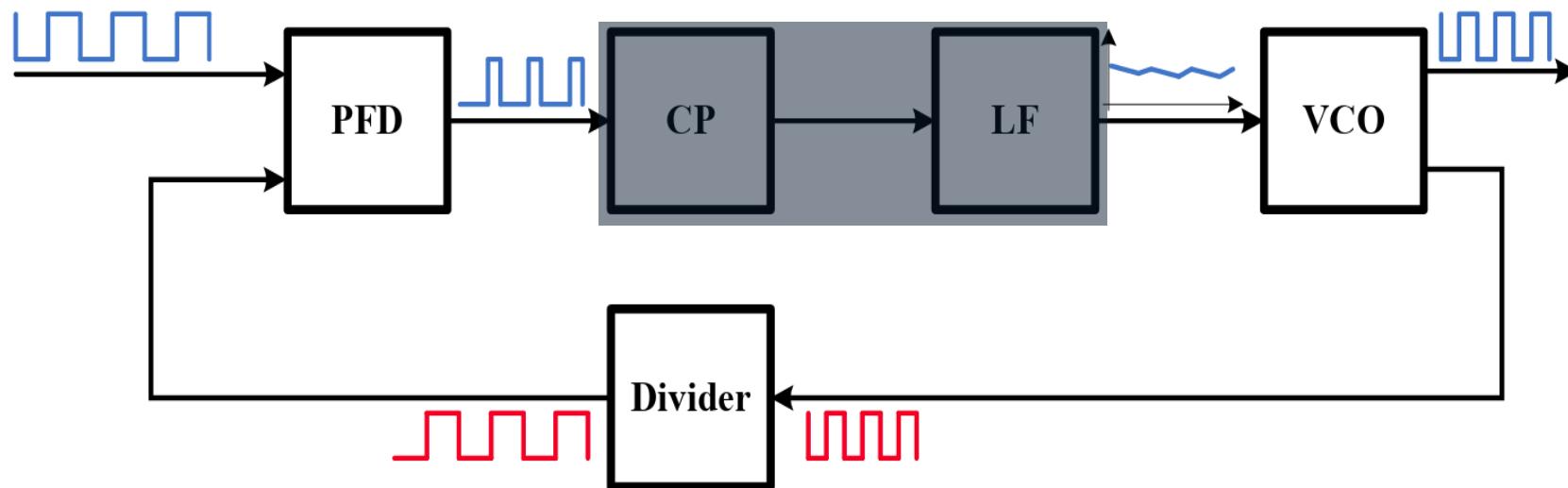
BLOCK DIAGRAM

- ❖ Basic block diagram of PLL (frequency synthesizer) :



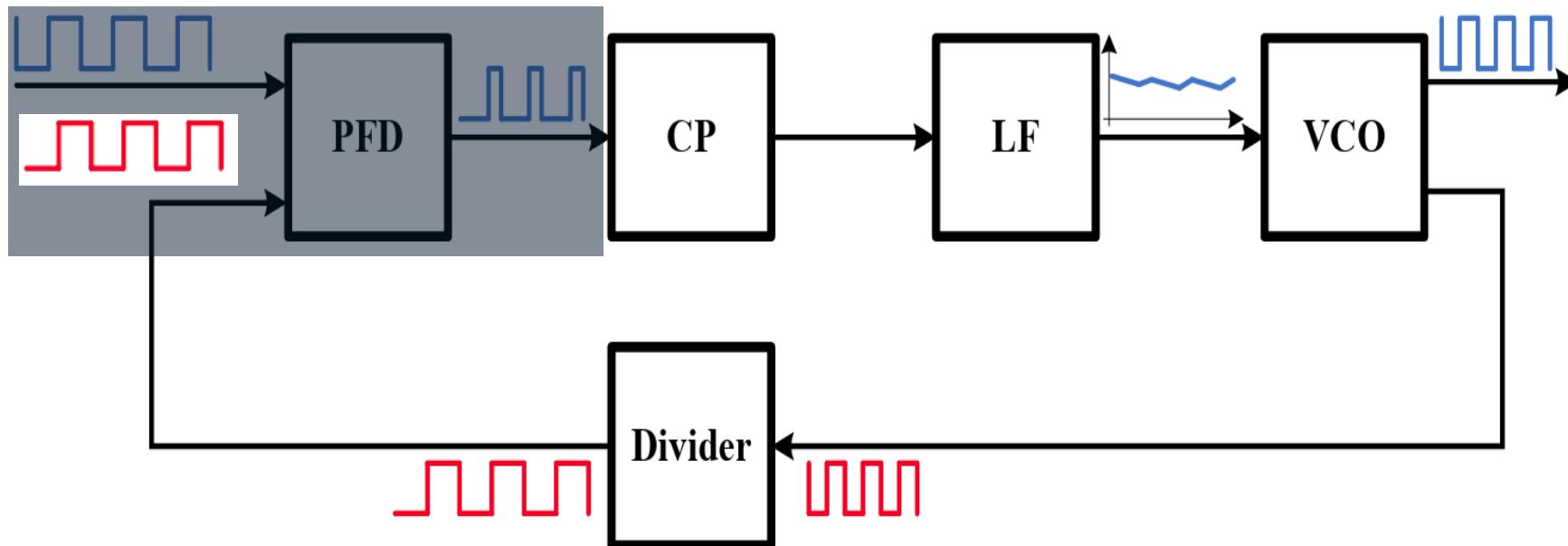
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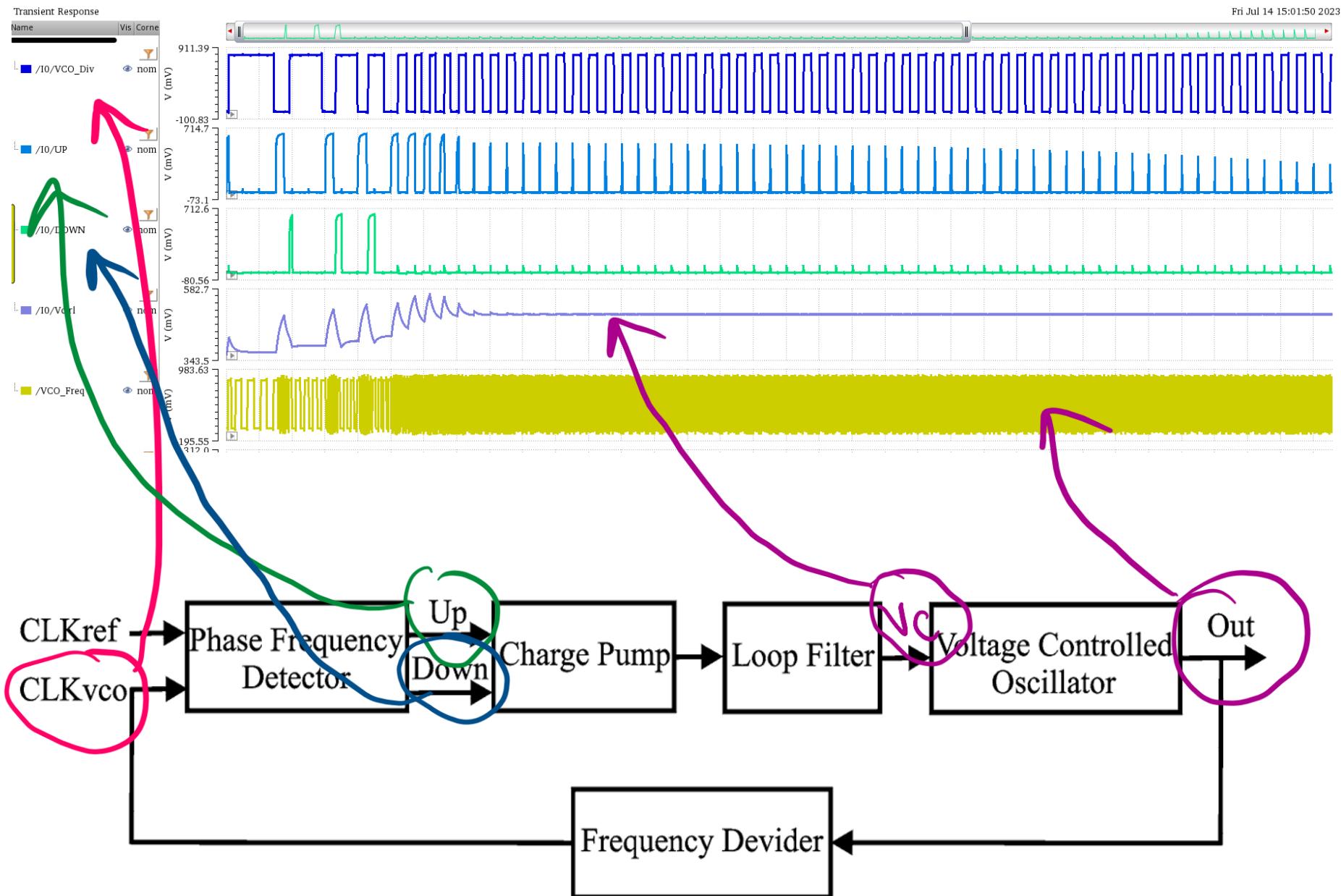
[Abolhasani, 2020]

Phase Frequency detector

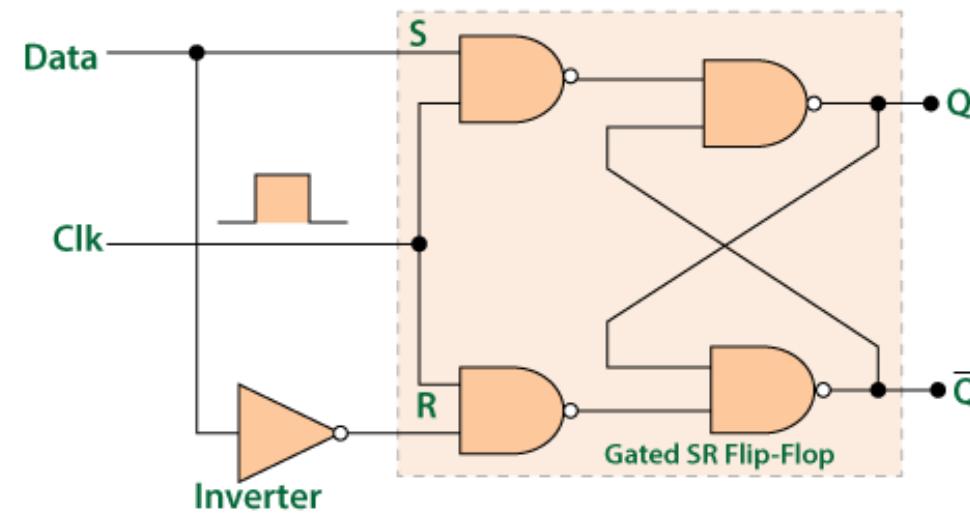
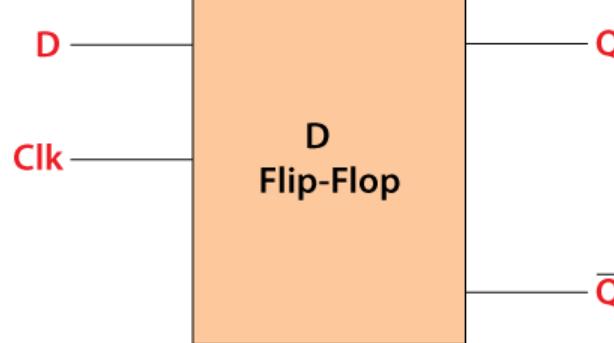


[Abolhasani, 2020]

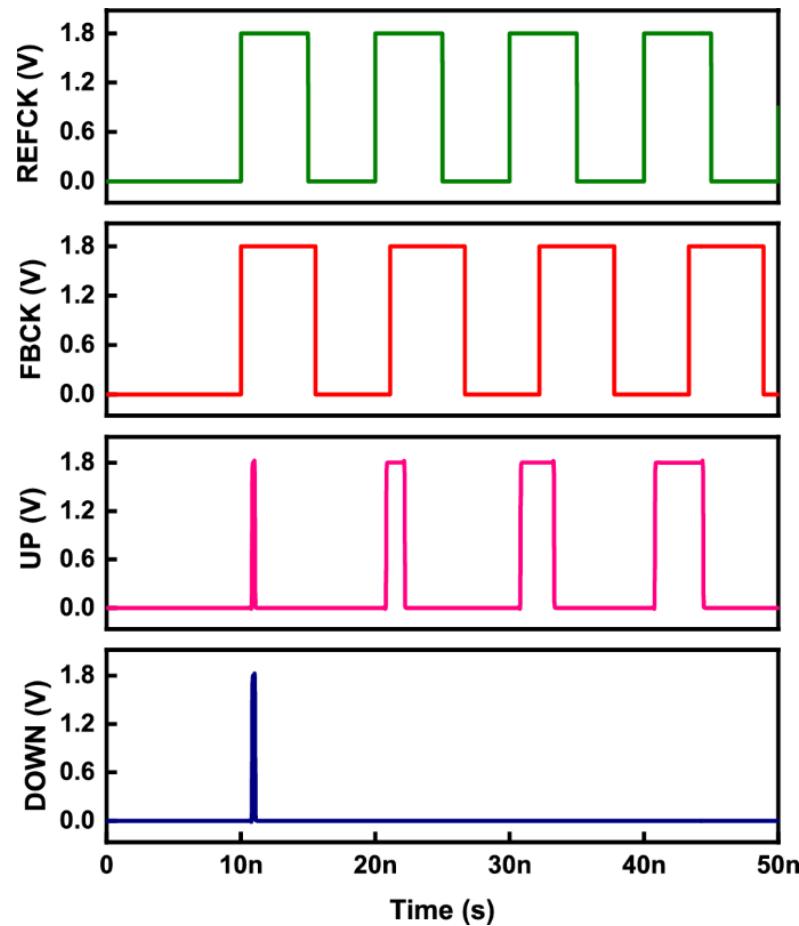
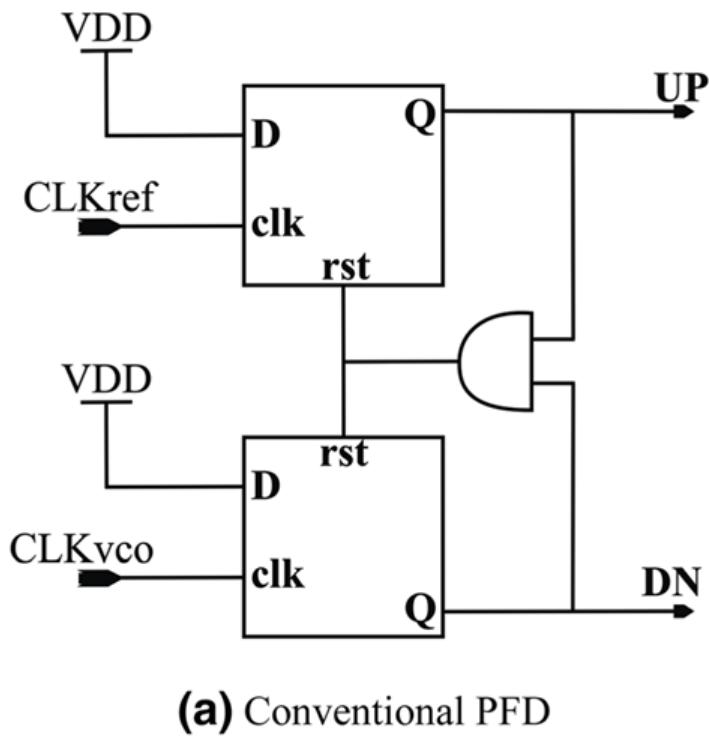
Actual PLL Output



Phase Frequency detector



Phase Frequency detector



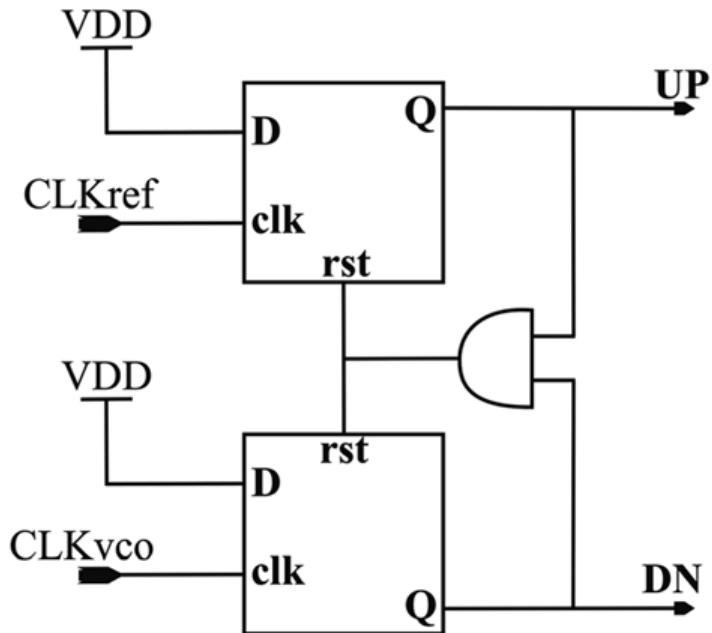
[Divya, M, 2023]

$$F_{\text{fb}} < F_{\text{ref}}$$

Result:

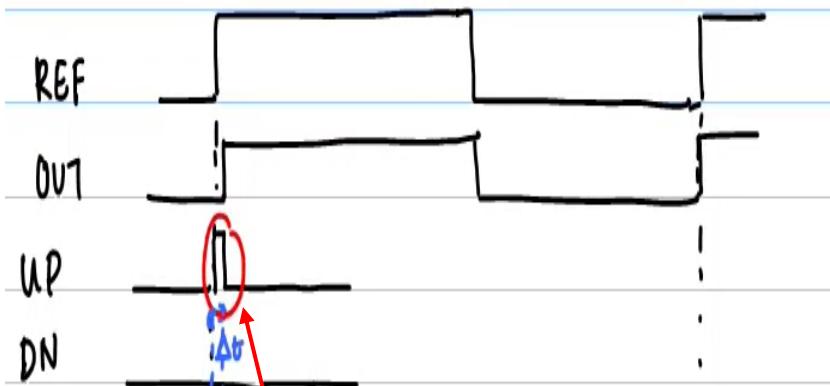
More up pulses to increase F_{fb}

Phase Frequency detector



(a) Conventional PFD

When the phase difference is near zero



[11]

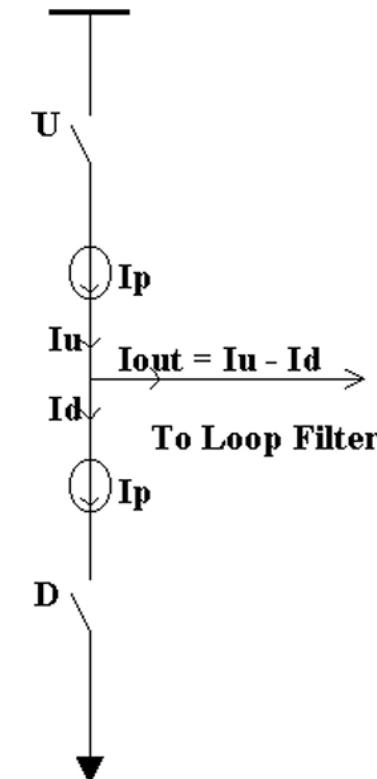
UP pulse is very narrow to turn on the switch!

Phase Frequency detector



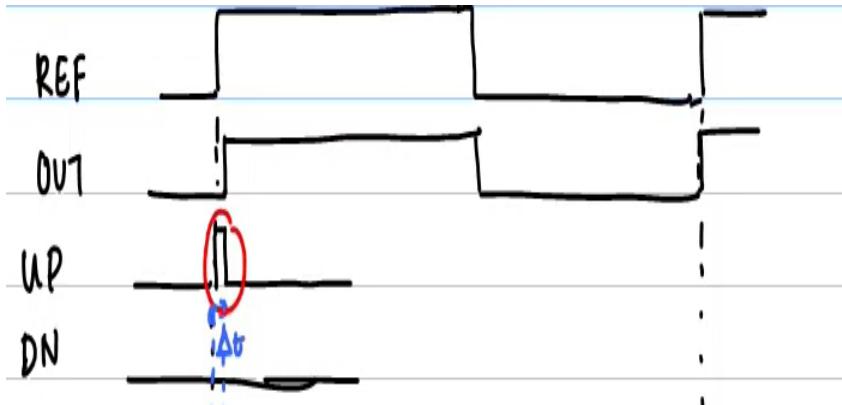
[11]

UP pulse is very narrow to turn on the switch!



[Lee, 2002]

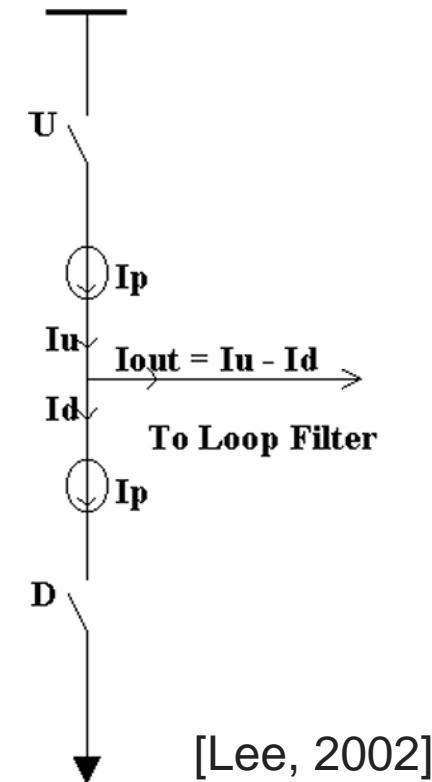
Phase Frequency detector



[11]

Solution?

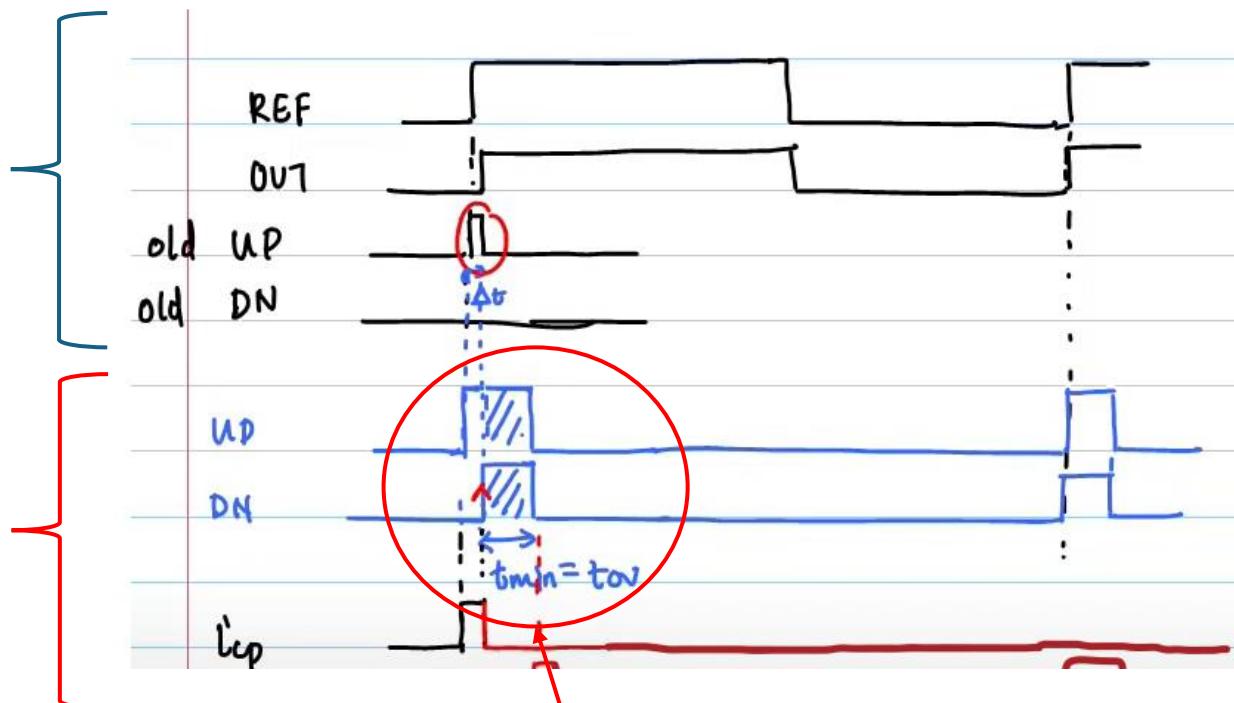
Extend the pulse with minimum overlap delay!



[Lee, 2002]

Phase Frequency detector

- Old design
 - Pulse width is too low
-
- New design
 - Pulse width is sufficiently high



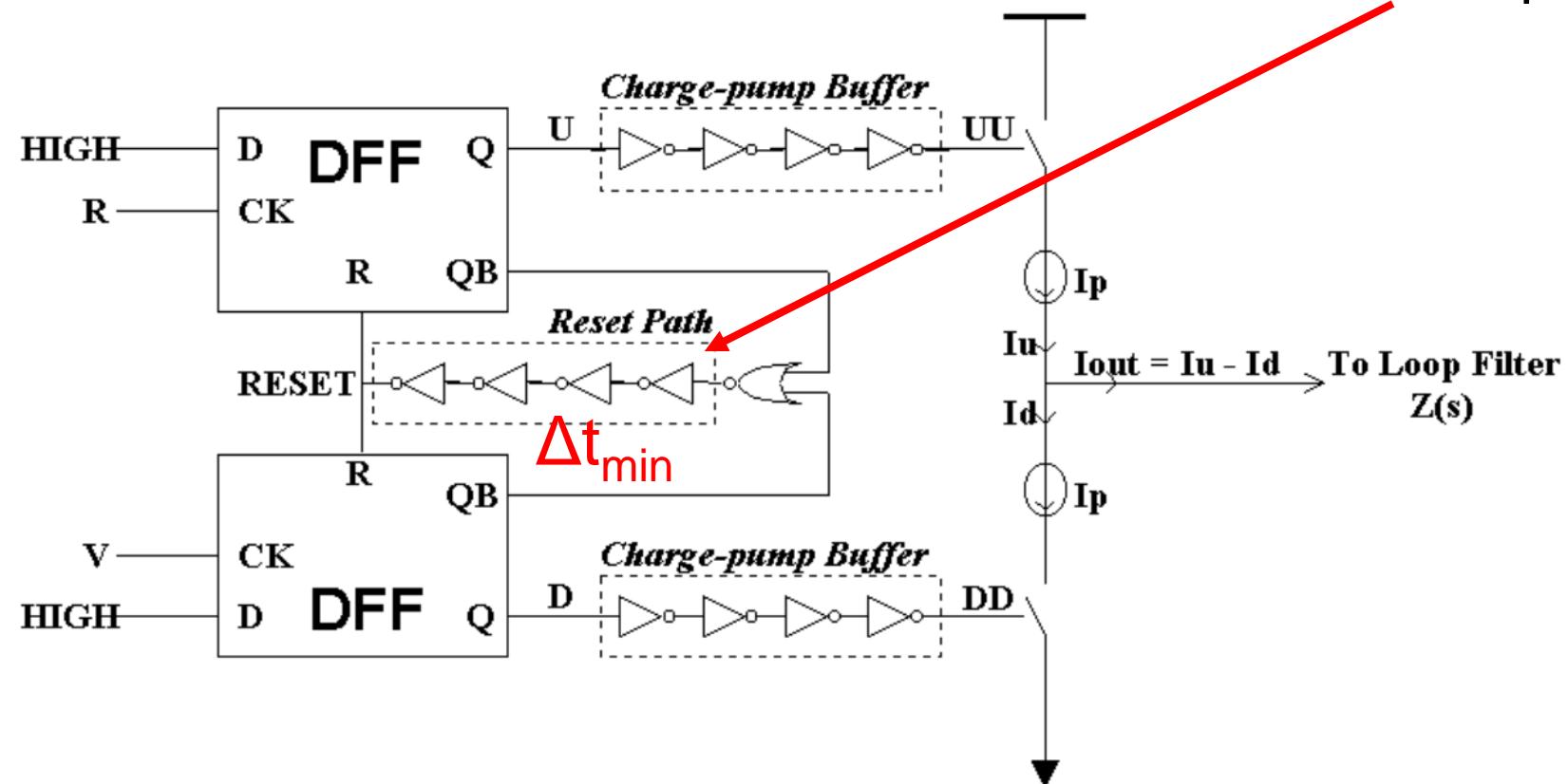
Pulse extension

[11]

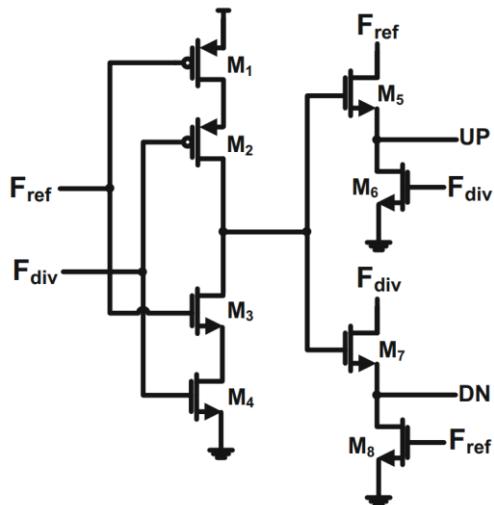
Phase Frequency detector

A solution to Dead Zone

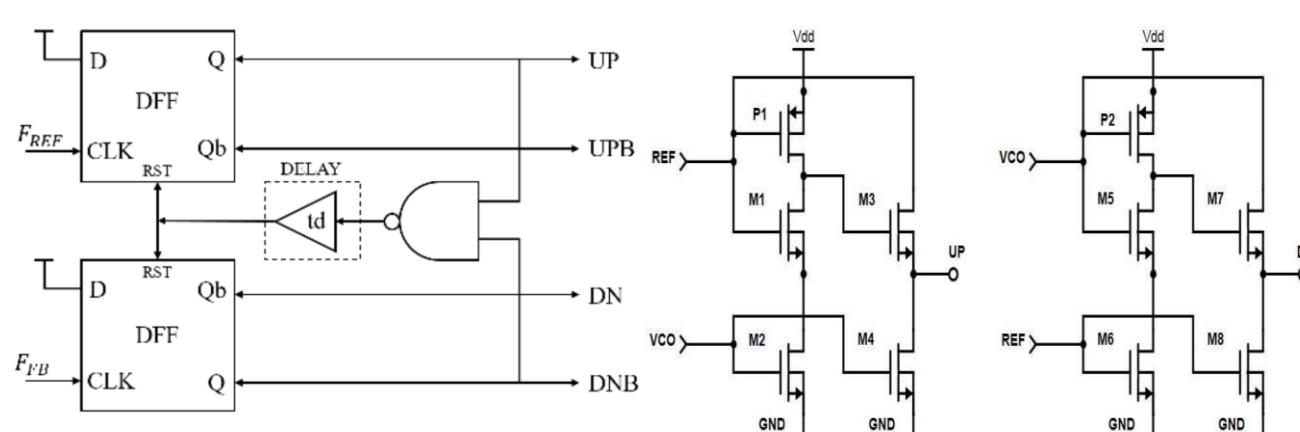
Delay chain in the Reset Path to increase pulse width



Different Architectures of Phase Frequency Detector



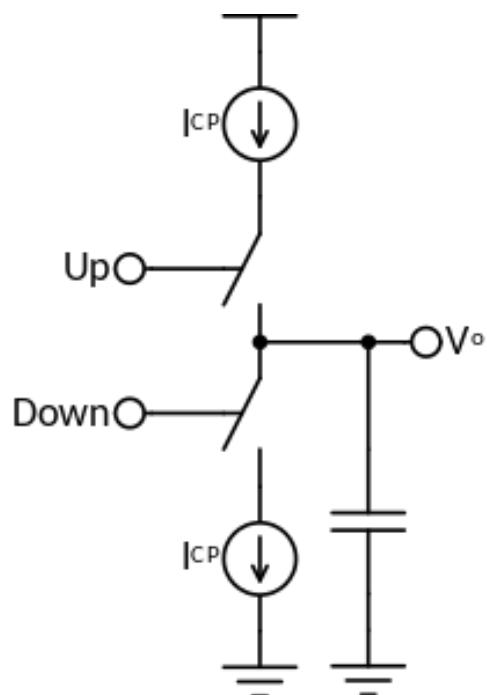
[Azadmoosavi, 2018]



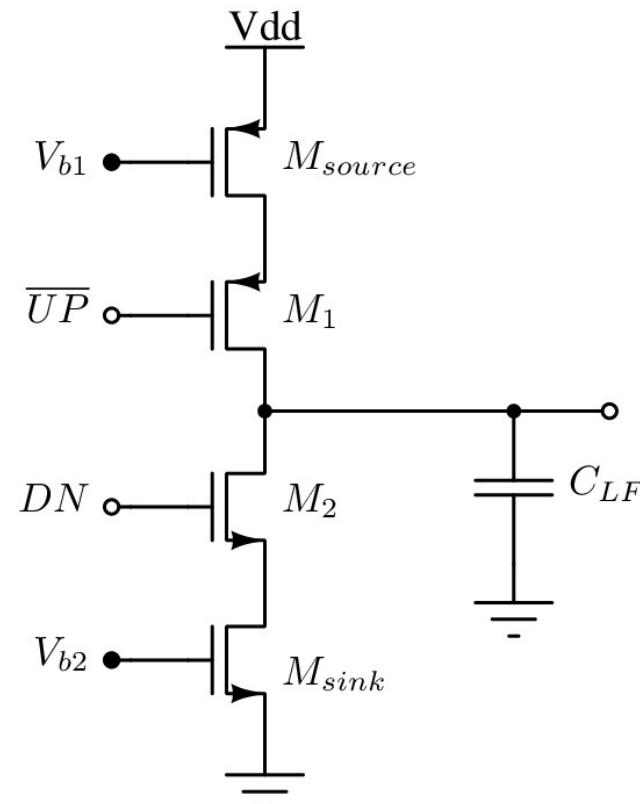
[S. M. M. Ahsan, 2020]

[K. Zouaq, 2018]

Charge Pump

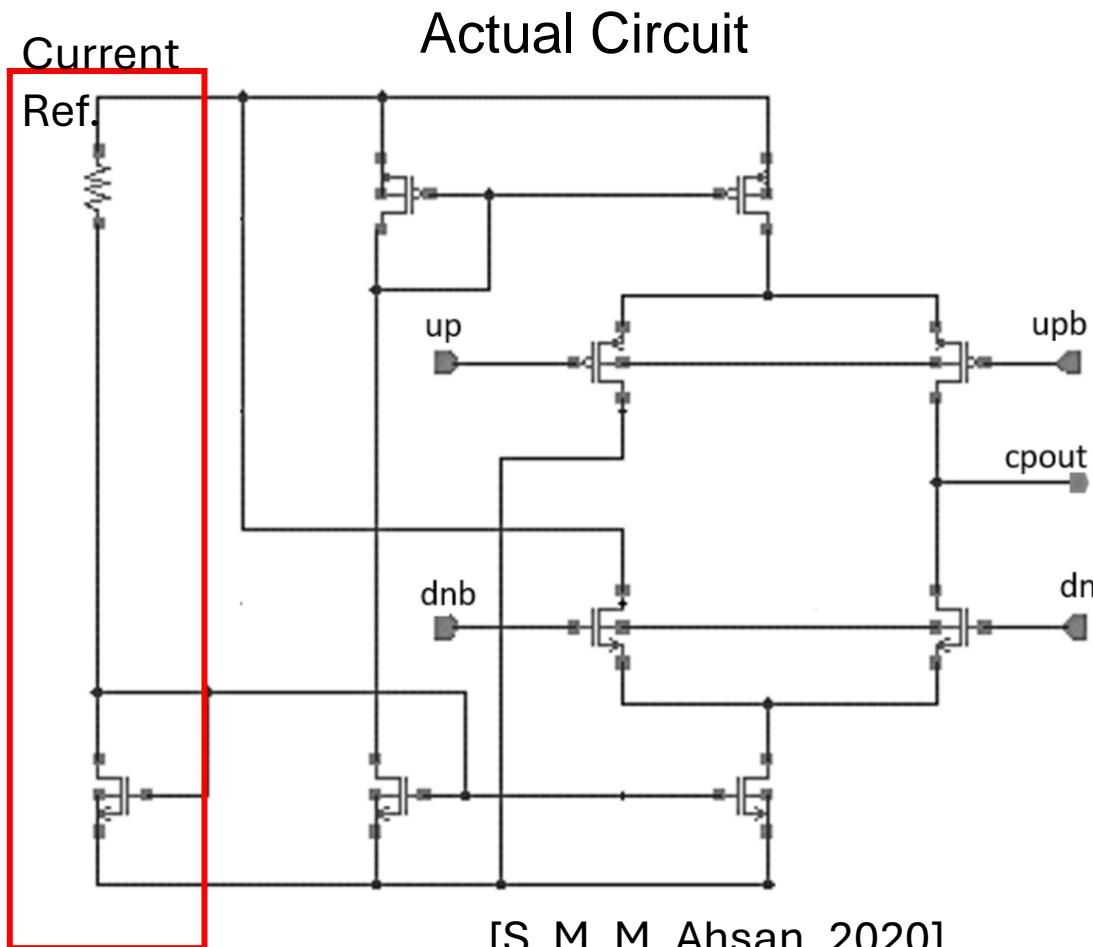
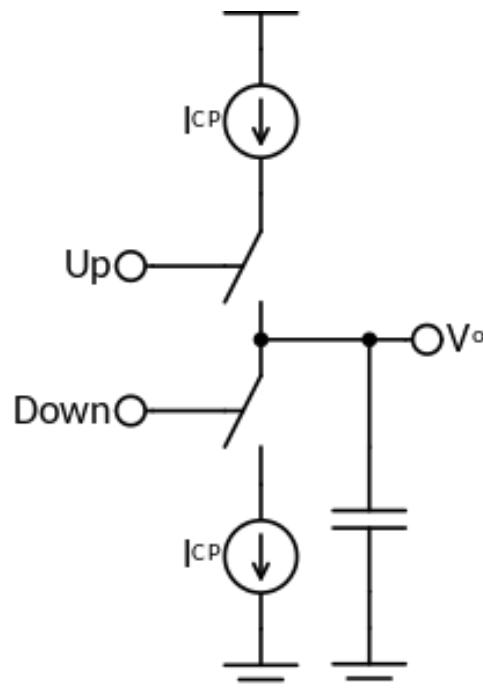


MOSFET
Representation



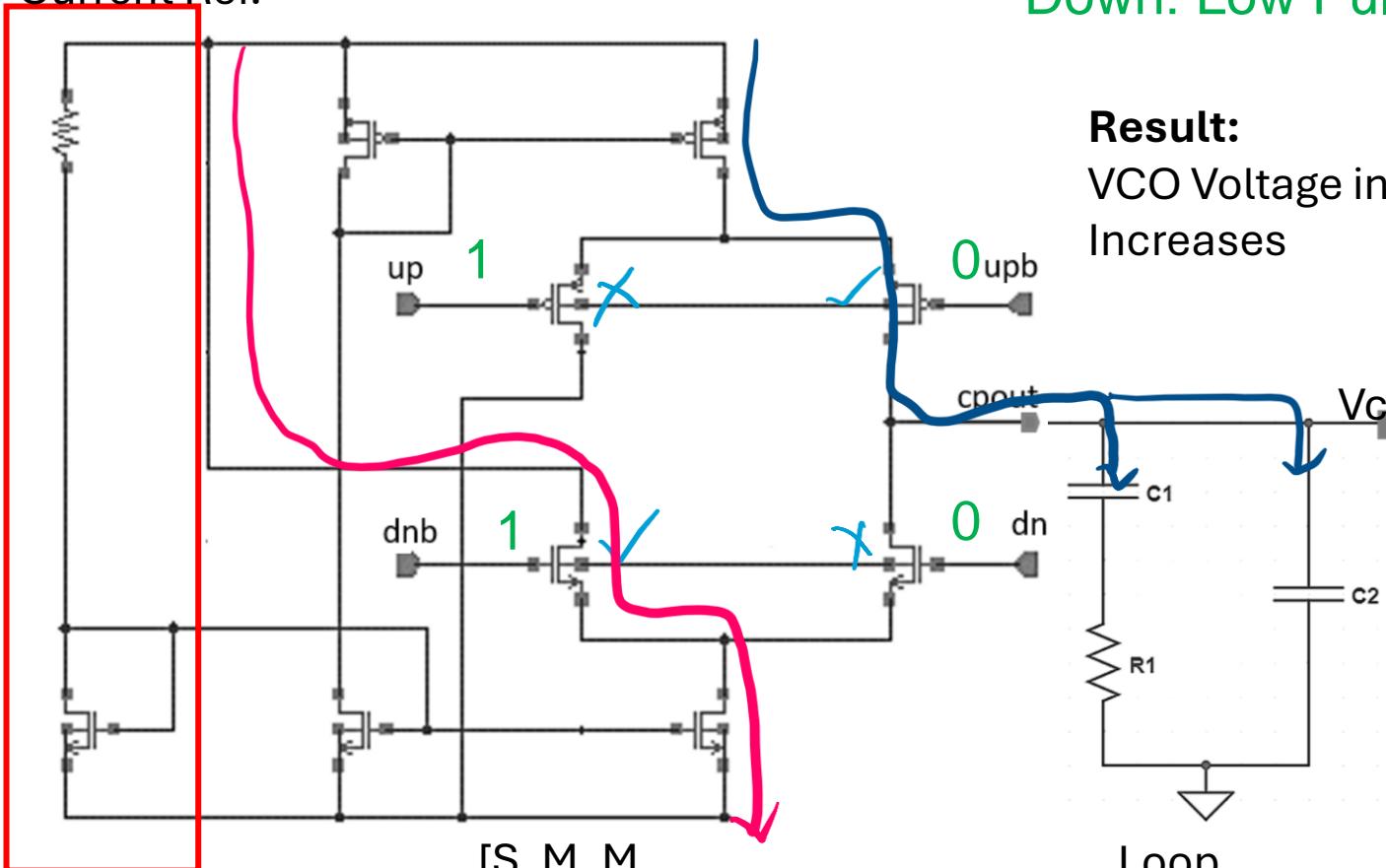
Charge Pump

Model Circuit



Charge Pump

Current Ref.



Case #1: Up: High Pulse
Down: Low Pulse

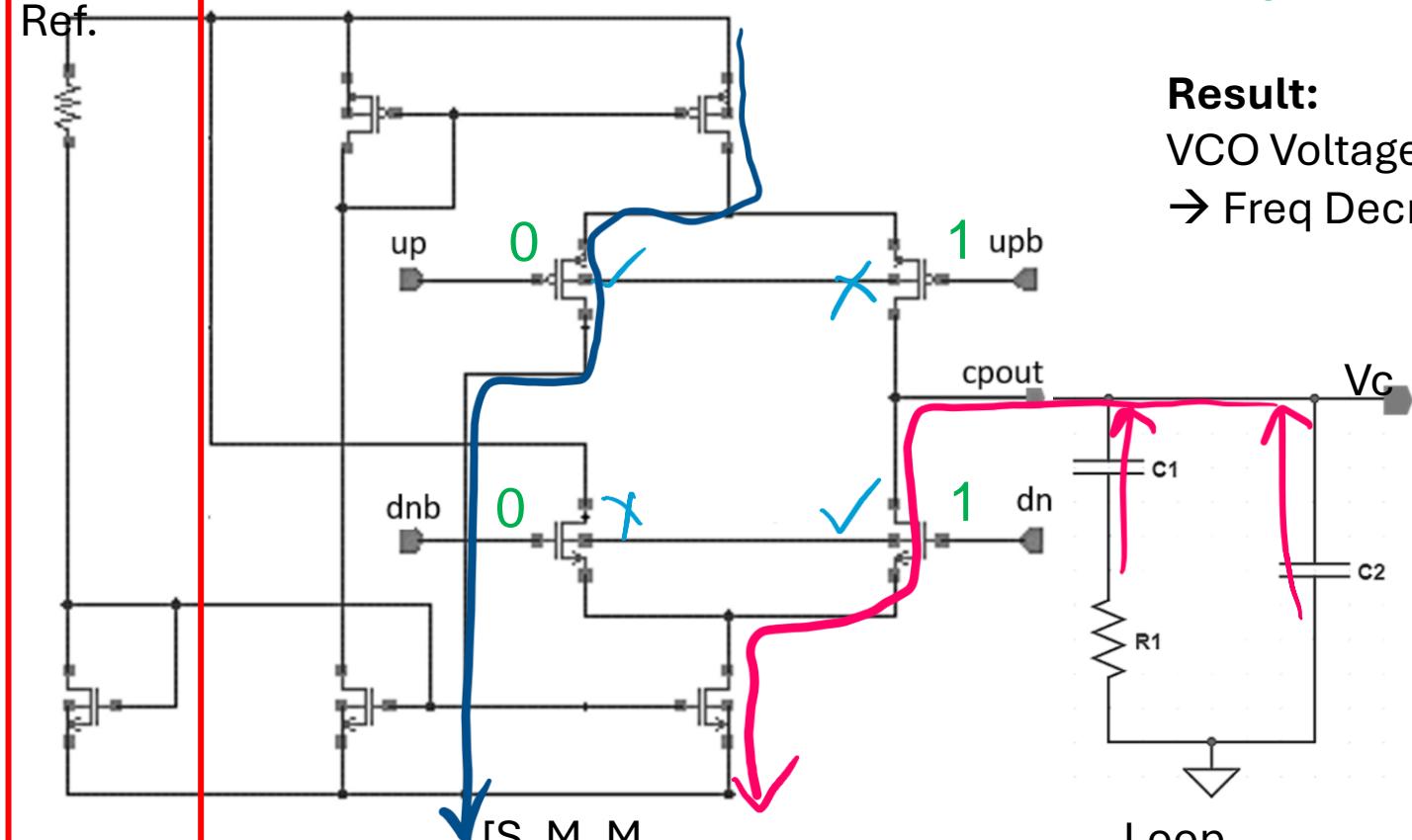
Result:

VCO Voltage increases → Freq Increases

Charge Pump

Current

Ref.



[S. M. M.
Ahsan, 2020]

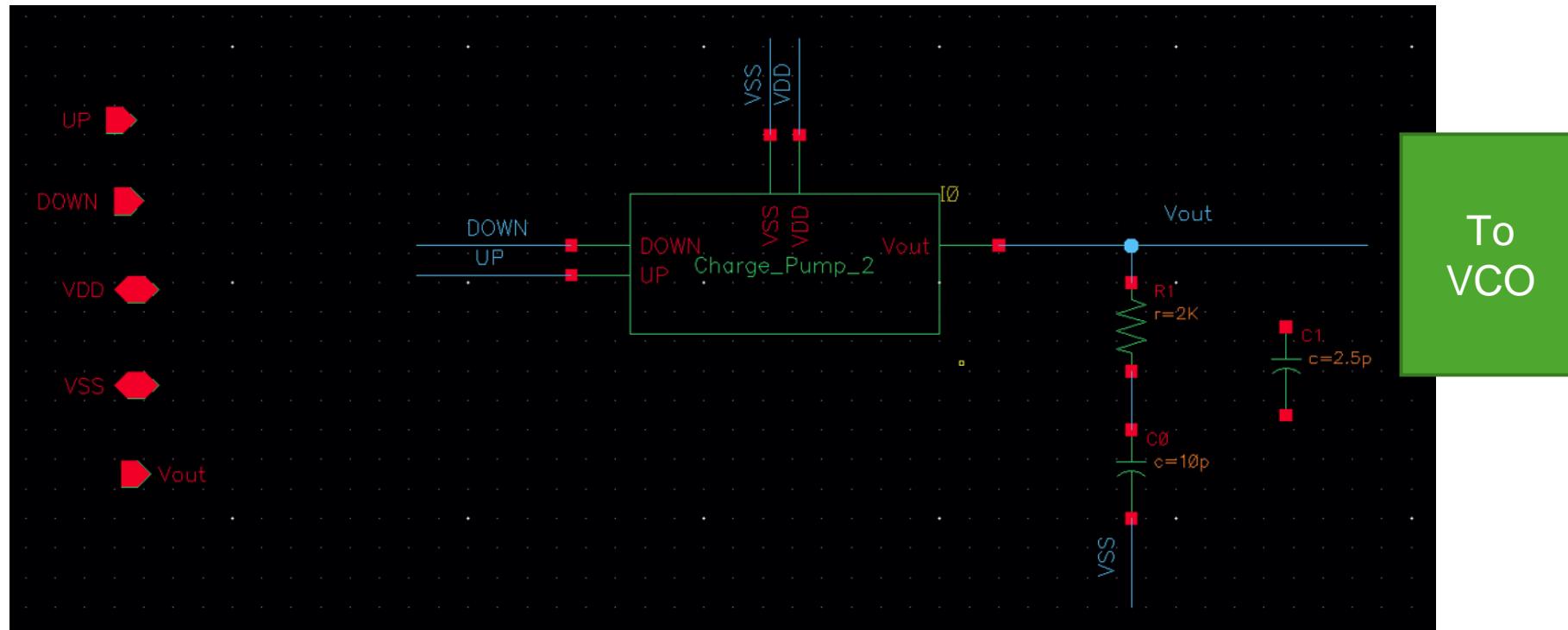
Case #2: Up: Low Pulse
Down: High Pulse

Result:

VCO Voltage Decreases
→ Freq Decreases

Filter Design

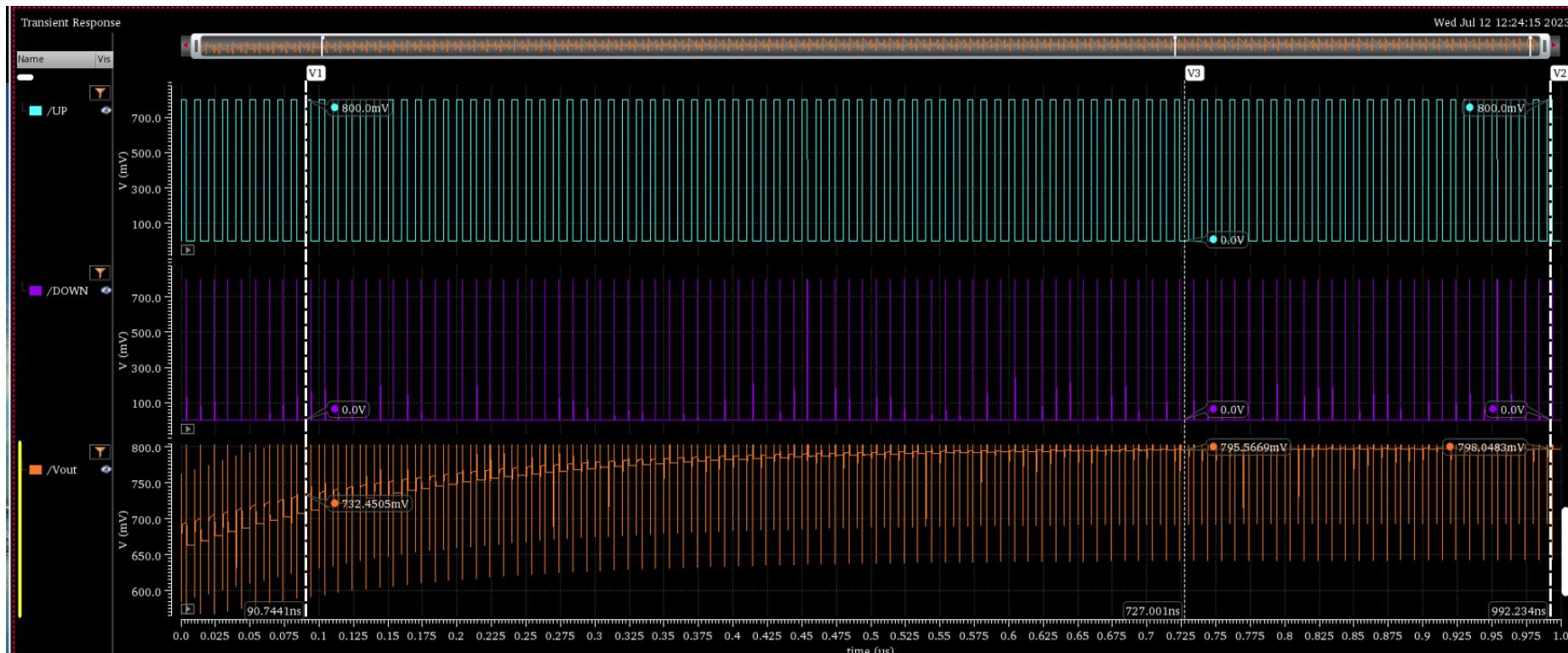
Can you guess the output for this RC filter?



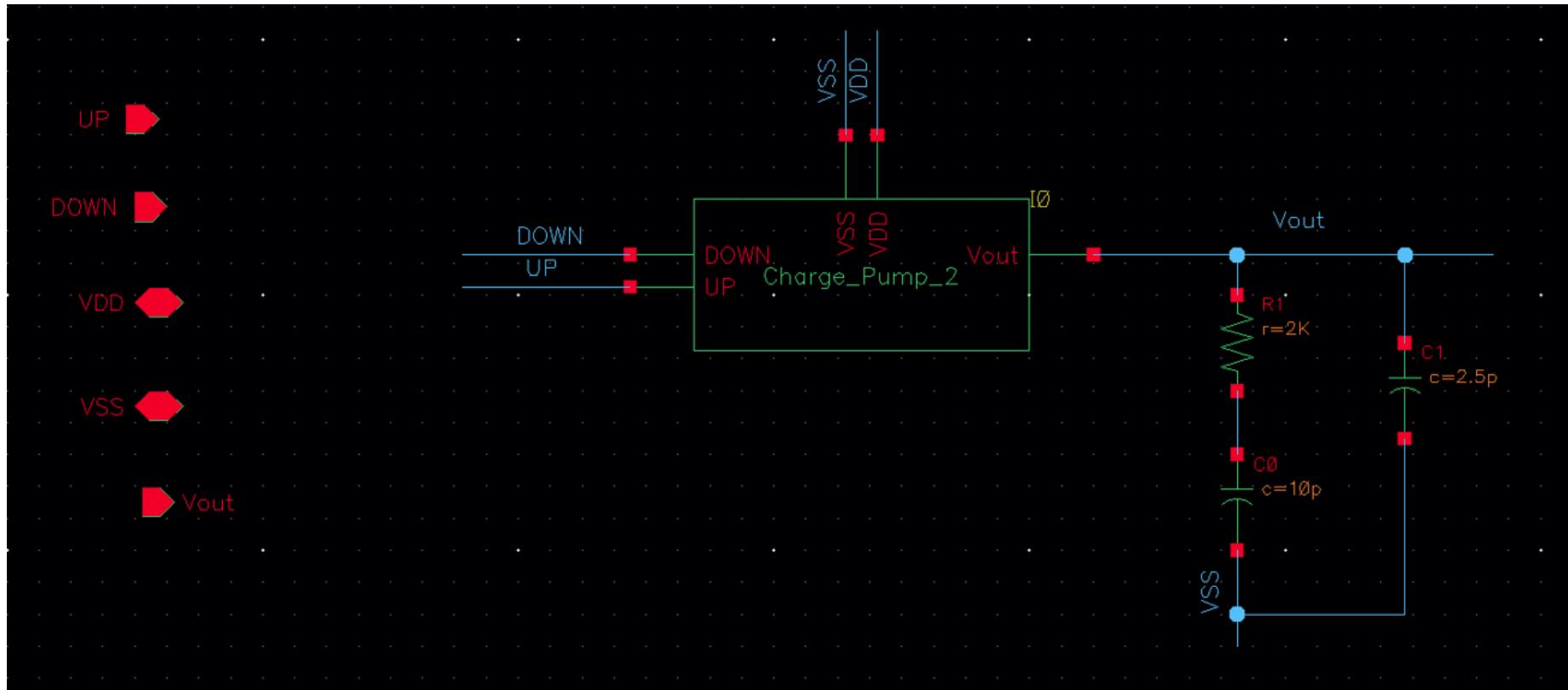
To
VCO

Filter Design

I don't want This!
Please HELP
Me!!!!

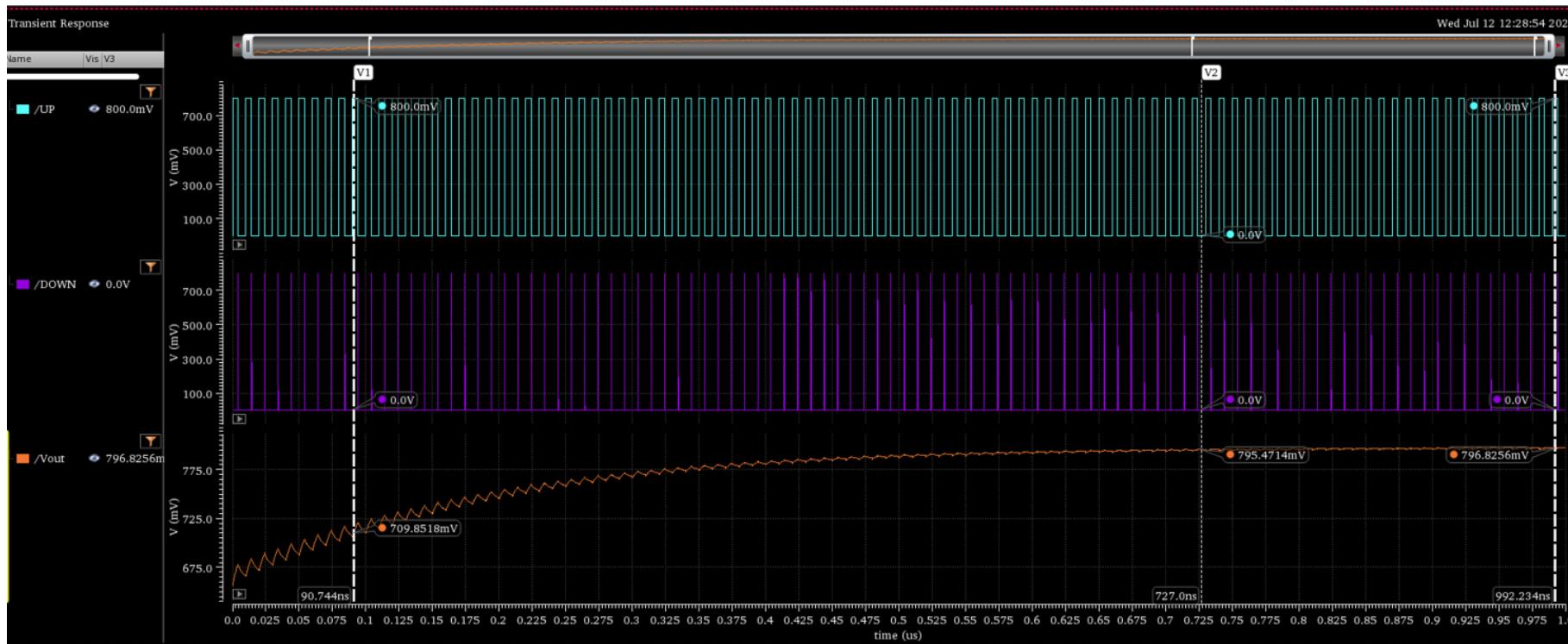


Filter Design



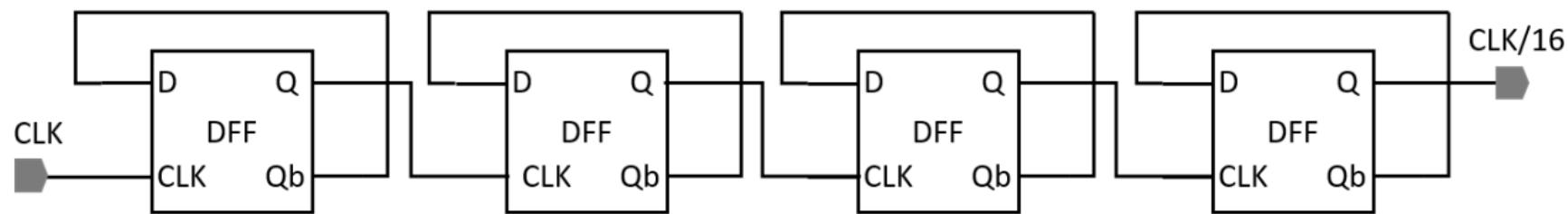
Filter Design

Ahhh!!!!
Sweeeet!



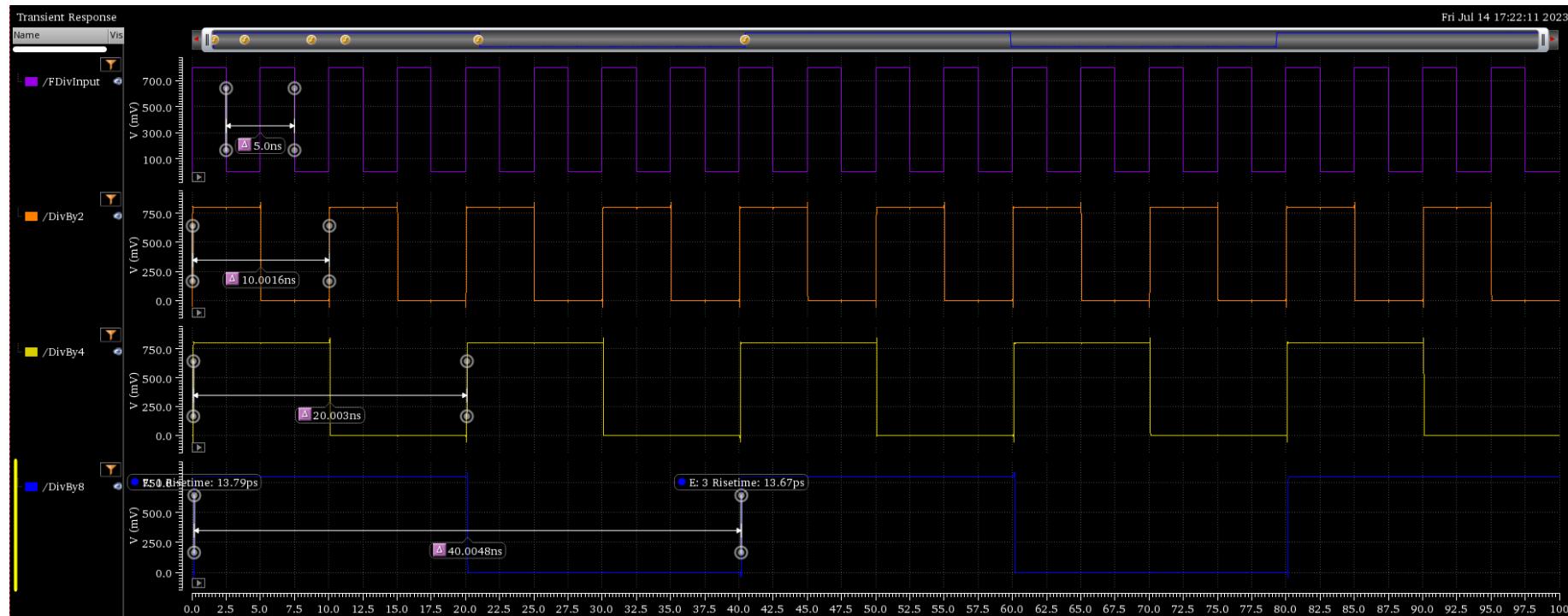
Frequency Divider

We can use DFF to divide frequency

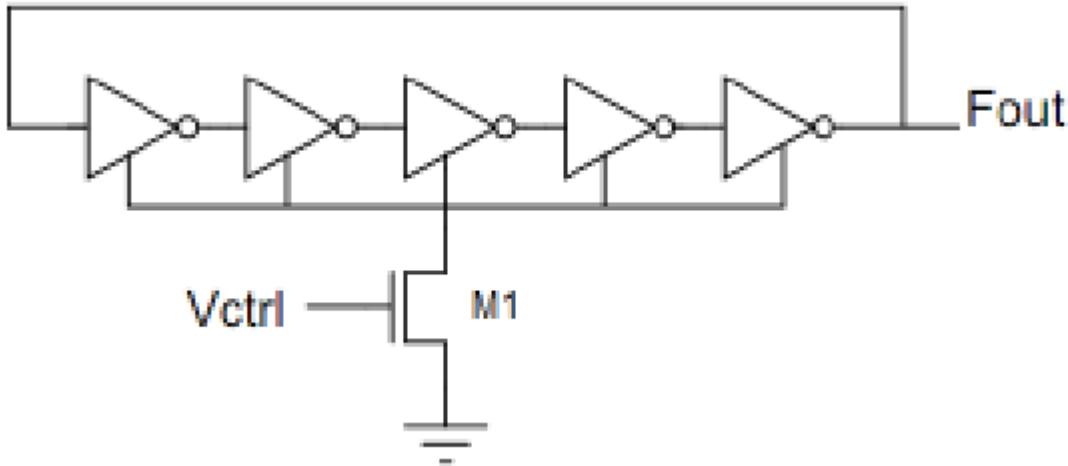


[S. M. M. Ahsan, 2020]

Frequency Divider



Ring Oscillator



$$f = \frac{1}{2tn}$$

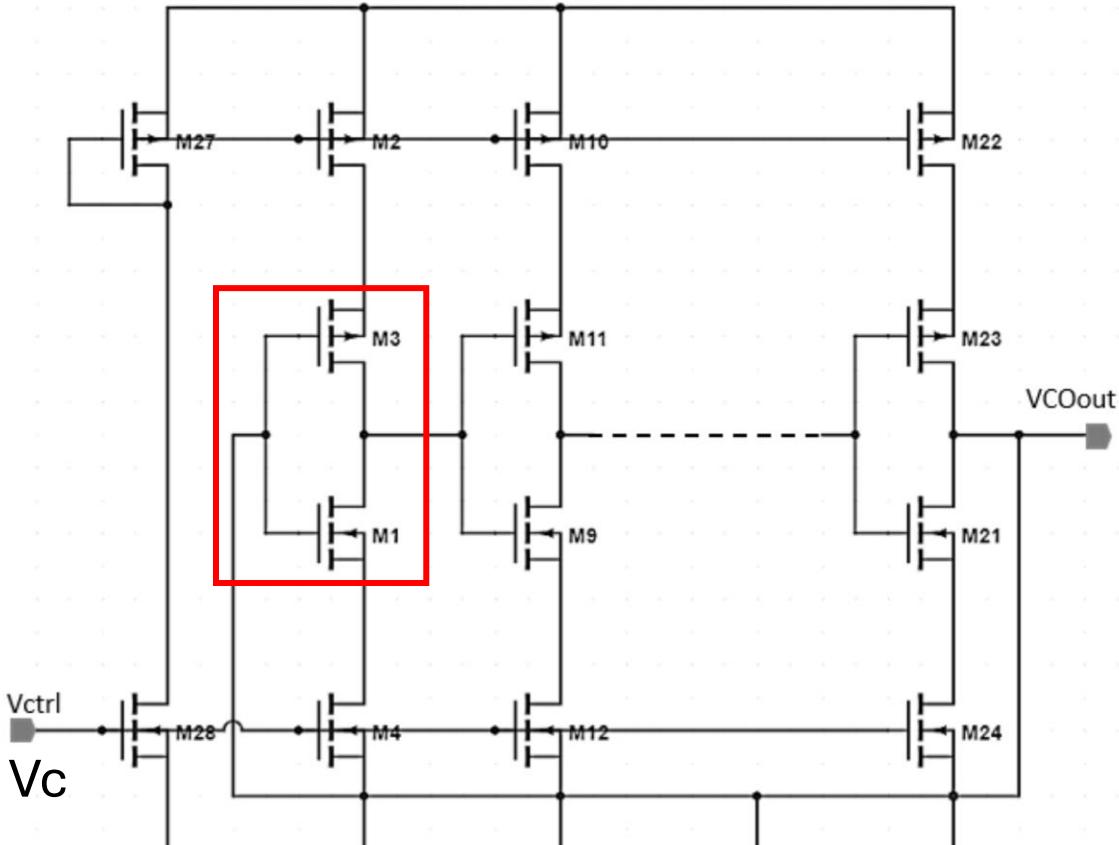
t → the time delay for a single inverter

n → the number of inverters in the inverter chain

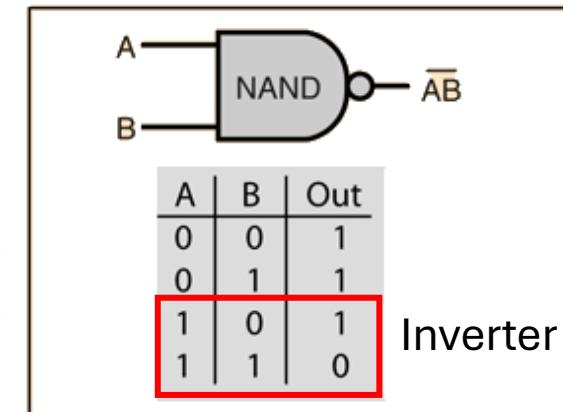
Caveat: The number of stages (n) MUST be odd

The more stages (n) there are, the lower the frequency will be.

Current Starved Ring Oscillator based VCO

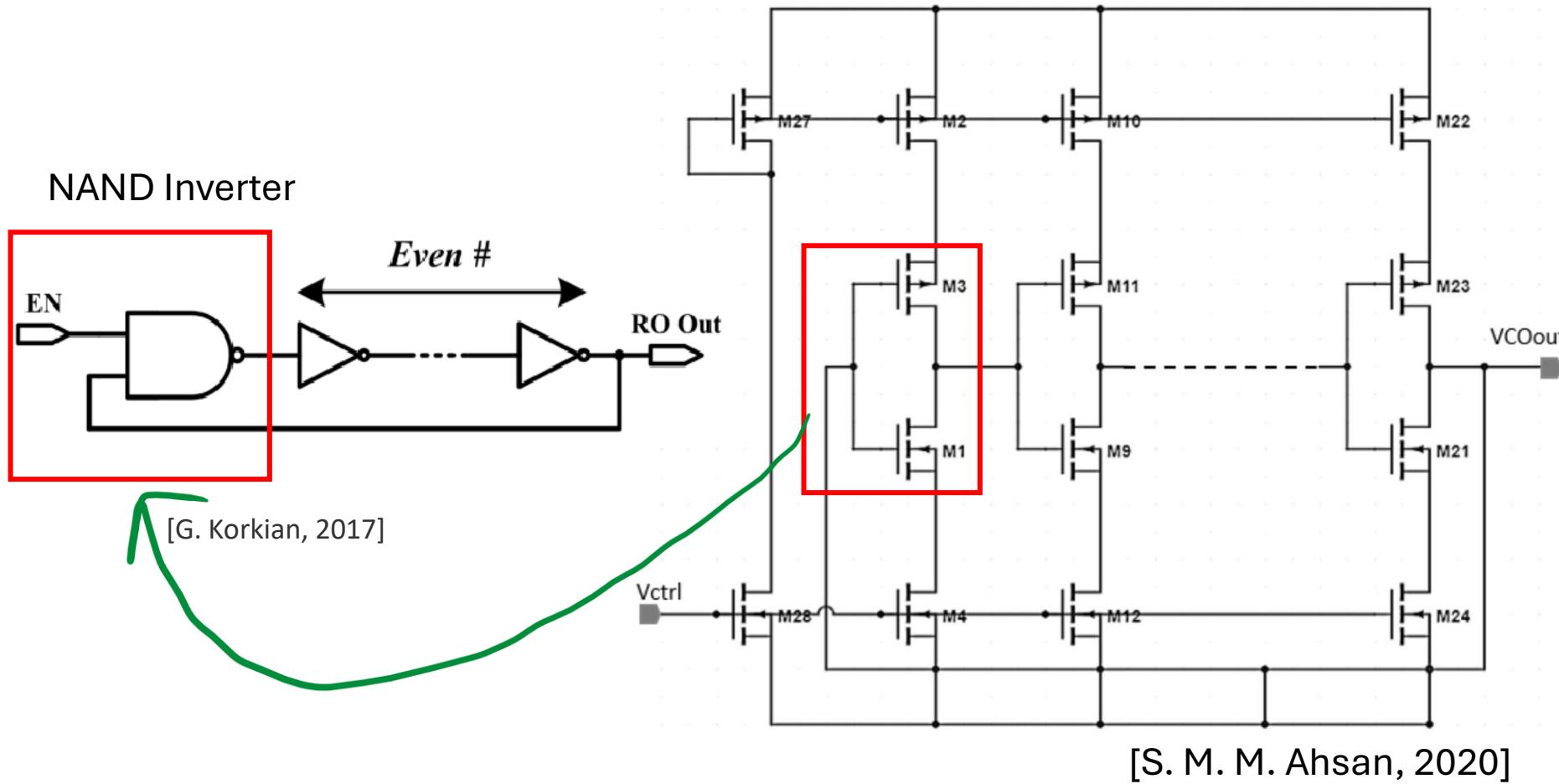


Watch out for the start-up initial condition!!!!

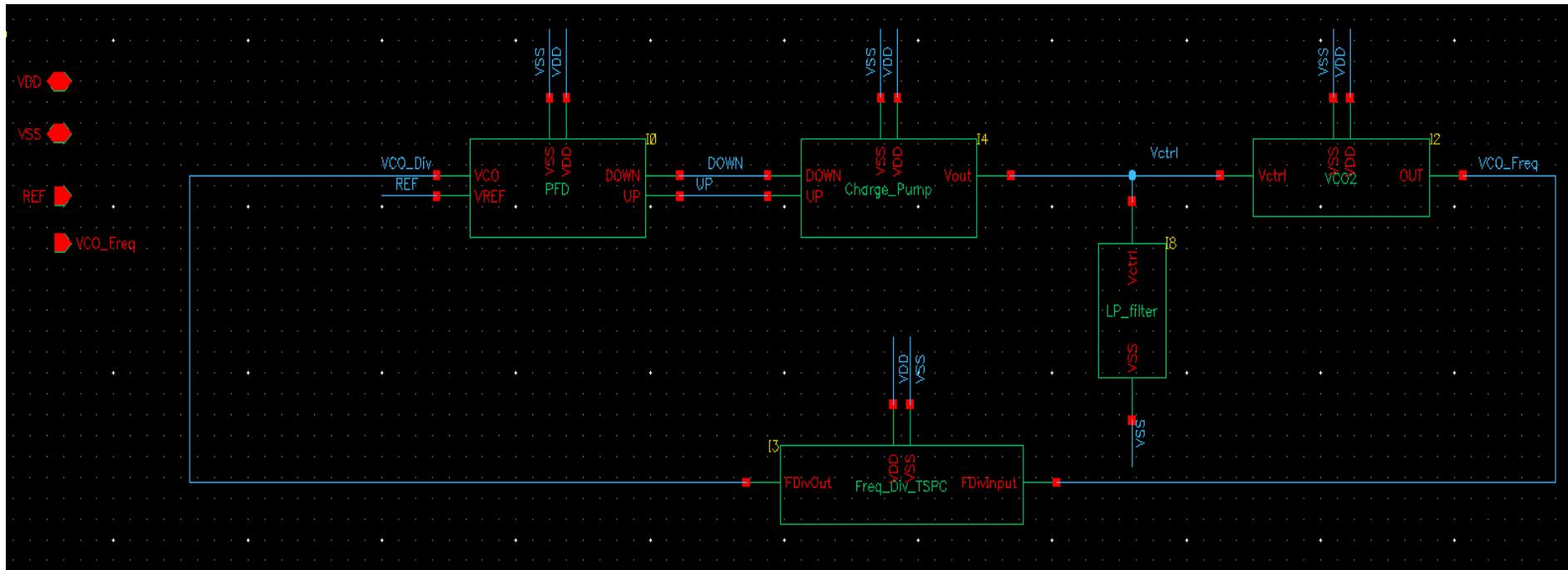


[S. M. M. Ahsan, 2020]

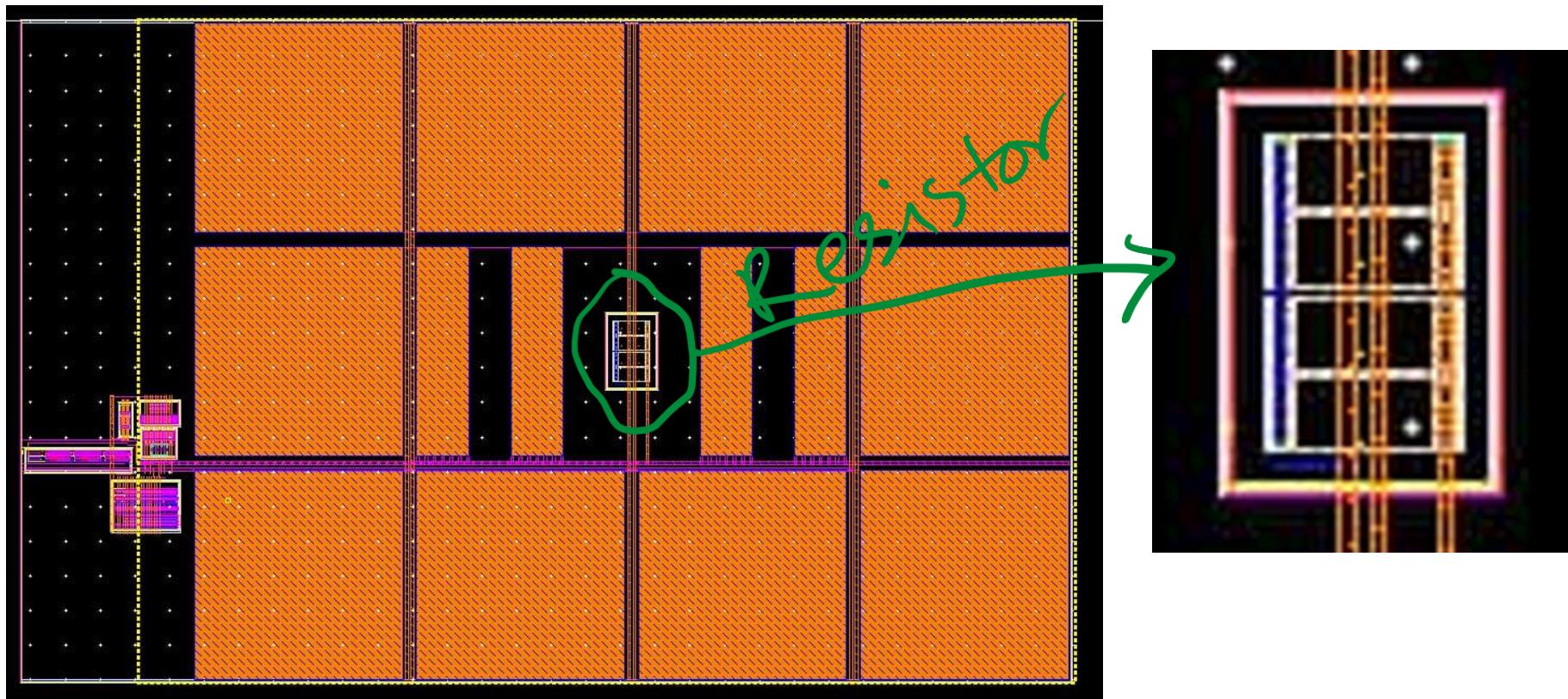
Current Starved Ring Oscillator based VCO



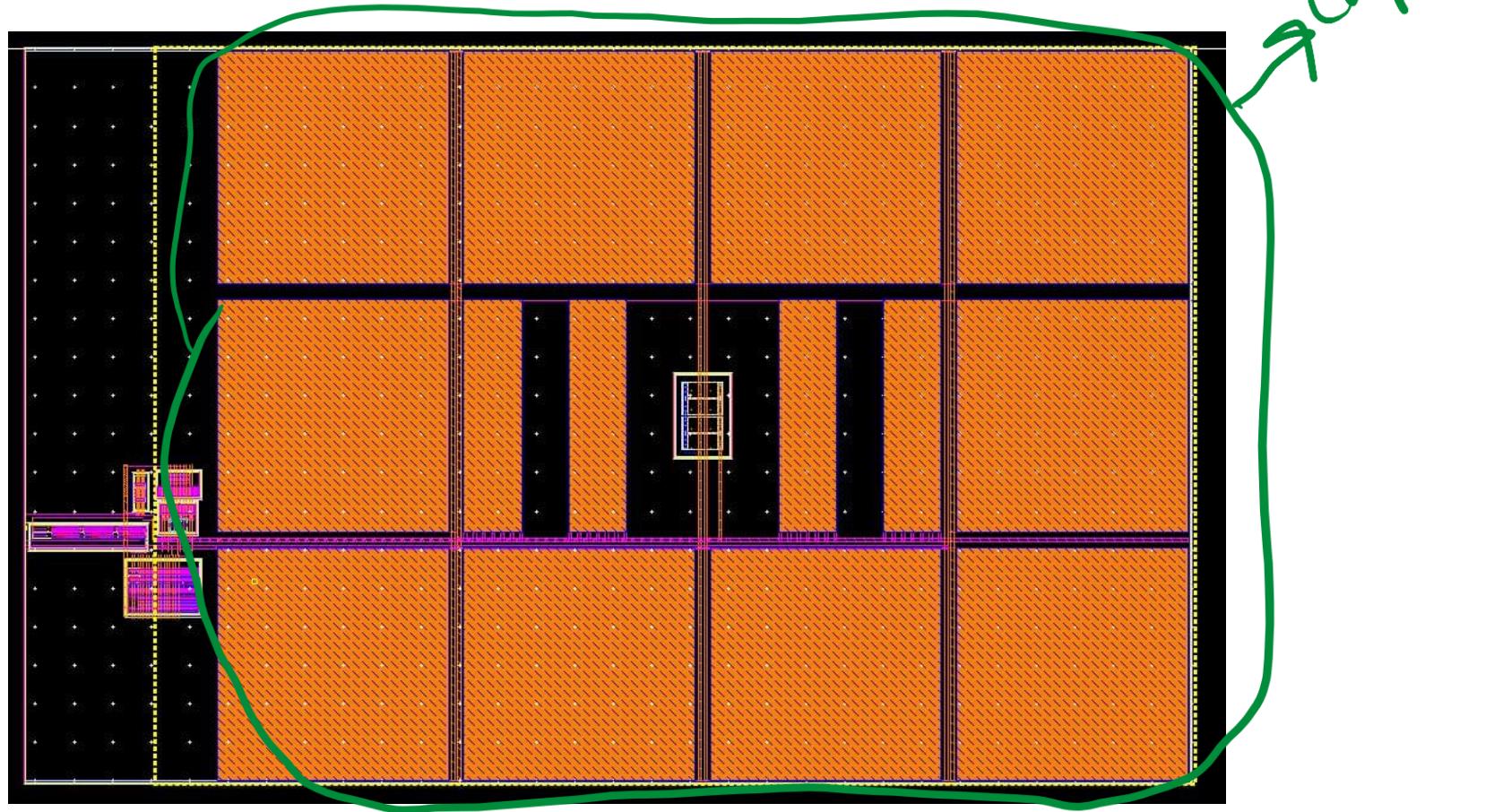
Whole PLL



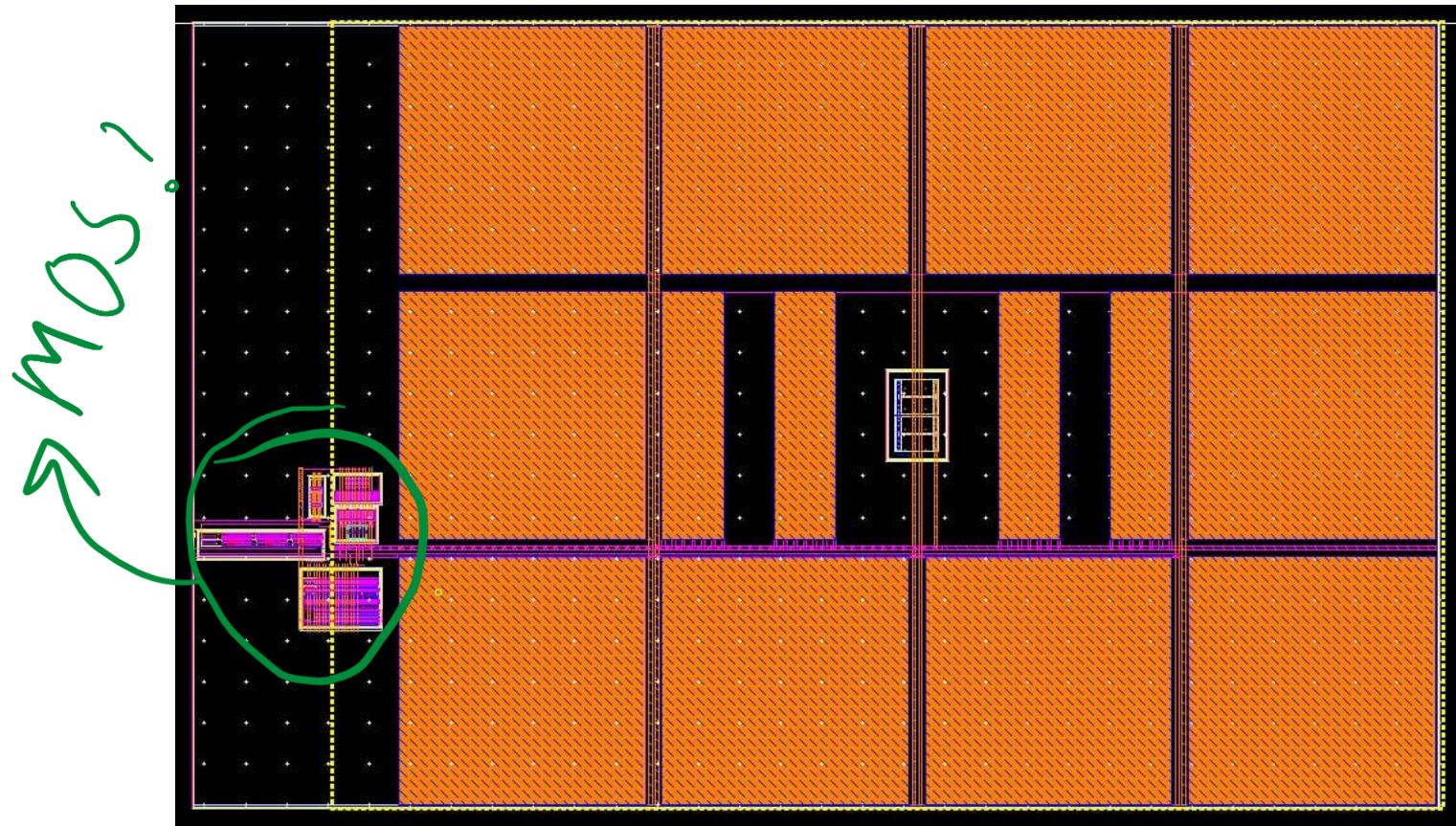
Layout of the Whole PLL



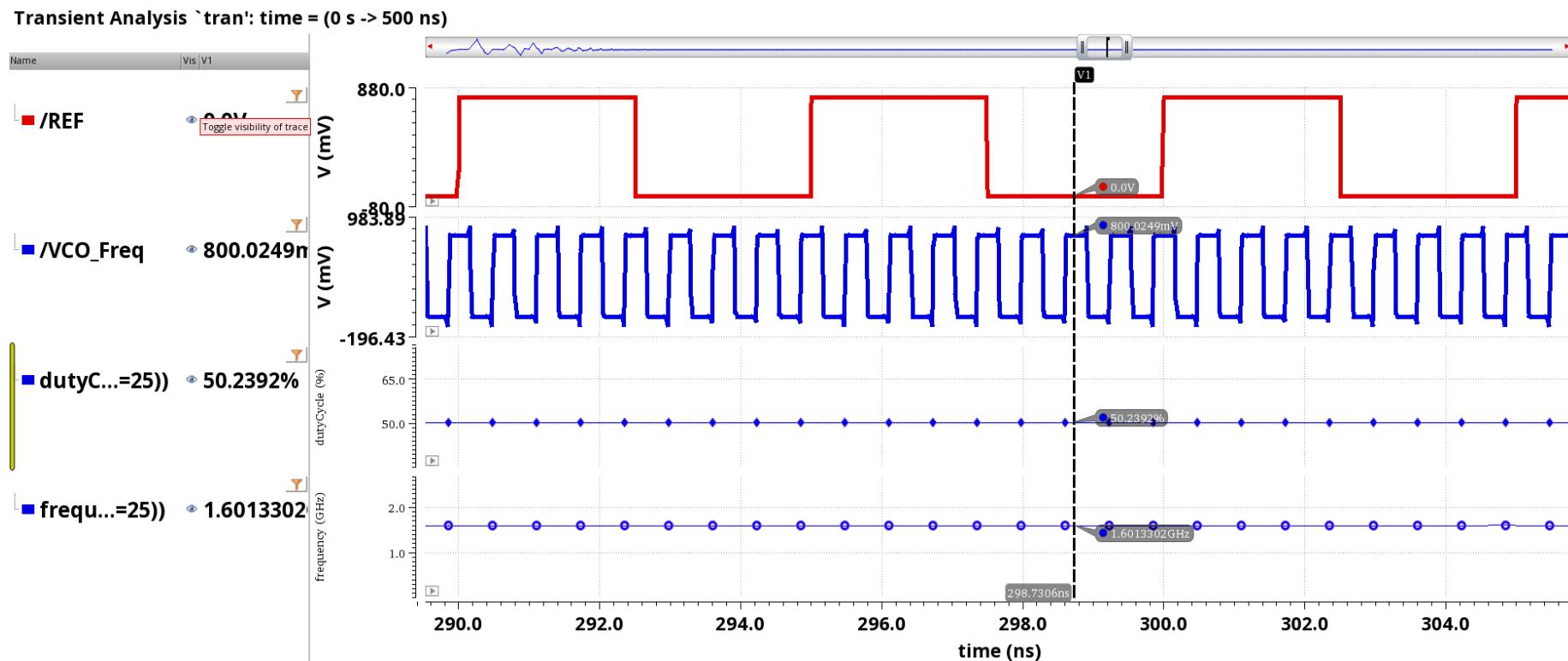
Layout of the Whole PLL



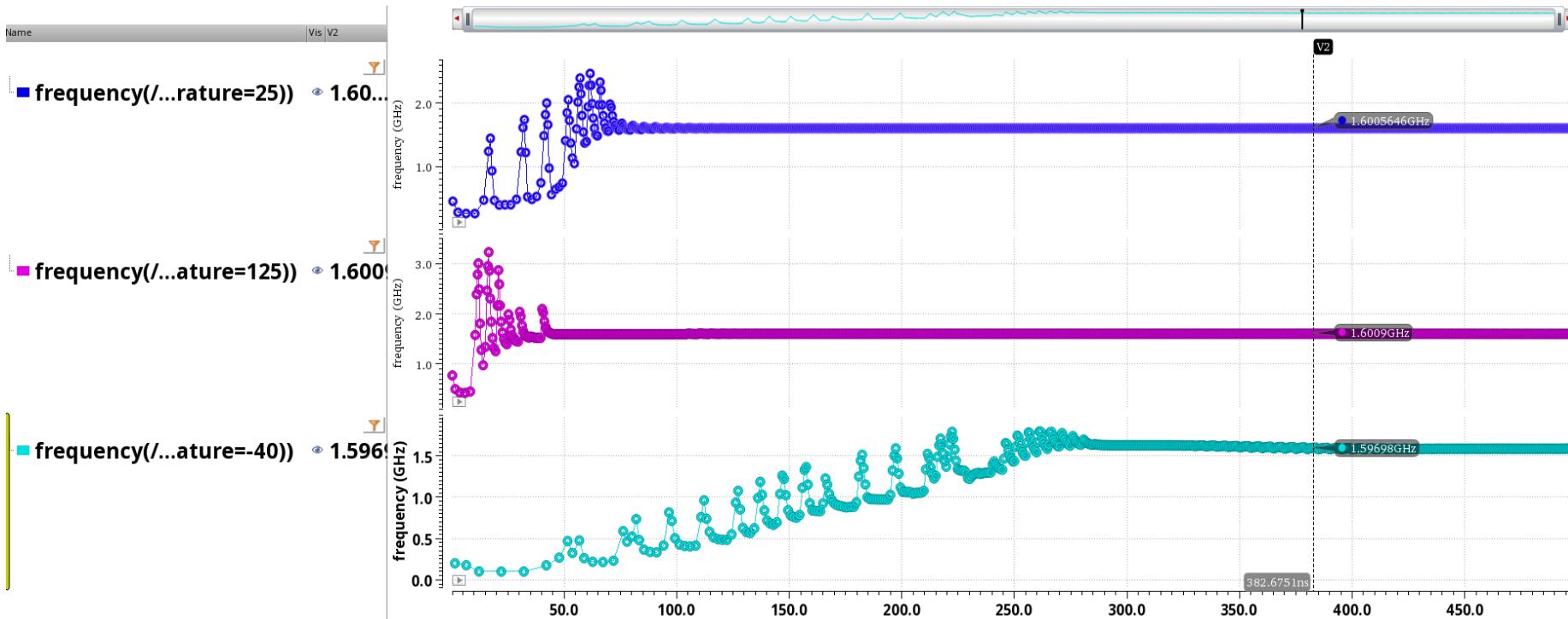
Layout of the Whole PLL



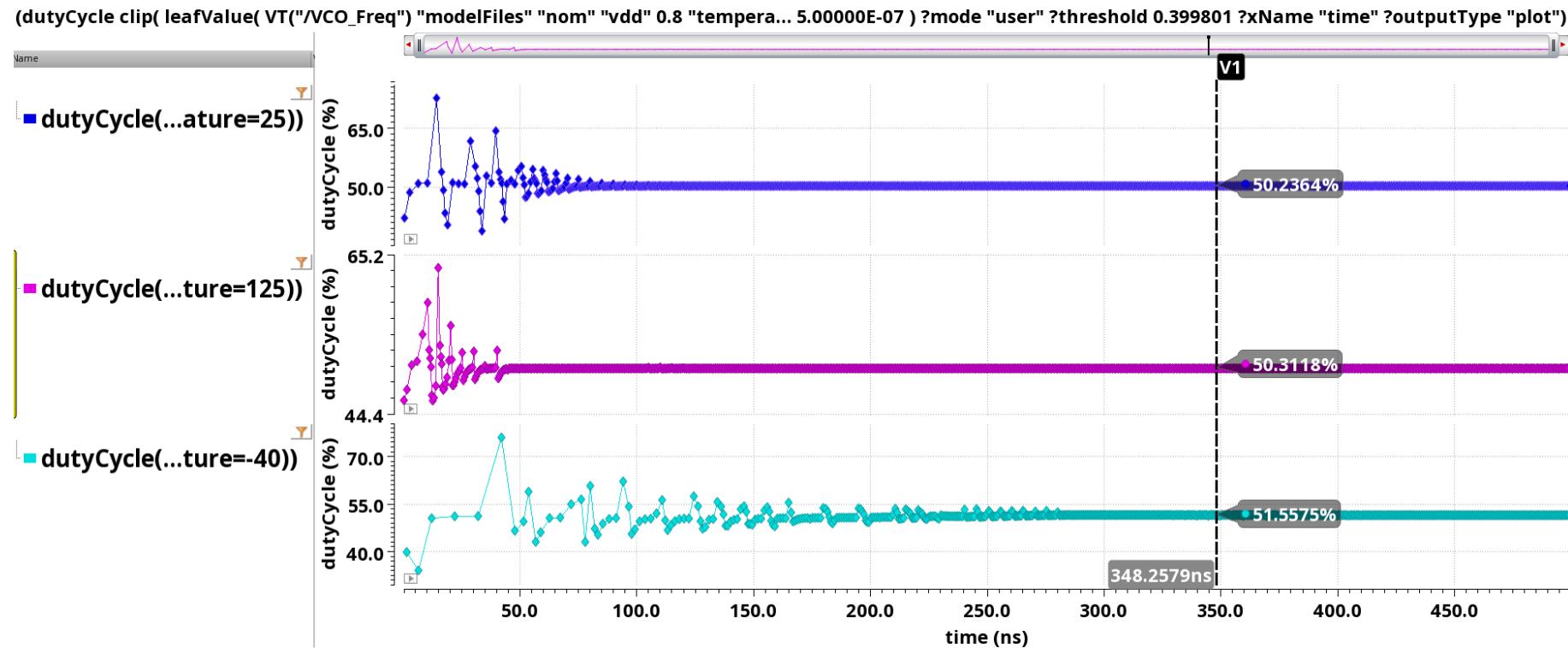
PLL Output



Frequency across PVT



Duty Cycle across PVT



Step by Step Design Guide of PLL in Cadence

Building Block of a PLL

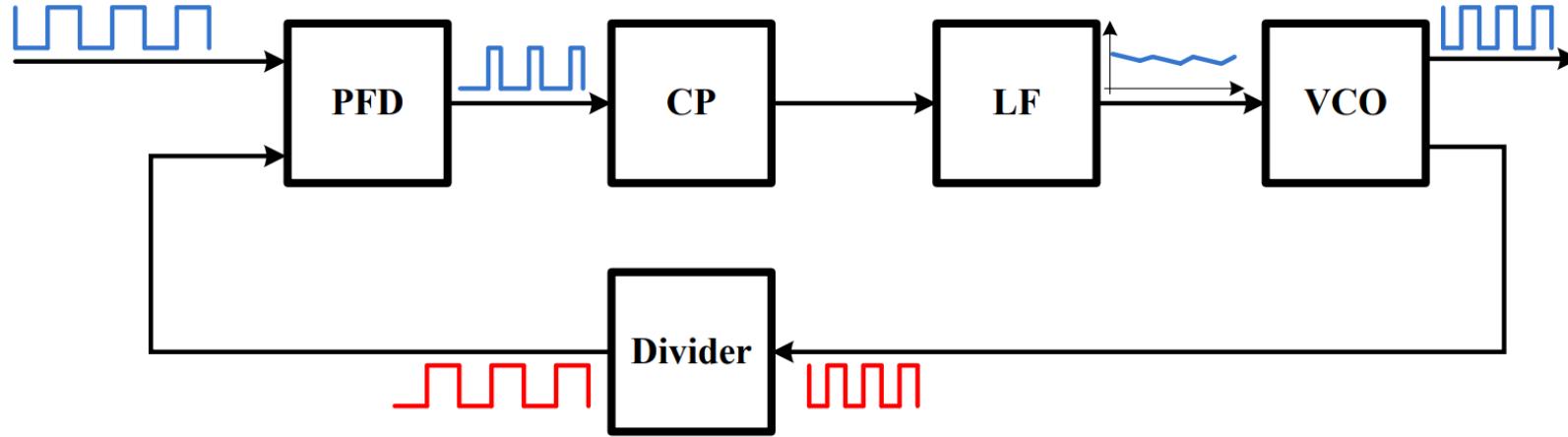


Fig. Block diagram of a PLL [1]

- A PLL primarily consists of 5 basic components
 - **Phase Frequency Detector (PFD):** $V_e \propto \phi_{er}$
 - **Charge Pump (CP):** $I_{cp} \propto V_e$
 - **Loop Filter:** $V_c \propto I_{cp}$ and filters out the high-frequency components
 - **Voltage Controlled Oscillator (VCO):** $F_{out} \propto V_c$
 - **Frequency Divider:** Divide the output freq (F_{out}) to generate the feedback signal

Features of the Designed PLL

- **Frequency Generation Range:** From 200 MHz to 1.6 GHz.
- **Supply Voltage:** 1.2 V
- **Transistor type:** Regular V_t (Threshold Voltage)
- **Settling Time and Average Power Consumption:**
 - **SS:** 873 ns and 110.5 μ W
 - **TT:** 715 ns and 163.4 μ W
 - **FF:** 507 ns and 215.3 μ W

Building Block of the PLL with Multiple Frequency Generation

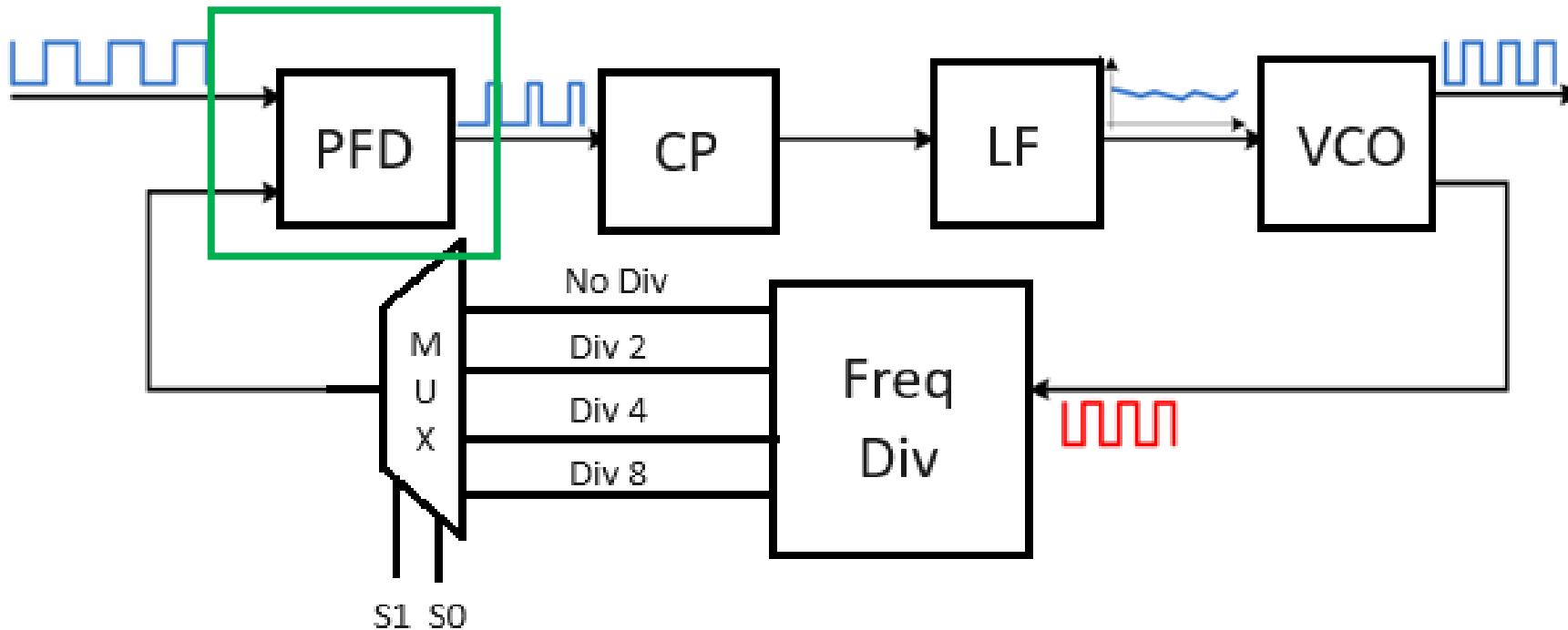


Fig. PLL with multiple frequencies

PFD Circuit

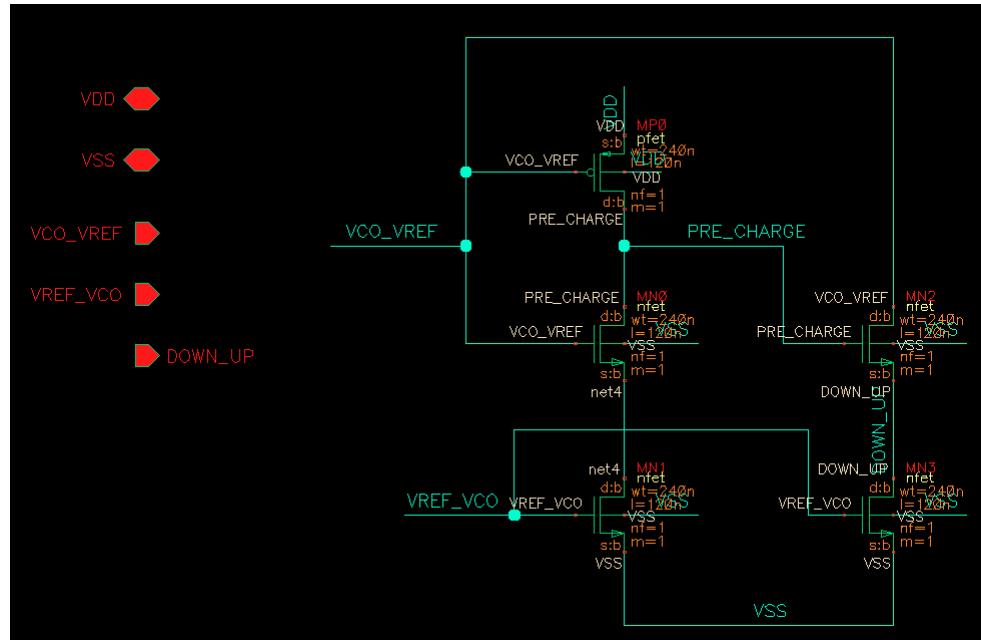


Fig. PFD Core Circuit

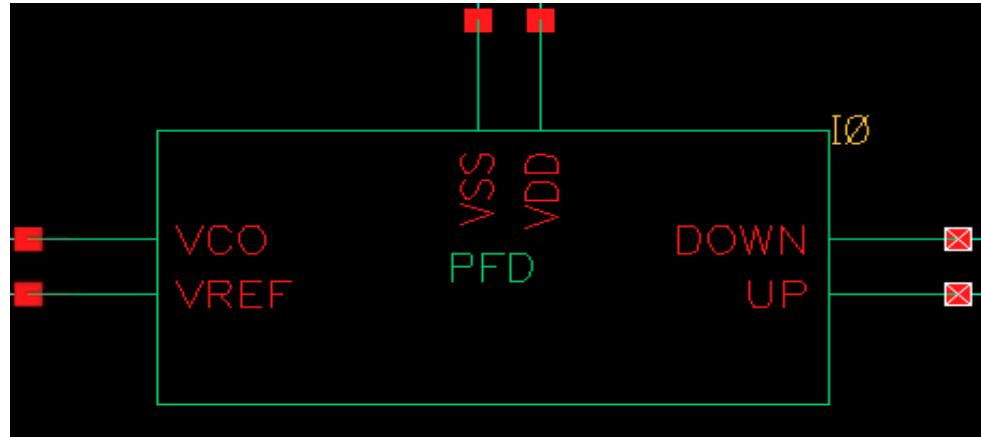


Fig. PFD Circuit Symbol

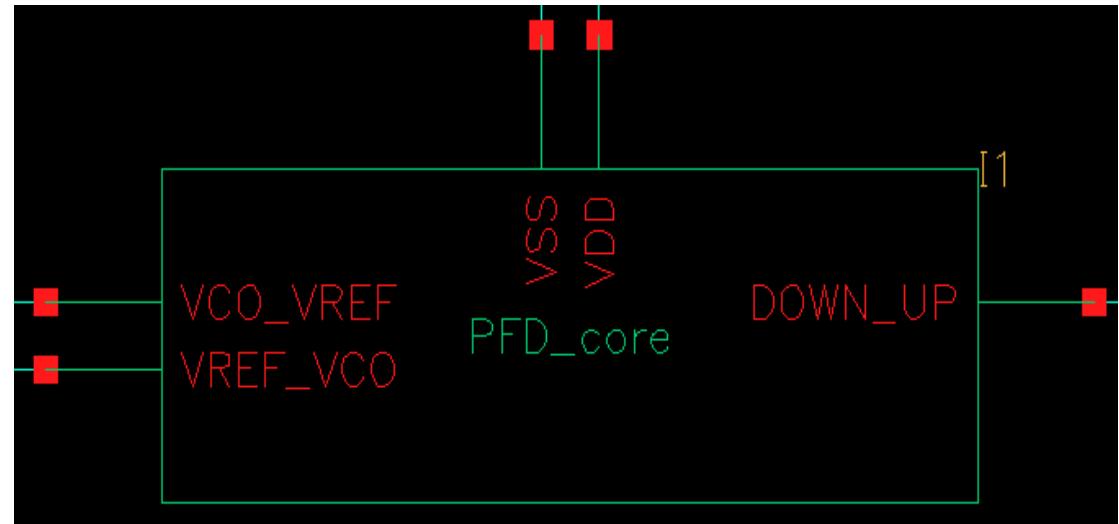


Fig. PFD Core Symbol

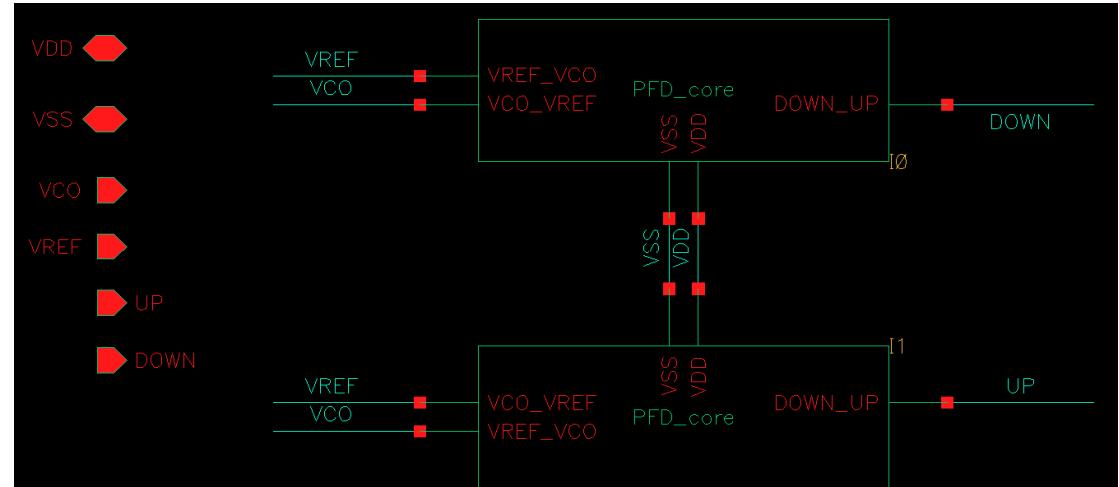


Fig. PFD Circuit

PFD Layout

VDD
 VSS
 VCO_VREF
 VREF_VCO
 DOWN_UP

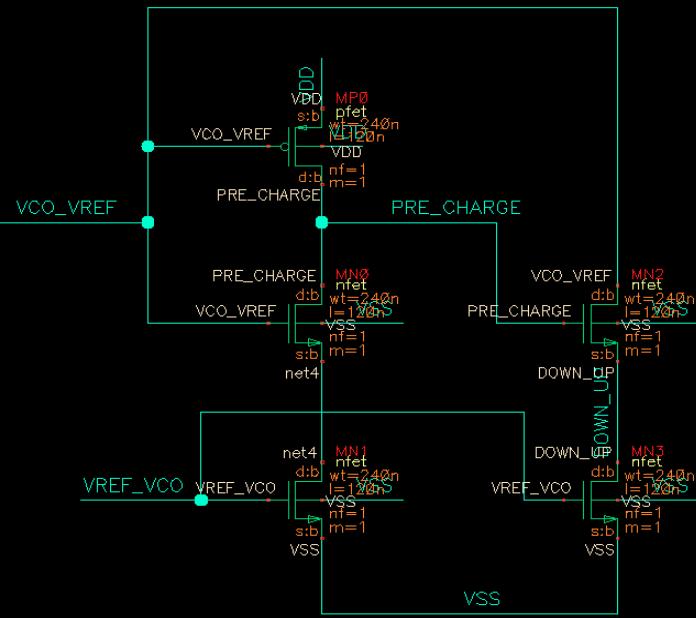


Fig. PFD Core



Fig. PFD Core Symbol

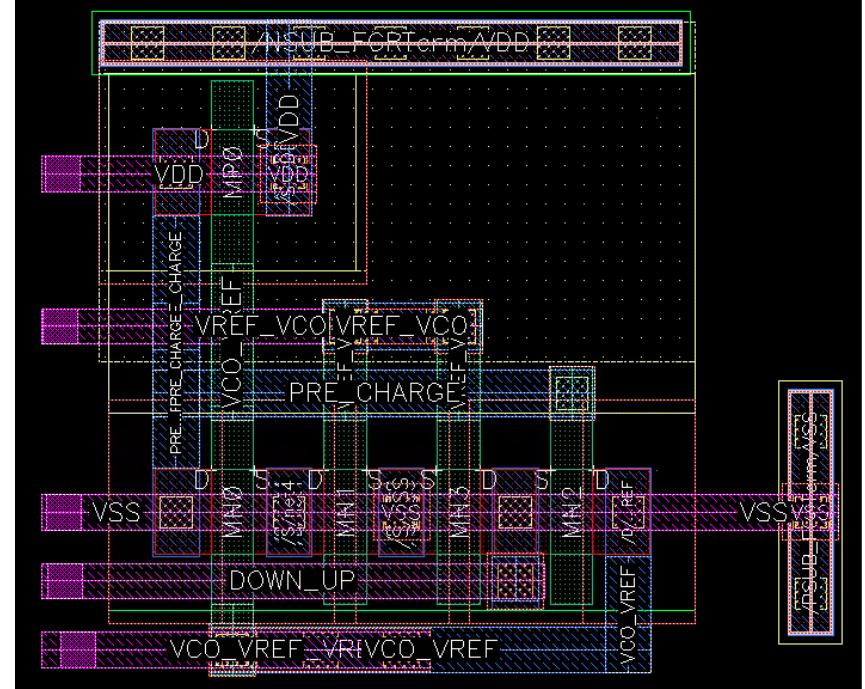


Fig. PFD Core Layout

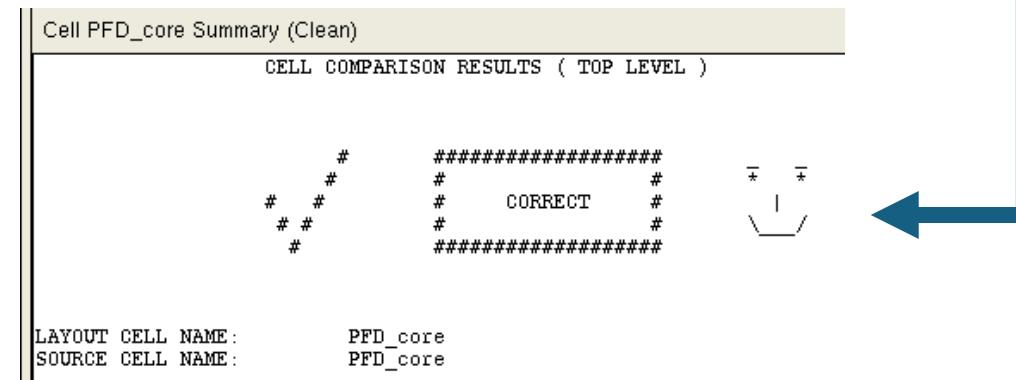


Fig. PFD Core LVS Report

PFD Layout

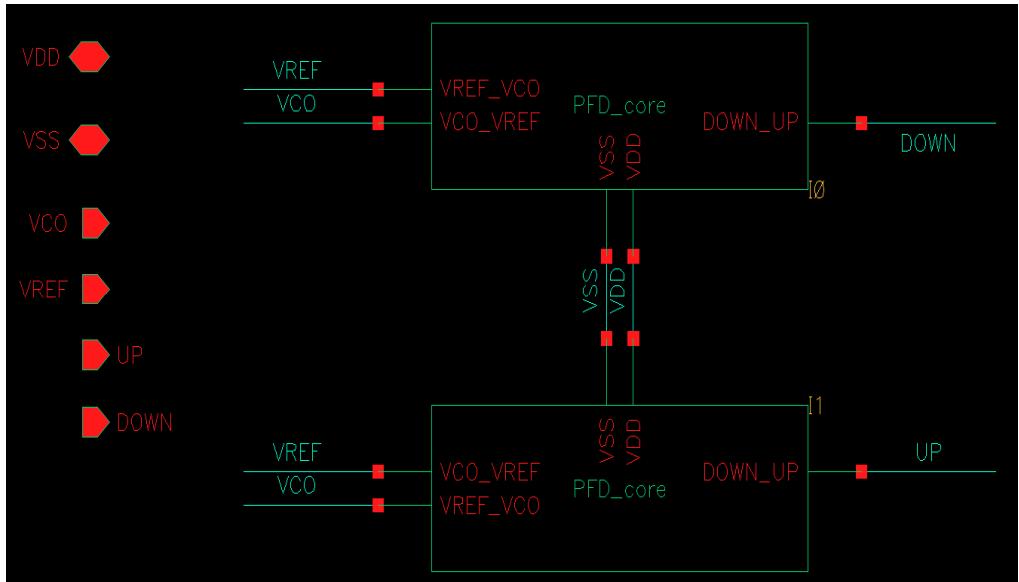


Fig. PFD Circuit

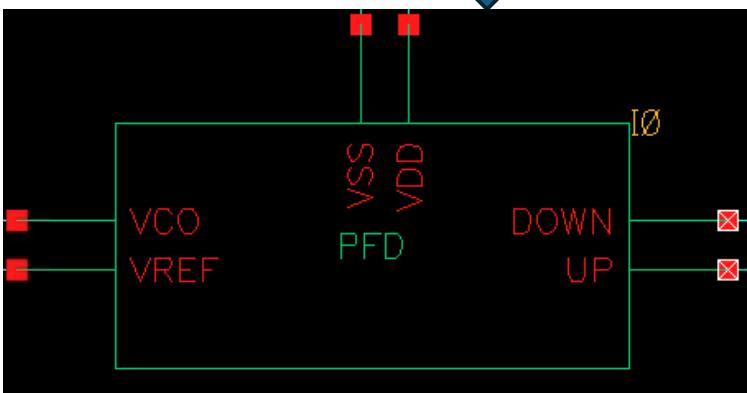


Fig. PFD Symbol

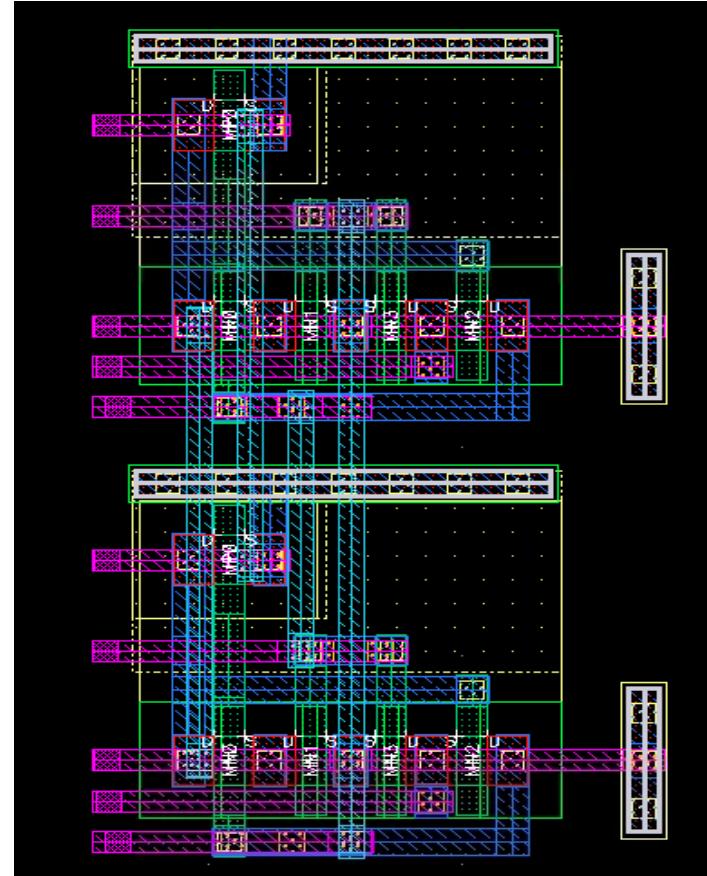


Fig. PFD Layout



Fig. PFD LVS Report

Testbench for the PFD

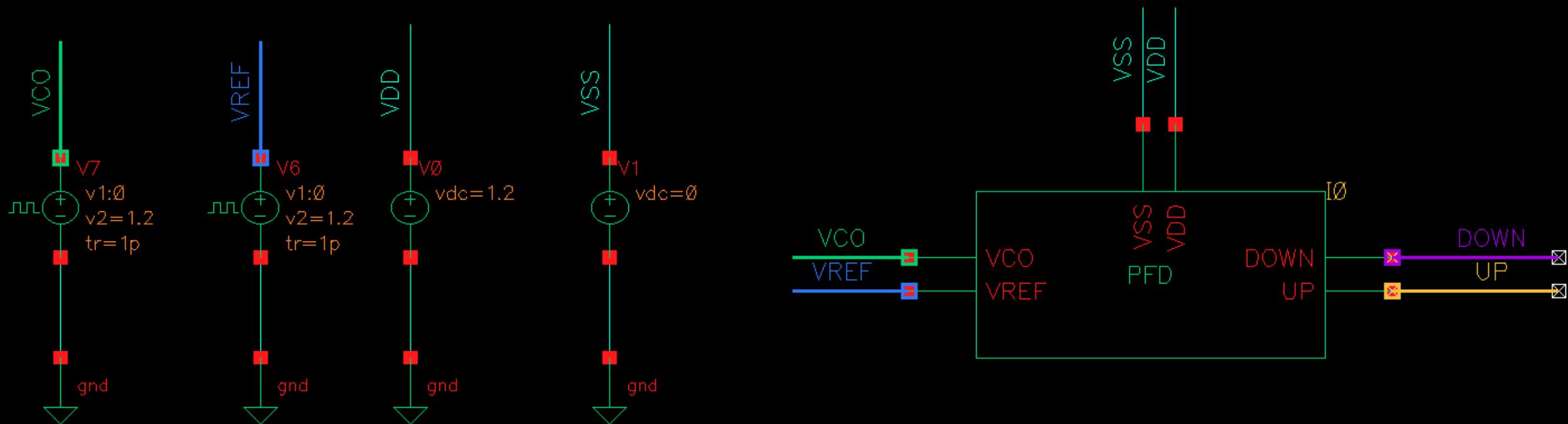
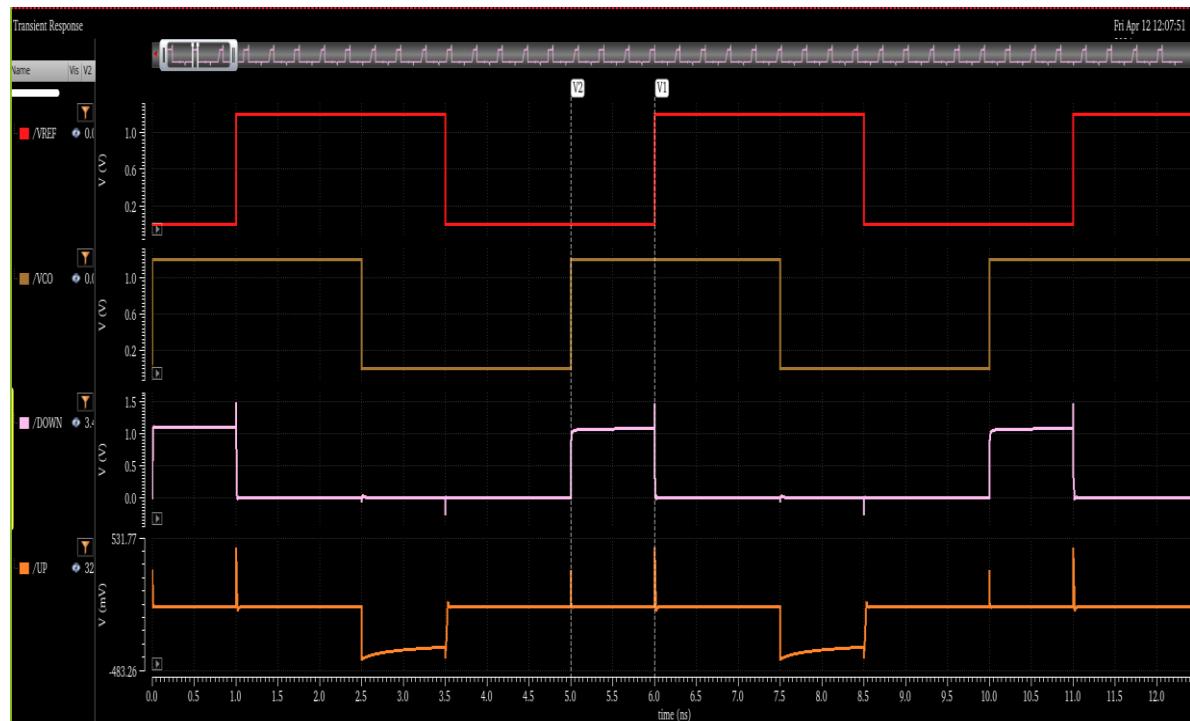
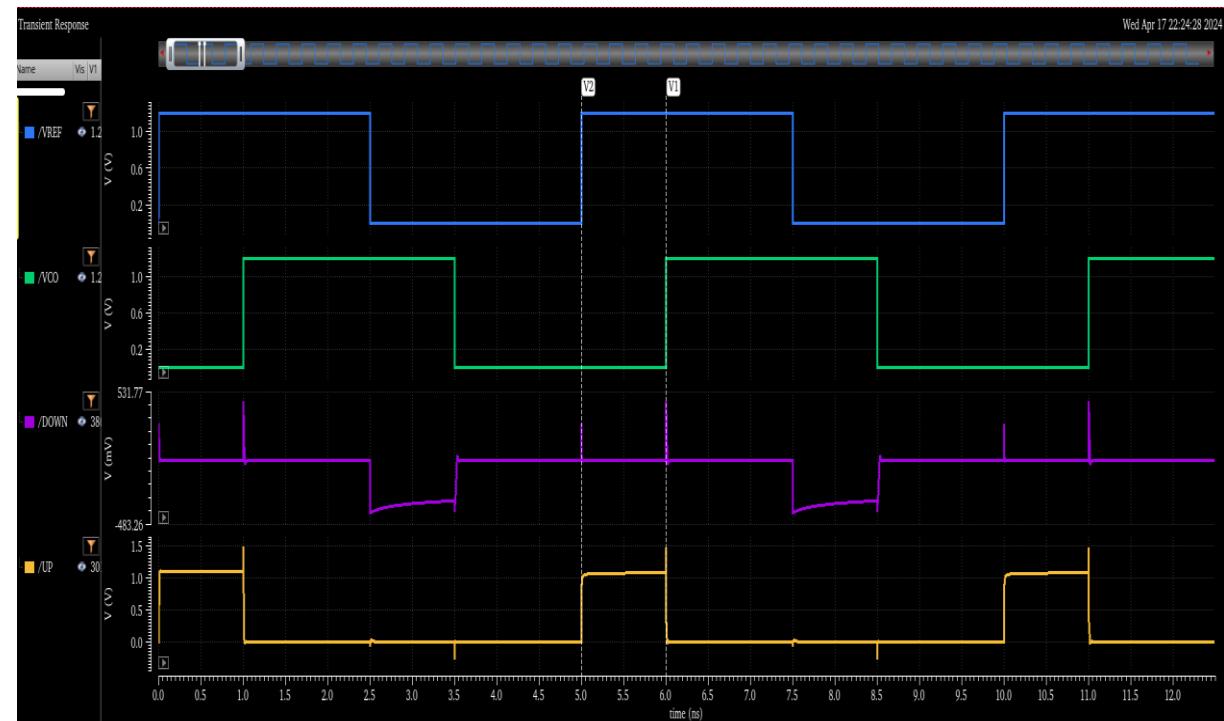


Fig. PFD Testbench Setup

Output of the PFD



F_{VCO} appears earlier than F_{Ref}



F_{VCO} appears later than F_{Ref}

Fig. PFD Output

Let's design the charge pump and loop filter

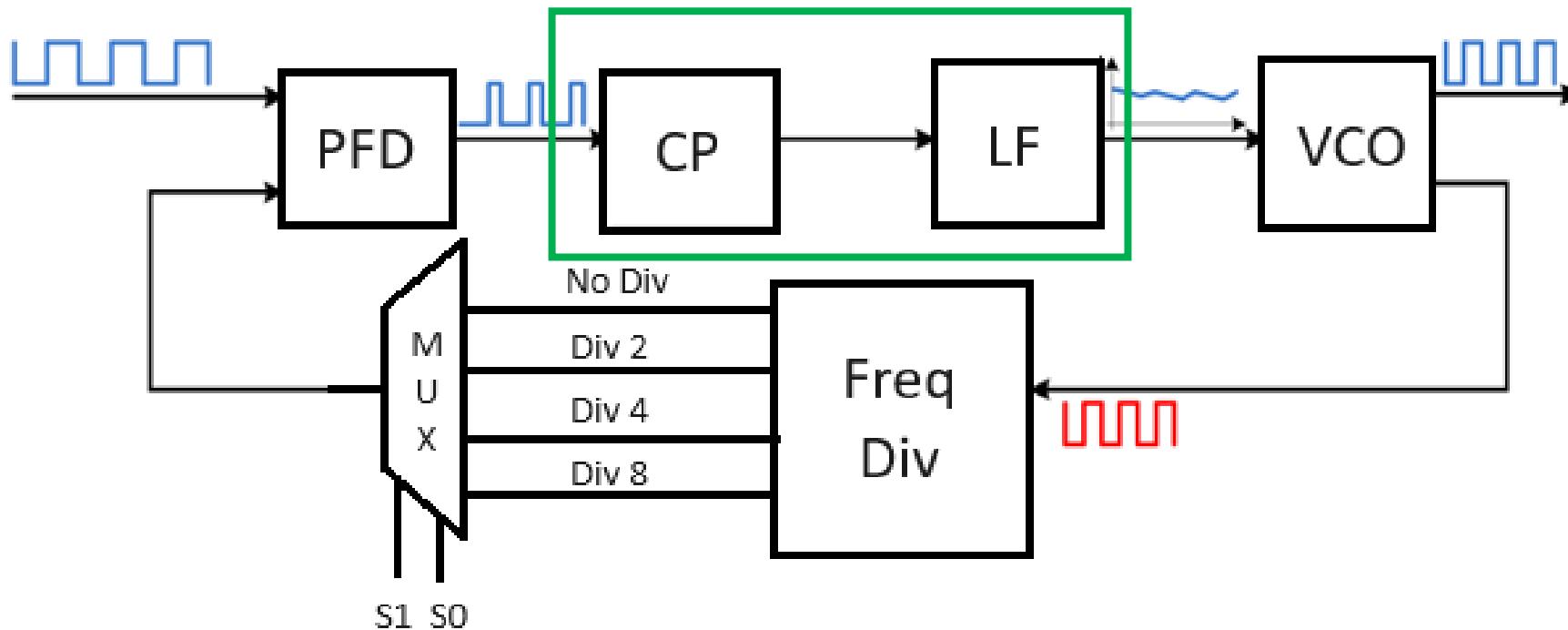


Fig. Charge pump and LF design

Charge Pump and LF

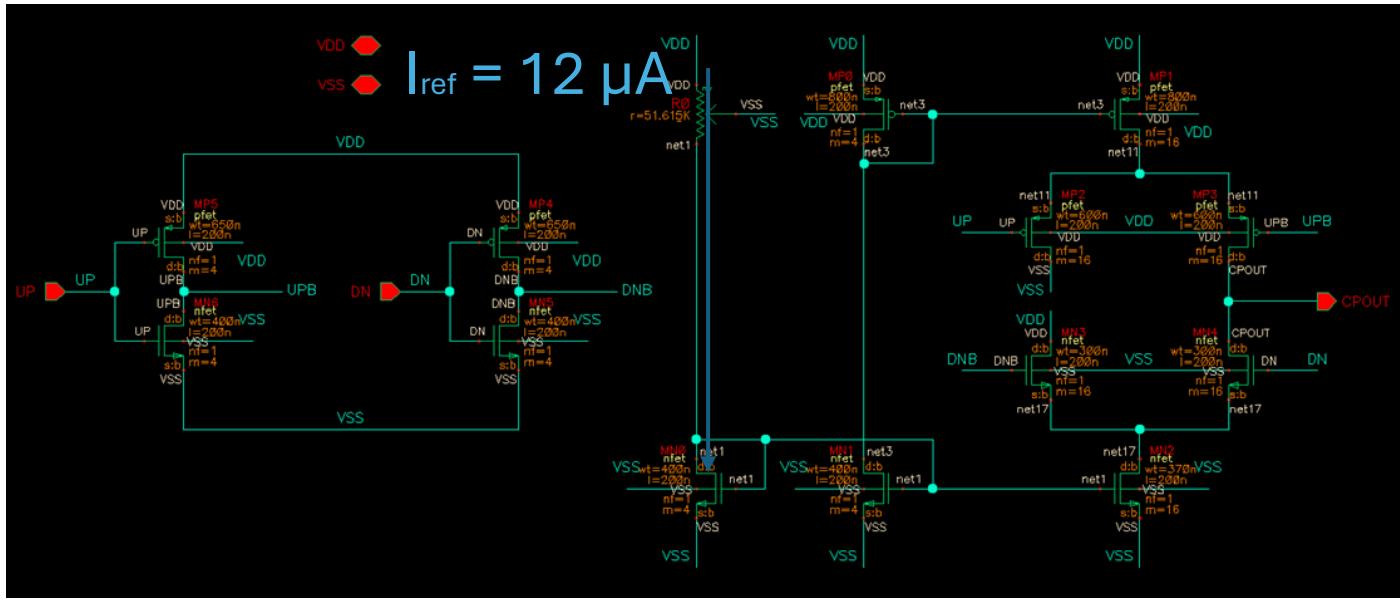


Fig. Schematic of Charge Pump

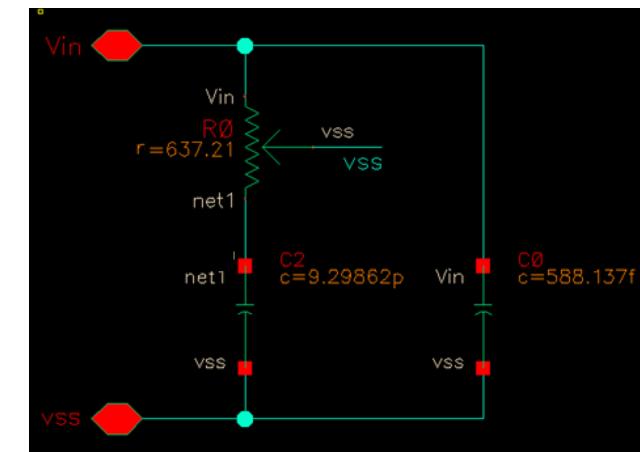


Fig. LF schematic

Testbench – CP & LF

- Two vbit modules to simulate the outputs from PFD
- LF is connected at the output of the Charge Pump
- Measure the voltage of CPOUT to validate the operation of the charge pump

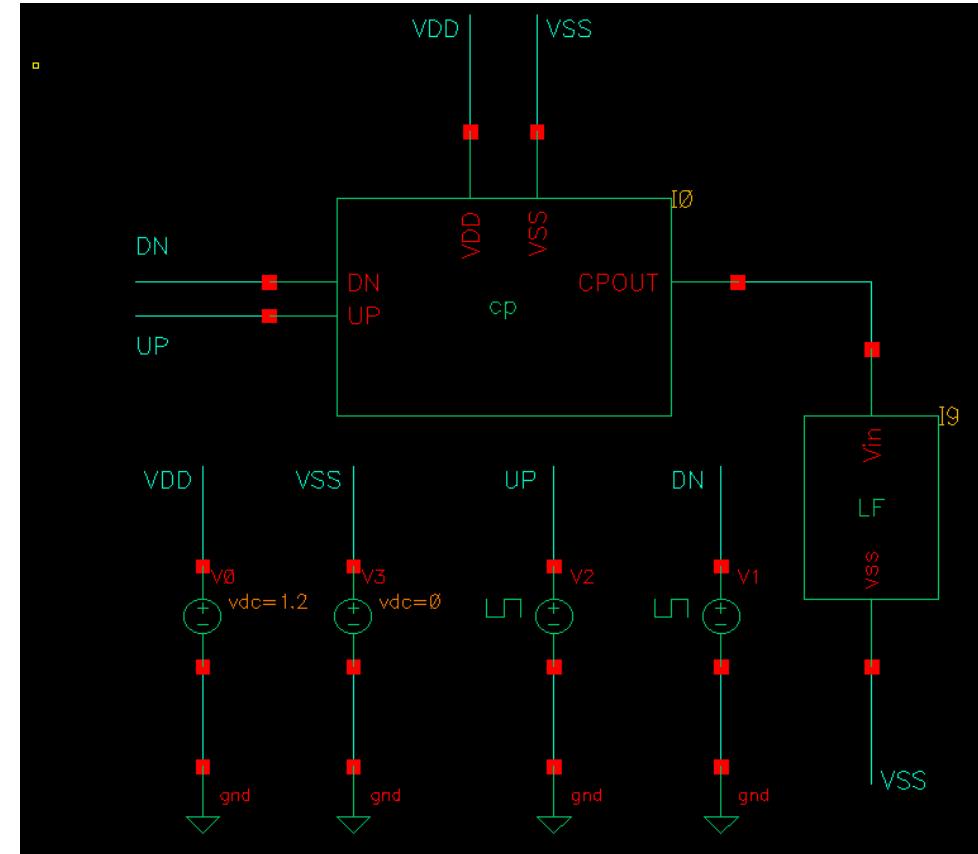


Fig. Testbench of CP & LF

Test Result – CP & LF

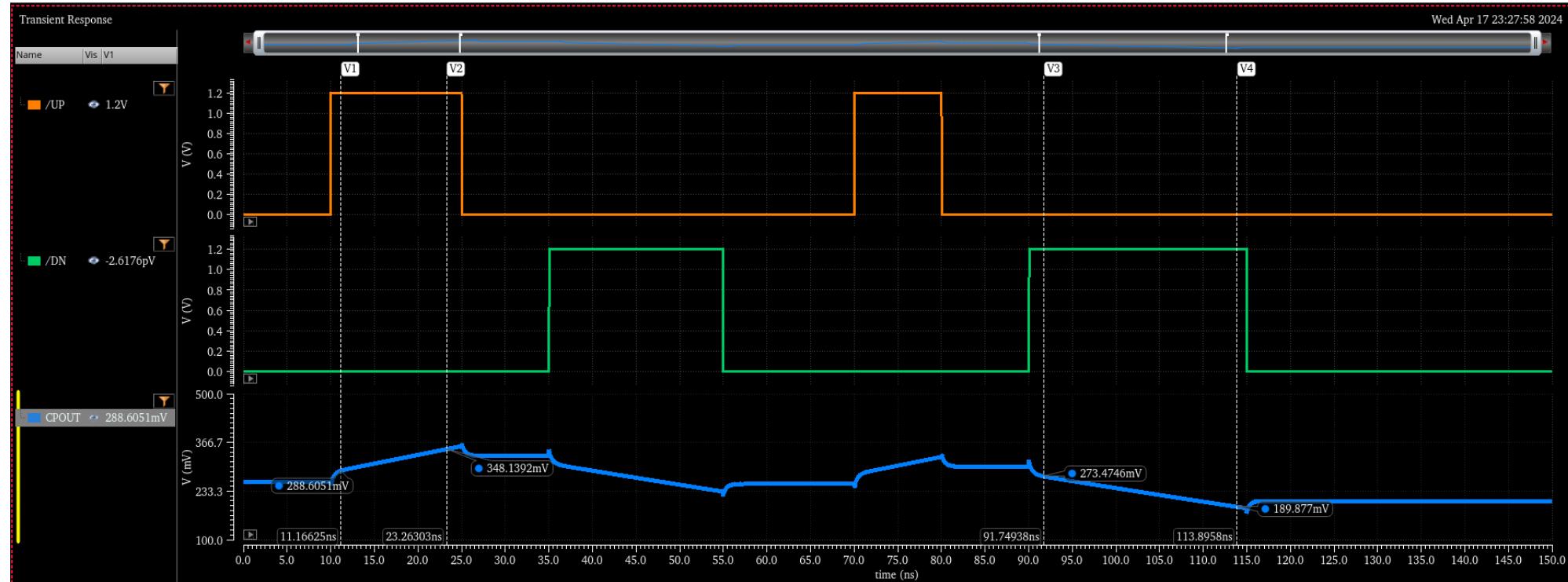


Fig. Simulation result of CP & LF

Let's design the VCO

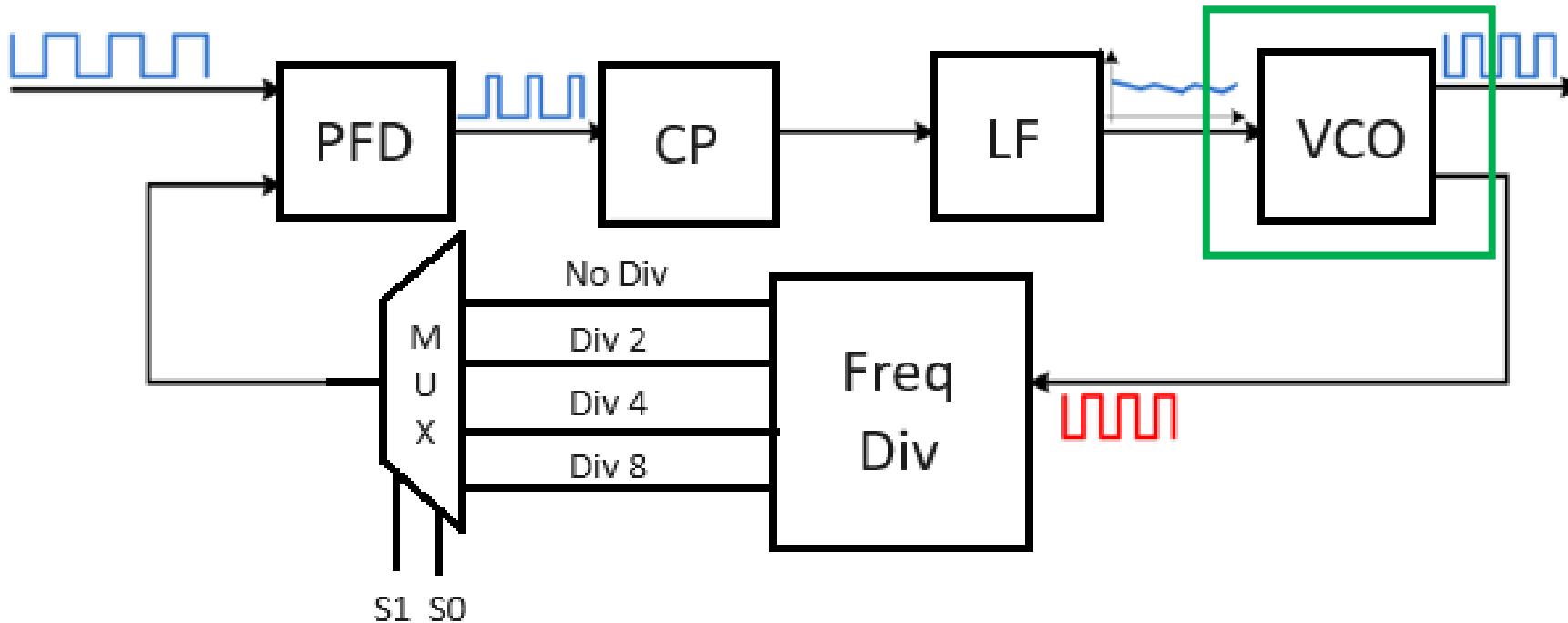


Fig. VCO design

Voltage-Controlled Oscillator (VCO)

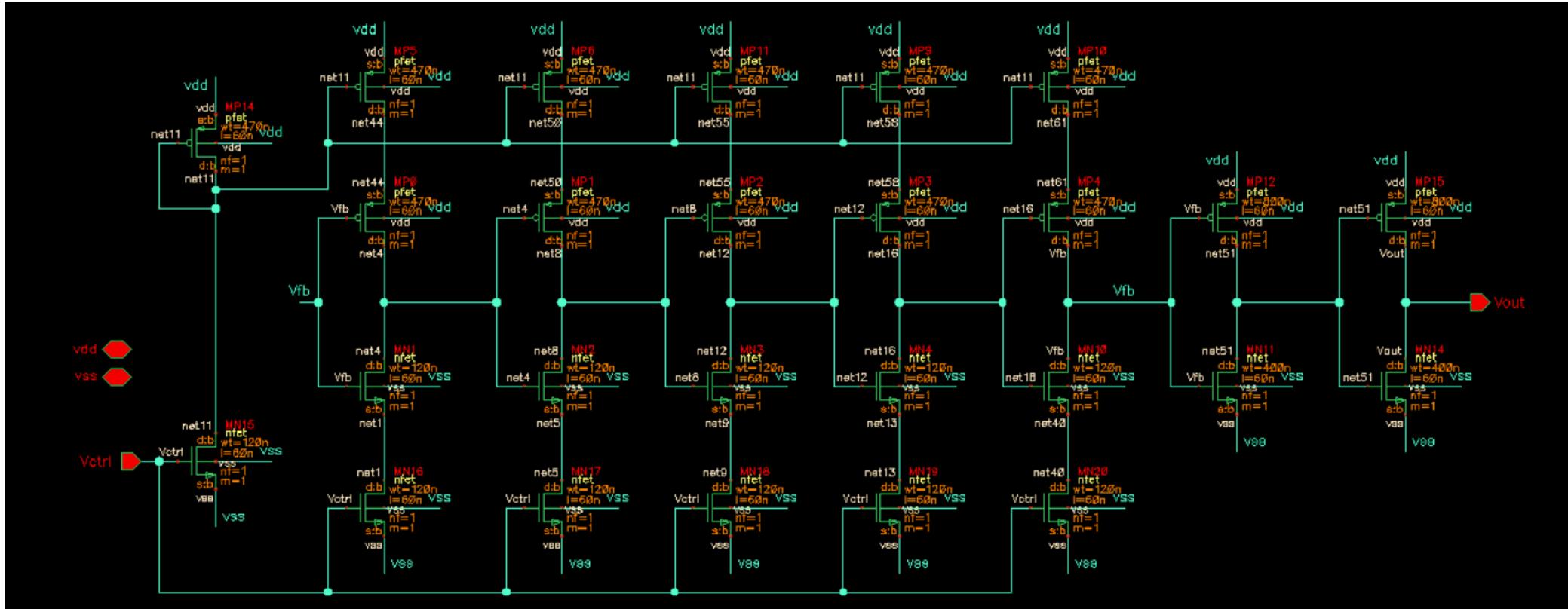


Fig. VCO schematic

Testbench – VCO

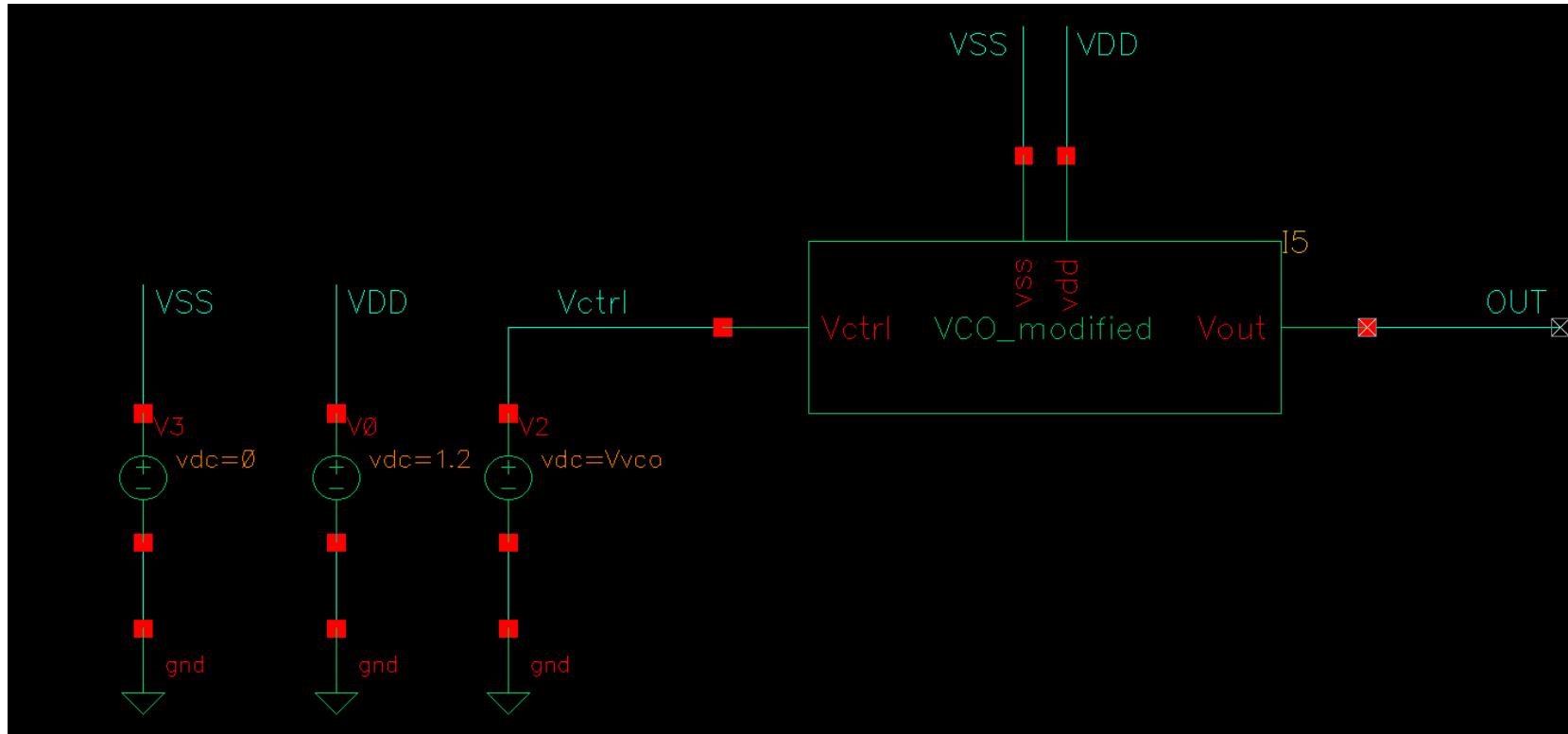


Fig. VCO testbench

Test Result – VCO

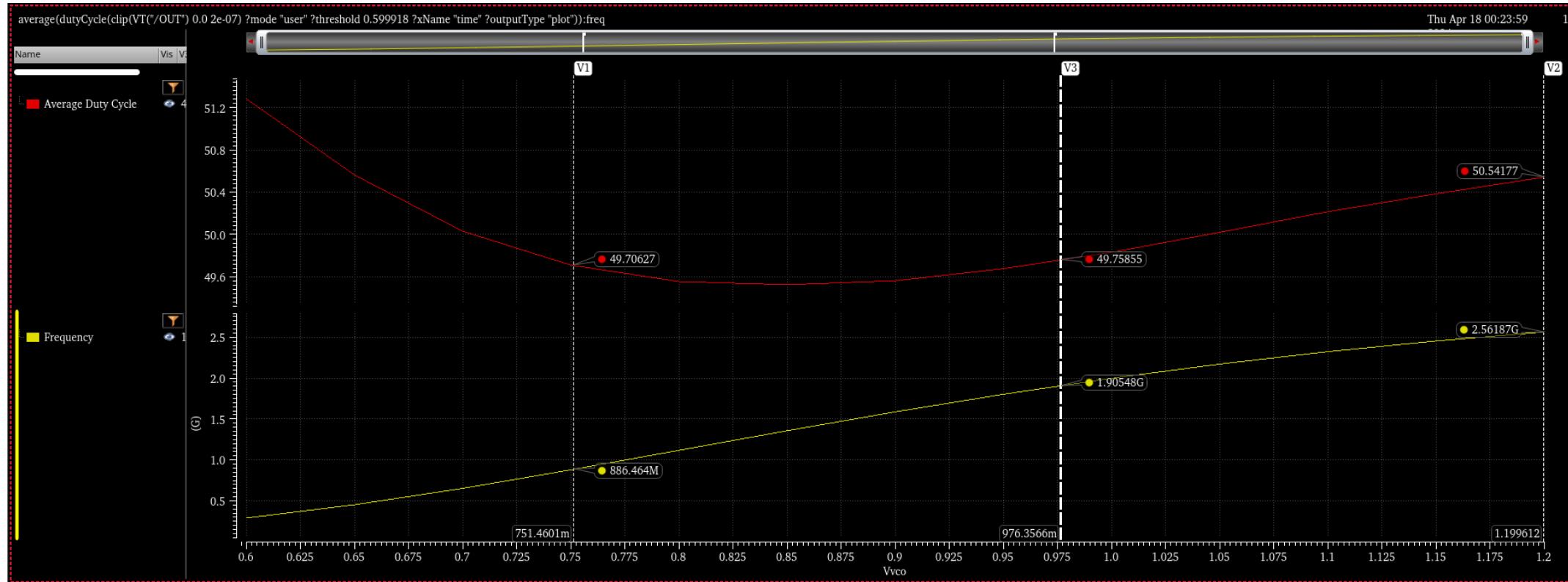


Fig. Frequency and Duty cycle vs Input voltage

Let's design the Frequency Divider with Programmable Feature

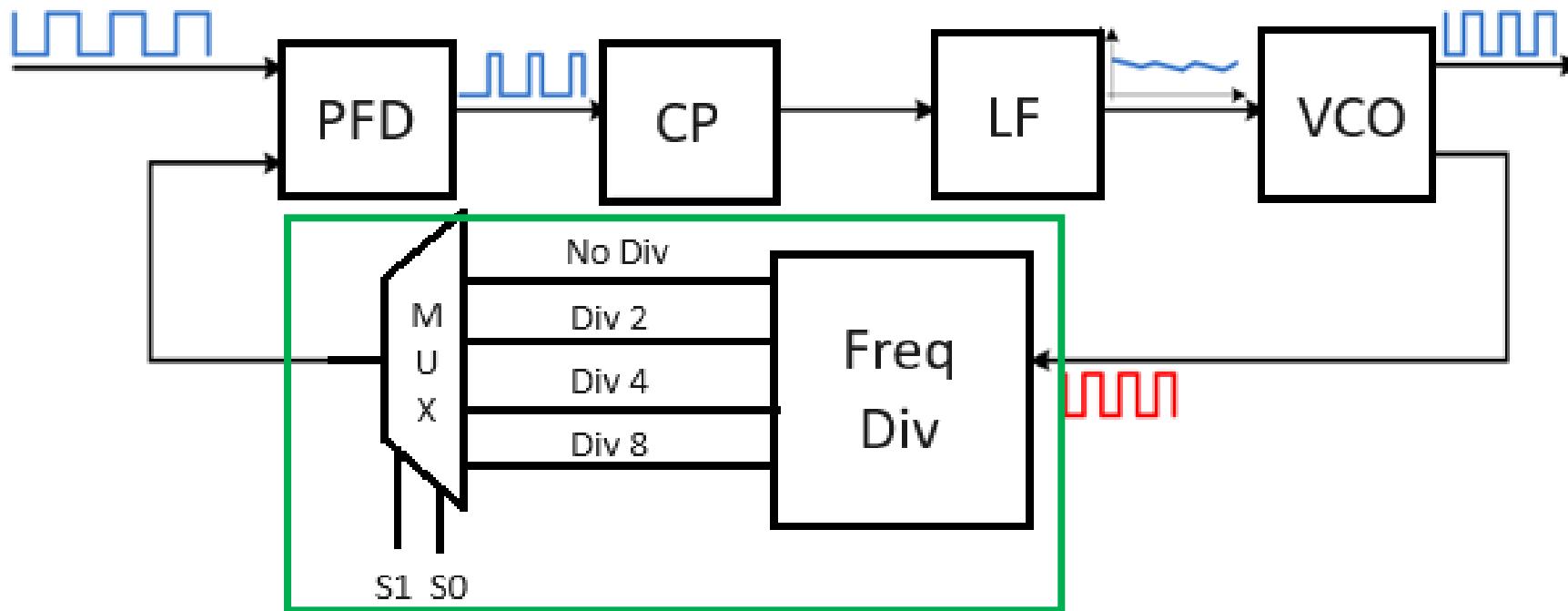


Fig. Frequency Divider with Programmable Feature

Frequency Divider

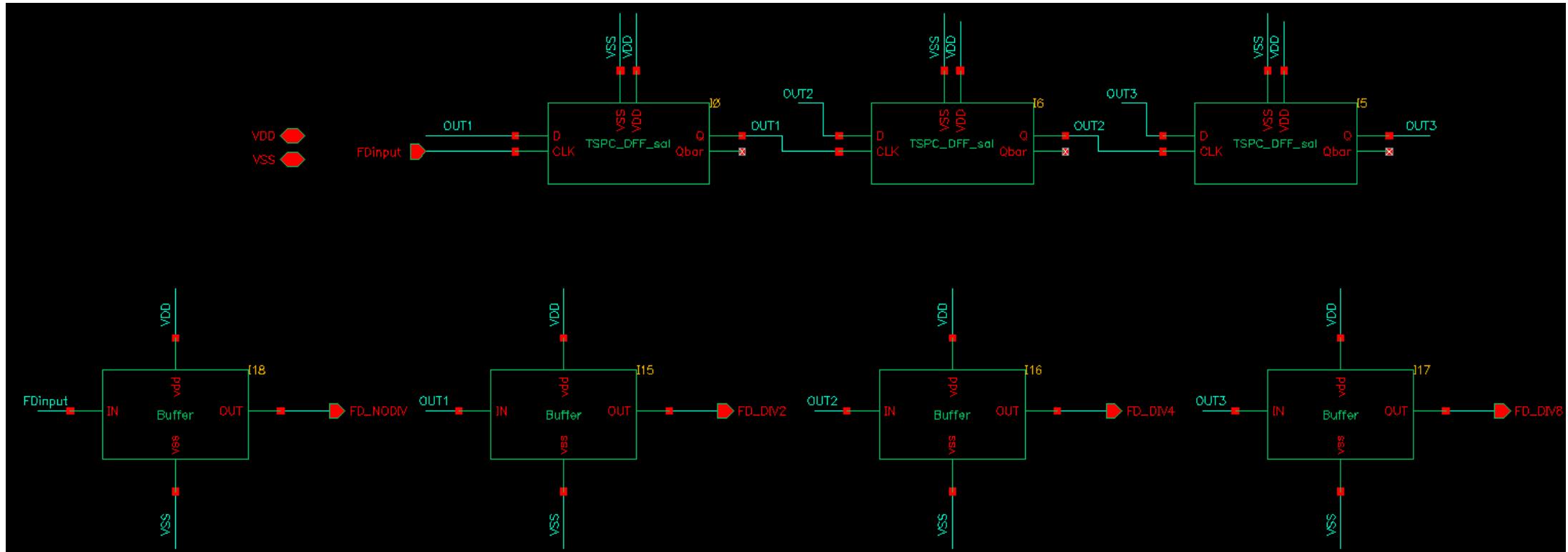


Fig. Schematic of Frequency Divider

Comparison between TSPC and Conventional DFF

Feature	TSPC DFF	Conventional DFF
Clocking	Single-phase	Two-phase or master-slave
Power Consumption	Lower dynamic, higher leakage	Higher dynamic, lower leakage
Speed	Faster	Slower
Design Complexity	Simpler (dynamic logic)	More complex (static logic)
Robustness	Less robust to noise, low-frequency issues	More robust across conditions
Area	Smaller	Larger

Since, we are designing relatively high frequency PLL, we will be using TSPC logic based DFF. Conventional DFF should also work!

Freq Divider – Cont.

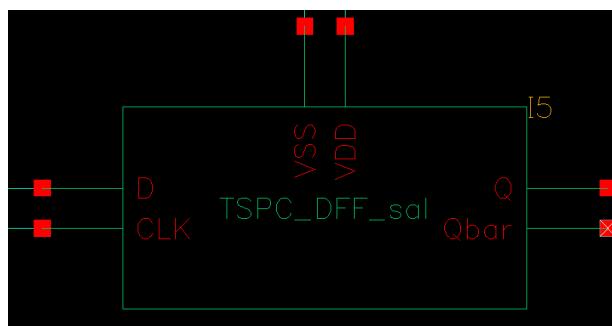


Fig. DFF symbol

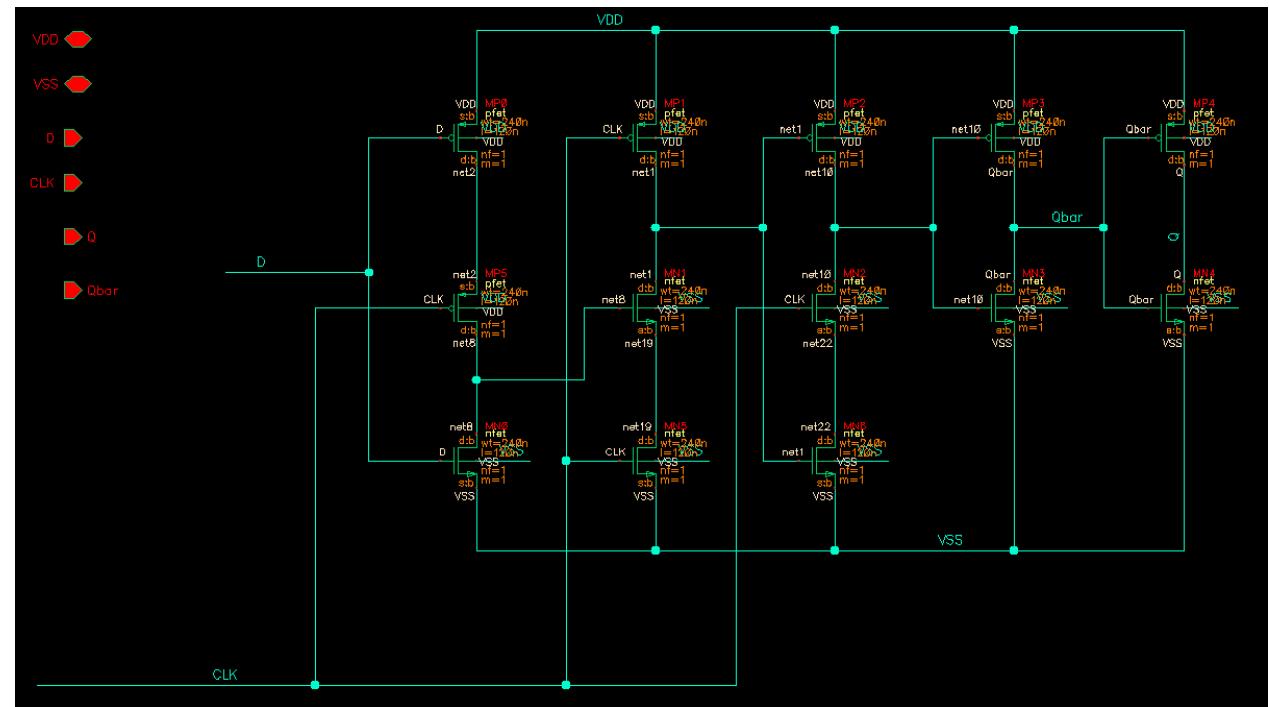


Fig. TSPC-DFF Schematic

Testbench – Freq Divider

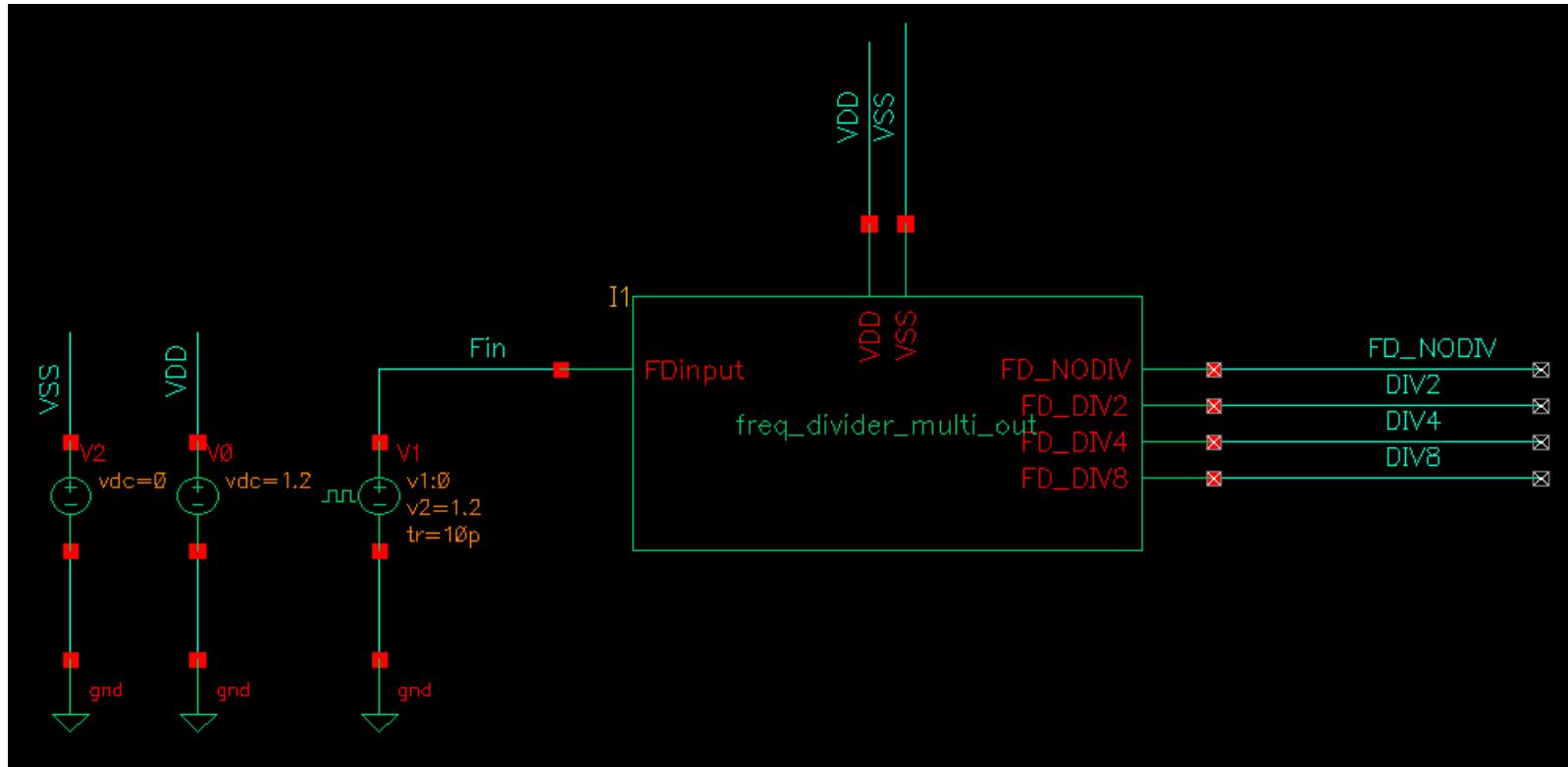


Fig. Testbench of Frequency Divider

Test Result – Freq Divider

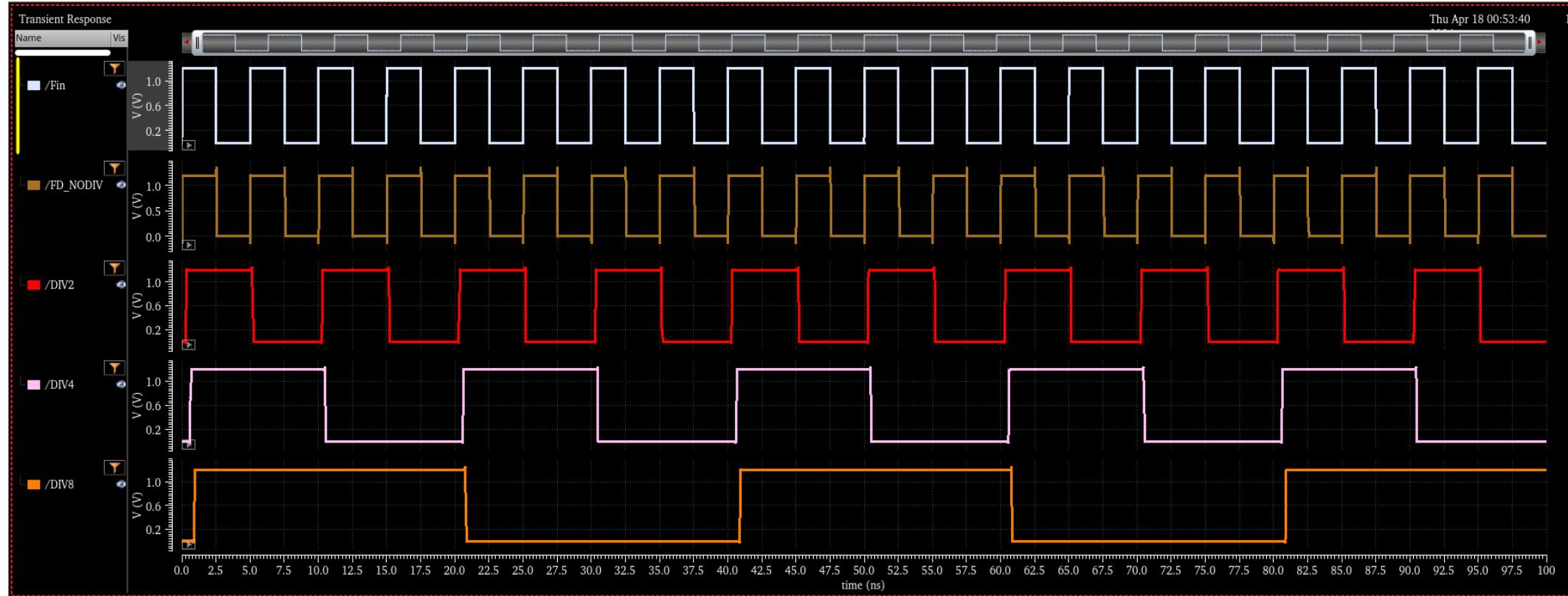


Fig. Simulation Results of Frequency Divider

4:1 Multiplexer

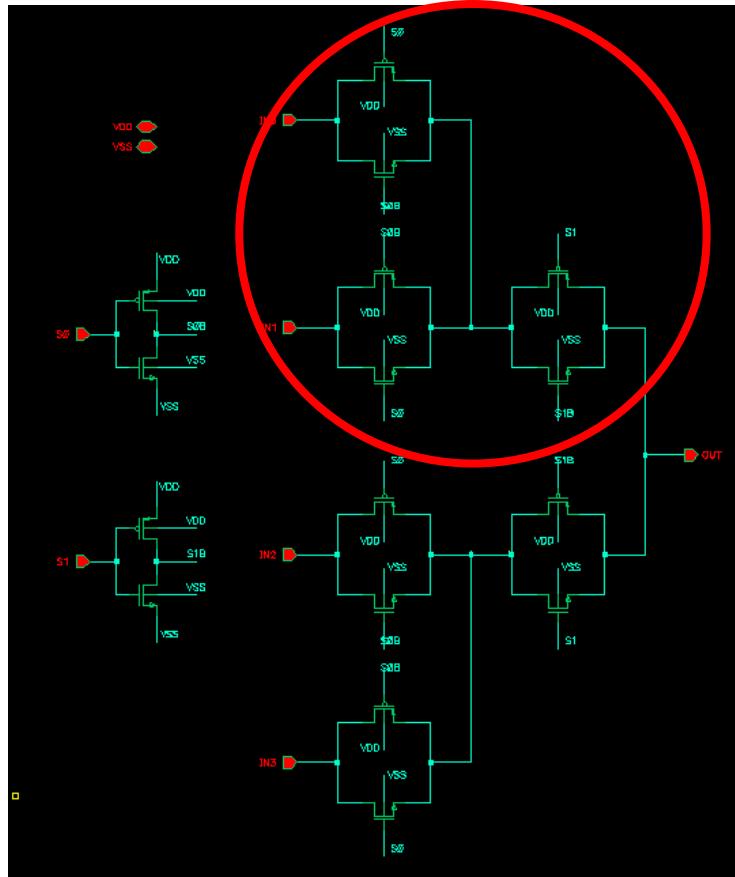


Fig. Schematic of MUX

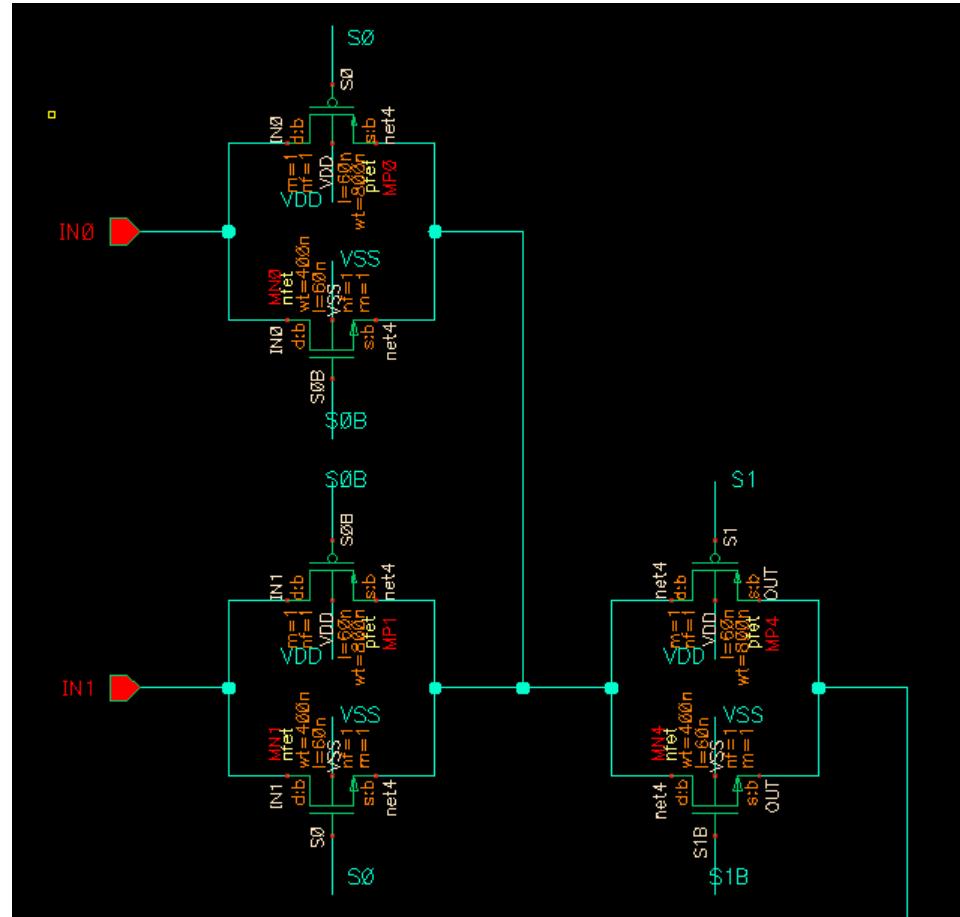


Fig. TG Based MUX

Testbench - MUX



Four vpulse
modules to generate
square waves with
different frequencies

Select bits

Fig. Testbench of MUX

Test Result – MUX

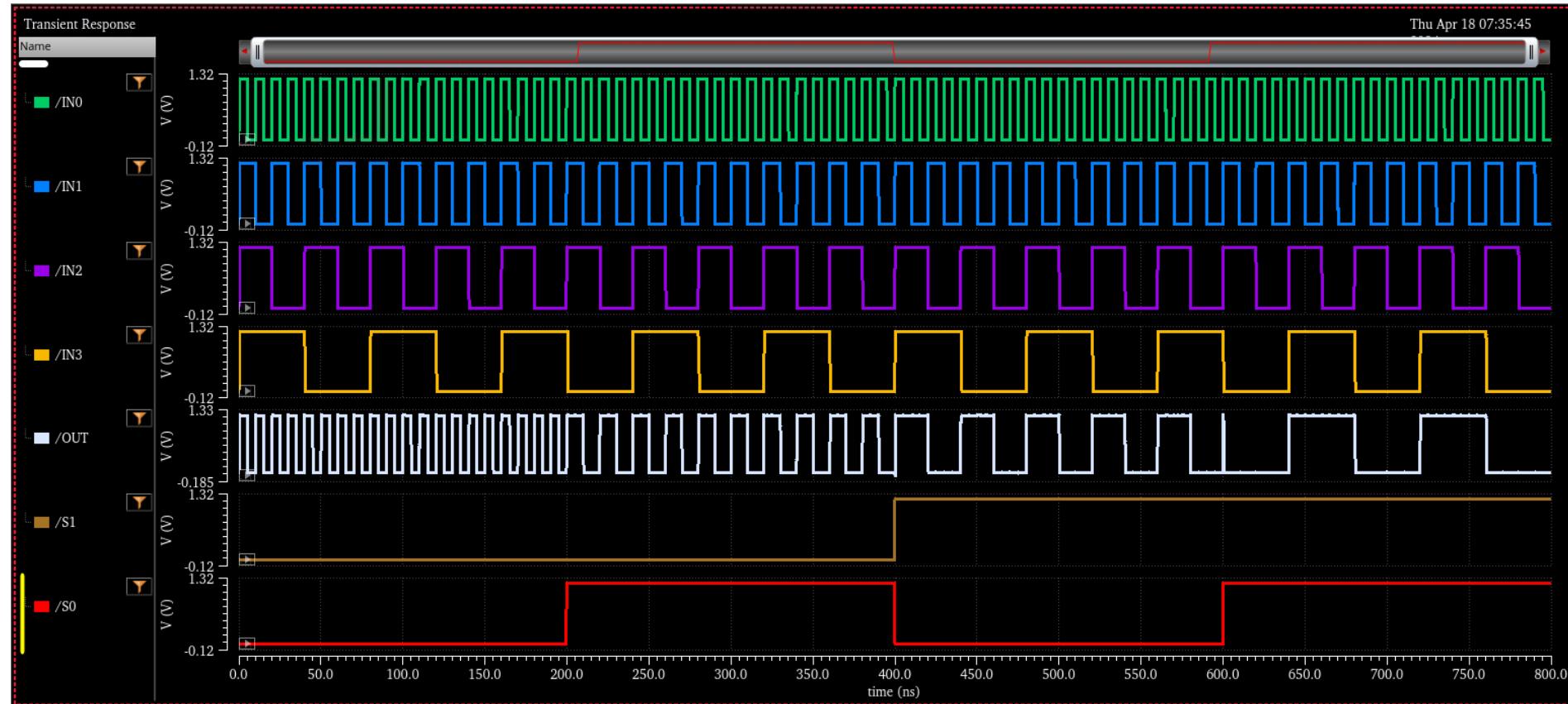


Fig. Test result of MUX

Schematic of the final PLL

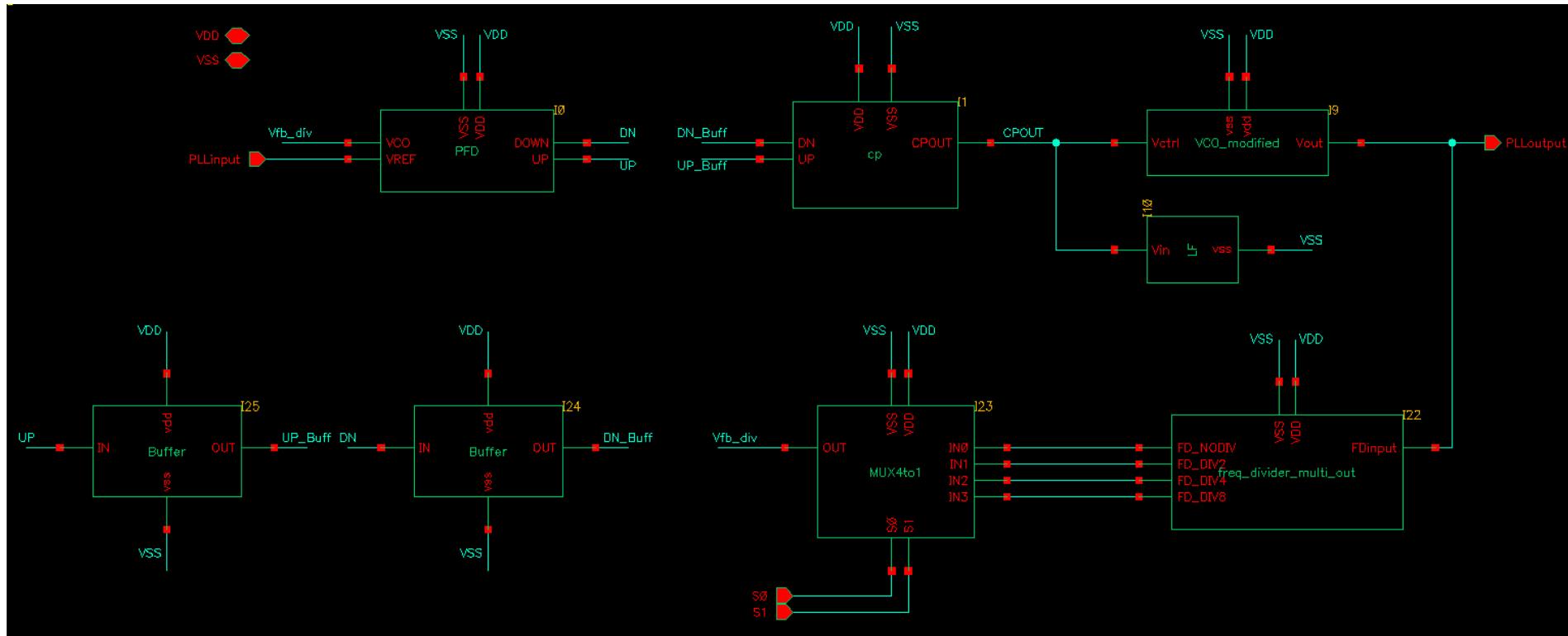


Fig. schematic

Testbench – PLL

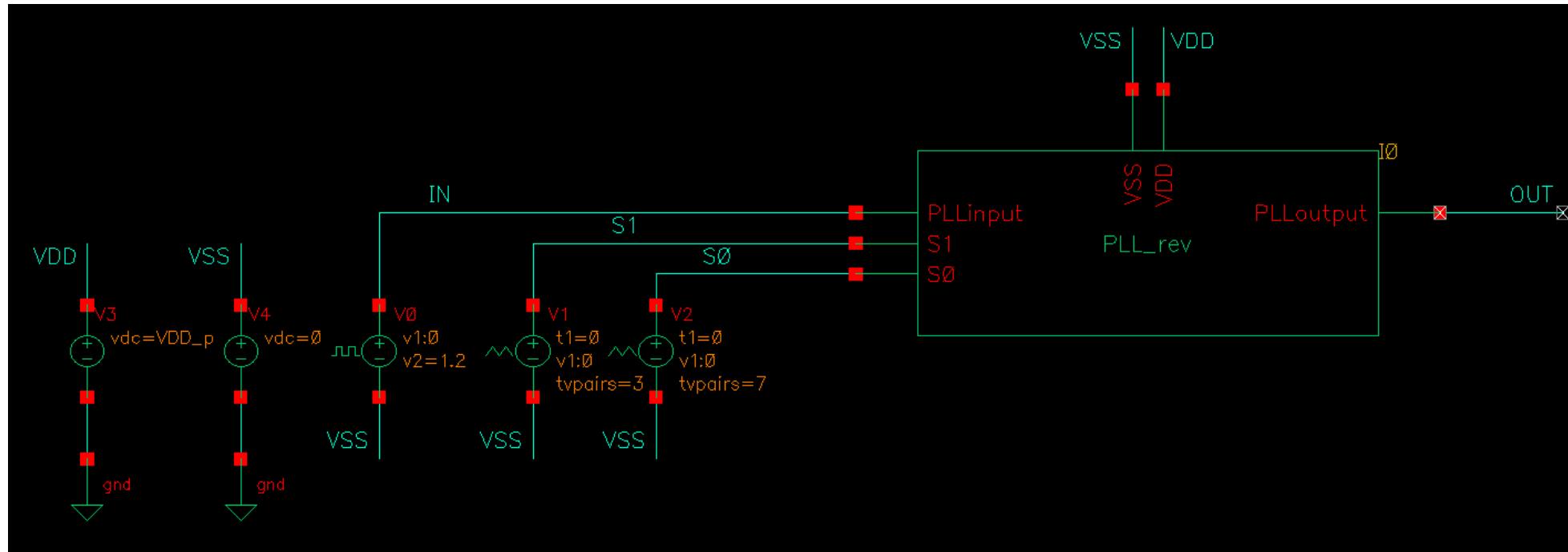
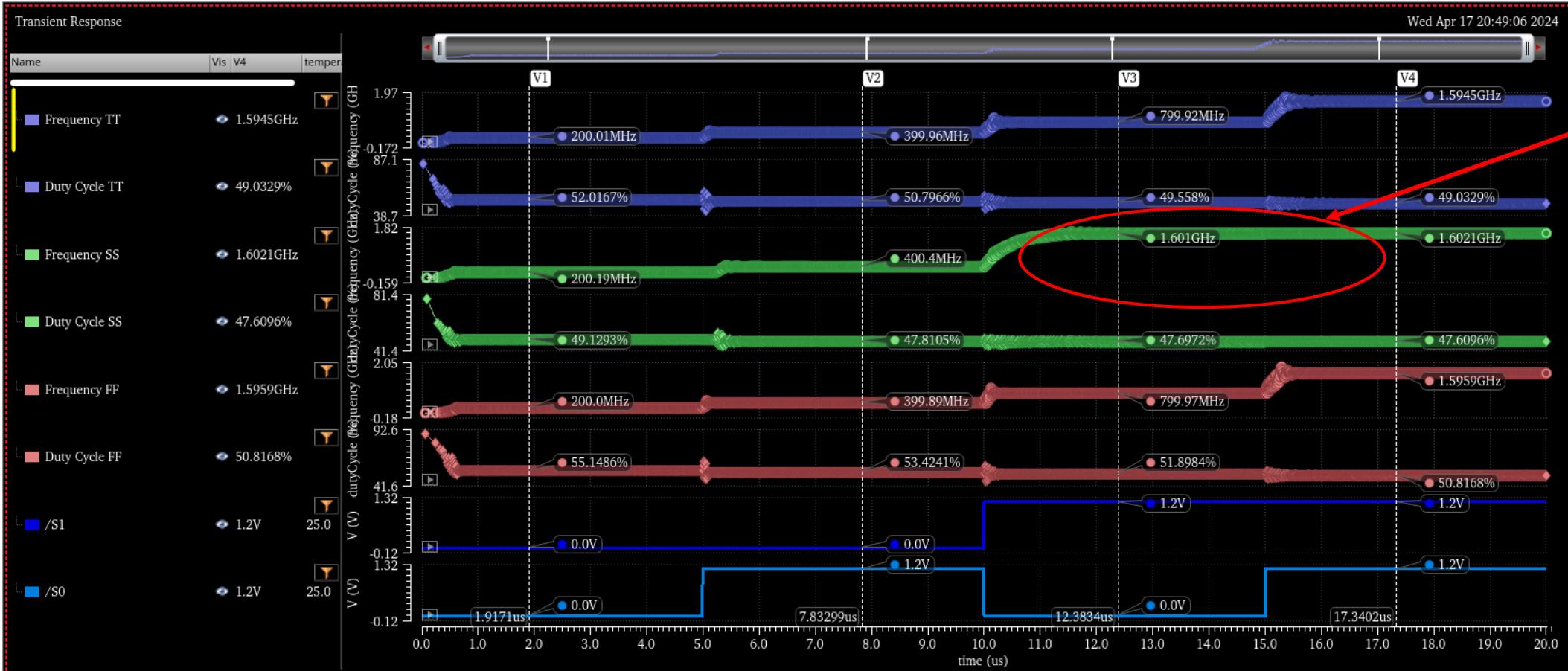


Fig. PLL testbench

Test Result – PLL



This PLL works for all three corners with 0.2 GHz, 0.4 GHz, 0.8GHz and 1.6GHz frequencies except for 0.8GHz SS corner.

Best of luck for your own
design!

Thanks

References

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