

# Programmable Phase Locked Loop Implementation using 65nm Technology Node

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**Abstract**—This paper presents the design of a fast locking PLL. It was designed using 65 nm technology. The use of a charge steering pump allows for the reduction of the lock time. The lock time is at at 520 ns, 567ns, and 760ns in FF, TT, and SS corners respectively. The total area of the PLL is 1.1 mm square. Pre and post layout simulations have been provided for the design of this PLL.

**Index Terms**—PLL, frequency divider.

## I. INTRODUCTION

A phase-locked loop (PLL) is an electronic control system that produces an output signal whose phase is in phase with the input reference signal. The basic components of a phase-locked loop include a phase-frequency detector (PFD), a charge pump (CP), a loop filter, a voltage-controlled oscillator (VCO), and a feedback loop. the PFD compares the phase of the input signal to the phase of the output of the VCO, generating a signal that represents the difference between the two phases. This error signal is processed and filtered by a charge pump to adjust the VCO to ensure that the output remains phase synchronized with the input. This dynamic process allows the PLL to lock onto the frequency of the input signal, maintaining precise frequency and phase alignment, which is critical in a variety of high-risk applications.

PLLs serve a large role in a wide range of technologies, from telecommunications that synthesize frequencies for signal transmission and reception, to digital electronics and precision control systems that improve accuracy and stability. In the next section, we have listed some of the research and explored their results, which have significantly improved the performance characteristics of PLLs, such as phase noise reduction, lock-time efficiency, and more.

The following studies have been instrumental in pushing the boundaries of PLL performance, addressing both theoretical aspects and practical implementations critical for the next generation of wireless and wireline applications. Each paper contributes unique insights and methodologies that collectively inform the current state of the art in PLL design.

[2] presents a PLL that uses a tri-state phase frequency detector (PFD) and a current steering charge pump to enhance performance in terms of phase noise and lock time. Notably, the PLL utilizes a current starved ring oscillator voltage-controlled oscillator (VCO), which significantly reduces output noise and improves stability across different process, voltage, and temperature (PVT) corners. The implementation in a 28nm CMOS process allowed for a compact layout, leading to significant area savings while maintaining performance, achieving a phase noise of -60.67 dBc/Hz at 1MHz from the carrier. This work emphasizes the role of precise control in charge pumps and PFDs to optimize PLL performance in varying conditions, crucial for applications in wireless and mobile communications where power efficiency and robustness are critical.

[3] introduces a sub-sampling PLL featuring an adaptive FLL that engages only when the system deviates from the lock state, thus not contributing to power consumption during steady-state operation. This PLL is designed for applications demanding ultra-low jitter and high power efficiency, such as advanced wireless communication systems. The configurable PFD enables rapid relocking with minimal dead zones, crucial for maintaining system stability against external disturbances. Achieving an extraordinarily low jitter of 103.58 fs rms and a figure of merit (FOM) of -257.8 dB, this design sets a high standard for low-power, high-performance frequency synthesizers.

[4] explores a PLL design that extends the loop bandwidth to mitigate the high phase noise typically associated with high-frequency VCOs. The innovation lies in using a power-gating injection-locked frequency multiplier-based phase detector which allows for a more stable frequency detection at higher bands, reducing RMS jitter to 47 fs. The PLL employs advanced noise filtering and correction techniques to handle the challenges posed by sub-THz frequencies, which are expected to be foundational for 6G technologies. This approach not only enhances performance but also contributes to the feasibility of higher-frequency PLL applications in

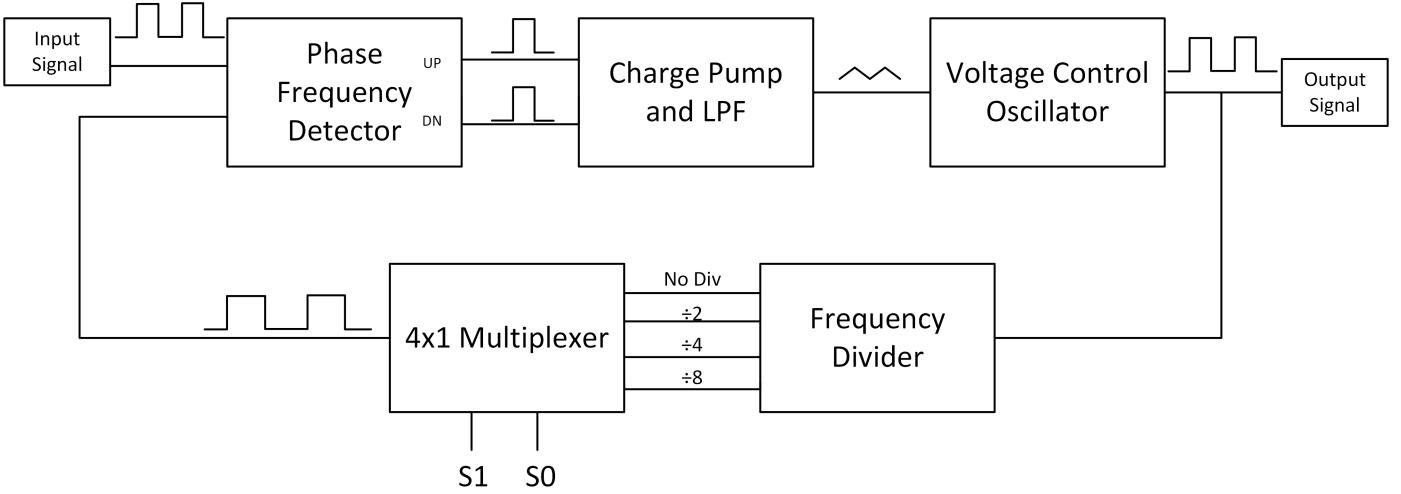


Fig. 1. Proposed Programmable Phase Locked Loop.

compact, integrated circuits.

## II. MOTIVATION AND OBJECTIVES

The motivation for Phase Locked Loop (PLL) development stems from an array of evolving factors and demands within the realm of modern digital computing technology. As the technological landscape and computing applications continually advance, the need for enhanced performance becomes increasingly apparent. This demand is paralleled by the exponential growth in power consumption and clocking frequencies required by newer technologies. Traditional crystal oscillators struggle to meet these escalating frequency and speed demands, necessitating alternative designs to bridge this gap.

A highly critical consideration arises from the necessity of operating digital circuitry at higher clock frequencies in order to accommodate modern performance standards. However, this transition brings forth a myriad of new challenges. Clock jitter, imperfect frequency generation, and instabilities in clock generation become pressing issues that must be addressed to ensure reliable performance. Without the incorporation of a system which can meet such speed demands successfully, failure of critical systems and technologies becomes imminent. Consequently, the increasingly important need for a PLL to generate high-frequency clocks in a dependable manner becomes apparent.

Considering all these constraints and growing needs, this paper proposes the design of a PLL utilizing 65 nm technology while also offering a programmable interface to handle multiple frequencies. Incorporating

this flexibility is paramount as modern computing tasks are not confined to a single frequency paradigm. Tasks demanding heightened CPU performance, such as 3D modeling, gaming, or physical simulations, may necessitate overclocking the CPU to operate at a higher clock frequency. Conversely, there are instances where operating at slower clock frequencies proves more efficient, such as during streaming, document writing, or basic communications.

Hence, it can be clearly seen that there arises a critical requirement to develop a variable frequency generator. Such a device must be capable of adapting to diverse performance needs from a single reference clock signal. This underscores the motivations behind the creation of a programmable PLL capable of supporting a spectrum of frequencies, catering to the dynamic demands of modern computing environments. By addressing these multifaceted needs, the proposed PLL design endeavors to enhance the versatility, efficiency, and overall performance of digital circuitry in contemporary technological applications.

## III. PROPOSED PROGRAMMABLE PHASE LOCKED LOOP

### A. Phase Frequency Detector

The Phase Frequency Detector (PFD) is a key component in a Phase Locked Loop (PLL) and has a significant impact on key performance metrics such as jitter, phase noise and lock time. Our PFD design, shown in Fig 3 and Fig 4, compares the order in which the rising edges of two square wave signals arrive. When the rising edge of the reference signal precedes the rising edge of the

feedback signal, it generates a pulse at the UP output. Conversely, when the rising edge of the feedback signal arrives before the rising edge of the reference signal, it generates a pulse at the DOWN output, Fig 2 illustrate the output of PFD for different inputs [3]. The width of the voltage pulse generated by the PFD is proportional to the phase difference between the reference and feedback signals.

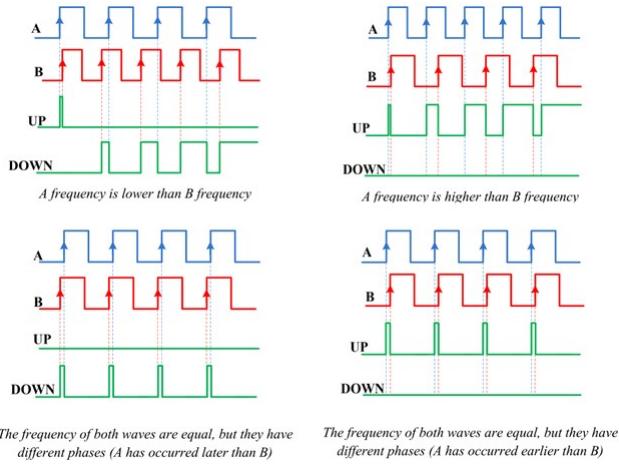


Fig. 2. Waveforms of the PFD for different input conditions [3].

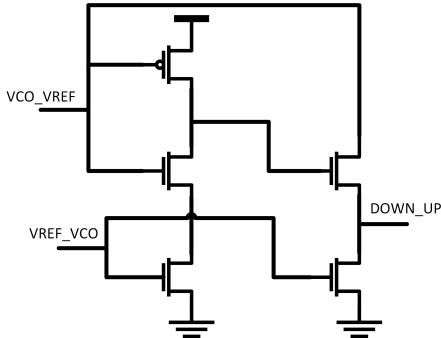


Fig. 3. The Core of Phase Frequency Detector

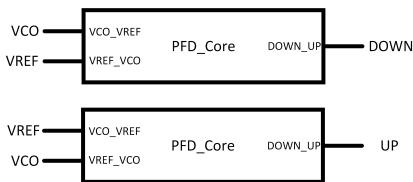


Fig. 4. Schematic of Phase Frequency Detector

### B. Charge Pump and Loop Filter

In a phase-locked loop (PLL), the charge pump is crucial for converting the digital pulses from a frequency

phase detector into a current flow. This current is used to charge or discharge a capacitor within the loop filter, thereby generating a voltage reference for the voltage-controlled oscillator (VCO). A current steering charge pump with a current reference circuit is shown in Fig 5.

The circuit is specifically designed to control the current during the charge and discharge phases of the pump. When an "Up" pulse is issued, the MP2 transistor activates, allowing current to flow through the sourcing MOSFET and MP2, charging the capacitor. Conversely, receiving a "Down" pulse turns on the MN2 transistor, directing current through MN2 and the sinking MOSFET, which discharges the capacitor. Additionally, the use of inverted pulse signals (upb and dnb) facilitates a low-resistance path for current transition from VDD to GND, enhancing the switching speed and creating a charge shunt [2].

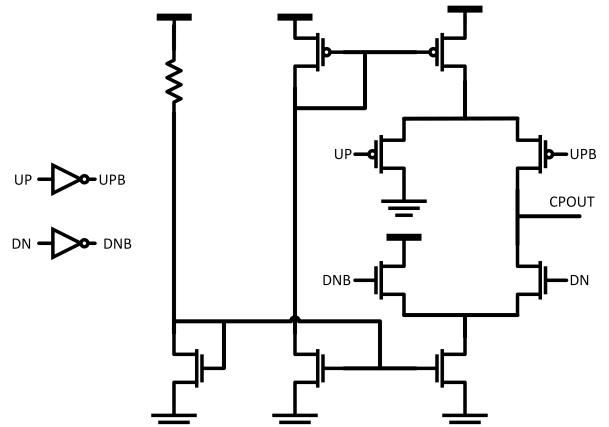


Fig. 5. Schematic of Charge Pump

### C. Voltage Control Oscillator

The voltage controlled oscillator (VCO) was developed on a ring, current-starved configuration. Referring to Figure 6, The structure makes use of five inverting stages followed by an output buffer made from two more inverting stages. The six topmost and bottommost transistors, respectively, serve as the VCO's current source and sink.

### D. Frequency Divider and Multiplexer

The frequency divider was developed from three D Flip-Flops using TSPC logic. The main advantage of using such logic is that it requires a single phase clock cycle to operate. This allows the components to be synchronized on one clock signal, improving design simplicity and efficiency. This configuration also adds an improvement from the researched papers [2] [3]. An

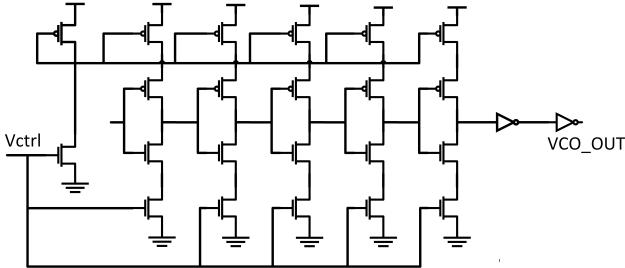


Fig. 6. Schematic of voltage controlled oscillator

buffer was inserted onto the output of each D Flip-Flop to allow for the configuration of multiple outputs of varying division factors. This allows the output frequency to be selected as either the same as the input or reduced by a factor of two, four, or eight (see Multiplexer).

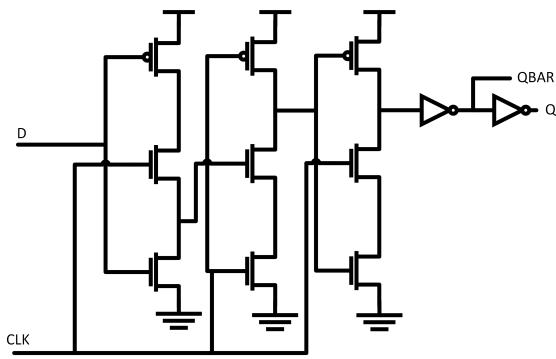


Fig. 7. Schematic of TSPC D Flip Flop

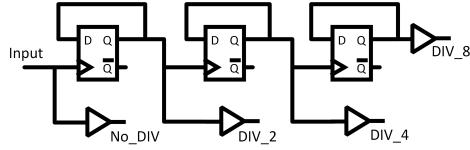


Fig. 8. Schematic of Frequency Divider

#### E. Improved VCO

By incorporating a NAND gate at the beginning of the chain, one effectively introduces a controlled asymmetry into the system. The NAND gate, unlike a simple inverter, requires two input signals, allowing one of the inputs to serve as an enabling condition. This setup ensures that the VCO has a definite starting point, as the NAND gate can be initially set in a specific logic state, effectively breaking the symmetry and providing a clear initial condition.

## IV. EXPERIMENT SETUP

In this section, we show the screenshot of the testbenches for all the subcomponent and the PLL.

#### A. Testbench for PFD

The purpose for the phase frequency divider (PFD) is to generate UP/DOWN signal depending on the timing of the reference and the VCO output signal. To test the individual block of the PFD, we have used a piecewise linear (PWL) signal to generate a varying frequency as our output to verify the functionality of the PFD module. Figure 9 shows the testbench for the PFD.

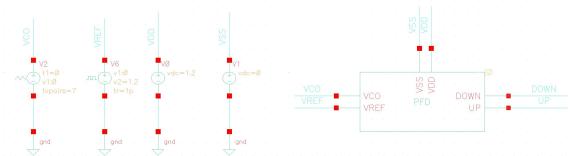


Fig. 9. Testbench setup for PFD

#### B. Testbench for Charge Pump and Loop Filter

The charge pump and the loop filter are the most critical block inside the whole PLL architecture as they are the only analog block. Depending on the Up and DOWN pulse generated from the preceding PFD block, the charge pump will inject or take away charge over time, essentially current to or from the capacitor inside the loop filter. Therefore, while creating a testbench for the charge pump and loop filter, we have used the pulse signals for both UP and DOWN pulses. Figure 10 illustrates the testbench setup for the CP and LF.

#### C. Testbench for VCO

Figure 11 shows the testbench for the VCO. We have created the testbench in such a way that we can mimic any value that may appear across the loop filter. For materialize that, we have swept the input voltage of the VCO from 0.6 to VDD (1.2 V) voltage.

#### D. Testbench for Frequency Divider and Multiplexer

Figure 12 and Figure 13 shows the testbench for Frequency Divider and Multiplexer. They are set are in such a way so that we can mimic their functionality when they will be used in the PLL top block.

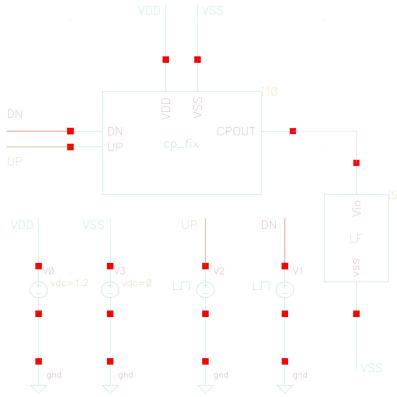


Fig. 10. Testbench setup for CP and LF

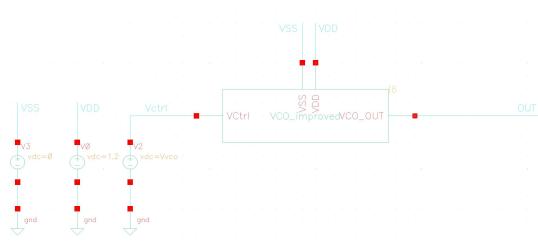


Fig. 11. Testbench setup the VCO

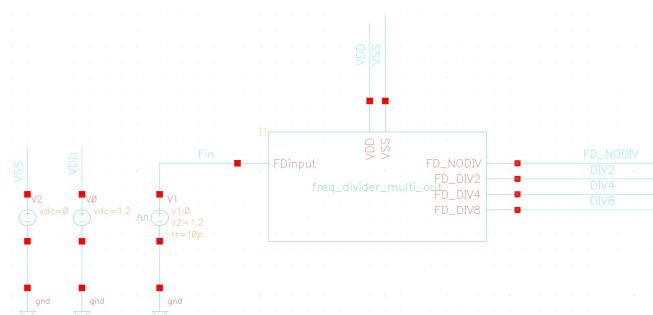


Fig. 12. Testbench setup for Frequency Divider

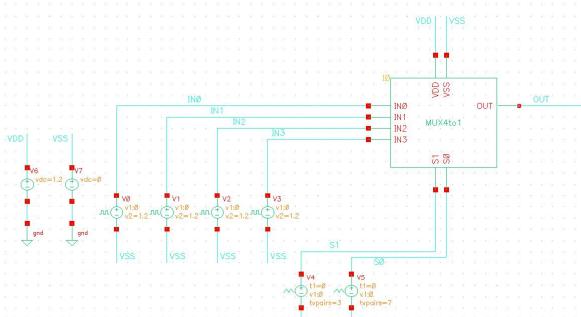


Fig. 13. Testbench setup for 4:1 Multiplexer

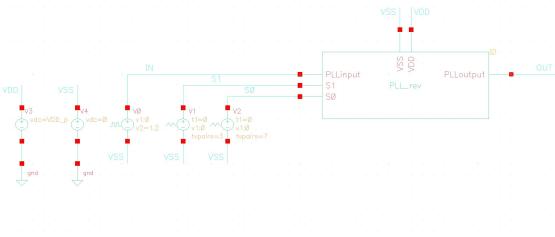


Fig. 14. Testbench setup for PLL

### E. Testbench for PLL

### F. PVT Corner

In chip design, PVT (Process, Voltage, Temperature) corners represent the extremes of these three key variables under which a semiconductor device must operate. Understanding and analyzing these corners is crucial for ensuring the reliability and performance of integrated circuits (ICs) across all possible conditions. The table below shows the Three PVT Corners we simulated.

TABLE I  
LIST OF SIMULATION CORNER

Corner	Temperature (C)	Voltage (V)
SS	-40	1.08
TT	25	1.2
FF	125	1.32

## V. SIMULATION RESULT

We have simulated the PLL by first doing simulation for each of the subblock. At first, we did pre layout simulation and then created a layout using Virtuoso. After completing the layout, we have done pex and then generated the post layout simulation. We have used only the post layout simulation screenshots for the digital blocks.

### A. PFD

The simulation result shows that when the rising edge of the reference signal is presented before the feedback signal, it generates a UP pulse. When the rising edge of the feedback signal arrives before the reference signal, it generates a pulse DOWN pulse.

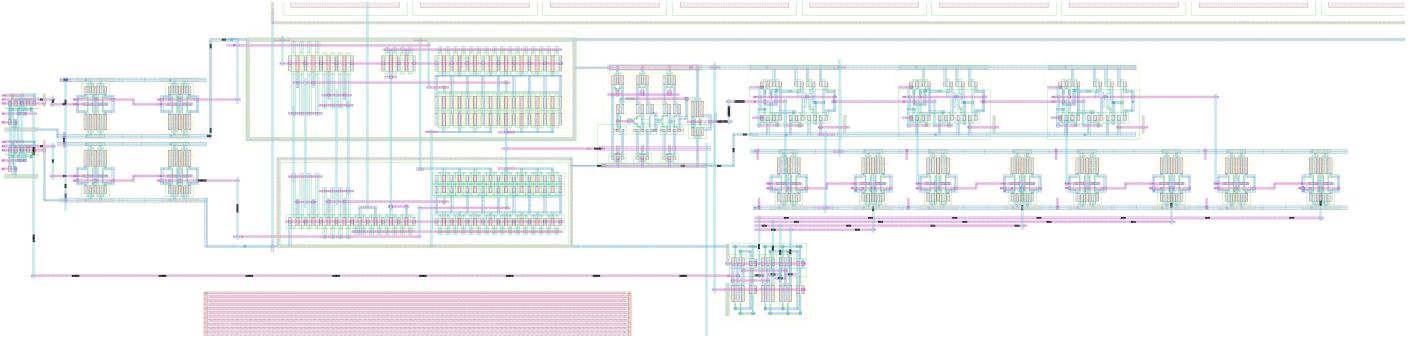


Fig. 15. Layout of PLL without Capacitors and Resistors

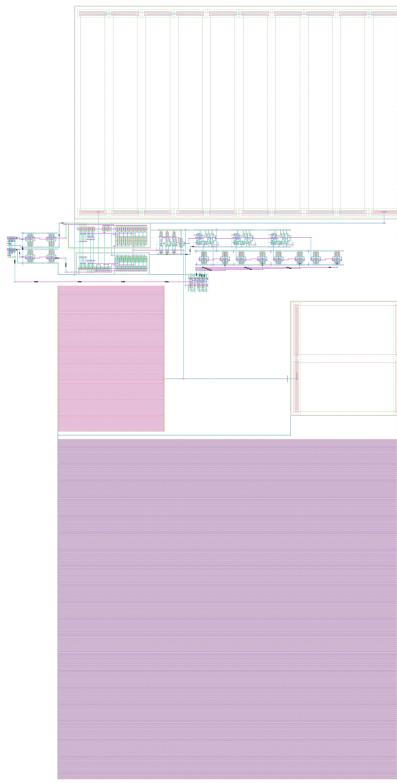


Fig. 16. Full layout of PLL

### B. CP and LF

The simulation result shown in Figure 18 and Figure 19 has proved that the charge pump is working normally along with the Loop Filter, when a UP pulse is presented, the output voltage increase and when a DOWN pulse is presented, the output voltage decrease.

### C. VCO

The simulation result for VCO is shown in Figure 20. The frequency for the VCO can go up to 1.5GHz.

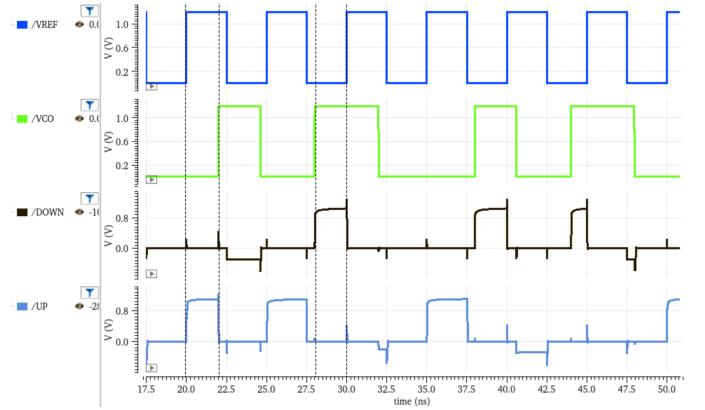


Fig. 17. Post-layout Simulation for PFD

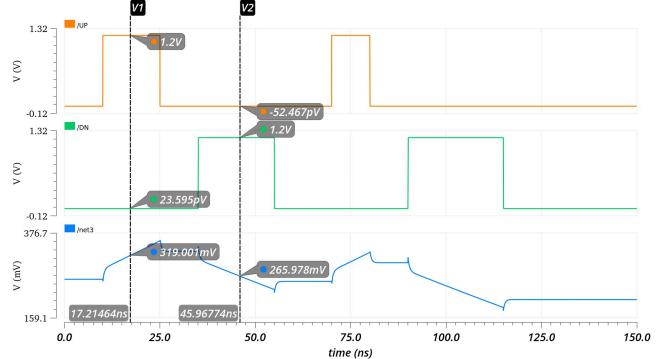


Fig. 18. Pre-layout Simulation for CP and LF

### D. Frequency Divider and MUX

The post-layout simulation for Frequency Divider is shown in Figure 21. The frequency divider took a reference signal and divided by 1, 2, 4, 8 respectively. As for Multiplexer, the S1 and S0 control bit control the signal the can pass through. The result is shown in Figure 22.

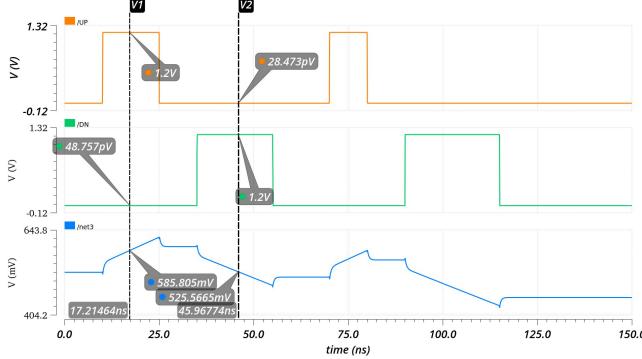


Fig. 19. Post-layout Simulation for CP and LF

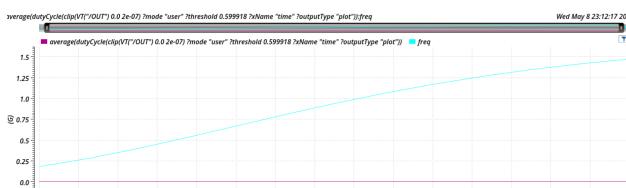


Fig. 20. Post-layout Simulation for VCO

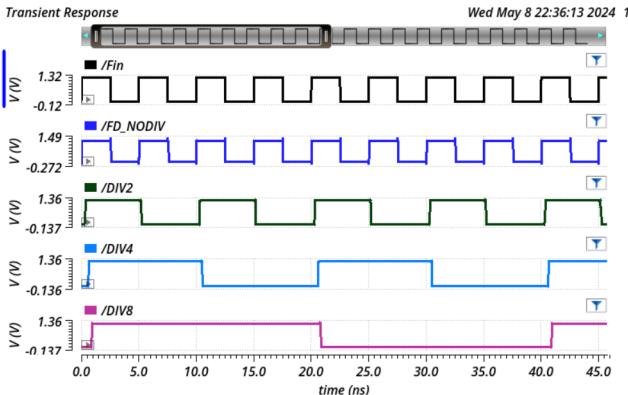


Fig. 21. Post-layout Simulation for Frequency Divider

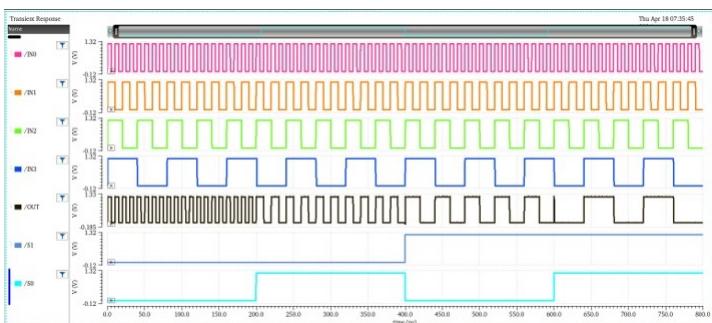


Fig. 22. Post-layout Simulation for Multiplexer

## E. PLL

The Pre-layout simulation for the PLL is shown in Figure 23, the frequency locked for both FF and TT corner. However, for SS corner, the frequency will not lock when S1 S0 is set to 10.

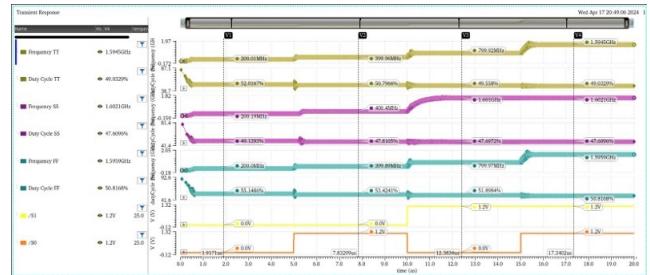


Fig. 23. Pre-layout Simulation for PLL

## VI. CONCLUSION

In conclusion, this paper has introduced the design of a fast locking Phase Locked Loop (PLL) implemented using 65 nm technology. By incorporating a charge steering pump, the PLL achieves a notable reduction in lock time, with measured values of 520 ns, 567 ns, and 760 ns in FF, TT, and SS corners respectively. Despite its rapid locking capability, the PLL maintains a compact footprint, occupying a total area of 1.1 mm square. Furthermore, the design's efficacy has been verified through comprehensive pre and post-layout simulations. Overall, the presented PLL design offers a compelling solution for applications requiring swift lock times and efficient utilization of silicon real estate in contemporary integrated circuit designs.

## REFERENCES

- [1] W. Bae, "State-of-the-Art Circuit Techniques for Low-Jitter Phase-Locked Loops: Advanced Performance Benchmark FOM Based on an Extensive Survey," 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea, 2021, pp. 1-5, doi: 10.1109/ISCAS51556.2021.9401059.
- [2] S. M. M. Ahsan, T. Hassan, S. I. Hasan, N. Afroz and S. A. Raisa, "Design and Performance Analysis of A Low Power, Low Noise 1.6GHz Charge Pump Integer-N PLL in Different PVT Corners," 2020 11th International Conference on Electrical and Computer Engineering (ICECE), Dhaka, Bangladesh, 2020, pp. 190-193, doi: 10.1109/ICECE51571.2020.9393111.
- [3] A. Abolhasani, M. Mousazadeh, and A. Khoei, "A high-speed, power efficient, dead-zone-less phase frequency detector with differential structure," Microelectronics Journal, vol. 97, p. 104719, Mar. 2020, doi: 10.1016/j.mejo.2020.104719.
- [4] S. Ji et al., "A 2.4-GHz Sub-Sampling PLL With an Adaptive and No Power Contribution FLL Achieving 103.58 fs rms Jitter and -257.8 dB FOM," in IEEE Microwave and Wireless Components Letters, vol. 32, no. 5, pp. 403-405, May 2022, doi: 10.1109/LMWC.2022.3149274.

- [5] W. Bae, "State-of-the-Art Circuit Techniques for Low-Jitter Phase-Locked Loops: Advanced Performance Benchmark FOM Based on an Extensive Survey," 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea, 2021, pp. 1-5, doi: 10.1109/ISCAS51556.2021.9401059.
- [6] Y. Liang et al., "A Low-Jitter and Low-Reference-Spur 320 GHz Signal Source With an 80 GHz Integer-N Phase-Locked Loop Using a Quadrature XOR Technique," in IEEE Transactions on Microwave Theory and Techniques, vol. 70, no. 5, pp. 2642-2657, May 2022, doi: 10.1109/TMTT.2022.3156901.
- [7] J. Bang, S. Jung, J. Kim, S. Park and J. Choi, "A Sub-50-fs RMS Jitter, 103.5-GHz Fundamental-Sampling PLL With an Extended Loop Bandwidth," in IEEE Solid-State Circuits Letters, vol. 6, pp. 201-204, 2023, doi: 10.1109/LSSC.2023.3296083.
- [8] Z. Jin and T. Yi, "High Performance Injection-Locked PLL Architectures: An Overview," 2022 7th International Conference on Integrated Circuits and Microsystems (ICICM), Xi'an, China, 2022, pp. 386-389, doi: 10.1109/ICICM56102.2022.10011234.
- [9] S. Ji et al., "A 2.4-GHz Sub-Sampling PLL With an Adaptive and No Power Contribution FLL Achieving 103.58 fs rms Jitter and 257.8 dB FOM," in IEEE Microwave and Wireless Components Letters, vol. 32, no. 5, pp. 403-405, May 2022, doi: 10.1109/LMWC.2022.3149274.
- [10] T. -S. Yang, H. -Y. Hsieh and L. -H. Lu, "A 2.4-GHz Ring-VCO-Based Sub-Sampling PLL With a 70-dBc Reference Spur by Adopting a Capacitor-Multiplier-Based Sub-Sampling DLL," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 9, pp. 3545-3556, Sept. 2023, doi: 10.1109/TCSI.2023.3284294.
- [11] Y. Song, H. -G. Ko, C. Kim and D. -K. Jeong, "A 1.05-to-3.2 GHz All-Digital PLL for DDR5 Registering Clock Driver With a Self-Biased Supply-Noise-Compensating Ring DCO," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 3, pp. 759-763, March 2022, doi: 10.1109/TCII.2021.3123610.
- [12] S. M. M. Ahsan, T. Hassan, S. I. Hasan, N. Afroz and S. A. Raisa, "Design and Performance Analysis of A Low Power, Low Noise 1.6GHz Charge Pump Integer-N PLL in Different PVT Corners," 2020 11th International Conference on Electrical and Computer Engineering (ICECE), Dhaka, Bangladesh, 2020, pp. 190-193, doi: 10.1109/ICECE51571.2020.9393111.
- [13] A. Abolhasani, M. Mousazadeh, and A. Khoei, "A high-speed, power efficient, dead-zone-less phase frequency detector with differential structure," Microelectronics Journal, vol. 97, p. 104719, Mar. 2020, doi: 10.1016/j.mejo.2020.104719.
- [14] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, Fourth edition. 2019.
- [15] Haruksa Kondoh, Hiromi Notani, T. Yoshiura, Yoshio Matsuda, A1.5-V 250-MHz to 3.3-V 622Mhz CMOS phase locked loop with precharge type CMOS phase detector, IEICE Trans. Electron. E78-C (4) (1999) 381–388.
- [16] KK Abdul Majeed, Binsu J. Kailath, A novel phase frequency detector for a high frequency PLL design, Procedia Eng. 64 (2013) 377–384.
- [17] W. Zhu et al., "A 5.8-GHz Wideband TSPC Divide-by-16/17 Dual Modulus Prescaler," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 1, pp. 194-197, Jan. 2015, doi: 10.1109/TVLSI.2014.2300871.
- [18] Dwivedi, Amit Krishna, et al. "Versatile Noise Suppressed Variable Pulse Voltage Controlled Oscillator." Power 10 (2015): 8.