Shirazush Salekin Chowdhury

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Summary

- Hands-on experience in full-flow Digital, Analog, and Mixed-Signal IC layout design and verification (block to top-level), including GDSII generation and physical verification (LVS, DRC, EM, IR) using industry-standard EDA tools.
- Practical experience with semiconductor process technologies and foundry nodes: GlobalFoundries (GF12LP, GF22FDX, GF28nm, GF55nm, GF130BCD) and TSMC (28nm, 180BCD).
- Experienced in high-performance neuromorphic and mixed-signal circuit design for AI/ML hardware acceleration, emphasizing low-power and high-speed architectures.

Research Area

Analog Mixed-Signal Integrated Circuits, Neuromorphic Computing, AI Hardware Accelerator, and In-Memory Computing.

Education

Doctor of Philosophy, Electrical Engineering, Virginia Tech, USA, CGPA: 4.00/4.00 **Aug 2023 — May 2027**

Coursework: Advanced VLSI Circuit Design, RFIC Design, Advanced Analog Integrated Circuits, Advanced Machine Learning.

Master of Science, Electrical and Electronic Engineering, AIUB, Bangladesh, CGPA: 4.00/4.00 **Jun 2019 — Apr 2021**

Coursework: Semiconductor Materials and Hetero-structures, Quantum Phenomena in Nanostructures, Power Electronics.

Bachelor of Science, Electrical and Electronic Engineering, AIUB, Bangladesh, CGPA: 4.00/4.00 **Jan 2016 — May 2019**

Coursework: VLSI Circuit Design, Digital Design I and II, Analog and Digital Circuit Designs, Signals and System, Control Systems.

Internship Experience

Analog Design Intern at MACOM Technology Solutions **May 2025 — Aug 2025**
High Performance Connectivity Team **Shrewsbury, NJ**

- **100 Gb/s PAM4 Transimpedance Amplifier (TIA)**: Achieved BER of 10^{-5} at sensitivity (-12 dBm) and 10^{-12} at overload (7 dBm).
- **Low-Noise Transimpedance Amplifier (LiDAR)**: Reduced input-referred flicker noise by ∼43% to improve TIA sensitivity.

Industrial Experience

Senior Engineer **Aug 2019 — Jul 2023**

Globalfoundries Design-Technology Co-Optimization (ODC)
Circuit & System Design Department, Ulkasemi Pvt. Ltd. **Dhaka, Bangladesh**

- Analog Circuit Design and Layout.
- Custom Mixed-Signal IC Layout Design.
- Standard Cell Library Development.
- Hardware and Programming: Python, MATLAB, Bash, SKILL, Verilog, Verilog-A, and Verilog-AMS.
- Experienced in industry-standard tools such as Cadence Virtuoso, Spectre, Pegasus, Xcelium, Genus, Innovus, Voltus, and Liberate; Synopsys StarRC, HSPICE, ICC, ICC2; and Mentor Calibre.

Projects

- **Eye Tracking System**: High Speed Analog Front End (AFE) of MEMS indirect Time-of-Flight (iTOF) and Self Mixing Interferometry (SMI) based Eye Tracking. The system-level implementation measures the distance between the eye and the object by calculating the phase difference between the incident and reflected rays. Key blocks: TIA, DCDC Boost Converters, Mixers, ADC, and Neural engine.
  - **High Speed Transimpedance Amplifier (TIA):** Designed a DC–7 GHz inductorless TIA (114 dBΩ; input current 10 nA–1.2 µA) using dual-feedback loops and back-body biasing; integrated CTLE and LA for low-peaking, wideband signal processing.
  - **Ultra Low Power TIA:** Developing an ultra-low-power TIA (<500 µW) with automatic gain and offset control.
- **Random Number Generator:** Designed a parameterized 32-bit RNG in SystemVerilog using hybrid Fibonacci/Galois LFSRs, achieving a maximum repeat period of ∼133 billion iterations at 50 MHz, with full RTL-to-GDSII implementation and verification.
- **Image Classification AI Chip using Delay Feedback Reservoir Computing (DFR) in GF22FDX Technology:** Developed a DFR chip capable of character recognition in 2.03 µs with a power consumption of only 7.5 mW RMS. Achieved classification accuracies of 98.52% on the EMNIST dataset and 99.83% on the MNIST dataset. This chip has been taped out in GF 22FDX SOI technology.
- **Delta-Sigma Modulator in 55nm Technology [Github]:** The Delta Sigma Modulator, operates at 1.2V, supports 10KHz to 50KHz, uses 600mV reference voltage, 5-10MHz clock speed, 10µA reference current, and has 1-bit resolution.
- **Phase-Locked Loop (PLL) in 22nm and 65nm Technologies [Github]:** Designed a low-power PLL (200 MHz to 1.6 GHz, 1.2V) with 507-873 ns settling time and 110.5-215.3 µW power across PVT variations.
- **Bandgap Reference in 22nm Technology [Github]:** The Bandgap Reference operates at 1.8V, provides 1.06V output, with ±34.3 ppm/°C temp. coefficient, consumes 365.6 µW, and functions from -40°C to 125°C.
- **10-bit Successive-Approximation (SAR) ADC:** Developed and optimized a 10-bit SAR ADC with a 100 MS/s sampling rate, achieving 8.72 ENOB and 53.51 dB SINAD, with detailed noise analysis and mitigation across jitter, comparator, and clock phase noise sources.

Recent Tape-out Experience

- High speed AFE of MEMS iTOF and SMI based eye tracking using GF22FDX technology [**Taped out on March 2025**].
- Image Classification AI Chip based on Delay Feedback Reservoir Computing (DFR) using GF22FDX technology. This work includes mixed-signal circuit design and custom top-level chip layout from scratch [**Taped out on May 2024**].

Selected Publications

1. **Chowdhury**, **S. S.**, Sarkar, M. R. & Yi, C. Y. *Energy-Efficient Reconfigurable MRAM-Enabled Delay Feedback Reservoir Computing at the Edge.* [Ongoing]. 2025.
2. Sarkar, M. R. & **Chowdhury**, **S. S.** *An In-Memory Power Efficient Computing Architecture with Emerging VGSOT MRAM Device* in *2024 IEEE International Symposium on Circuits and Systems (ISCAS)* (2024), 1–5.
3. Sarkar, M. R. & **Chowdhury**, **S. S.** *Phase Signal Classification with Reservoir Computing* in *2025 IEEE 34th Microelectronics Design and Test Symposium (MDTS)* (2025).