

# Shirazush Salekin Chowdhury

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## SUMMARY

Industrially experienced in the full flow of Analog Mixed-Signal IC design and verification from block level to top-level design, GDS generation, physical verification (LVS, DRC, EM, IR), and tape-out using commercial EDA tools.

## RESEARCH AREA

Analog Mixed-Signal Integrated Circuits, Neuromorphic Computing, AI Hardware Accelerator, and In-Memory Computing.

## EDUCATION

Doctor of Philosophy, Electrical Engineering, Virginia Tech, USA, CGPA: 4.00/4.00	Aug 2023 — Present
Master of Science, Electrical and Electronic Engineering, AIUB, Bangladesh, CGPA: 4.00/4.00	Jun 2019 — Apr 2021
Bachelor of Science, Electrical and Electronic Engineering, AIUB, Bangladesh, CGPA: 4.00/4.00	Jan 2016 — May 2019

## WORK EXPERIENCE

<b>Graduate Research Assistant</b> , MICS and BRICC Lab, Electrical Engineering, Virginia Tech	May 2024 — Present
<ul style="list-style-type: none"><li>Taped out an image classification AI hardware based on Reservoir Computing in GF 22FDX technology.</li><li>Current project: Designing and developing of Analog Front End (AFE) of MEMS indirect Time-of-Flight (iTOF) for Eye Tracking.</li></ul>	

<b>Graduate Teaching Assistant</b> , Electrical Engineering, Virginia Tech	Aug 2023 — May 2024
<ul style="list-style-type: none"><li>Conducted courses titled Digital Design - I, and Intro to ECE Concepts.</li></ul>	

<b>Senior Engineer</b> Globalfoundries DTCO (ODC) Circuit & System Design Department, Ulkasemi Pvt. Ltd.	Aug 2019 — Jul 2023  Dhaka, Bangladesh
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### Analog Circuit Design and Layout

- Experienced in designing and layout of the analog circuit blocks, such as Bandgap Reference, Bias Generator, OpAmp, Switched Cap, Charge Pump, Oscillators, PLL, and Data Converters.
- Industry standard layout design.

### Intellectual Property Quality Assurance (IPQA)

- Automation of the IPQA flow for different IP types, such as LOGIC, IO, AMS, Memory, Complex IPs, etc.
- DRC Testcase generation to check abutment DRC for the standard cell library.

### Standard Cell Library Development

- Area efficient and high-performance Standard Cell Library development.
- LVS, DRC check and Library Characterization.

### Hardware & Programming Language

- Python, Bash, Skill, and Verilog.

## PROJECTS

### PLL Design for Frequency Generation

- Designed a PLL with frequency range of 200 MHz to 1.6 GHz at 1.2 V supply
- Achieved settling times of 873 ns (SS), 715 ns (TT), 507 ns (FF) with power consumption ranging from 110.5  $\mu$ W to 215.3  $\mu$ W
- Optimized for low power and fast settling across PVT variations
- Project details available on GitHub: [github.com/salekinchowdhury/PLL-Design-for-Frequency-Generation-Cadence](https://github.com/salekinchowdhury/PLL-Design-for-Frequency-Generation-Cadence)

### Bandgap Reference Circuit Design

- The Bandgap Reference Circuit operates at a supply voltage of 1.8 V, provides a constant output voltage of 1.06 V, has a temperature coefficient of less than  $\pm 34.3$  ppm/ $^{\circ}$ C, consumes 365.6  $\mu$ W of power, and is designed to function within a temperature range of  $-40^{\circ}$ C to  $125^{\circ}$ C.
- Project details available on GitHub: [github.com/salekinchowdhury/Bandgap-Reference-Circuit-in-Cadence](https://github.com/salekinchowdhury/Bandgap-Reference-Circuit-in-Cadence)

### Delta-Sigma Modulator Circuit Design

- The Delta Sigma Modulator is designed using 55nm technology with RVT devices, operates at a supply voltage of 1.2 V, supports a frequency range of 10KHz to 50KHz, utilizes a reference voltage of 600mV for the integrator and comparator, an external clock speed between 5MHz and 10MHz, and a reference current of 10 $\mu$ A for the differential amplifier. The modulator has a 1-bit resolution.
- Project details available on GitHub: [github.com/salekinchowdhury/Delta-Sigma-Modulator-in-Cadence](https://github.com/salekinchowdhury/Delta-Sigma-Modulator-in-Cadence)

## TECHNICAL SKILLS AND EXPERTISE

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- **Circuit and Layout Design:** Cadence Virtuoso.
- **Circuit Simulation:** Cadence Spectre, PrimeSim HSPICE.
- **RC Extraction:** Synopsys StarRC
- **DRC, LVS, ERC:** Mentor Graphics Calibre.
- **EM, IR:** Cadence Voltus.
- **Library Characterization:** Cadence Liberate

## EXTRACURRICULAR ACTIVITIES

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**Volunteer,** IEEE AIUB Student Branch  
**Electrical Crew Member,** AIUB Robotic Crew (ARC)

**Oct 2016 — Jul 2017**  
**Oct 2017 — Jul 2018**

## SELECTED PUBLICATIONS

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1. **Chowdhury, S. S.,** Sarkar, M. R. & Yi, C. Y. *Energy-Efficient MRAM-Enabled Delay Feedback Reservoir Computing at the Edge.* Manuscript in preparation. 2024.
2. Sarkar, M. R. et al. *An In-Memory Power Efficient Computing Architecture with Emerging VGSOT MRAM Device* in *2024 IEEE International Symposium on Circuits and Systems (ISCAS)* (2024), 1–5.
3. **Chowdhury, S. S. &** Arifin, F. *The Effects of the Substrate Doping Concentrations on 6H-SiC Nano-Scale ggNMOS ESD Protection Device* in *2021 2nd International Conference on Robotics, Electrical and Signal Processing Techniques (ICREST)* (2021), 329–333.