Vrije Universiteit Brussel

VOORBEREIDING BACHELOR PROEF
12/03/2014

CACHE SIMULATIE

Door: Lenaerts Sander

Begeleider: Mattias De Wael

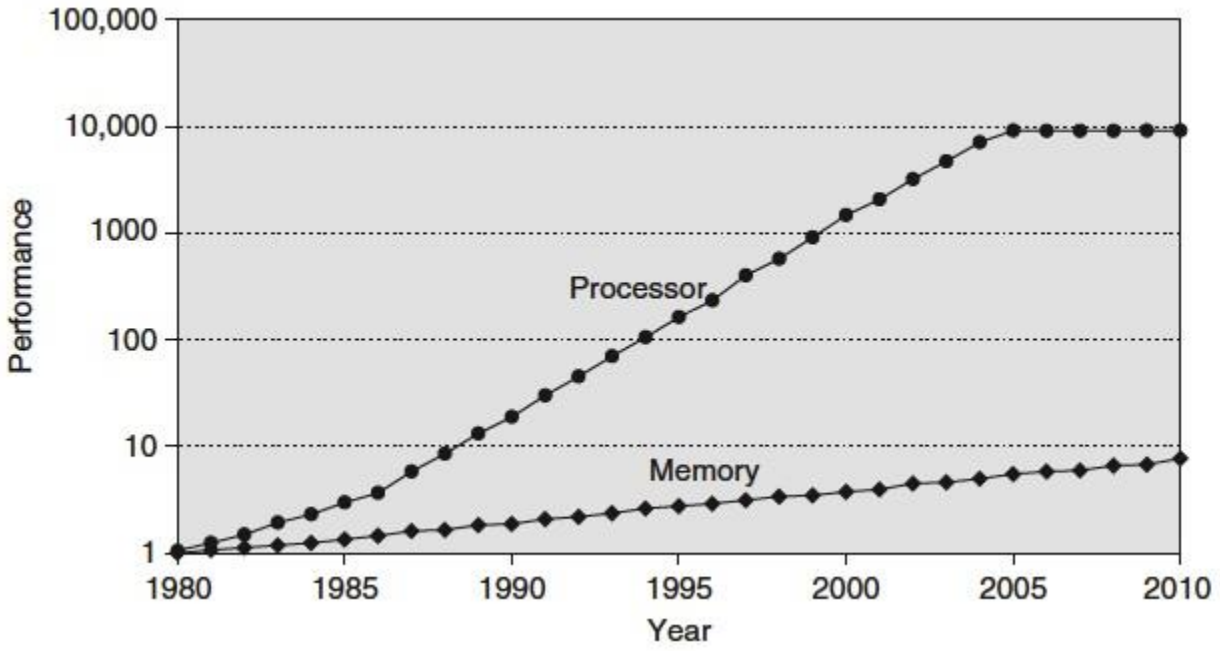
Promotor: Jennifer Sartor

Vrije
Universiteit
Brussel

Inhoud

- Doel van caches
- Wat zijn caches
- Waarom caches bestuderen
- Hoe werken caches
- Vier centrale vragen rond caches
- Coherency in multicore
- conclusie

Doel



Processor: 0.3 - 0.5 ns

=> 160 tot 666 keer sneller

Main Memory: 80 -200 ns

Wat zijn caches

- Hardware component
- Gereserveerd geheugen
- Link tussen CPU en main memory
- Bevat kopieën

Waarom

- Hardware fabrikanten
- Zelf caches samenstellen
- Cache simulatie
- Caches bestuderen

Locality

- (define (map lst function)
  (unless (null? lst)
  (function (car lst))
  (map (cdr lst) function)))

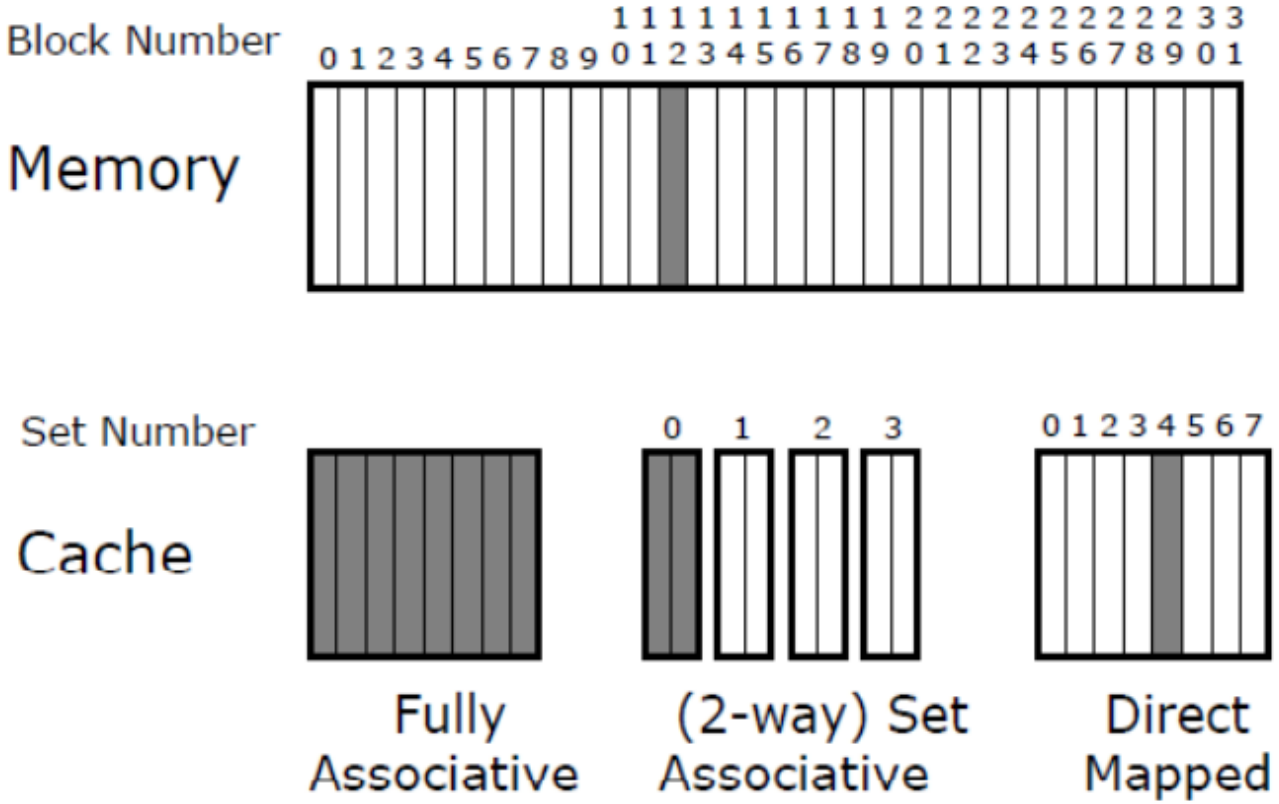
Locality

- (define (map lst function)
  (unless (null? lst)
  (function (car lst))
  (map (cdr lst) function)))

Locality

- (define (map lst function)
    (unless (null? lst)
      (function (car lst))
      (map (cdr lst) function)))

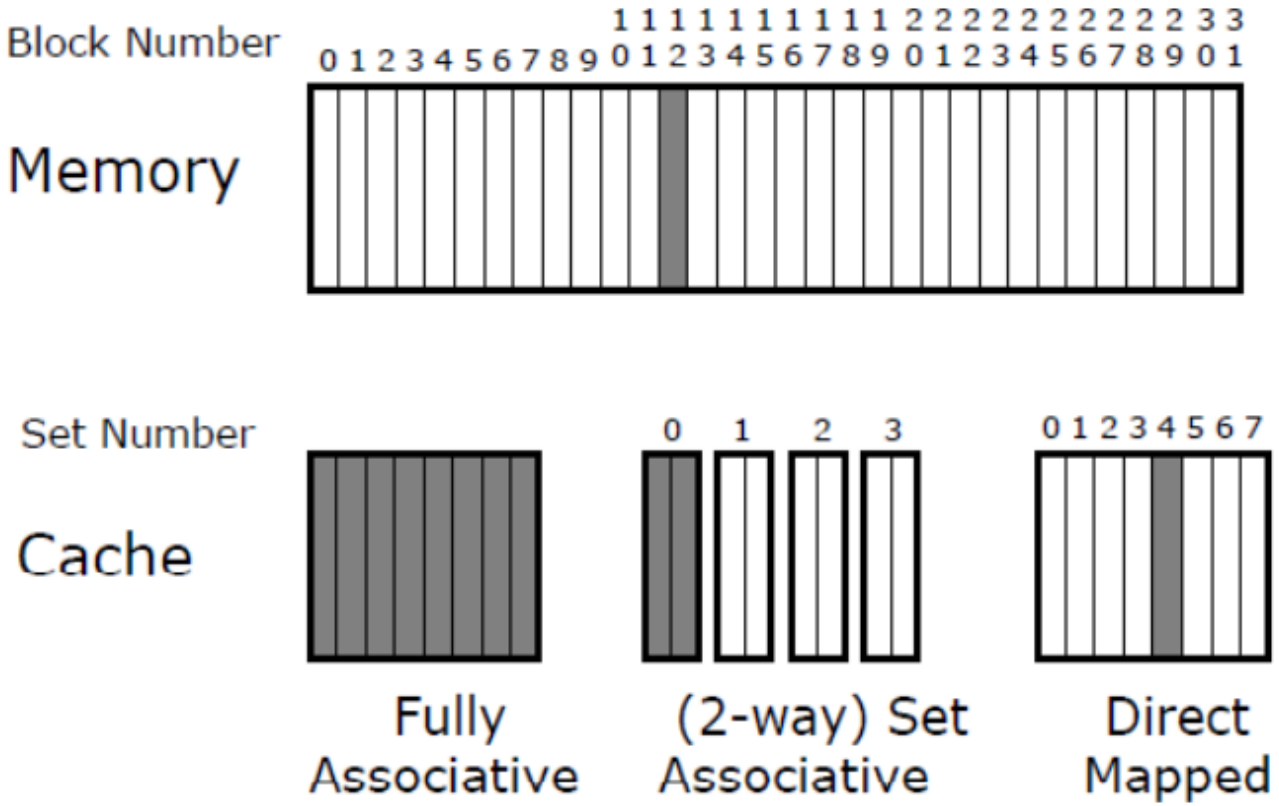
Block placement



Block identification

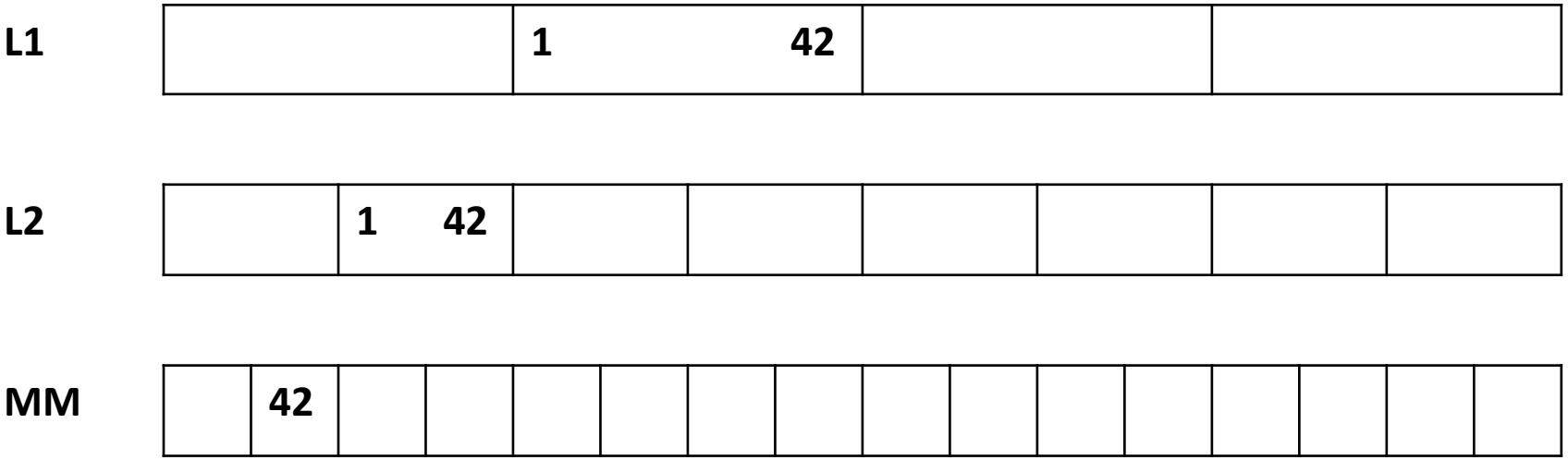
Read 5 / write 5 12

Block replacement



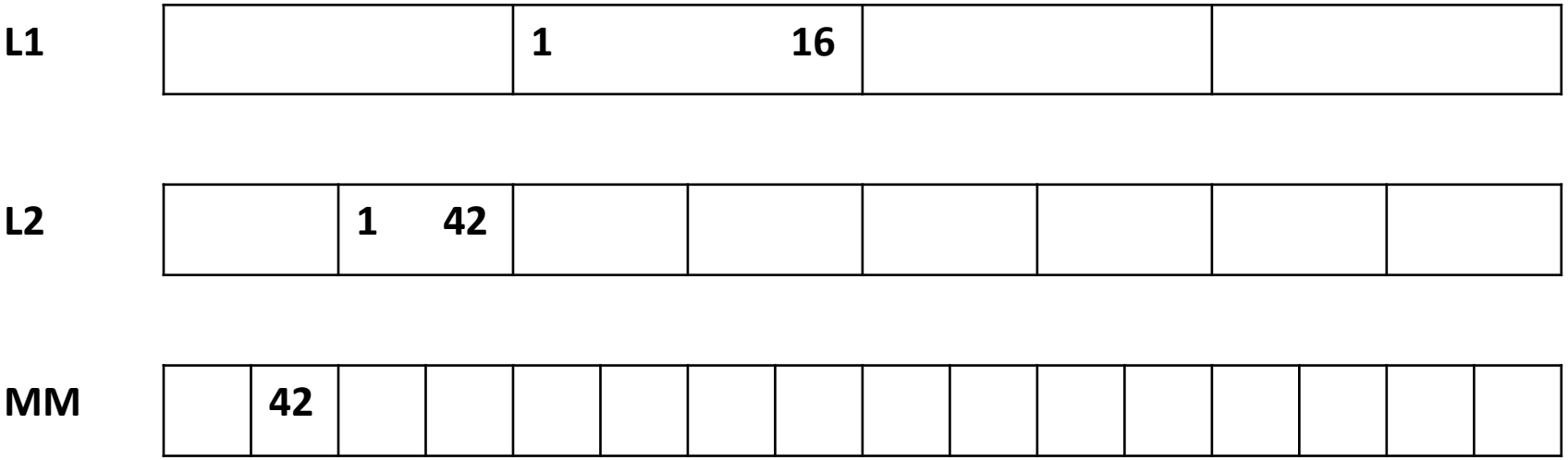
Write strategy

Write-through: write 1 16



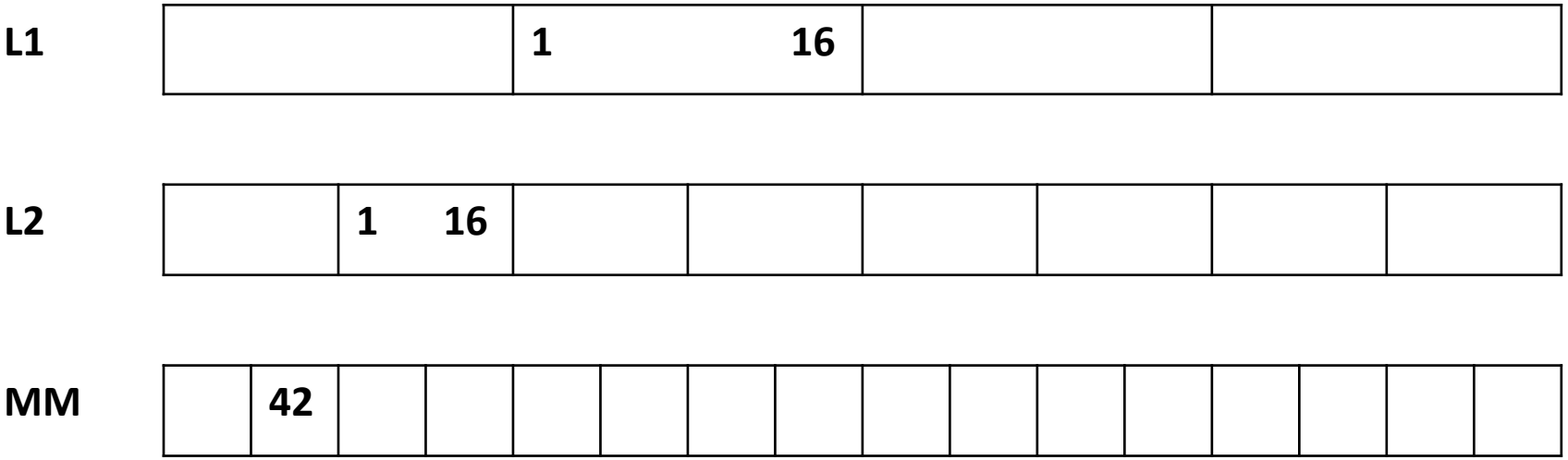
Write strategy

Write-through: write 1 16



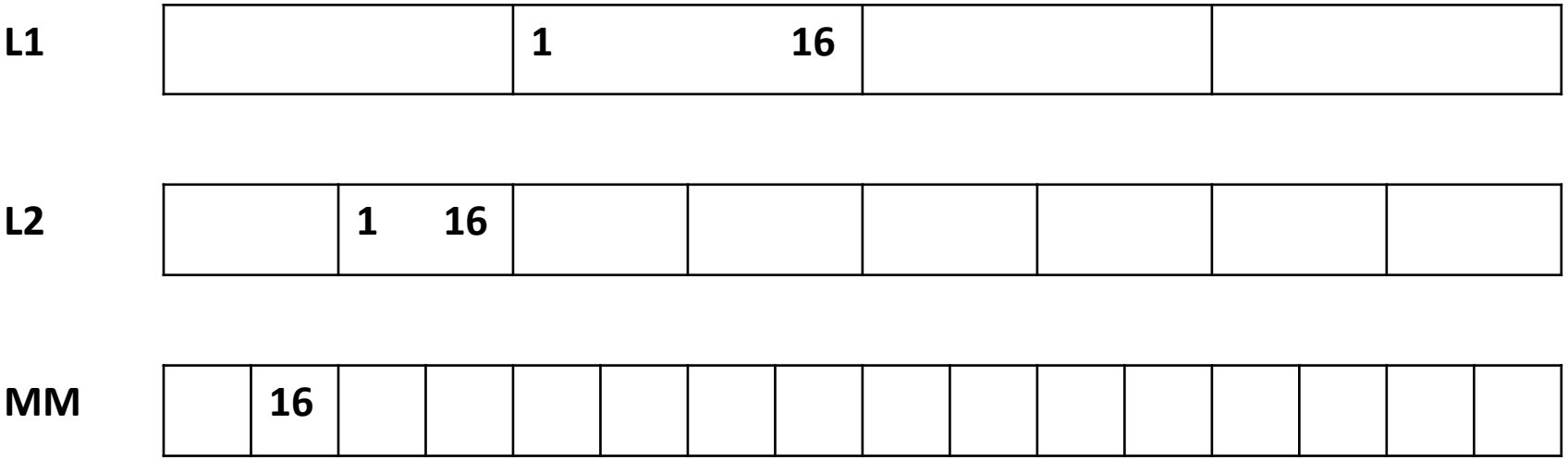
Write strategy

Write-through: write 1 16



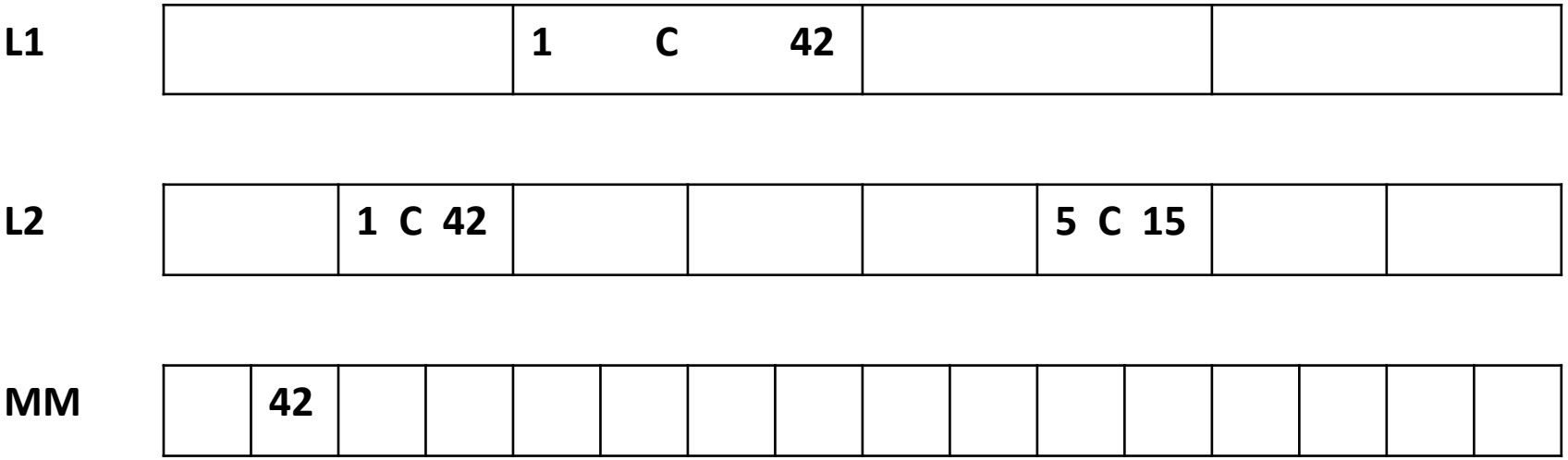
Write strategy

Write-through: write 1 16



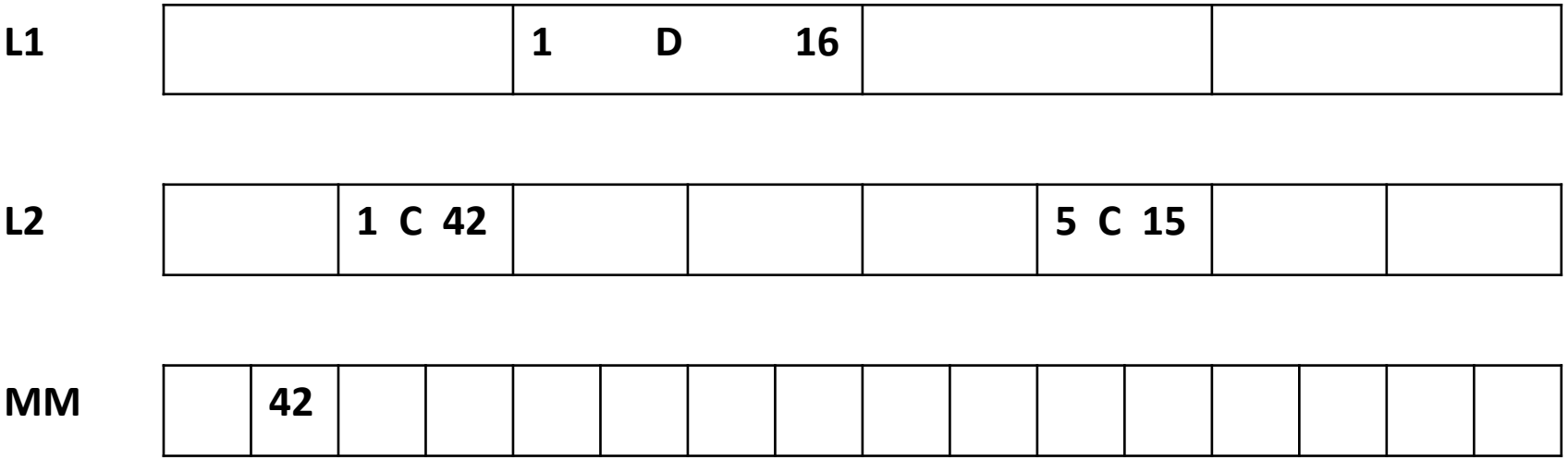
Write strategy

Write-back: write 1 16



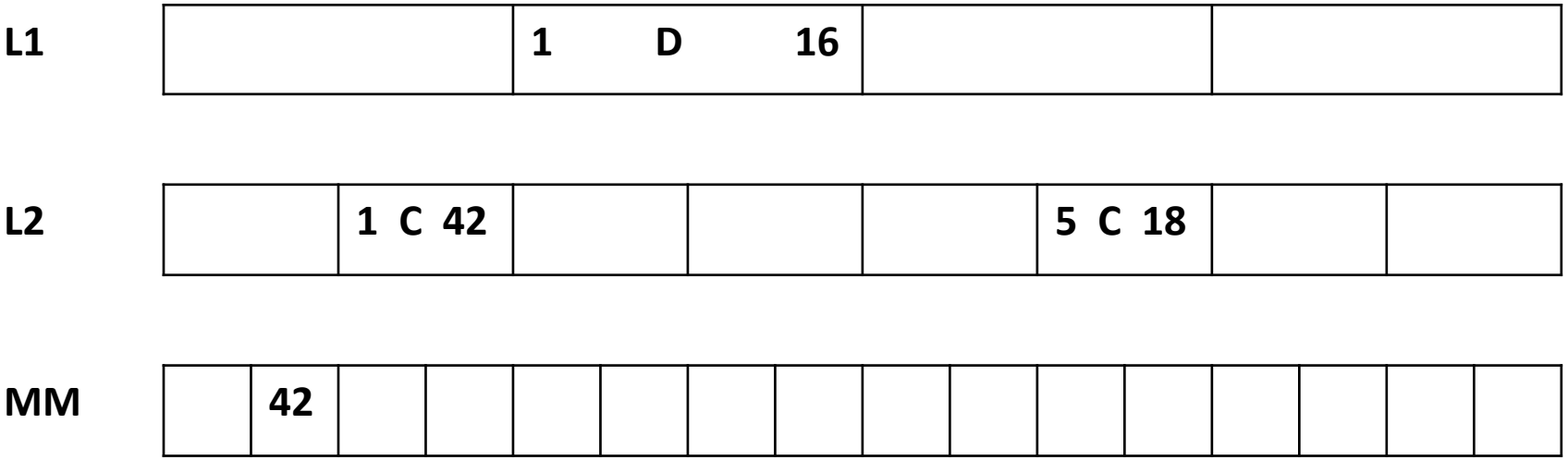
Write strategy

Write-back: write 1 16



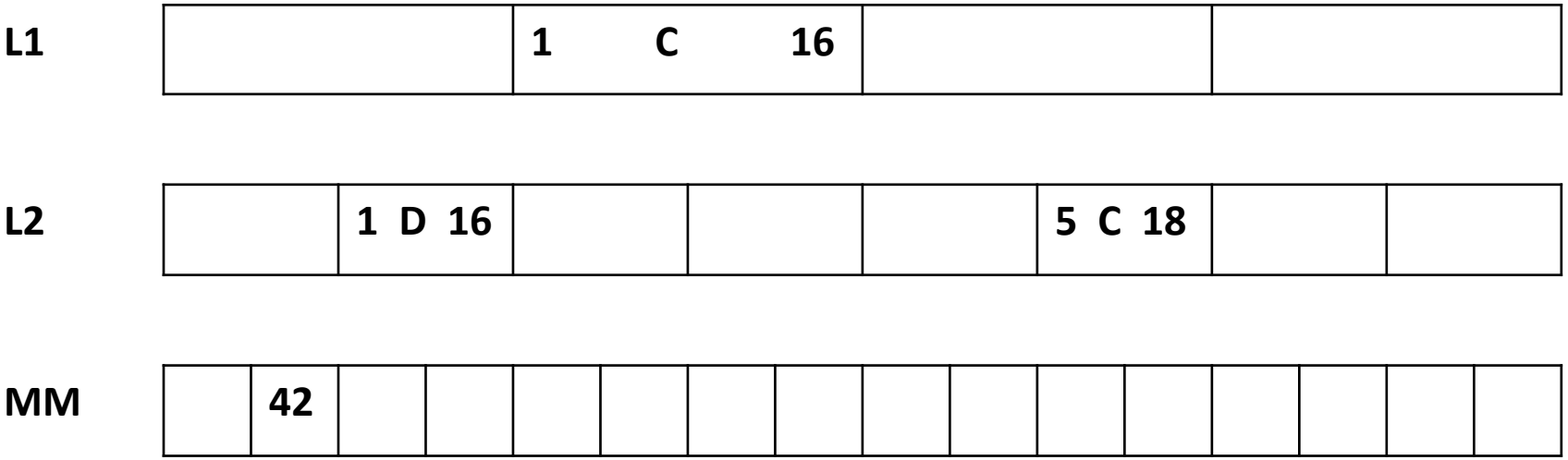
Write strategy

Write-back: Read 5



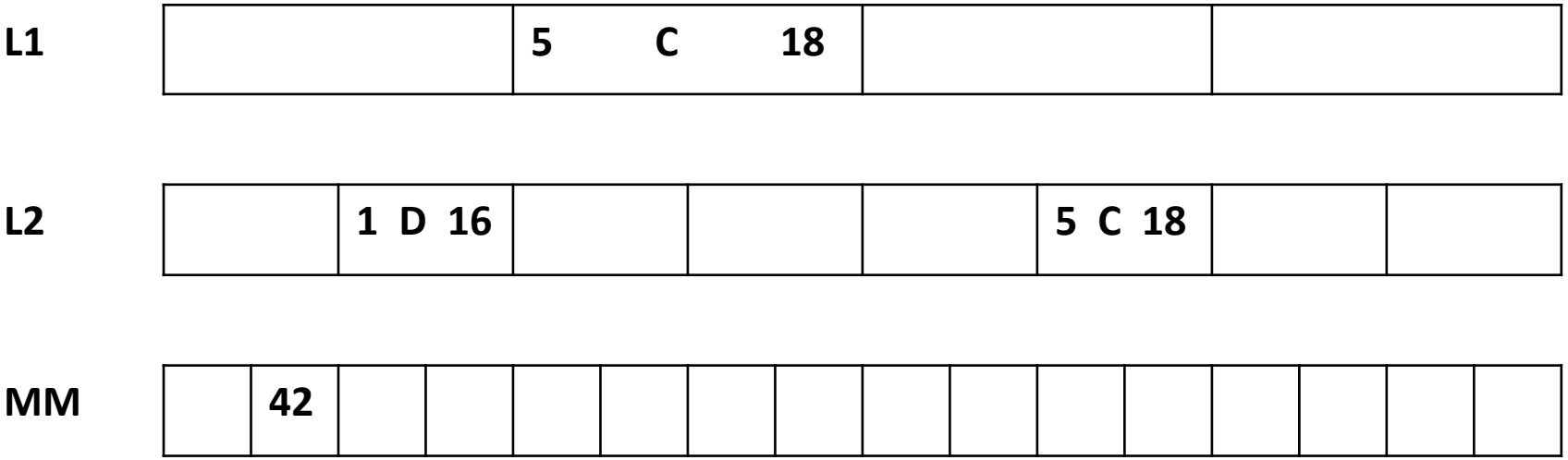
Write strategy

Write-back: Read 5



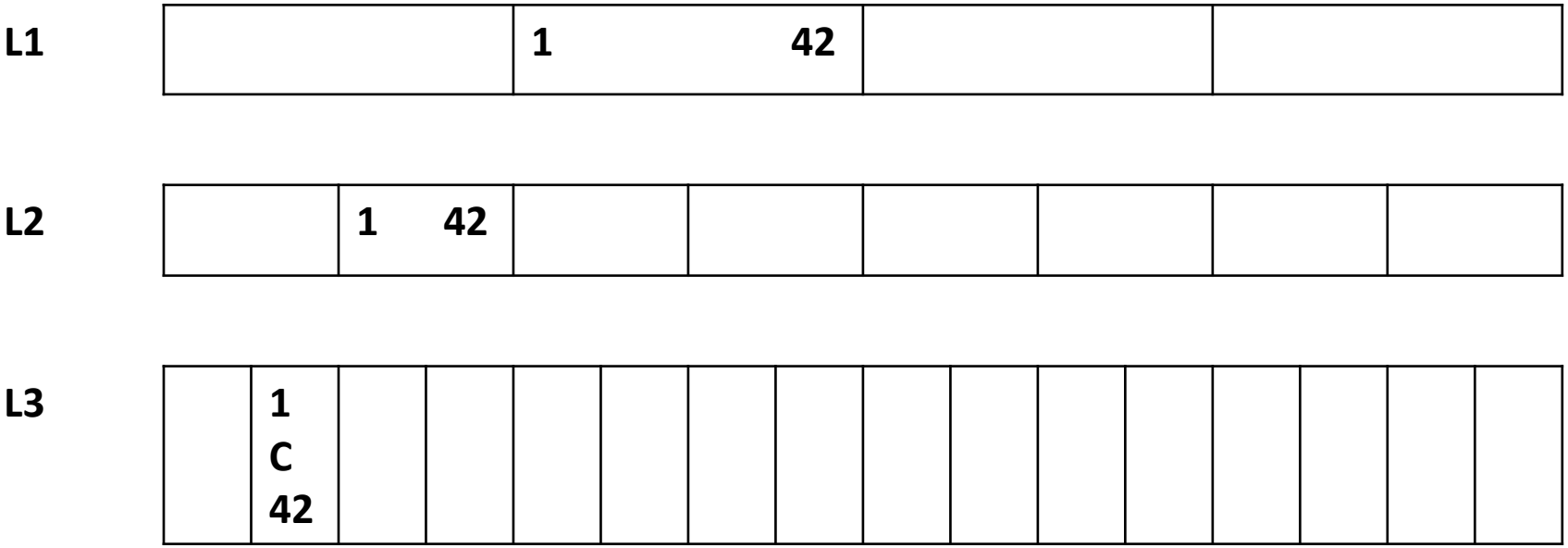
Write strategy

Write-back: Read 5



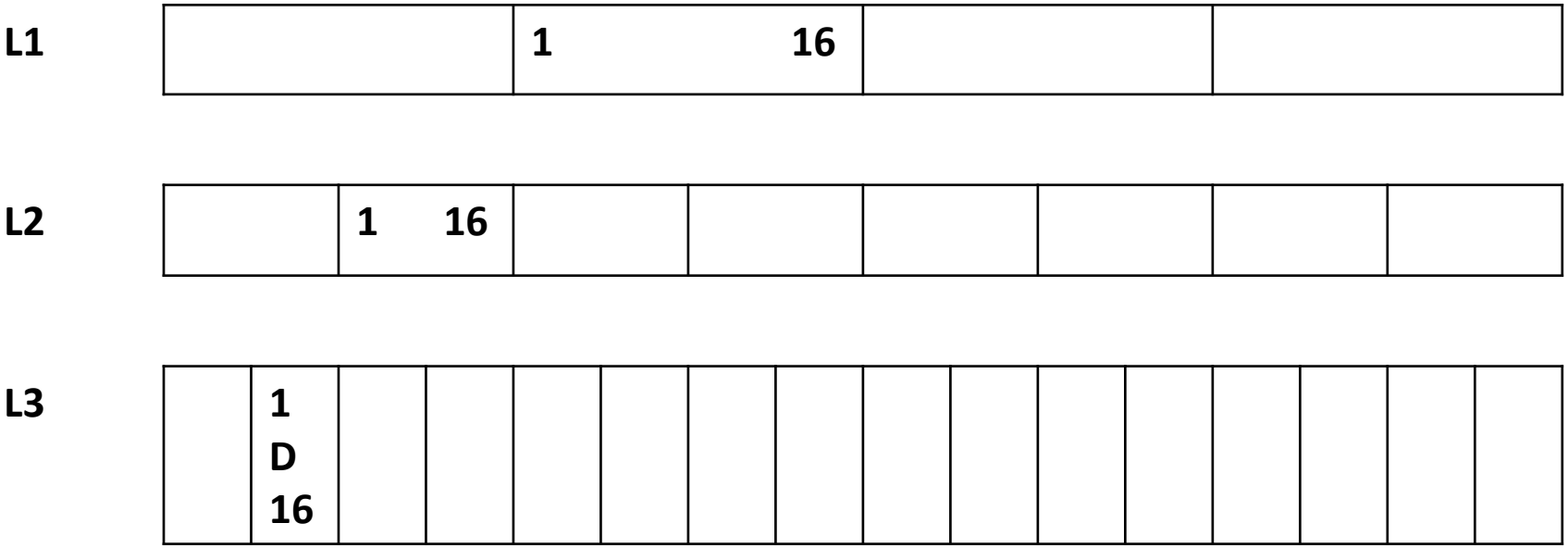
Write strategy

Combo: write 1 16



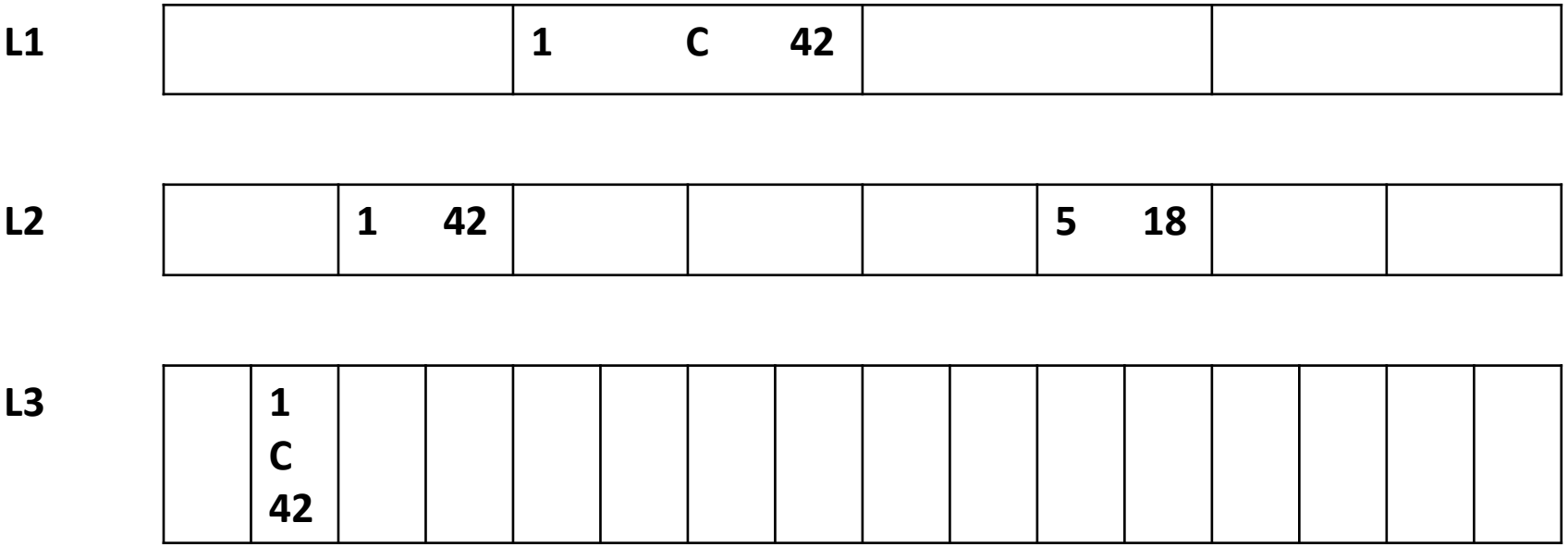
Write strategy

Combo: write 1 16



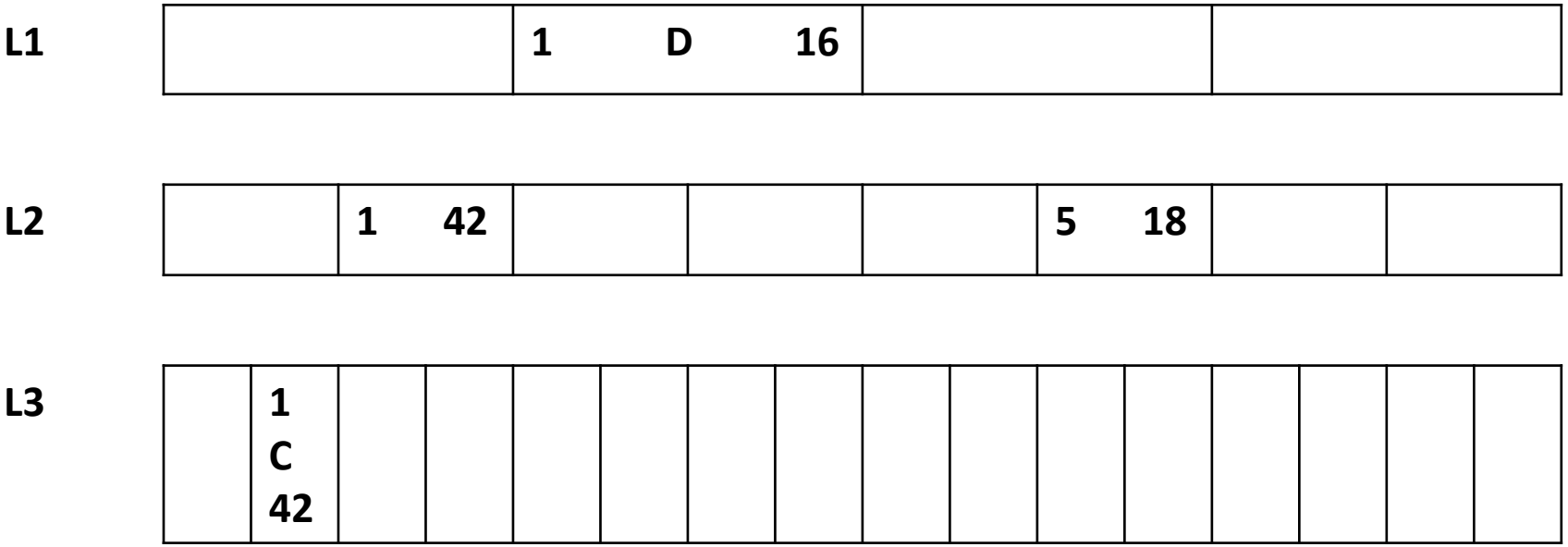
Write strategy

Combo: write 1 16



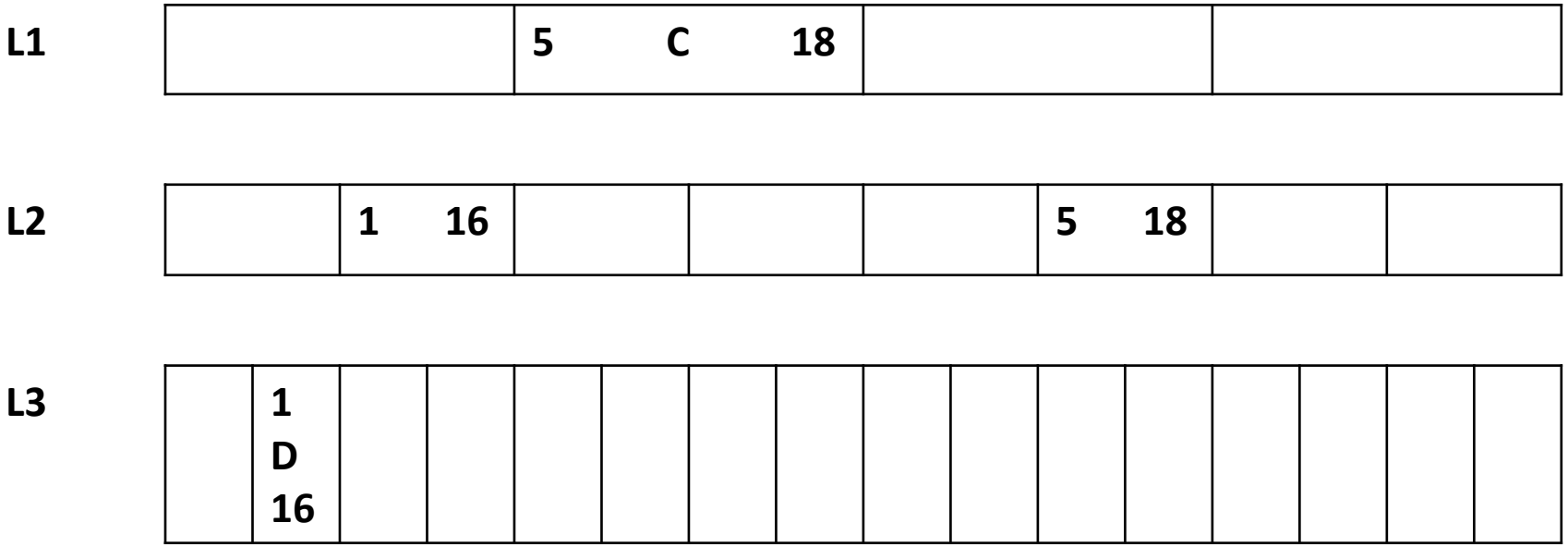
Write strategy

Combo: Read 5



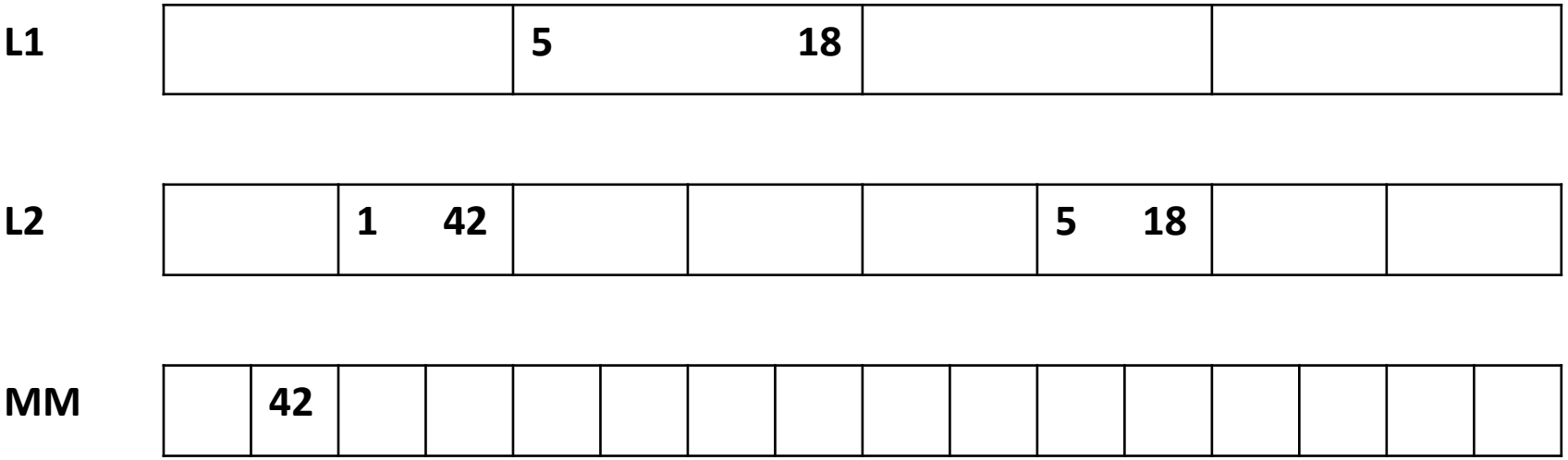
Write strategy

Combo: Read 5



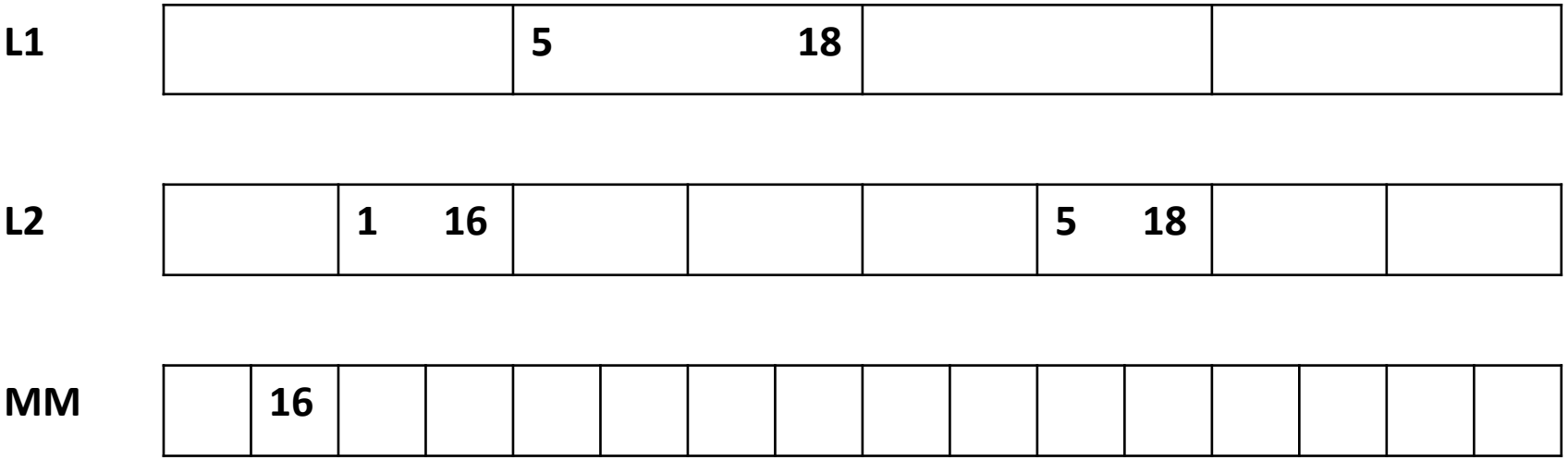
Write strategy

Write 1 16



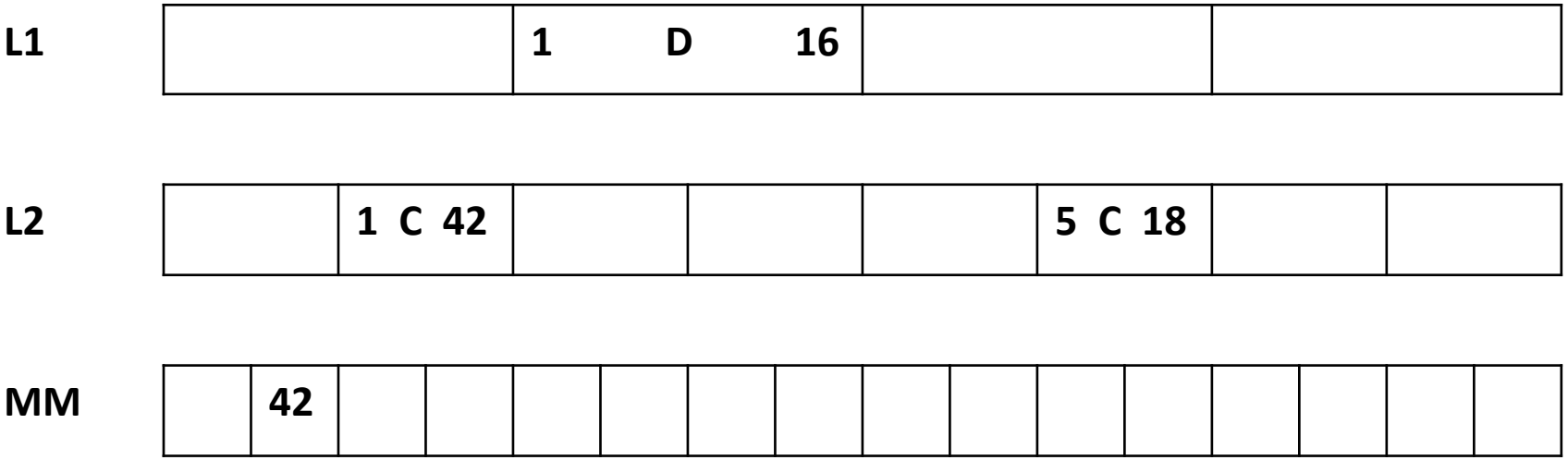
Write strategy

Write-through: Write 1 16

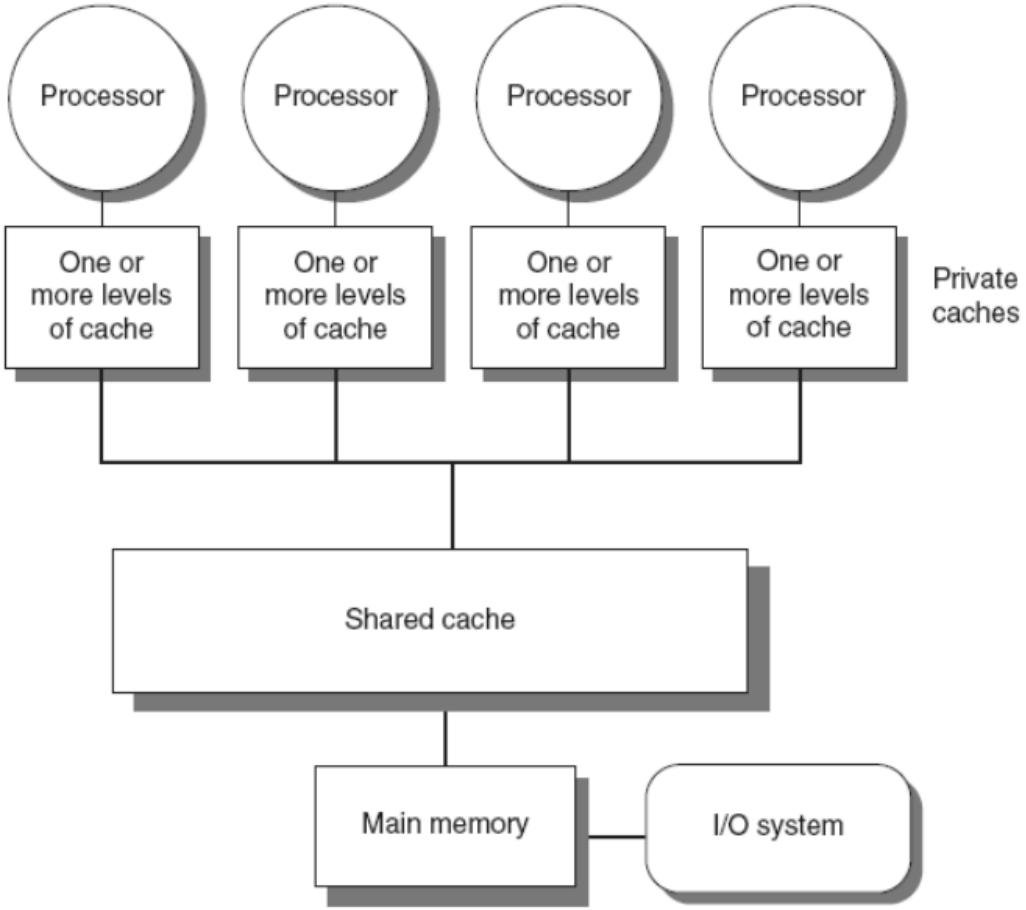


Write strategy

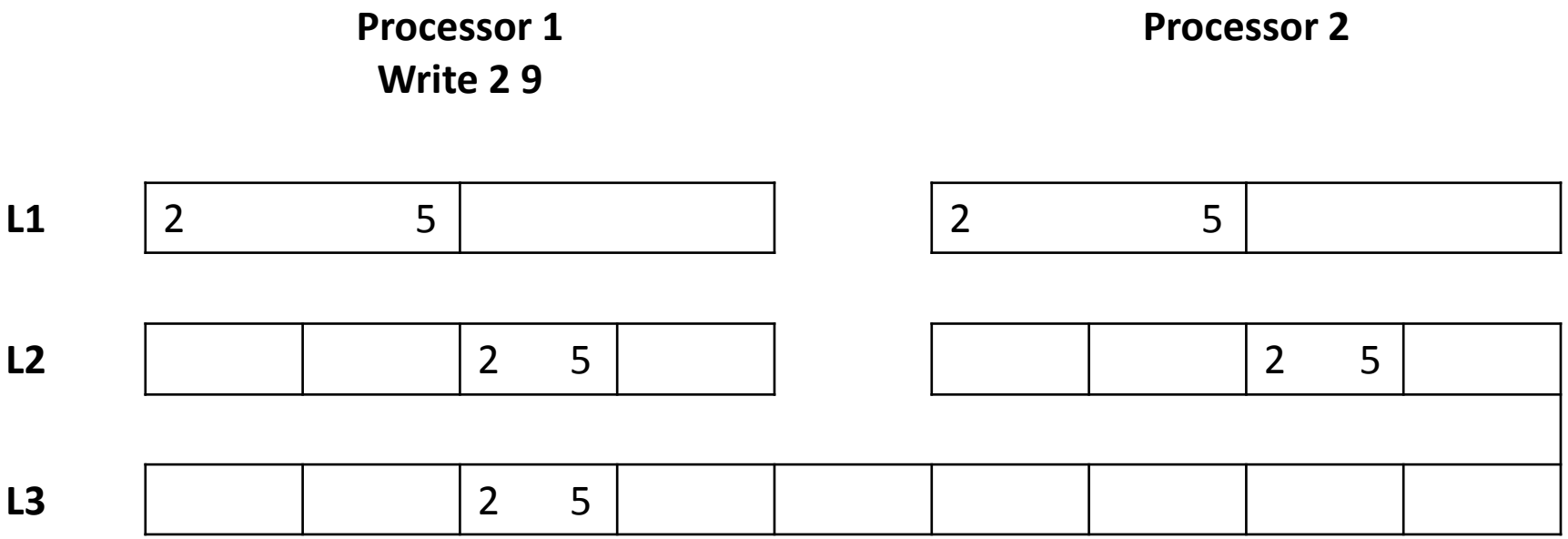
Write-back: Write 1 16



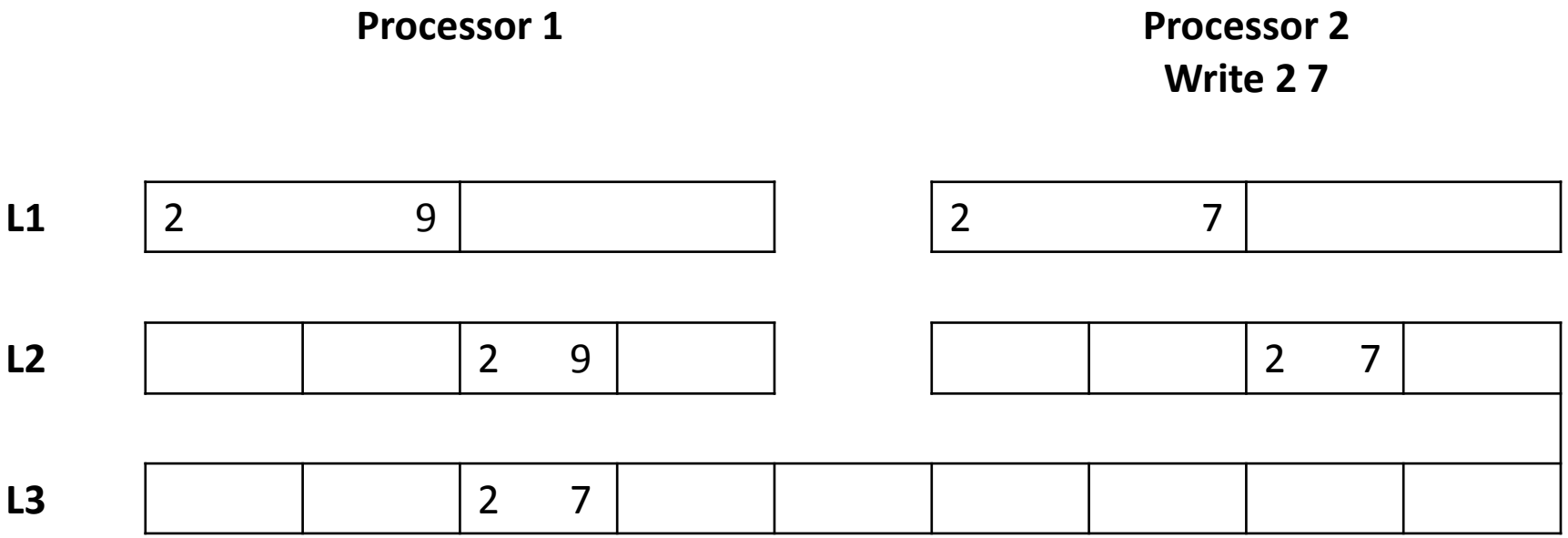
Multicore processoren



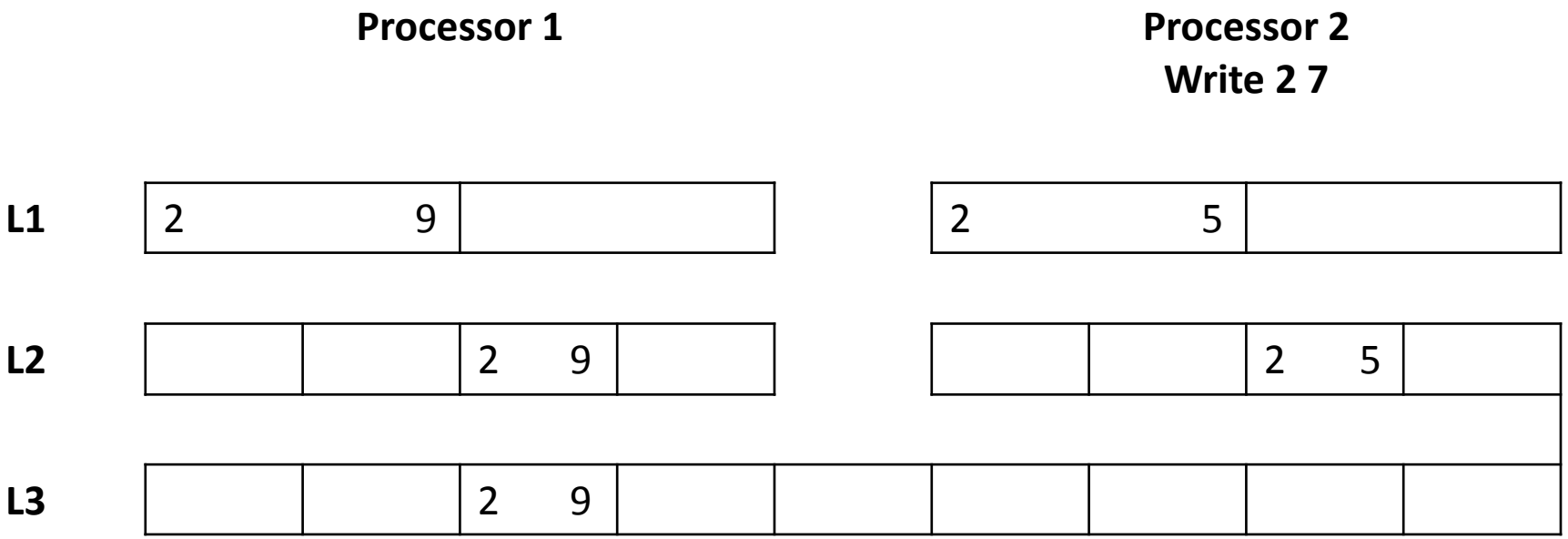
Coherency protocols



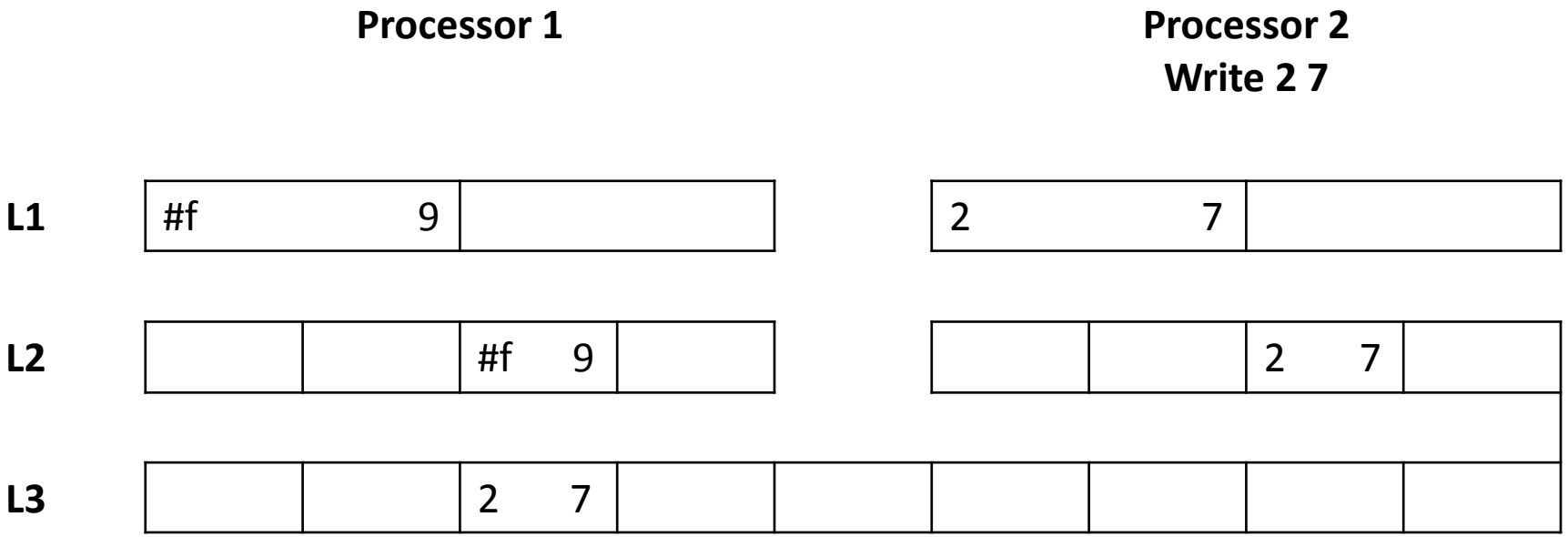
Coherency protocols



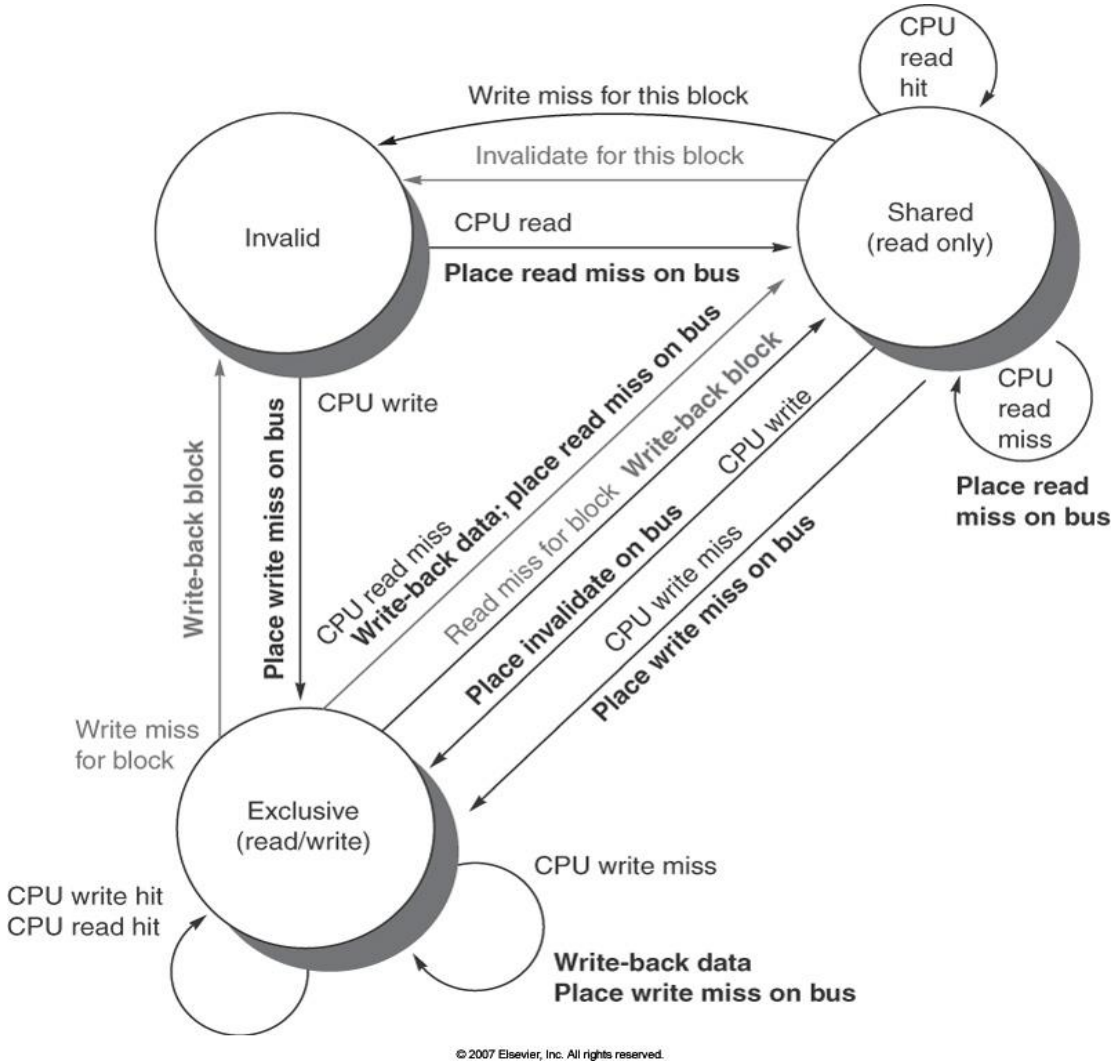
Coherency protocols



Coherency protocols



Coherency protocols



Vrije Universiteit Brussel

Conclussie

- *Drie methoden*
  - *Read*
  - *Write*
  - *Invalidate*

Conclusie

- variatie punten
  - Blok placement: 3
  - Replacement strategie: 4
  - Write strategie: 4
  - Coherence protocolen: 5
  - Multilevel in/exclusion: 2
  - Read boven write: 2
  - Prefetching/pipelining/way-predicition: 3
  - Single / non-blocking caches: 2

  => 4320

Conclusie

- Zes knoppen
  - Cache creatie
  - Vind set adres
  - Vind blok
  - Na cache operatie
  - Replacement strategy
  - Write strategy