Ultra Data Sheet

Ultra is a 32-bit microcontroller featuring the ARM Cortex M7 processor. This microcontroller is intended for applications where efficiency and simple system integration is important. The Ultra microcontroller is suitable for applications such as:

- General embedded devices
- Industrial devices
- Point-of-sale devices

13 x 13

Core

- ARM Cortex-M7 processor running up to 300 MHz
- 32 KB I-cache and 32 KB D-cache
- 256 KB L2 cache
- 256 KB tightly coupled memory (TCM)
- Double precision Floating Point Unit (FPU)

Memories and memory interfaces

- Up to 1 MB of on-chip SRAM (including TCM)
- 256 KB L2 cache can be configured as general purpose SRAM
- Flexible serial bus supporting serial NOR flash, HyperRAM, Octal PSRAM, and serial NAND flash
- LPDDR2 controller
- Two SD host controllers
- FlexBus external bus interface and SDRAM controller

Timers

- Two 6-ch, 16-bit general purpose/PWM timers
- Two 2-ch, 16-bit generral purpose timers/PWM timers
- 32-bit low-power timer
- Real-time clock with independent power domain

Security and integrity modules

- CAAM hardware encryption accelerator
- 32 KB secure RAM
- DryIce tamper detection

Operating Characteristics

- Voltage range: 1.71 to 3.6 V???
- Temperature range (ambient): -40 to 105°C

Human-machine interface

- Up to xx general-purpose I/O (GPIO)
- Three SAI modues
- One SPD/IF
- Microphone?

Analog modules

- Two 12-bit SAR ADCs (1 us conversion rate)
- Two 12-bit DACs

System peripherals

- Flexible low-power modes, multiple wake-up sources
- 32-channel DMA controller
- Independent external and software watchdog monitor

Clocks

- Two crystal oscillators: 32 kHz (RTC) and 19.2 MHz or 24 MHz
- Internal 24 MHz RC oscillator intended for low power operation
- Five PLLs for generating internal clocks

Communication interfaces

- 10/100 Ethernet controller supporting MII and RMII PHY interfaces
- Two HS USB-OTG ports with integrated USB PHYs
- Four UARTs, four SPIs, 4 I2C
- Two CAN modules with CAN-FD support
- Two EMVSIM

Ordering Information

Part Number	Memory		Maximum number of I/O's
	Flash (KB)	SRAM (KB)	

Related Resources

Type	Description	Document
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector	
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	
Data Sheet	The Data Sheet is this document. It includes electrical characteristics and signal connections.	
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_*x*N50M[1]
Package drawing	Package dimensions	Package drawing:

1. To find the associated resource, go to freescale.com and perform a search using this term with the *x* replaced by the revision of the device you are using.

Table of Contents

1 Ratings
(view resource)

1.1 Thermal handling ratings
(view resource)

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings
(view resource)

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings
(view resource)

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current absolute max ratings (view resource)

Symbol	Description	Min.	Max.	Unit
VDD_SOC_IN	Core supply voltage (to LDO_SOC regulator)	–0.3	1.5	V
VDD_SOC_CAP	Internal supply voltage	–0.3	1.3	V
VDD_HIGH_IN	Supply to internal regulators (to LDO_2P5, LDO_1P1, and LDO_SNVS)	–0.3	3.6	V
VDD_HIGH_CAP	Internal 2.5V supply	–0.3	2.75	V
VDD_SNVS_IN	Secure non-volatile storage supply (to LDO_SNVS)	–0.3	3.6	V
VDD_SNVS_CAP	Backup battery supply	–0.3	??	V
VDD_PLL	PLL supply	–0.3	??	V
VDD_DDR	DDR IO supply voltage?	–0.4	1.975	V
VDD25_DDR	DDR 2.5V supply voltage?	–0.4	2.75	V
VDD18_DDR	DDR 1.8V supply voltage?	–0.4	1.975	V
VDD_ADC33	ADC 3.3V supply voltage	–0.3	3.6	V
USBn_VBUS	USB VBUS voltage detect (to LDO_USB)	–0.3	5.5	V
VDD_USB_CAP	Internal USB voltage	–0.3	3.6?	V
VDD_PTx	GPIO supply voltages	–0.5	3.6	V
V_{DIO}	Digital input voltage	–0.5	VDD_PTx + 0.3	V
V_{AIO}	Analog input voltage[1]	–0.3	VDD_PTx + 0.3	V
$V_{DTamper}$	Tamper input voltage	–0.3	VDD_SNVS_CAP + 0.3?	V
V_{DDRIO}	Digital DDR input voltage	–0.3	VDD_DDR + 0.3	V
V_{USBn_DP}	USBn_DP input voltage	–0.3	3.63	V
V_{USBn_DM}	USBn_DM input voltage	–0.3	3.63	V
IDD_SOC_IN	Core supply current	—	500	mA
IDD_HIGH_IN	Internal regulators supply current[2]	—	125	mA
IDD_SNVS_IN	SNVS supply current[3]	—	500	uA
IDD_PLL	PLL supply current	—	TBD	mA
IDD_DDR	DDR IO supply current	—	(See)[4]	mA
IDD25_DDR	DDR 2.5V supply current	—	50	mA
IDD18_DDR	DDR 1.8V supply current	—	TBD	mA
IDD_DDR_VREF	DDR VREF supply current	—	1	mA
IDD_ADC33	ADC 3.3V supply current	—	TBD	mA
IDD_USBn_VBUS	USB VBUS supply current	—	50[5]	mA

Table continues on the next page...

Symbol	Description	Min.	Max.	Unit
IDD_PTx	Digital I/O port supply voltage (should this be removed?)	—	Use maximum IO equation[6]	mA
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
2. The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration
3. The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.
4. The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the i.MX 6UltraLite Power Consumption Measurement Application Note (AN5170) for examples of DRAM power consumption during specific use case scenarios.
5. This is the maximum current per active USB physical interface.
6. General equation for estimated, maximum power consumption of an IO power supply: Imax = N x C x V x (0.5 x F) Where: N—Number of IO pins supplied by the power line C—Equivalent external capacitive load V—IO voltage (0.5 x F) —Data change rate. Up to 0.5 of the clock rate (F) In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

1.5 Power-up sequence (view resource)

The below restrictions must be followed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- VDD_HIGH_IN should be turned on before VDD_SOC_IN.

NOTE

The ONOFF input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the ONOFF input, the internal POR module takes control. See the Ultra Reference Manual (RM) for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB0_VBUS, USB1_VBUS, and VDD_ADC33 are not part of the power supply sequence and may be powered at any time.

1.6 Power-down sequence
(view resource)

The below restrictions must be followed:

- VDD_SNVS_IN supply must be turned off after any other power supply or be connected (shorted) with the VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after any other supply is switched off.

NOTE

VDD_HIGH_IN should be turned off after VDD_SOC_IN is switched off.

2 General
(view resource)

2.1 AC electrical characteristics
(view resource)

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

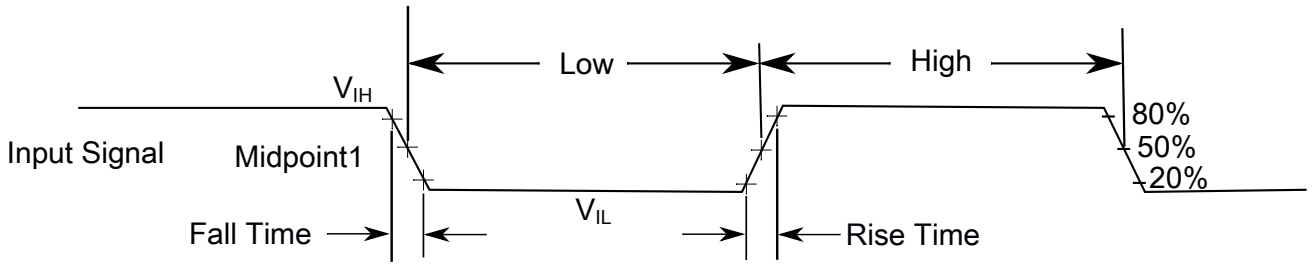


Figure 1. Input signal measurement reference

What IO control options (of any) will be supported for Ultra, and what register fields control them? And which ones do we want to use as the default assumptions for timing?

All digital I/O switching characteristics assume:

1. output pins
   - have C_L=30pF loads,
   - are configured for fast slew rate (PORTx_PCRn[SRE]=0), and
   - are configured for high drive strength (PORTx_PCRn[DSE]=1)
2. input pins
   - have their passive filter disabled (PORTx_PCRn[PFE]=0)

2.2 Nonswitching electrical specifications (view resource)

2.2.1 Power supply operating requirements (view resource)

Table 1. Power supply operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_SOC_IN	Core supply voltage - Run mode, LDO enabled	1.275	—	1.5	V	1
	Core supply voltage - Run mode, LDO bypassed	1.15	—	1.3	V	
	Core supply voltage - Suspend mode Does this mean that you have to be able to decrease the VDD_SOC_IN to use suspend?	0.9	—	1.3	V	
VDD_SOC_CAP	Internal supply voltage	1.15	—	1.3	V	
VDD_HIGH_IN	Supply to internal regulators	2.8	—	3.6	V	2

Table continues on the next page...

Table 1. Power supply operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_HIGH_CAP	Internal 2.5V supply voltage	2.25	2.5	2.75	V	
VDD_SNVS_IN	Backup battery supply voltage	2.4	—	3.6	V	3
VDD_SNVS_CAP	Internal backup battery supply voltage	??		??	V	
VDD_PLL	PLL supply voltage	??	1.1?	??	V	
VDD_DDR	DDR IO supply voltage	1.14	1.2	1.3	V	
VDD25_DDR	DDR 2.5V supply voltage	2.25	2.5	2.75	V	
VDD18_DDR	DDR 1.8V supply voltage	1.65	1.8	1.95?	V	
VDD_ADC33	ADC/DAC 3.3V supply voltage	3.0	3.15	3.6	V	4, 5
USBn_VBUS	USB VBUS supply voltage	4.40	5	5.5	V	
VDD_USB_CAP	Internal USB supply voltage	3.0	3.3?	3.6?	V	
VDD_PTx	GPIO supply voltages	1.65	1.8, 2.8, 3.3	3.6	V	

1. VDD_SOC_IN must be 125 mV higher than the LDO Output Set Point (VDD_SOC_CAP) for correct supply voltage regulation.
2. Must match the range of voltages that the backup battery supports.
3. Can be combined with VDD_HIGH_IN, if the system does not require keeping real time and other data during OFF state.
4. VDD_ADC33 must be powered even if the ADC is not used.
5. VDD_ADC33 cannot be powered when the other SoC supplies (except VDD_SNVS_IN) are off.

2.2.2 Integrated LDOs
(view resource)

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The on-chip LDOs are intended for internal use only and should not be used to power any external circuitry. See the Reference Manual for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO operation only.

2.2.2.1 LDO_SOC Regulator
(view resource)

The LDO_SOC regulator provides power to the digital SoC power domains. This linear regulator converts a supply voltage (1.275V - 1.5V) to produce a 0.9V - 1.3V output voltage. The input voltage must be 125mV higher than the output voltage.

The LDO_SOC regulator can operate in one of the three modes:

- Internal bypass - Allows bypass when an external high power efficient regulator, such as a companion PMIC, is used as a direct source for the SoC loads.
- Power gate - The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode - The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

NOTE

The input voltage must be 125mV higher than the output voltage.

The VDD_SOC_CAP pin requires external decoupling caps. At minimum one 22uF and three 0.22uF caps should be used.

2.2.2.2 LDO_2P5 (view resource)

The LDO_2P5 regulator implements a programmable linear-regulator function from VDD_HIGH_IN. Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. The LDO_2P5 supplies most of the analog circuitry of the integrated PHYs, special I/Os, efuse, and other analog and mixed signal components integrated into the SoC.

A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 ohm.

The VDD_HIGH_CAP is the output for the 2.5V regulator. The VDD_HIGH_CAP output can be routed on the board to power the VDD25_DDR supply. The VDD_HIGH_CAP pin requires external decoupling caps. At minimum one 10uF and one 0.22uF caps should be used.

NOTE

The VDD_HIGH_CAP output is only designed to supply on-chip loads, no extra loads should be connected to the supply.

For additional information, see the Reference Manual.

Table 2. LDO_2P5 parameters

Specification	Min	Typ	Max	Unit	Comments
VDD_HIGH_IN	2.8	3.3	3.6	V	IO supply
VDD_HIGH_CAP?	2.3	2.5	2.6	V	Regulator output
I_out	—	—	350	mA	@500mV drop out
[P:][C:] Regulator output programming range	2.0	2.5	2.75	V	Programmable in 25mV steps
[P:][C:] Brownout Voltage	2.25	2.33	—	V	
[C:] Brownout offset step	0	—	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	—	—	µF	low ESR

2.2.2.3 LDO_1P1 (view resource)

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN. Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies digital portions of the USB PHYs, PLLs, and the internal 24 MHz oscillator.

A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For additional information, see the Reference Manual.

Table 3. LDO_1P1 parameters

Specification	Min	Typ	Max	Unit	Comments
VDD_HIGH_IN	2.8	3.3	3.6	V	IO supply
VDD_1P1_OUT	0.9	1.1	1.2	V	Regulator output
I_out	—	—	150	mA	>= 300mV drop out
[P:][C:] Regulator output programming range	0.8	1.1	1.4	V	Programmable in 25mV steps
[P:][C:] Brownout Voltage	0.85	0.94	—	V	
[C:] Brownout offset step	0	—	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	—	—	µF	low ESR

2.2.2.4 USB regulator (LDO_USB) (view resource)

The LDO_USB regulator implements a programmable linear-regulator function from the USB VBUS voltages (4.4V-5.5V) to produce a nominal 3.0V output voltage. This regulator has a built-in power-mux that allows the user to run the regulator from either one of the VBUS supplies when both are present. If one of the VBUS voltages is present, the regulator automatically selects that supply. The LDO_2P5 supplies most of the analog circuitry of the integrated PHYs, special I/Os, efuse, and other analog and mixed signal components integrated into the SoC.

A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current limit is also included to help the system meet in-rush current targets.

The VDD_USB_CAP pin requires external decoupling caps. At minimum one 10uF and one 0.1uF caps should be used.

For additional information, see the Reference Manual.

Table 4. LDO_USB parameters

Specification	Min	Typ	Max	Unit	Comments
USBn_VBUS	4.4	5.0	5.25	V	
VDD_USB_CAP?	2.9	3.0	3.1	V	Regulator output at default setting
I_out	—	—	100?	mA	@500mV drop out

Table continues on the next page...

Table 4. LDO_USB parameters (continued)

Specification	Min	Typ	Max	Unit	Comments
[P:][C:] Regulator output programming range	2.625	3.0	3.4	V	Programmable in 25mV steps
[P:][C:] Brownout Voltage	2.75	2.85	—	V	
[C:] Brownout offset step	0	—	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	—	—	µF	low ESR

2.2.2.5 Backup battery regulator (SNVS_IN) (view resource)

The SNVS regulator takes the SNVS_IN supply and generates the SNVS_CAP supply, which powers the real time clock and the low power section of the SNVS block.

The VDD_SNVS_CAP pin requires external decoupling caps. At minimum one 0.22uF cap should be used.

For additional information, see the Reference Manual.

2.2.3 IO DC parameters (view resource)

Table 5. IO DC parameters

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage • [P:] I_{OH} = -0.1mA (DSE=001,010) • [P:] I_{OH} = -1mA (DSE=011,100,101,110,11)	VDD_PTx – 0.15	—	V	
V_{OL}	Output low voltage • [P:] I_{OH} = 0.1mA (DSE=001,010) • [P:] I_{OH} = 1mA (DSE=011,100,101,110,11)	—	0.15	V	
V_{IH}	Input high voltage	0.7*VDD_PTx	—	V	
V_{IL}	Input low voltage	—	0.3*VDD_PTx	V	
V_{HYS}	Input hysteresis	250	—	mV	

Table continues on the next page...

Table 5. IO DC parameters (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{TH+}	Schmitt trigger VT+	0.5*VDD_PTx	—	mV	
V_{TH-}	Schmitt trigger VT-	—	0.5*VDD_PTx	mV	
RPU_22K	Pull-up resistor (22 kohm pullup), V_{in}=0V	—	212	uA	
RPU_22K	Pull-up resistor (22 kohm pullup), V_{in}=VDD_PTx	—	1	uA	
RPU_47K	Pull-up resistor (47 kohm pullup), V_{in}=0V	—	100	uA	
RPU_47K	Pull-up resistor (47 kohm pullup), V_{in}=VDD_PTx	—	1	uA	
RPU_100K	Pull-up resistor (100 kohm pullup), V_{in}=0V	—	48	uA	
RPU_100K	Pull-up resistor (100 kohm pullup), V_{in}=VDD_PTx	—	1	uA	
RPD_100K	Pull-down resistor (100 kohm pulldown), V_{in}VDD_PTx	—	48	uA	
RPD_100K	Pull-down resistor (100 kohm pullup), V_{in}=0V	—	1	uA	
I_{IN}	Input current (no PU/PD), V_{in}=0V or VDD_PTx	-1	1	uA	
R_{KEEPER}	Keeper circuit resistance, V_{in}=0.3*VDD_PTx or 0.7*VDD_PTx	105	175	kohm	

2.2.4 LPDDR2 I/O DC parameters

(view resource)

Table 6. LPDDR2 I/O DC parameters

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage, I_{OH} = -0.1mA	0.9*VDD_DDR	—	V	
V_{OL}	Output low voltage, I_{OH} = 0.1mA	—	0.1*VDD_DDR	V	
V_{REF}	Input reference voltage	0.49*VDD_DDR	0.51*VDD_DDR	V	
V_{IH_DC}	DC input high voltage	V_{REF}+0.13	—	V	
V_{IL_DC}	DC input low voltage	—	V_{REF}-0.13	V	
V_{IH_DIFF}	Differential input high voltage	0.26	—	V	
V_{IL_DIFF}	Differential input low voltage	—	-0.26	V	
MM_{PUPD}	Pull-up/pull-down impedance mismatch	-15	15	%	
R_{RES}	240 ohm unit calibration resolution	—	10	ohm	
R_{KEEP}	Keeper circuit resistance, V_{in}=0 or VDD_DDR	110	175	kohm	
I_{IN}	Input current (no PU/PD), V_{in}=0V or VDD_DDR	-2.5	2.5	uA	

2.2.5 LVD and POR operating requirements
(view resource)

I didn't find any LVD/POR specs for iMX6UL. Do we have any LVD for Ultra?

2.2.6 EMC radiated emissions operating behaviors
(view resource)

Table 7. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15-50	TBD	dBuV	1
V_{RE2}	Radiated emissions voltage, band 2	50-150	TBD	dBuV	
V_{RE3}	Radiated emissions voltage, band 3	150-500	TBD	dBuV	
V_{RE4}	Radiated emissions voltage, band 4	500-1000	TBD	dBuV	
V_{RE_IEC}	IEC level	0.15-1000	L	-	2, 3

1. Determined according to IEC Standard 61967-1, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions and IEC Standard 61967-2, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method.
3. IEC Level Maximums: M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV

2.2.7 Designing with radiated emissions in mind
(view resource)

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

(view resource)

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF
C_{IN_DDR}	Input capacitance: DDR pins	—	7	pF
C_{IN_TAMPER}	Input capacitance: ~~DDR~~ pins	—	7	pF

2.3 Power consumption and power mode transitions
(view resource)

2.3.1 Power mode transition operating behaviors
(view resource)

All specifications except t_{POR} in the following table assume this clock configuration:

- Core, cache and NIC clocks = 300 MHz
- AXBS-Lite and DMA clock = 150 MHz
- IP Bus clock = 75 MHz

Table 9. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	[L:] After a POR event, amount of time from the point ONOFF negates to execution of the first instruction across the operating temperature range of the chip.	—	—	TBD	µs	
	SLEEP → RUN	—	—	TBD	µs	
	Partial STOP → RUN	—	—	TBD	µs	
	STOP → RUN	—	—	TBD	µs	

2.3.2 Power consumption operating behaviors
(view resource)

The current parameters in the table below are derived from code executing a while(1) loop from on-chip SRAM1, unless otherwise noted.

The IDD typical values represent the statistical mean at 25°C, and the IDD maximum values for RUN, WAIT, STOP, Partial STOP, and SLEEP represent data collected at 125°C junction temperature unless otherwise noted. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 10. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
IDD_ADC33	Analog supply current	—	—	See note	mA	
IDD_RUN_SOC_IN	Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from SRAM1, VDD_SOC_CAP = 1.1V	—	163	TBD	mA	
IDD_RUN_HIGH_IN	Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from SRAM1, VDD_HIGH_CAP = ??	—	TBD	TBD	mA	
IDD_RUN_SOC_IN	Run mode current - all peripheral clocks enabled, CoreMark benchmark code executing from SRAM1, VDD_SOC_CAP = 1.1V	—	163	TBD	mA	
IDD_RUN_HIGH_IN	Run mode current - all peripheral clocks enabled, CoreMark benchmark code executing from SRAM1, VDD_HIGH_CAP = ??	—	TBD	TBD	mA	
IDD_RUN_SOC_IN	Run mode current - all peripheral clocks disabled, while(1) code executing from SRAM1, VDD_SOC_CAP = 1.1V	—	163	TBD	mA	
IDD_RUN_HIGH_IN	Run mode current - all peripheral clocks disabled, while(1) code executing from SRAM1, VDD_HIGH_CAP = ??	—	TBD	TBD	mA	
IDD_RUN_SOC_IN	Run mode current - all peripheral clocks enabled, while(1) code executing from SRAM1, VDD_SOC_CAP = 1.1V	—	163	TBD	mA	
IDD_RUN_HIGH_IN	Run mode current - all peripheral clocks enabled, while(1) code executing from SRAM1, VDD_HIGH_CAP = ??	—	TBD	TBD	mA	
IDD_RUN_DDR	Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from LPDDR2	—	TBD	TBD	mA	
IDD25_RUN_DDR	Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from LPDDR2	—	TBD	TBD	mA	
IDD18_RUN_DDR	Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from LPDDR2	—	TBD	TBD	mA	
IDD_WAIT_SOC_IN	Wait mode high frequency current - all peripheral clocks disabled, VDD_SOC_CAP = 1.1V	—	TBD	TBD	mA	

Table continues on the next page...

Table 10. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
IDD_WAIT_HIGH_IN	Wait mode high frequency current - all peripheral clocks disabled, VDD_HIGH_CAP = ??	—	TBD	TBD	mA	
IDD_WAIT_SOC_IN	Wait mode low frequency current - all peripheral clocks disabled, VDD_SOC_CAP = 1.1V	—	TBD	TBD	mA	
IDD_WAIT_HIGH_IN	Wait mode low frequency current - all peripheral clocks disabled, VDD_HIGH_CAP = ??	—	TBD	TBD	mA	
IDD_PSTOP_SOC_IN	Partial STOP mode high frequency current - all peripheral clocks disabled, VDD_SOC_CAP = 1.1V	—	TBD	TBD	mA	
IDD_PSTOP_HIGH_IN	Partial STOP mode high frequency current - all peripheral clocks disabled, VDD_HIGH_CAP = ??	—	TBD	TBD	mA	
IDD_PSTOP_SOC_IN	Partial STOP mode low frequency current - all peripheral clocks disabled, VDD_SOC_CAP = 1.1V	—	TBD	TBD	mA	
IDD_PSTOP_HIGH_IN	Partial STOP mode low frequency current - all peripheral clocks disabled, VDD_HIGH_CAP = ??	—	TBD	TBD	mA	
IDD_STOP_SOC_IN	STOP mode, VDD_SOC_CAP = 1.0V	—	TBD	TBD	mA	
IDD_STOP_HIGH_IN	STOP mode, VDD_HIGH_CAP = ??	—	TBD	TBD	mA	
IDD_SLEEP_SOC_IN	SLEEP mode, SOC power gated	—	0	0	mA	
IDD_SLEEP_HIGH_IN	STOP mode, SOC power gated	—	0	0	mA	

2.3.3 Diagram: Typical IDD_RUN operating behavior (view resource)

The following data was measured under these conditions:

- System PLL enabled for all frequencies ?? and up. System PLL disabled for 24 MHz. All other PLLs disabled?
- No GPIOs toggled

- Code execution from on-chip SRAM1 with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled

TBD

2.3.4 Low power mode peripheral current adders (view resource)

Table 11. Low power mode peripheral adders—typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN24MHz}$	[C:] 24 MHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 24 MHz IRC enabled.	TBD	TBD	TBD	TBD	TBD	TBD	µA
$I_{EREFSTEN24MHz}$	[C:] External 24 MHz crystal clock adder. Measured by entering STOP mode with the crystal enabled.	TBD	TBD	TBD	TBD	TBD	TBD	uA
$I_{EREFSTEN32KHz}$	[C:] External 32 kHz crystal clock adder. Measured by entering STOP mode with the crystal enabled.	TBD	TBD	TBD	TBD	TBD	TBD	nA
I_{LPTMR}	[C:] LPTMR peripheral adder measured by placing the device in STOP mode with internal 24MHz clock source and LPTMR configured for 1 minute match. Includes selected clock source power consumption.	TBD	TBD	TBD	TBD	TBD	TBD	nA
I_{LPIT}	[C:] LPIT peripheral adder measured by placing the device in STOP mode with internal 24MHz clock source and LPIT configured for 1 minute match. Includes selected clock source power consumption.	TBD	TBD	TBD	TBD	TBD	TBD	nA
I_{RTC}	[C:] RTC peripheral adder measured by placing the device in STOP mode with external 32 kHz crystal enabled and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	TBD	TBD	TBD	TBD	TBD	TBD	nA
I_{TPM}	[C:] TPM peripheral adder measured by placing the device in STOP mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.	TBD	TBD	TBD	TBD	TBD	TBD	nA

Table continues on the next page...

Table 11. Low power mode peripheral adders—typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I_{LPUART}	[C:] LPUART peripheral adder measured by placing the device in STOP mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.	TBD	TBD	TBD	TBD	TBD	TBD	nA
I_{LPSPI}	[C:] LPSPI peripheral adder measured by placing the device in STOP mode with ???. Includes selected clock source power consumption.	TBD	TBD	TBD	TBD	TBD	TBD	nA
I_{LPI2C}	[C:] LPI2C peripheral adder measured by placing the device in STOP mode with ???. Includes selected clock source power consumption.	TBD	TBD	TBD	TBD	TBD	TBD	nA
I_{ADC}	[C:] ADC peripheral adder combining the measured values at ??? by placing the device in STOP. ADC is configured for ??? and continuous conversions.	TBD	TBD	TBD	TBD	TBD	TBD	nA
I_{DAC}	[C:] DAC peripheral adder combining the measured values at ??? by placing the device in STOP. DAC is configured for ???	TBD	TBD	TBD	TBD	TBD	TBD	nA
I_{SAI}	[C:] SAI peripheral adder measured by placing the device in STOP mode with ???. Includes selected clock source power consumption.	TBD	TBD	TBD	TBD	TBD	TBD	nA

2.4 Switching specifications
(view resource)

2.4.1 Device clock specifications
(view resource)

Table 12. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Run mode					
f_{CORE}	M7 core clock	—	300	MHz	
f_{CACHE}	L2 cache clock	—	300	MHz	1
f_{NIC}	NIC crossbar clock	—	150	MHz	2

Table continues on the next page...

Table 12. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{DDR}	DDR core clock	—	300	MHz	
f_{AXBS}	AXBS-Lite crossbar clock	—	150	MHz	
f_{DMA}	DMA clock	—	150	MHz	
f_{IPBUS}	IP bus clock	—	75	MHz	
Partial STOP mode 1 (PLL enabled)					
f_{AXBS}	AXBS-Lite crossbar clock	—	75	MHz	
f_{DMA}	DMA clock	—	75	MHz	
f_{IPBUS}	IP bus clock	—	75	MHz	
Partial STOP mode 2 (PLL disabled, clocks from internal 24 MHz oscillator)					
f_{AXBS}	AXBS-Lite crossbar clock	—	24	MHz	
f_{DMA}	DMA clock	—	24	MHz	
f_{IPBUS}	IP bus clock	—	24	MHz	

1. f_{CACHE} must be equal to f_{CORE}.
2. f_{NIC} must be an even divide of f_{CORE}.

2.4.2 General switching specifications (view resource)

These general purpose specifications apply to all signals configured for GPIO, FlexIO, UART, FlexCAN, and timers.

Is this the best place to add specs for mode input pins? Or should that be its own section?

Table 13. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	[L:] GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	[L:] External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	3
	[L:] GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	4
	[O:] Port rise and fall time				5
	• Slew disabled	—			
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	10	ns	
	• 2.7 ≤ V_{DD} ≤ 3.6V		5	ns	
	• Slew enabled	—			

Table 13. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	• $1.71 \le V_{DD} \le 2.7V$	—	30	ns	
	• $2.7 \le V_{DD} \le 3.6V$		16	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
5. 25 pF load

2.5 Thermal specifications
(view resource)

2.5.1 Thermal operating requirements
(view resource)

Table 14. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

2.5.2 Thermal attributes
(view resource)

Board type	Symbol	Description	13 x13 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	TBD	°C/W	
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	TBD	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	TBD	°C/W	2

Table continues on the next page...

Board type	Symbol	Description	13 x13 MAPBGA	Unit	Notes
—	$R_{\theta JC}$	Thermal resistance, junction to case	TBD	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	TBD	°C/W	4
—	R_{JB}	Thermal characterization parameter, junction to package bottom outside center (natural convection)	TBD	°C/W	

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
3. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
4. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

3 Peripheral operating requirements and behaviors (view resource)

3.1 Core modules (view resource)

3.1.1 Debug trace timing specifications (view resource)

Table 15. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T1	TRACE_CLKOUT frequency of operation	—	166	MHz
T2	TRACE_CLKOUT period	1/T1	—	MHz
T3	Low pulse width	2	—	ns
T4	High pulse width	2	—	ns
T5	Clock and data rise time	—	1	ns
T6	Clock and data fall time	—	1	ns
T7	Data setup	2	—	ns
T8	Data hold	1	—	ns

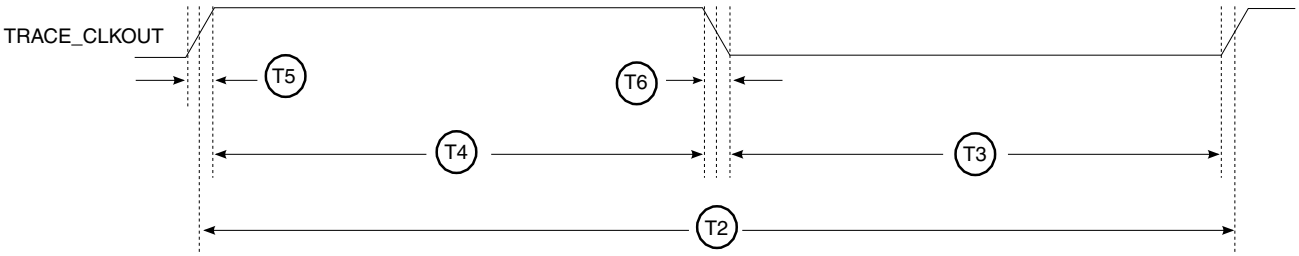


Figure 2. TRACE_CLKOUT specifications

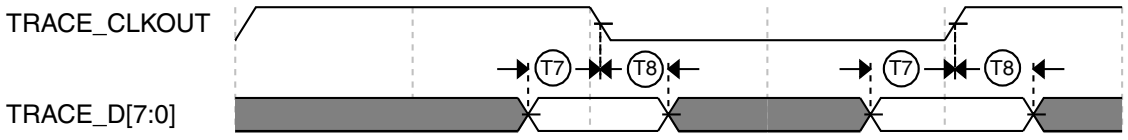


Figure 3. Trace data specifications

3.1.2 JTAG electricals
(view resource)

Table 16. JTAG electricals

Symbol	Description	Min.	Max.	Unit
J1	[O:] TCLK frequency of operation • Boundary Scan • JTAG and CJTAG	 0 0	 10 20	MHz MHz
J2	[O:] TCLK cycle period	1/J1	—	ns
J3	[O:] TCLK clock pulse width • Boundary Scan • JTAG and CJTAG	 50 25	 — —	 ns ns
J4	[O:] TCLK rise and fall times	—	3	ns
J5	[O:] Boundary scan input data setup time to TCLK rise	20	—	ns
J6	[O:] Boundary scan input data hold time after TCLK rise	1	—	ns
J7	[O:] TCLK low to boundary scan output data valid	—	25	ns
J8	[O:] TCLK low to boundary scan output high-Z	—	25	ns
J9	[O:] TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	[O:] TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	[O:] TCLK low to TDO data valid	—	19	ns
J12	[O:] TCLK low to TDO high-Z	—	19	ns

Table continues on the next page...

Table 16. JTAG electricals (continued)

Symbol	Description	Min.	Max.	Unit
J13	[O:] $\overline{\text{TRST}}$ assert time	100	—	ns
J14	[O:] $\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

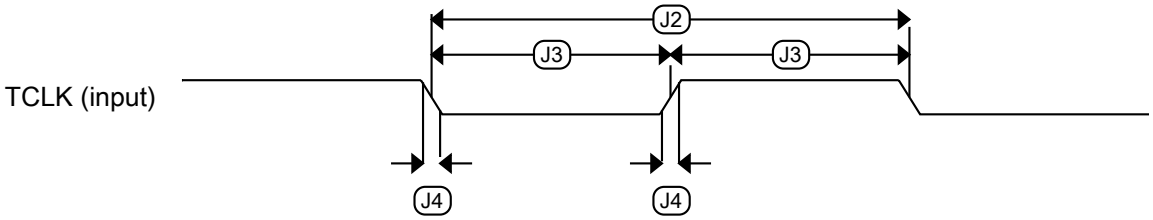


Figure 4. Test clock input timing

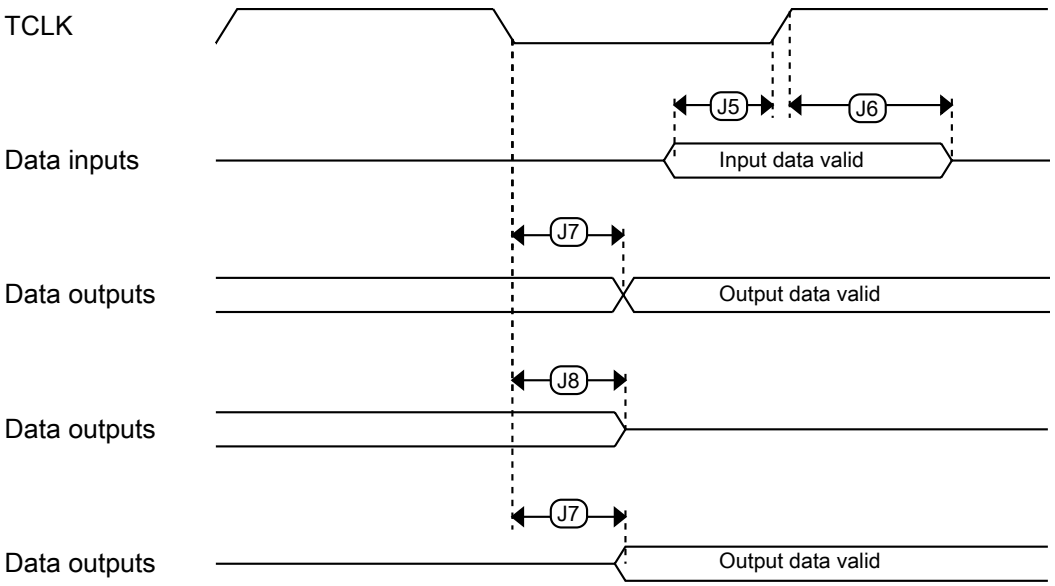


Figure 5. Boundary scan (JTAG) timing

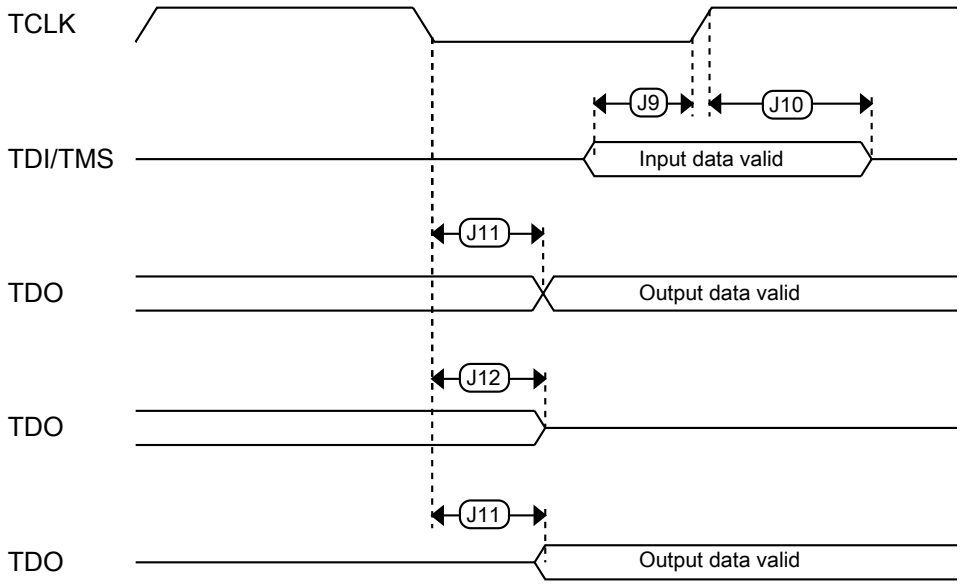


Figure 6. Test Access Port timing

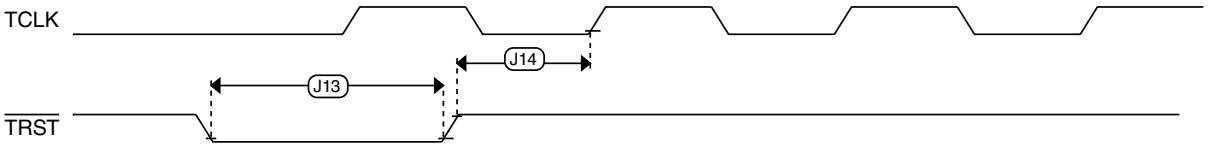


Figure 7. $\overline{\text{TRST}}$ timing

3.1.3 SWD electricals

(view resource)

Table 17. SWD electricals

Symbol	Description	Min.	Max.	Unit
S1	[O:] SWD_CLK frequency of operation • Serial wire debug	0	33	MHz
S2	[O:] SWD_CLK cycle period	1/S1	—	ns
S3	[O:] SWD_CLK clock pulse width • Serial wire debug	15	—	ns

Table continues on the next page...

Table 17. SWD electricals (continued)

Symbol	Description	Min.	Max.	Unit
S4	[O:] SWD_CLK rise and fall times	—	3	ns
S9	[O:] SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	[O:] SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	[O:] SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	[O:] SWD_CLK high to SWD_DIO high-Z	5	—	ns

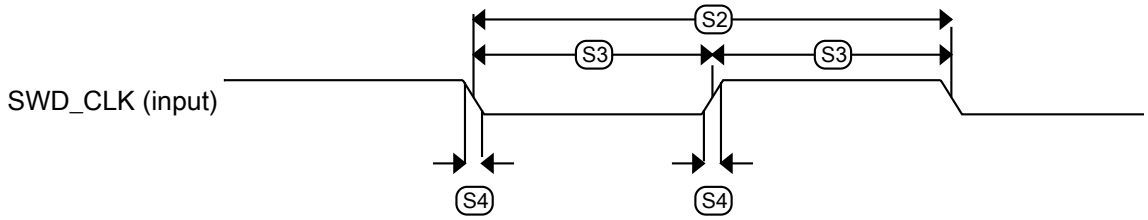


Figure 8. Serial wire clock input timing

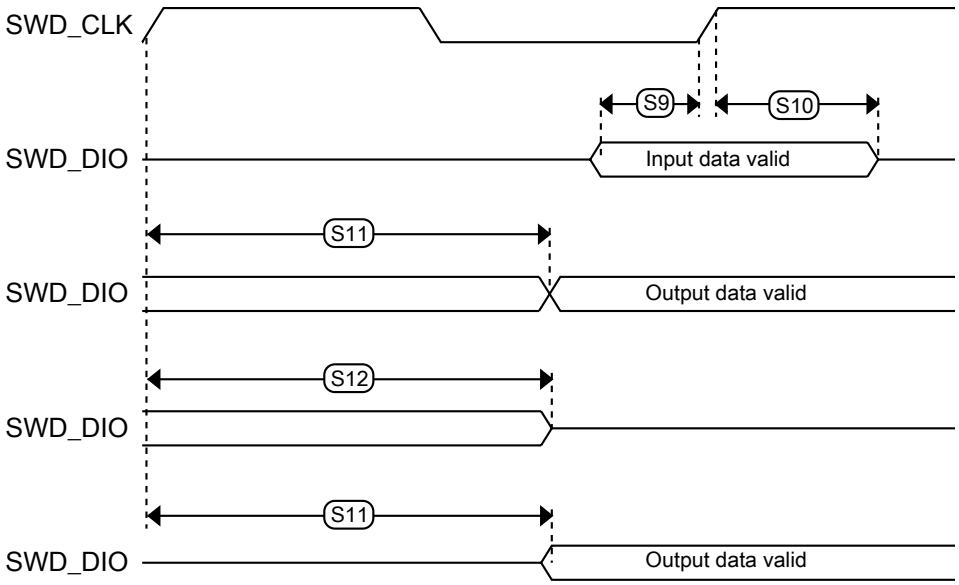


Figure 9. Serial wire data timing

3.2 Clocks and PLL specifications (view resource)

3.2.1 24 MHz or 19.2 MHz oscillator specifications (view resource)

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended to achieve a gain margin of 5.

Table 18. 24 MHz or 19.2 MHz external oscillator electrical characteristics

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
f_{osc}	[L:] Crystal oscillator range	—	—	24 or 19.2	—	MHz
f_{acc}	[L:] Input clock/oscillator accuracy	—	TBD	—	TBD	% or ppm
I_{osc}	Startup current	—	—	< 5	—	mA
t_{uposc}	[L:] Oscillator startup time	—	—	< 5	—	ms
C_{IN}	[O:] Input Capacitance	EXTAL and XTAL pins	—	9	—	pF
VIH	[P:][C:] XTAL pin input high voltage	—	0.8 x VDD_PLL[1]	—	VDD_PLL +0.3	V
VIL	[P:][C:] XTAL pin input low voltage	—	VSS -0.3	—	0.2 x VDD_PLL	V

1. VDD_PLL = 1.1V +/- 10%, T_A = -40 to +85 C, unless otherwise specified.

3.2.2 32 KHz Oscillator Specifications (view resource)

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a backup battery (VDD_SNVS_IN) or 1.1V derived from the VDD_HIGH_IN, so the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to a crude internal ring oscillator. The frequency range of this block is approximately 10–45 kHz. It highly depends on the process, voltage, and temperature.

The OSC32k runs from VDD_SNVS_CAP supply, which comes from the VDD_HIGH_IN/VDD_SNVS_IN. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDD_HIGH_IN range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell. For example, for Panasonic ML621:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, Rs = (3.2-2.5)/0.6 m = 1.17 k

Table 19. OSC32K Main Characteristics

	Notes	Min	Typ	Max
[L:] F_{OSC}	This frequency is nominal and determined mainly by the crystal selected.	—	32.768 KHz	—
[L:] F_{acc}	Input clock/crystal accuracy	TBD	—	TBD
[O:] Current consumption	The 4 µA is the consumption of the oscillator alone (OSC32k). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 µA when ring oscillator is inactive, 20 µA when the ring oscillator is running. Another 1.5 µA is drawn from vdd_rtc in the power_detect block. So, the total current is 6.5 µA on vdd_rtc when the ring oscillator is not running.	—	4 µA	—
[L:] Bias resistor	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.	—	14 MΩ	—
V_{IH}	RTC_XTAL pin input high voltage	0.8V	—	1.1V
V_{IL}	RTC_XTAL pin input low voltage	—	—	0.2V
Crystal Properties				
C_{LOAD}	Usually crystals can be purchased tuned for different C_{LOAD}s. This C_{LOAD}value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher C_{LOAD}will decrease oscillation margin, but increases current oscillating through the crystal	—	12.5 pF	—
ESR	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.	—	50 kΩ	—

3.2.3 Fast internal RC oscillator (24 MHz) electrical characteristics

(view resource)

This section describes a fast internal RC oscillator (FIRC).

Table 20. Fast internal oscillator electrical characteristics

Symbol	Parameter	Condition[1]	Value			
			Min	Typ	Max	Unit
f_{RCM}	RC oscillator high frequency	T_A= 25 °C, trimmed	—	24	—	MHz
I_{RCMRUN}	RC oscillator high frequency current in running mode	T_A= 25 °C, trimmed	—	55	—	µA
I_{RCMPWD}	RC oscillator high frequency current in power down mode	T_A= 25 °C	—	100	—	nA
RCMTRIM	RC oscillator precision after trimming of f_{RC}	T_A= 25 °C	-1	—	+1	%
RCMVAR	[P:][C:] RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high frequency configuration		-5		+5	%

1. VDD_SOC_CAP = 1.2 V, T_A = -40 to +85 °C, unless otherwise specified.

3.2.4 PLL specifications

(view resource)

3.2.4.1 PLL0 and PLL1 (480 MHz USB PLL) Electrical Parameters

(view resource)

Table 21. PLL0 and PLL1 Electrical Parameters

Parameter	Value
[P:][C:] Clock output range	480 MHz PLL output
Reference clock	24 or 19.2 MHz
[L:] Lock time	<383 reference cycles
[L:] Period jitter(p2p)	<140 ps
[L:] Duty Cycle	48.9%~51.7% PLL output

3.2.4.2 PLL2 (528 MHz System PLL) Electrical Parameters

(view resource)

Table 22. PLL2 Electrical Parameters

Parameter	Value
[P:][C:] Clock output range	528 MHz PLL output

Table continues on the next page...

Table 22. PLL2 Electrical Parameters (continued)

Parameter	Value
Reference clock	24 or 19.2 MHz
[L:] Lock time	<11250 reference cycles
[L:] Period jitter(p2p)	<140ps
[L:] Duty Cycle	48.9%~51.7% PLL output

3.2.4.3 PLL3 (Ethernet PLL) Electrical Parameters (view resource)

Table 23. PLL3 Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles
Cycle to cycle jitter (p2p)[1]	<400ps @ 50 MHz
Duty Cycle	45%~55%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out to an IO pad.

3.2.4.4 PLL4 (Audio PLL) Electrical Parameters (view resource)

Table 24. PLL4 Electrical Parameters

Parameter	Value
[P:] [C:] Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
[L:] Lock time	<11250 reference cycles
[L:] Long term jitter(RMS)	<42ps @1128MHz
[L:] Period jitter(p2p)[1]	<115ps@1128MHz
[L:] Duty Cycle	43%~57%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out on IO pad.

3.3 Memories and memory interfaces (view resource)

3.3.1 FlexSPI AC specifications

(view resource)

- All data is based on a negative edge data launch from the device and a positive edge data capture, as shown in the timing diagrams in this section.
- Measurements are with a load of 15pf (1.8V) and 35pf (3V) on output pins. Input slew: 1ns
- Timings assume a setting of 0x0000_000x for QuadSPI _SMPR register (see the reference manual for details).

The following table lists the QuadSPI delay chain read/write settings. Refer the device reference manual for register and bit descriptions.

Table 25. QuadSPI delay chain read/write settings

Mode	QuadSPI registers				Notes
	QuadSPI_MCR[DQS_EN]	QuadSPI_SOCCR[SOCCFG]	QuadSPI_MCR[SCLKCFG]	QuadSPI_FLSHCR[TDH]	
SDR	Yes	3Fh	5	No	Delay of 63 buffer and 64 mux
DDR	Yes	3Fh	1	2	Delay of 63 buffer and 64 mux
Hyperflash	RDS driven from Flash	0h	No	2	Delay of 1 mux

SDR mode

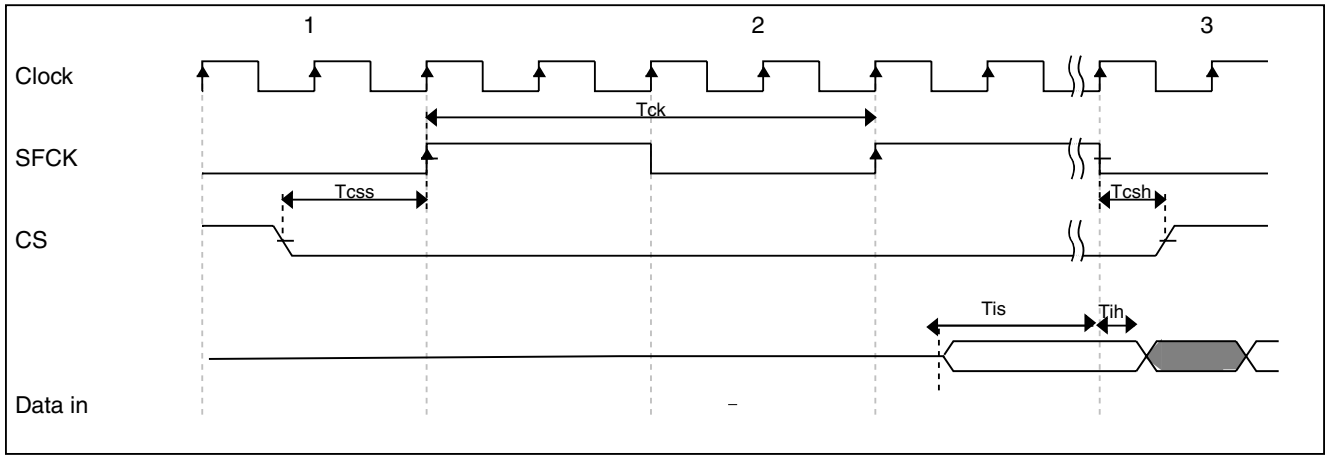


Figure 10. QuadSPI input timing (SDR mode) diagram

NOTE

- The below timing values are with default settings for sampling registers like QuadSPI_SMPR.

- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.
- The below timing are for a load of 15pf (1.8V) and 35pf (3V) or output pads
- All board delays need to be added appropriately
- Input hold time being negative does not have any implication or max achievable frequency

Table 26. QuadSPI input timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	[O:]Setup time for incoming data	4	-	ns
T_{ih}	[O:]Hold time requirement for incoming data	1.5	-	ns

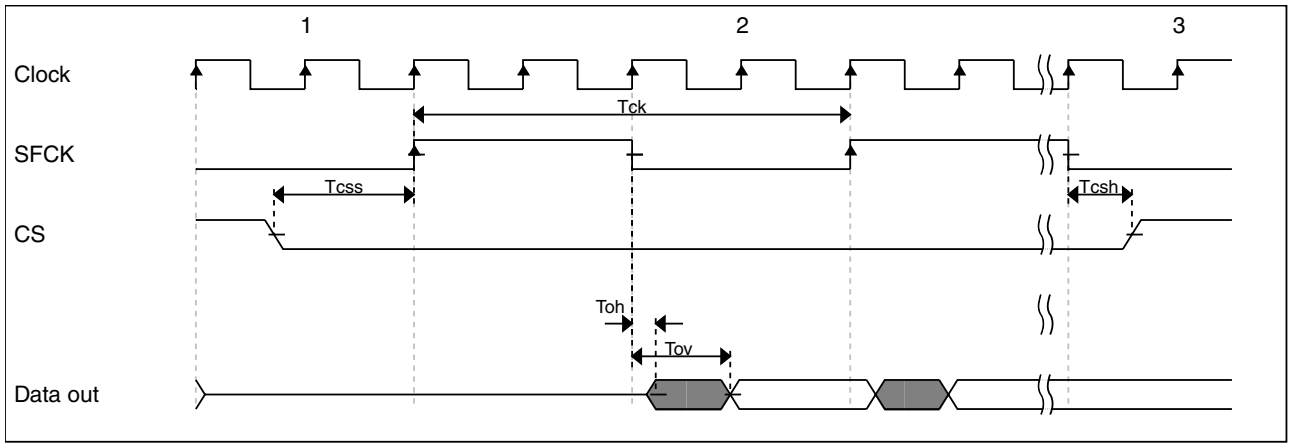


Figure 11. QuadSPI output timing (SDR mode) diagram

Table 27. QuadSPI output timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	[O:]Output Data Valid	-	2.8	ns
T_{oh}	[O:]Output Data Hold	-1.4	-	ns
T_{ck}	SCK clock period	-	100	MHz
T_{css}	Chip select output setup time	2	-	ns
T_{csh}	Chip select output hold time	-1	-	ns

NOTE

For any frequency setup and hold specifications of the memory should be met.

DDR Mode

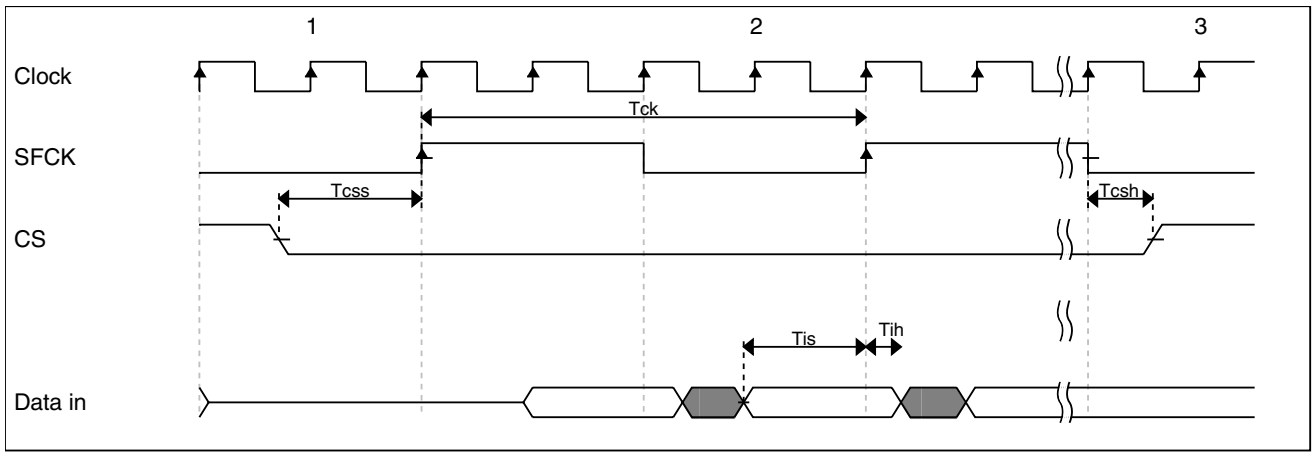


Figure 12. QuadSPI input timing (DDR mode) diagram

NOTE

- Numbers are for a load of 15pf (1.8V) and 35pf (3V)
- The numbers are for setting of hold condition in register QuadSPI_SMPR[DDRSNP]

Table 28. QuadSPI input timing (DDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	[O:]Setup time for incoming data	4 (Without learning)	-	ns
		1 (With learning)		
T_{ih}	[O:]Hold time requirement for incoming data	1.5	-	ns

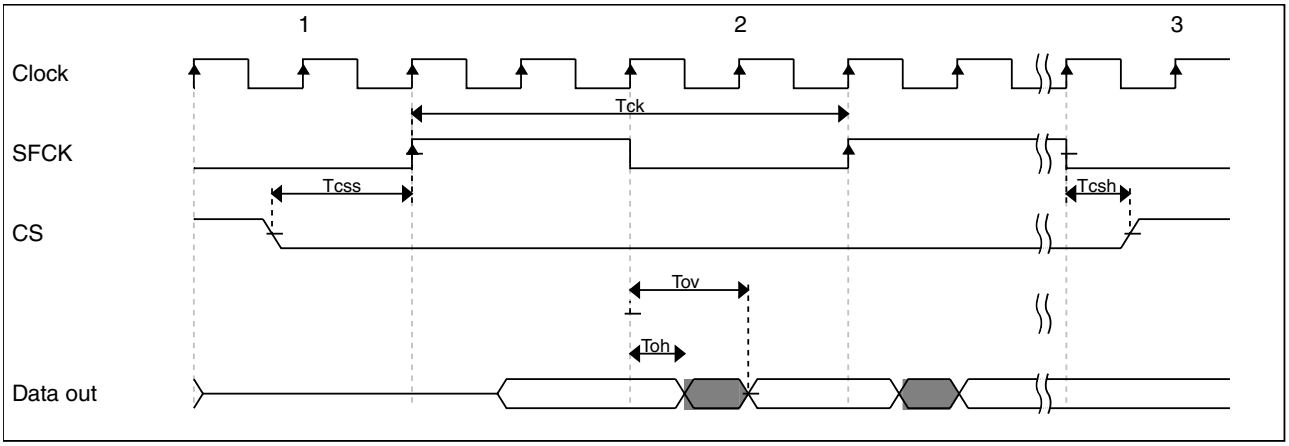


Figure 13. QuadSPI output timing (DDR mode) diagram

Table 29. QuadSPI output timing (DDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	[O:]Output Data Valid	-	4.5	ns
T_{oh}	[O:]Output Data Hold	1.5	-	ns
T_{ck}	SCK clock period	-	75 (with learning)	MHz
		-	45 (without learning)	
T_{css}	Chip select output setup time	2	-	Clk(sck)
T_{csh}	Chip select output hold time	-1	-	Clk(sck)

Hyperflash mode

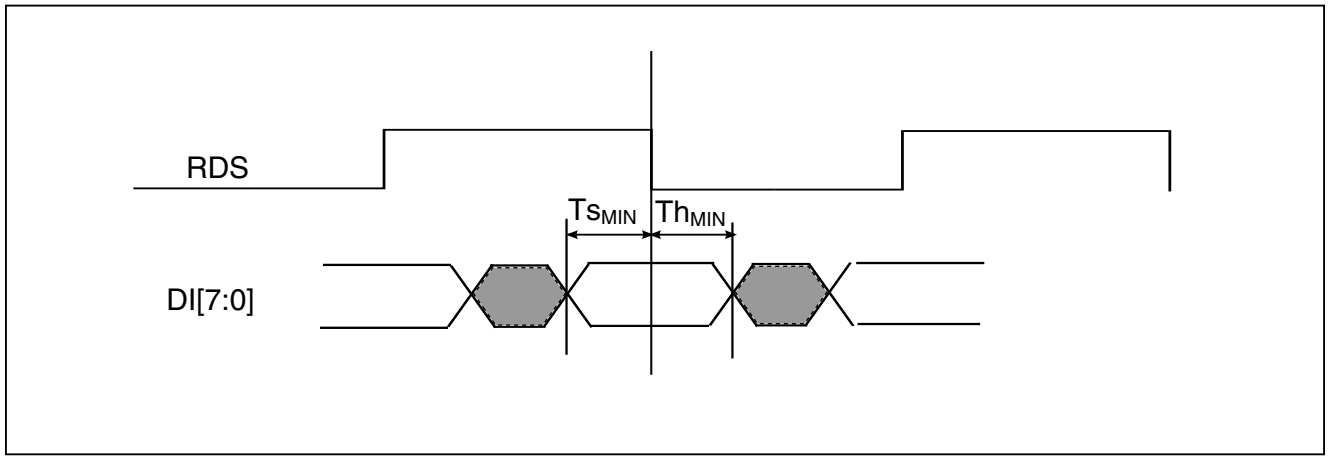


Figure 14. QuadSPI input timing (Hyperflash mode) diagram

Table 30. QuadSPI input timing (Hyperflash mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
Ts_{MIN}	[O:]Setup time for incoming data	2	-	ns
Th_{MIN}	[O:]Hold time requirement for incoming data	2	-	ns

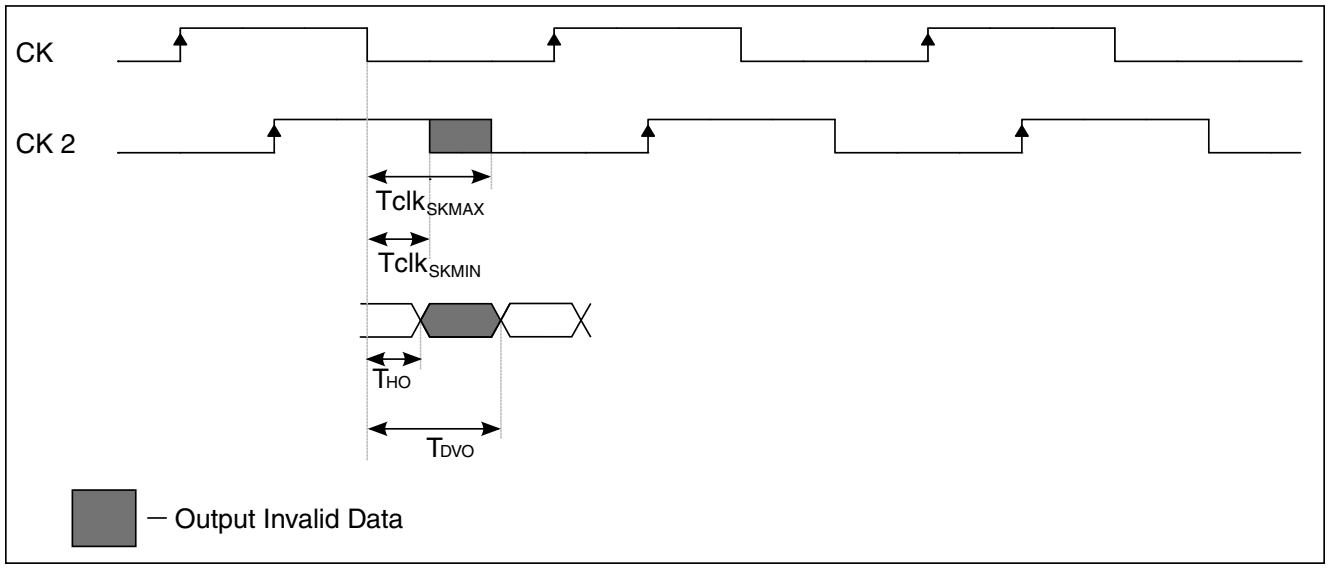


Figure 15. QuadSPI output timing (Hyperflash mode) diagram

Table 31. QuadSPI output timing (Hyperflash mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
Tdv_{MAX}	[O:]Output Data Valid	-	4.3	ns

Table continues on the next page...

Table 31. QuadSPI output timing (Hyperflash mode) specifications (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Tho	[O:]Output Data Hold	1.3	-	ns
$Tclk_{SKMAX}$	Ck to Ck2 skew max	-	T/4 + 0.5	ns
$Tclk_{SKMIN}$	Ck to Ck2 skew min	T/4 - 0.5	-	ns

NOTE

Maximum clock frequency = 75 MHz.

3.3.2 LPDDR2 controller specifications (view resource)

The following timing numbers must be followed to properly latch or drive data onto the DDR memory bus. All timing numbers are relative to the DQS byte lanes.

Table 32. DDR controller — AC timing specifications

Symbol	Description	Min.	Max.	Unit	Notes
	[O:] Frequency of operation	—	300	MHz	1
t_{DDRCK}	[O:] Clock period	3.33	—	ns	
V_{IX-AC}	[O:] DDR_CLK and DDR_DQSn AC differential cross point voltage	DDR_VREF - 0.12	DDR_VREF + 0.12	V	
t_{DDRCKH}	[O:] DDR_CLK Pulse width high	0.45	0.55	t_{DDRCK}	2
t_{DDRCKL}	[O:] DDR_CLK Pulse width low	0.45	0.55	t_{DDRCK}	2
t_{CMV}	[O:] Address, DDR_CKE, $\overline{\text{DDR\_CAS}}$, $\overline{\text{DDR\_RAS}}$, $\overline{\text{DDR\_WE}}$, $\overline{\text{DDR\_CSn}}$ — output setup	—	1.5	ns	
t_{CMH}	[O:] Address, DDR_CKE, $\overline{\text{DDR\_CAS}}$, $\overline{\text{DDR\_RAS}}$, $\overline{\text{DDR\_WE}}$, $\overline{\text{DDR\_CSn}}$ — output hold	1.2	—	ns	
t_{DSS}	[L:] Write DDR_DQSn falling edge to DDR_CLK setup	0.2 x t_{DDRCK}	—	ns	
t_{DSH}	[L:] Write DDR_DQSn falling edge hold time from DDR_CLK	0.2 x t_{DDRCK}	—	ns	
t_{DS}	[L:] Write DDR_Dn and DDR_DMn setup time to DDR_DQSn	1.1	—	ns	
t_{DH}	[L:] Write DDR_Dn and DDR_DMn hold time after DDR_DQSn	1.1	—	ns	
t_{DQSQ}	[L:] Read DDR_DQSn to DDR_Dn skew	—	0.7	ns	
t_{QHS}	[L:] Read DDR_Dn hold skew factor	—	1	ns	

1. DDR data rate = 2 x DDR clock frequency

2. Pulse width high plus pulse width low cannot exceed min and max clock period.

3.3.3 SDRAM controller specifications (view resource)

Table 33. SDRAM Timing

NUM	Characteristic	Symbol	Mln	Max	Unit
	Frequency of operation	—	—	75	MHz
D0	Clock period	—	1/CLKOUT	—	ns [1]
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	—	9	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}		9	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	2	—	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	2	—	ns
D5	SDRAM read data valid to CLKOUT high (setup)	t_{DDVCH}	5	—	ns
D6	CLKOUT high to SDRAM read data invalid (hold)	t_{CHDDI}	1.5	—	ns
D7	CLKOUT high to SDRAM write data valid	t_{CHDDVW}	—	9	ns
D8[2]	CLKOUT high to SDRAM write data invalid	t_{CHDDIW}	1.5	—	ns

1. CLKOUT is same as FB_CLK, maximum frequency can be 75 MHz
2. D7 and D8 are for write cycles only.

The following figure shows an SDRAM read cycle.

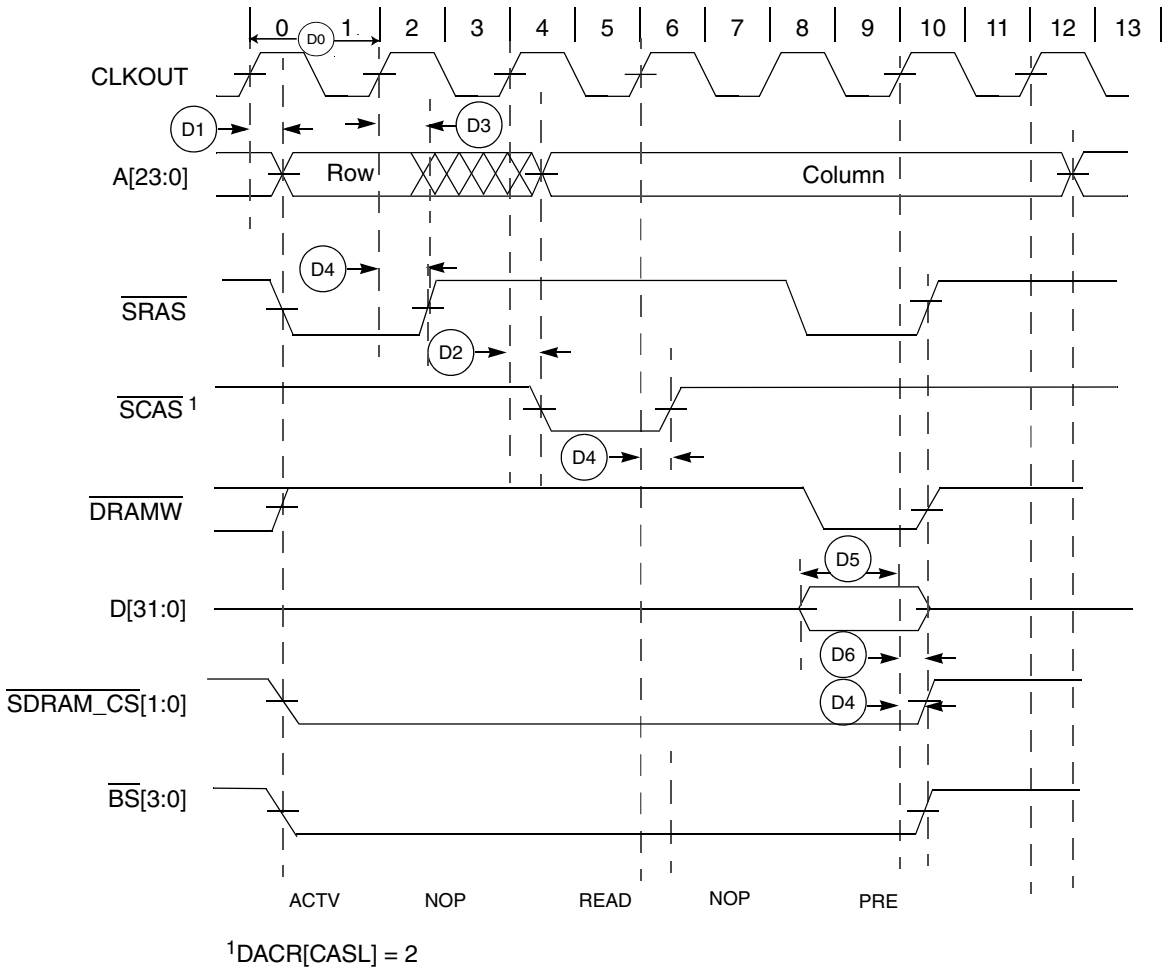


Figure 16. SDRAM read timing diagram

The following figure shows an SDRAM write cycle.

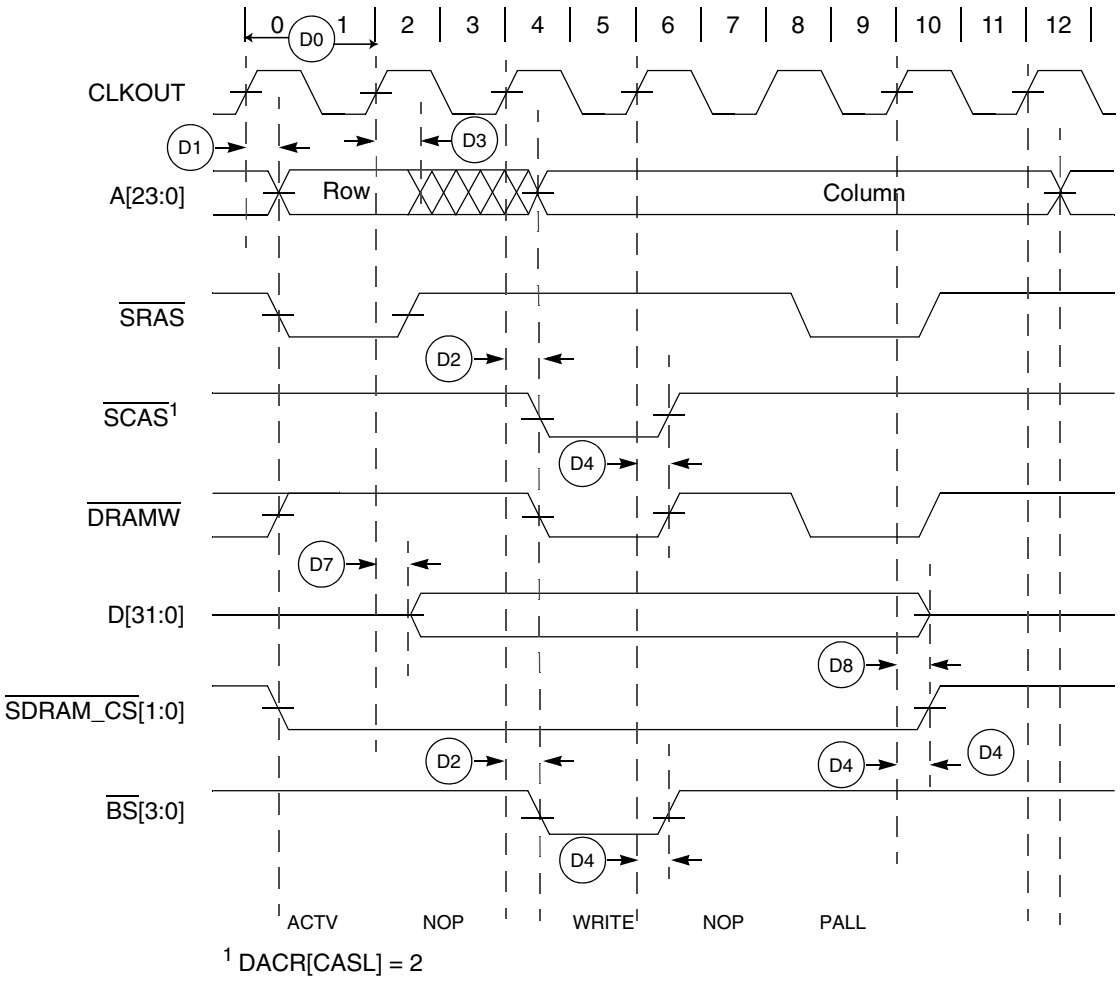


Figure 17. SDRAM write timing diagram

3.3.4 Flexbus switching specifications (view resource)

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 34. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Frequency of operation	—	75	MHz	
FB1	[O:] Clock period	1/FB_CLK	—	ns	
FB2	[P:] Address, data, and control output valid	—	7	ns	
FB3	[C:] Address, data, and control output hold	1	—	ns	1
FB4	[P:] Data and $\overline{\text{FB\_TA}}$ input setup	3.5	—	ns	2
FB5	[C:] Data and $\overline{\text{FB\_TA}}$ input hold	0	—	ns	3

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_BE}}$/BWE*n*, $\overline{\text{FB\_CS}}$*n*, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$, $\overline{\text{FB\_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB\_TS}}$.
2. TA can be split into its own setup and hold specs if it has worse timing than the data lines.
3. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

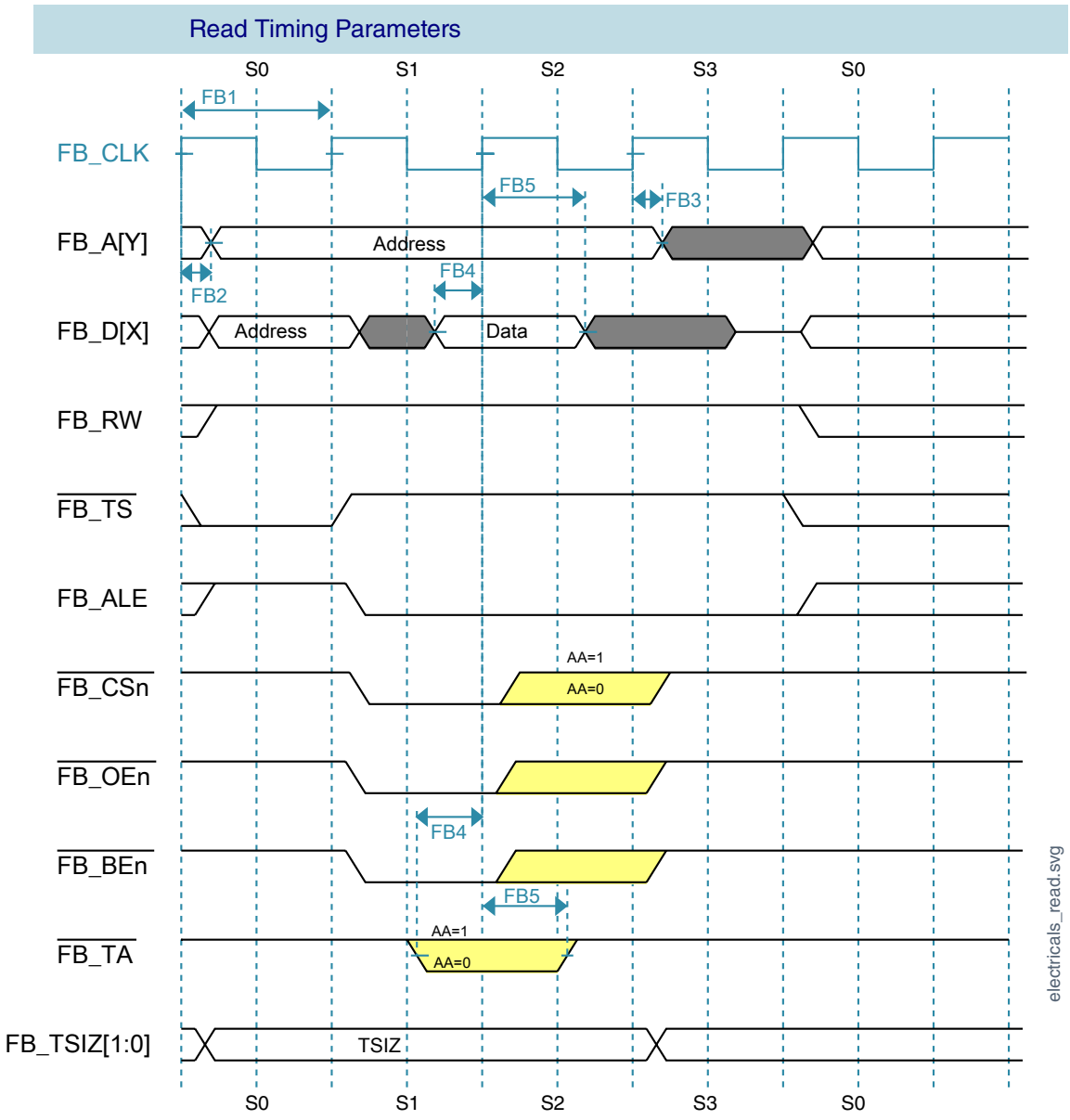


Figure 18. FlexBus read timing diagram

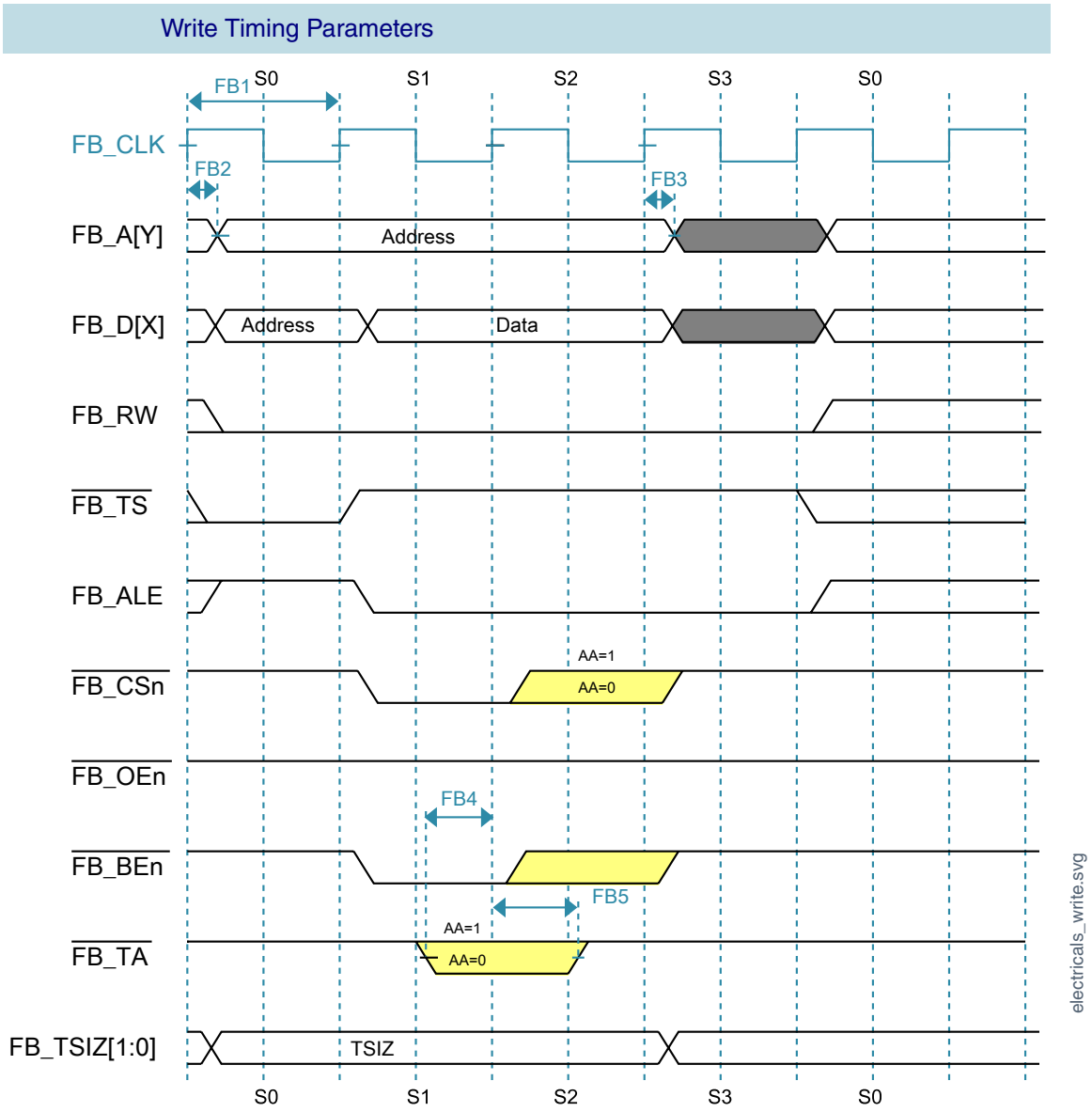


Figure 19. FlexBus write timing diagram

3.3.5 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) specifications

(view resource)

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4/4.41 (Dual Date Rate) timing and SDR104/50(SD3.0) timing.

3.3.5.1 SD/eMMC4.3 (Single Data Rate) specifications (view resource)

Table 35. SD/eMMC4.3 Interface Timing specifications

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
Card input clock				
SD1	Clock Frequency (Low Speed)	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	0	20/52	MHz
	Clock Frequency (Identification Mode)	100	400	kHz
SD2	Clock Low Time	7	—	ns
SD3	Clock High Time	7	—	ns
SD4	Clock Rise Time	—	3	ns
SD5	Clock Fall Time	—	3	ns
SDHC output/card inputs SDHC_CMD, SDHC_Dn (reference to SDHC_CLK)				
SD6	SDHC_CMD and SDHC_Dn output setup time to SDHC_CLK	-6.6	3.6	ns
SDHC input/card outputs SDHC_CMD, SDHC_Dn (reference to SDHC_CLK)				
SD7	SDHC_CMD and SDHC_Dn input setup time to SDHC_CLK	2.5	—	ns
SD8	SDHC_CMD and SDHC_Dn hold time from SDHC_CLK[1]	1.5	—	ns

1. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

The figure below depicts the timing of SD/eMMC4.3.

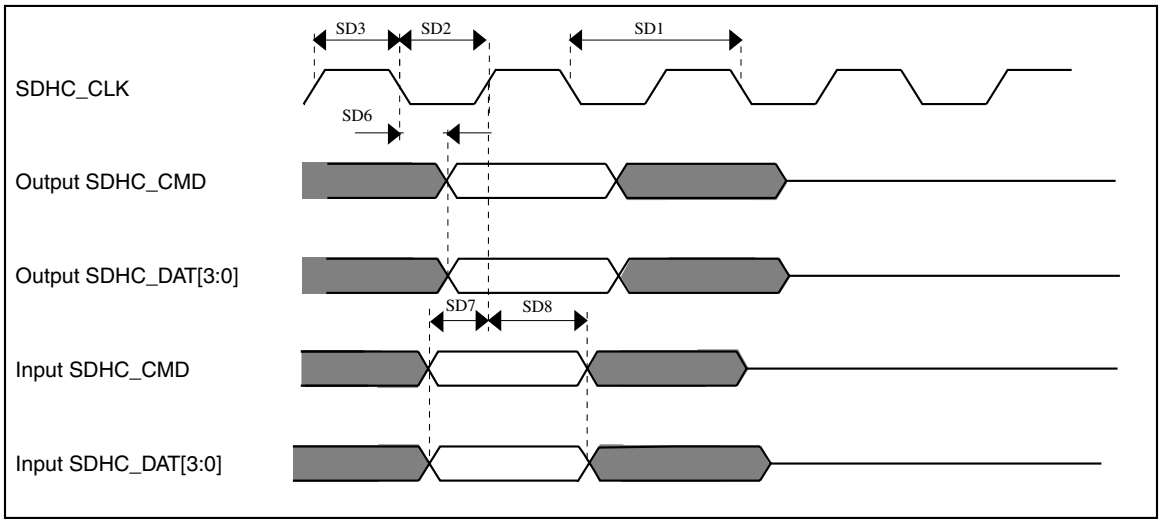


Figure 20. SD/eMMC4.3 timing

3.3.5.2 eMMC4.4/4.41 (Dual Data Rate) specifications

(view resource)

Table 36. SD/eMMC4.3 Interface Timing specifications

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
Card input clock				
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	0	52	MHz
	Clock Frequency (SD3.0 DDR)	0	50	MHz
SDHC output/card inputs SDHC_CMD, SDHC_Dn (reference to SDHC_CLK)				
SD2	SDHC_CMD and SDHC_Dn output valid time to SDHC_CLK	2.5	7.1	ns
SDHC input/card outputs SDHC_CMD, SDHC_Dn (reference to SDHC_CLK)				
SD3	SDHC_CMD and SDHC_Dn input setup time to SDHC_CLK	2.6	—	ns
SD4	SDHC_CMD and SDHC_Dn hold time from SDHC_CLK	1.5	—	ns

The figure below depicts the timing of eMMC4.4/4.41. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

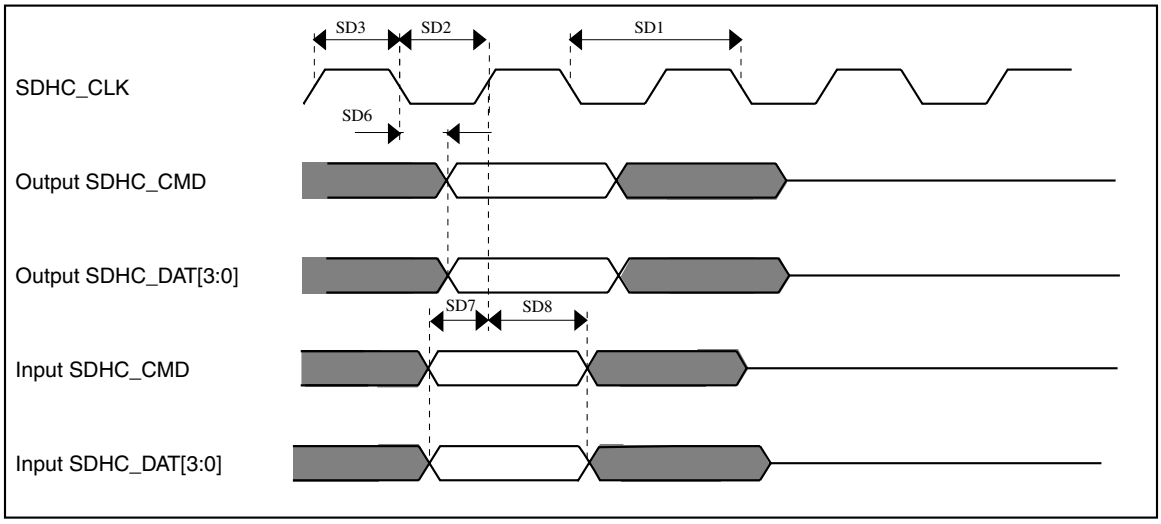


Figure 21. eMMC4.4/4.41 Timing

3.3.5.3 SDR50/SDR104 specifications

(view resource)

Table 37. SDR50/SDR104 Interface Timing specifications

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	1.95	V
Card input clock				

Table continues on the next page...

Table 37. SDR50/SDR104 Interface Timing specifications (continued)

Symbol	Description	Min.	Max.	Unit
SD1	Clock Frequency	0	20	MHz
SD2	Clock Frequency Period	5.0	—	ns
SD3	Clock Low Time	0.3 x SD2	0.7 x SD2	ns
SD4	Clock High Time	0.3 x SD2	0.7 x SD2	ns
SDHC output/card inputs SDHC_CMD, SDHC_Dn in SDR50 (reference to SDHC_CLK)				
SD5	SDHC_CMD and SDHC_Dn output valid time to SDHC_CLK	-3	1	ns
SDHC output/card inputs SDHC_CMD, SDHC_Dn in SDR104 (reference to SDHC_CLK)				
SD6	SDHC_CMD and SDHC_Dn output valid time to SDHC_CLK	-1.6	1	ns
SDHC input/card outputs SDHC_CMD, SDHC_Dn in SDR50 (reference to SDHC_CLK)				
SD7	SDHC_CMD and SDHC_Dn input setup time to SDHC_CLK	2.5	—	ns
SD8	SDHC_CMD and SDHC_Dn hold time from SDHC_CLK	1.5	—	ns
SDHC input/card outputs SDHC_CMD, SDHC_Dn in SDR104 (reference to SDHC_CLK)[1]				
SD7	Card output data window	0.5 x SD2	—	ns

1. Data window in SDR104 mode is variable.

The figure below depicts the timing of SDR50/104.

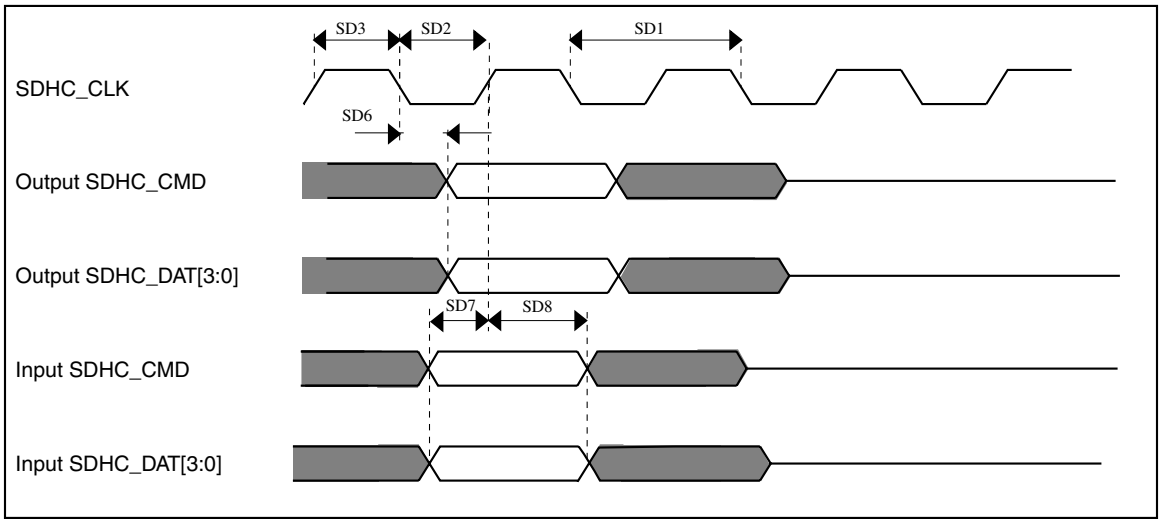


Figure 22. SDR50/SDR104 Timing

3.3.5.4 HS200 specifications

(view resource)

Table 38. HS200 Interface Timing specifications

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	1.95	V
Card input clock				
SD1	Clock Frequency	0	166	MHz
SD2	Clock Frequency Period	6	—	ns
SD3	Clock Low Time	0.3 x SD2	0.7 x SD2	ns
SD4	Clock High Time	0.3 x SD2	0.7 x SD2	ns
SDHC output/card inputs SDHC_CMD, SDHC_Dn (reference to SDHC_CLK)				
SD2	SDHC_CMD and SDHC_Dn output valid time to SDHC_CLK	-1.6	1	ns
SDHC input/card outputs SDHC_CMD, SDHC_Dn (reference to SDHC_CLK)[1]				
SD3	Card output data window	0.5 x SD2	—	ns

1. HS200 is for 8 bits while SDR104 is for 4 bits

The figure below depicts the timing of HS200.

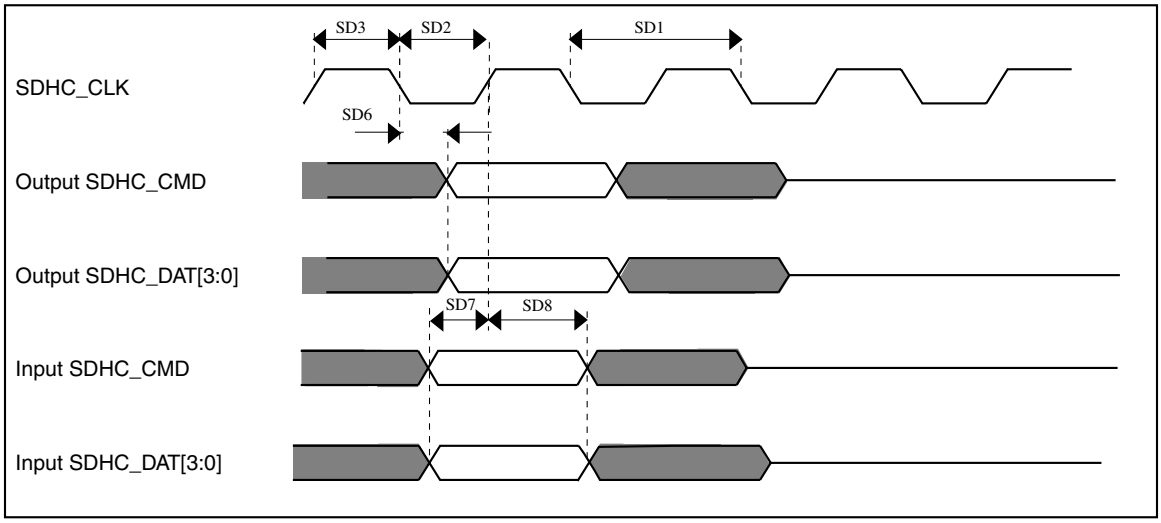


Figure 23. HS200 Timing

3.4 Analog

(view resource)

3.4.1 ADC electrical specifications

(view resource)

3.4.1.1 12-bit ADC operating conditions (view resource)

Table 39. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
VDD_ADC33	Supply voltage	Absolute	2.5	—	3.6	V	
ΔV_{DD_ADC33}	Supply voltage	Delta to V_{DD} (V_{DD} – VDD_ADC33)	-100	0	+100	mV	
ΔV_{SSAD}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSAD})	-100	0	+100	mV	
V_{REFH}	ADC reference voltage high		1.13	V_{DDAD}	VDD_ADC33	V	
V_{REFL}	ADC reference voltage low		V_{SSAD}	V_{SSAD}	V_{SSAD}	V	
V_{ADIN}	Input voltage	—	VREFL	—	VREFH	V	
C_{ADIN}	Input capacitance	8-bit / 10-bit / 12-bit modes	—	1.5	2	pF	
R_{ADIN}	Input series resistance	• ADLPC=0, ADHSC=1 • ADLPC=0, ADHSC=0 • ADLPC=1, ADHSC=0	— — —	5 12.5 25	7 15 30	kΩ kΩ kΩ	
R_{AS}	Analog source resistance	12-bit mode f_{ADCK} = 40MHz ADLSMP=0, ADSTS=10, ADHSC=1	—	—	1	kΩ	T_{samp} = 150ns[2]
f_{ADCK}	ADC conversion clock frequency	• ADLPC=0, ADHSC=1 12-bit mode • ADLPC=0, ADHSC=0 12-bit mode • ADLPC=1, ADHSC=0 12-bit mode	4 4 4	— — —	40 30 20	MHz MHz MHz	

1. Typical values assume VDD_ADC33 = 3.0 V, Temp = 25 °C, f_{ADCK} = 20 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. R_{AS} depends on the Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time vs R_{AS}

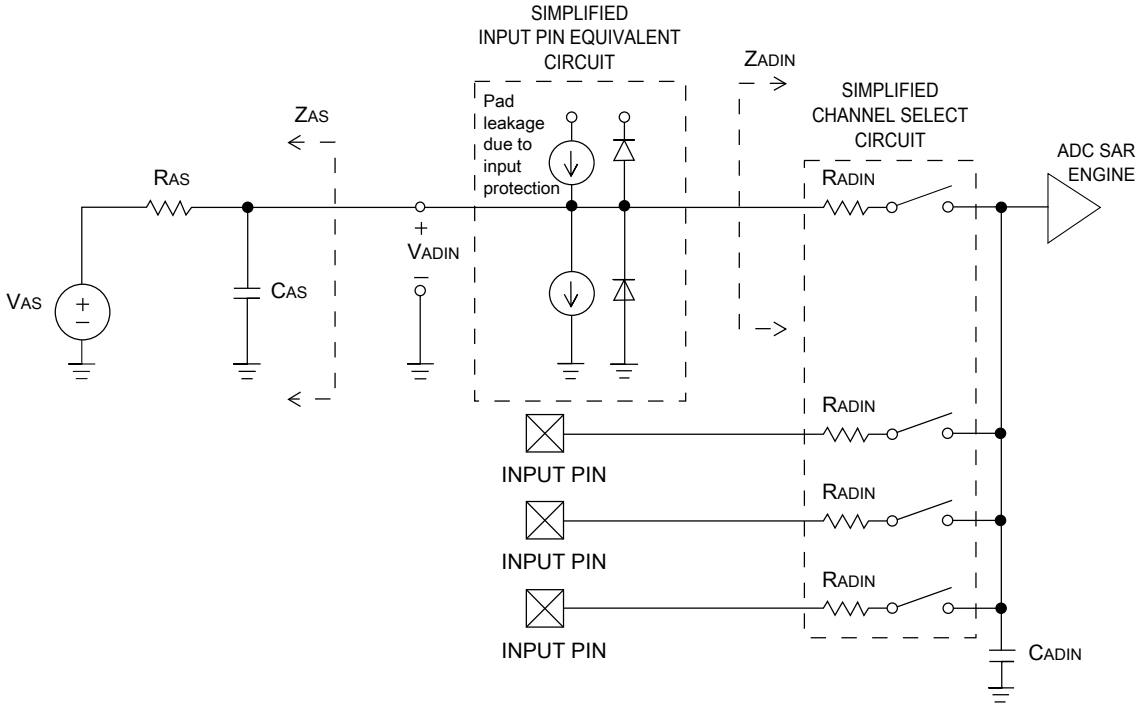


Figure 24. ADC input impedance equivalency diagram

3.4.1.2 12-bit ADC electrical characteristics (view resource)

Table 40. 12-bit ADC characteristics (V_{REFH} = V_{DD_ADC33}, V_{REFL} = V_{SSAD})

Symbol	Description	Conditions[1]	Min.	Typ.	Max.	Unit	Notes
I_{DDAD_ADC}	[L:] Supply current	• ADLPC = 1, ADHSC = 0 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	— — —	250 350 400	— — —	µA µA µA	ADLSMP = 0, ADSTS = 10, ADCO = 1
I_{DDAD_ADC}	[C:] Supply current	• Stop, reset, module off	—	0.01	0.8	µA	—
f_{ADACK}	ADC Asynchronous Clock Source	• ADHSC=0 • ADHSC=1	—	10 20	—	MHz MHz	t_{ADACK} = 1/ f_{ADACK}
C_{SAMP}	Sample Cycles	• ADLSMP=0, ADSTS=00 • ADLSMP=0, ADSTS=01 • ADLSMP=0, ADSTS=10	—	2 4 6 8 12 16	—	cycles	—

Table continues on the next page...

Table 40. 12-bit ADC characteristics (V_{REFH} = V_{DD_ADC33}, V_{REFL} = V_{SSAD}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.	Max.	Unit	Notes
		• ADLSMP=0, ADSTS=11 • ADLSMP=1, ADSTS=00 • ADLSMP=1, ADSTS=01 • ADLSMP=1, ADSTS=10 • ADLSMP=1, ADSTS=11		20 24			
C_{CONV}	Conversion Cycles	• ADLSMP=0, ADSTS=00 • ADLSMP=0, ADSTS=01 • ADLSMP=0, ADSTS=10 • ADLSMP=0, ADSTS=11 • ADLSMP=1, ADSTS=00 • ADLSMP=1, ADSTS=01 • ADLSMP=1, ADSTS=10 • ADLSMP=1, ADSTS=11	—	28 30 32 34 38 42 46 50	—	cycles	—
T_{CONV}	Conversion Time	• ADLSMP=0, ADSTS=00 • ADLSMP=0, ADSTS=01 • ADLSMP=0, ADSTS=10 • ADLSMP=0, ADSTS=11 • ADLSMP=1, ADSTS=00 • ADLSMP=1, ADSTS=01 • ADLSMP=1, ADSTS=10 • ADLSMP=1, ADSTS=11	—	0.7 0.75 0.8 0.85 0.95 1.05 1.15 1.25	—	µs	F_{adc} = 40 MHz

Table continues on the next page...

Table 40. 12-bit ADC characteristics (V_{REFH} = V_{DD_ADC33}, V_{REFL} = V_{SSAD}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.	Max.	Unit	Notes
TUE	[P:][C:] Total unadjusted error	• 12-bit mode • 10-bit mode • 8-bit mode	—	4.5 2 1.5	—	LSB	—
DNL	[P:][C:] Differential non-linearity	• 12-bit mode • 10-bit mode • 8-bit mode	—	1 0.5 0.2	—	LSB	—
INL	[P:][C:] Integral non-linearity	• 12-bit mode • 10-bit mode • 8-bit mode	—	2.6 0.8 0.3	—	LSB	—
E_{ZS}	Zero-scale error	• 12-bit mode • 10-bit mode • 8-bit mode	—	-0.3 -0.15 -0.15	—	LSB	—
E_{FS}	Full-scale error	• 12-bit mode • 10-bit mode • 8-bit mode	—	-2.5 -0.6 -0.3	—	LSB	—
ENOB	[L:] Effective number of bits	• 12-bit mode	10.1	10.7	—	Bits	—
SINAD	[L:] Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	—

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = VDD_ADC33

3.4.2 12-bit DAC electrical characteristics (view resource)

3.4.2.1 12-bit DAC operating requirements (view resource)

Table 41. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Typ	Max.	Unit	Notes
VDD_ADC33	[C:] Supply voltage	3.0	3.3	3.6	V	
ADC_VREFH	[C:] Reference voltage	2.5	3.3	VDD_ADC33	V	1
C_L	[O:] Output load capacitance	—		100	pF	2
I_L	[O:] Output load current	—		1	mA	

1. User will need to set up DACx_STATCTRL [DACRFS]=1 to select the valid ADC_VREFH reference. When DACx_STATCTRL [DACRFS]=0, the DAC reference is connected to an internal ground node and is not a valid voltage reference. Note that the DAC and ADC share the ADC_VREFH reference simultaneously.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

3.4.2.2 12-bit DAC operating behaviors
(view resource)

Table 42. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	[L:] Supply current — low-power mode	—	—	100	µA	
I_{DDA_DACHP}	[L:] Supply current — high-power mode	—	—	500	µA	
t_{DACLP}	[L:] Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	10	15	µs	
t_{DACHP}	[L:] Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	3	5	µs	1
$t_{CCDACLP}$	[L:] Code-to-code settling time (0xBF8 to 0xC08)	—	TBD	—	µs	1
	low-power mode	—	5	—		
	high-power mode	—	1	—		
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	[P:][C:] Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	[P:][C:] Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	3
V_{OFFSET}	Offset error	—	±0.4	±3, we are telling customers: ±0.8	%FSR	
E_G	Gain error	—	±0.1	±0.6	%FSR	4
PSRR	[L:] Power supply rejection ratio, V_{DDA} =3 V, T = 25 C		70		dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
A_C	Offset aging coefficient	—	—	100	µV/yr	
Rop	Output resistance load = 3 kΩ	—	—	250	Ω	Not Confirmed
SR	[L:] Slew rate -80h→ F7Fh→ 80h	—	TBD	TBD	V/µs	
	High power (SP_{HP})	—	1.7	3		
	Low power (SP_{LP})	—	0.3	0.6		

Table continues on the next page...

Table 42. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
CT	[L:] Channel to channel cross talk	—	70	—	dB	Not Confirmed

1. Settling within ±1 LSB
2. The INL is measured for 0+100mV to V_{DACR}−100 mV
3. The DNL is measured for 0+100mV to V_{DACR}−100 mV
4. Calculated by a best fit curve from V_{SS}+100 mV to V_{DACR}−100 mV

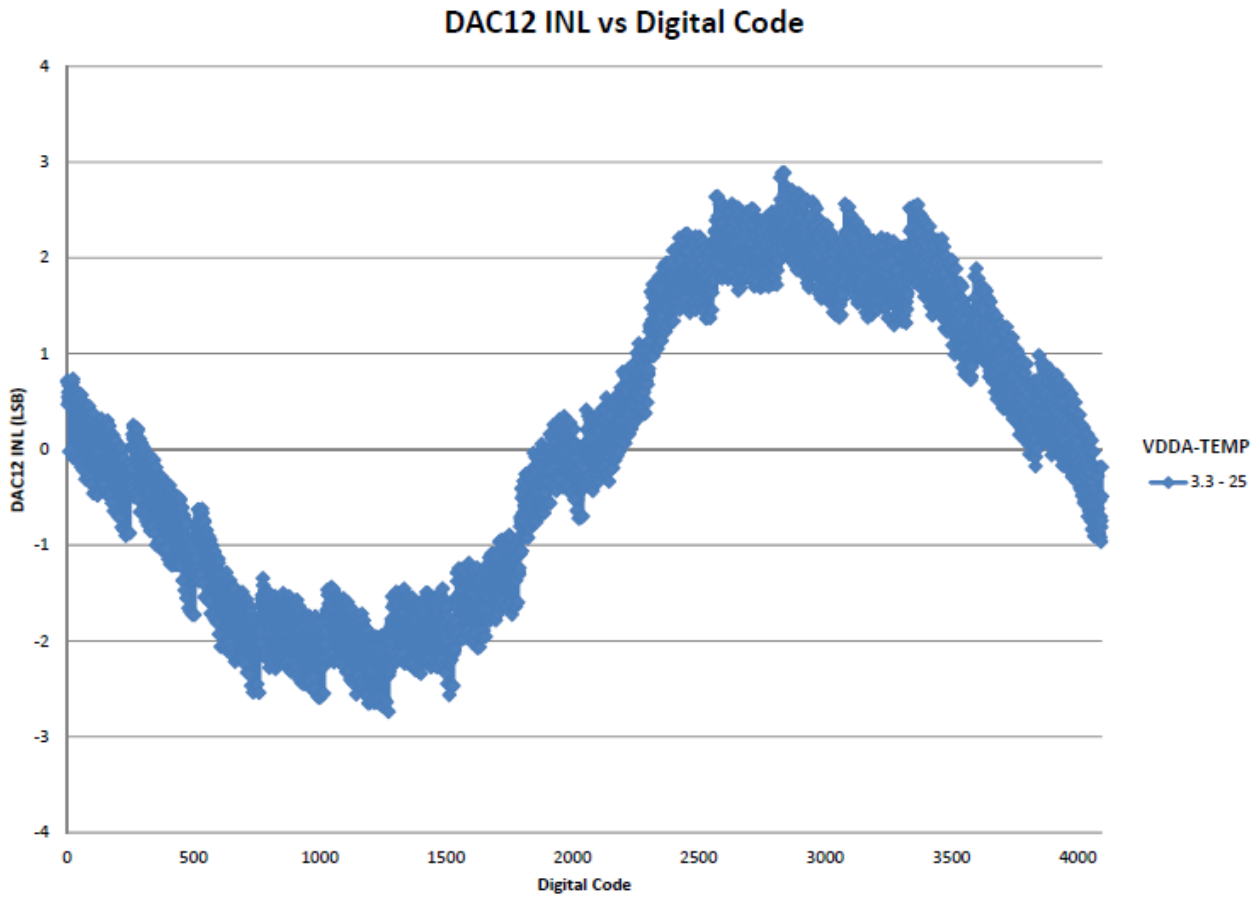


Figure 25. INL error vs. digital code

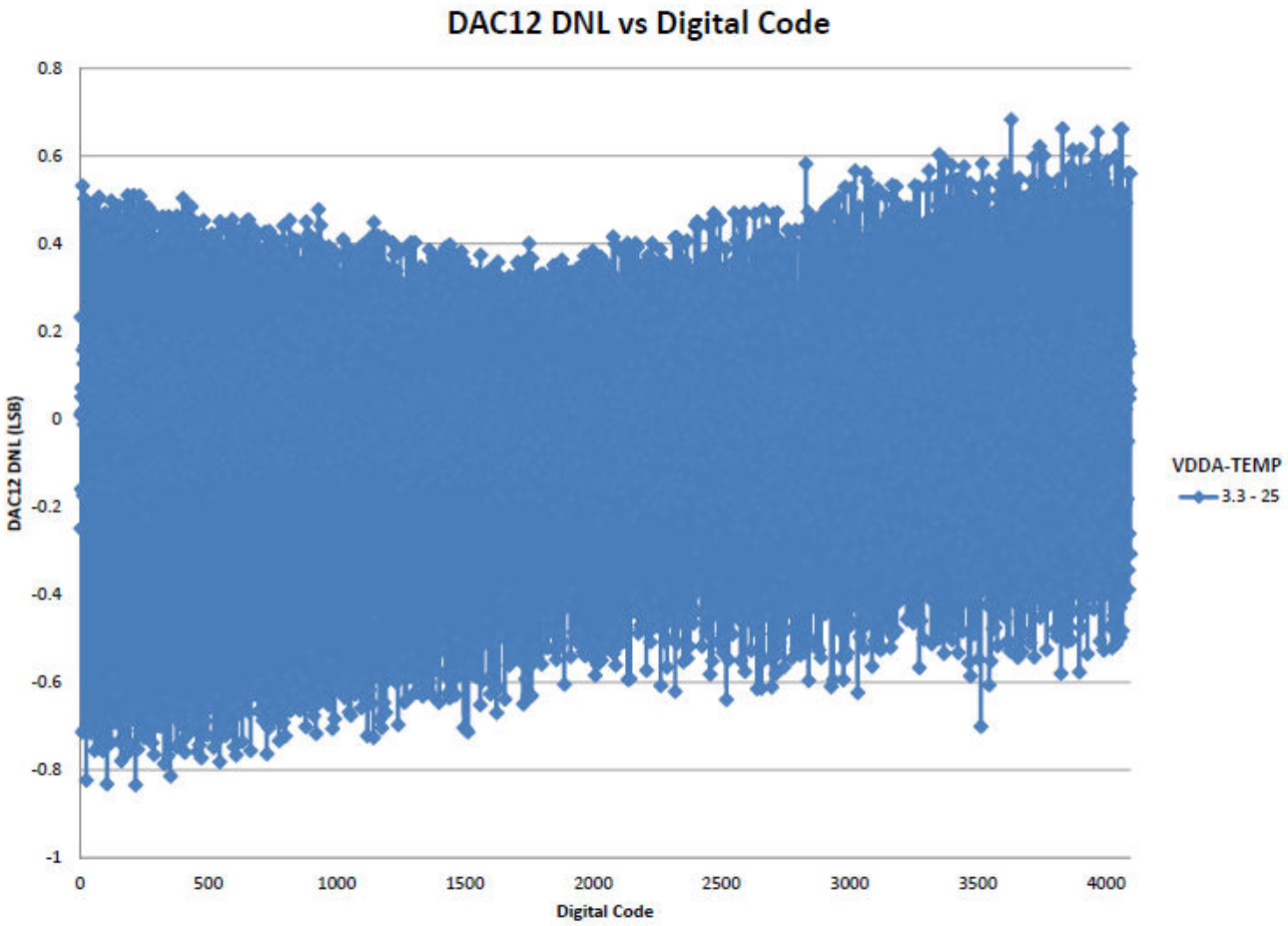


Figure 26. DNL error vs. digital code

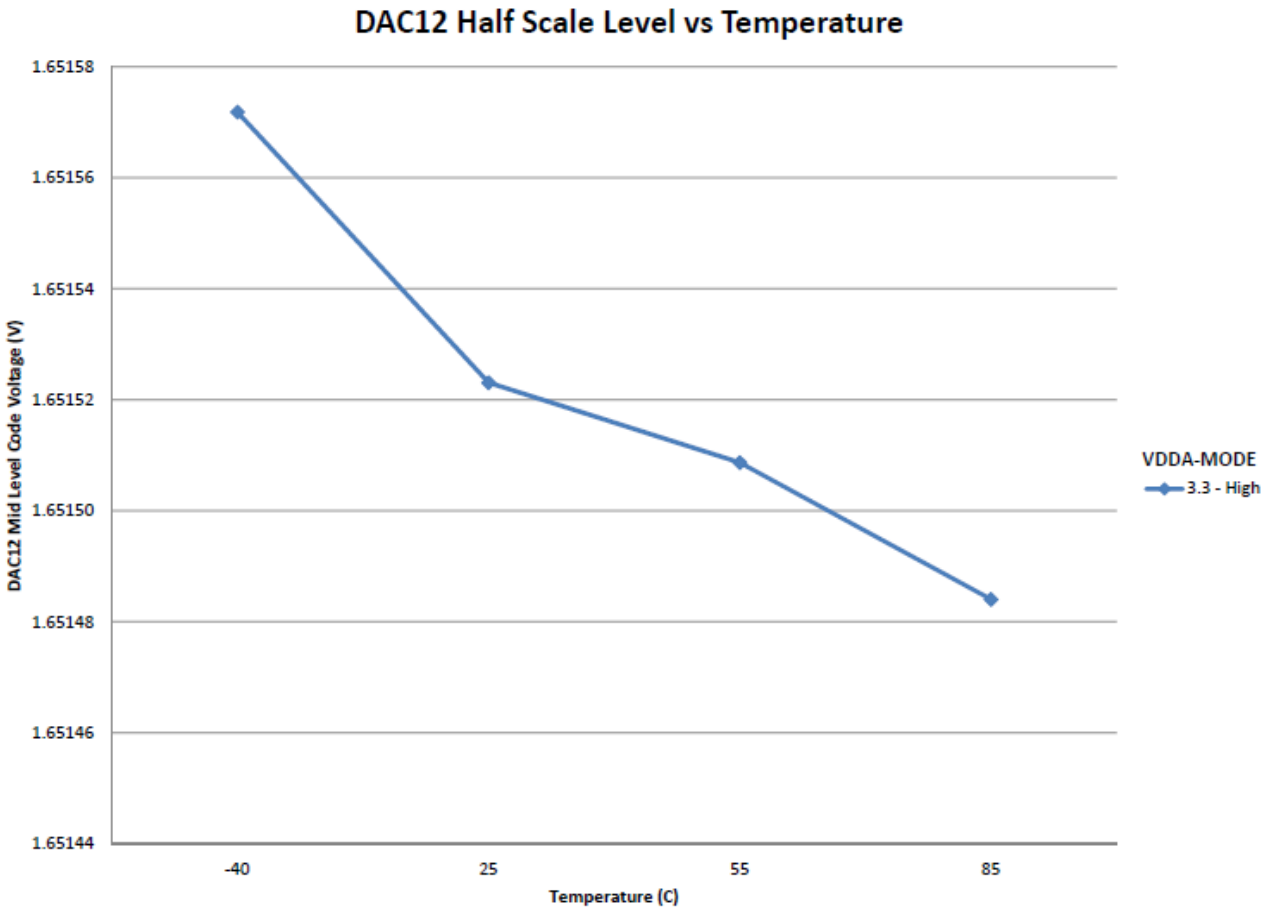


Figure 27. Offset at half scale vs. temperature

3.5 Timers
(view resource)

See General switching specifications.

3.6 Communication interfaces
(view resource)

3.6.1 LPUART switching specifications
(view resource)

See General switching specifications.

3.6.2 LPSPI switching specifications (view resource)

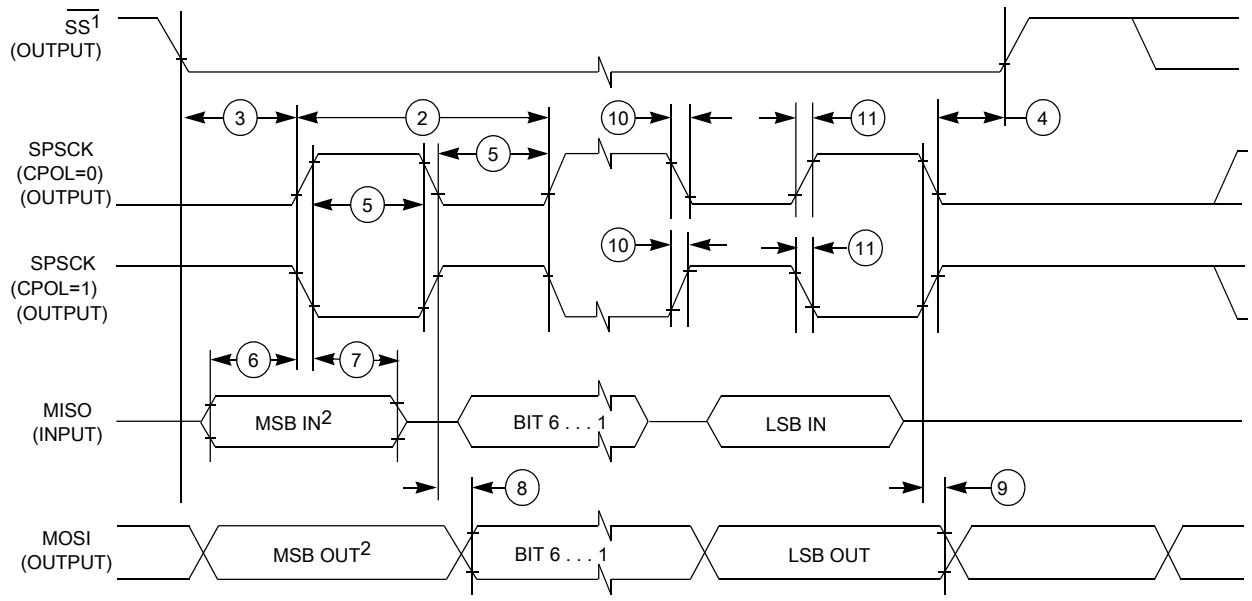
The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

Table 43. LPSPI master mode timing

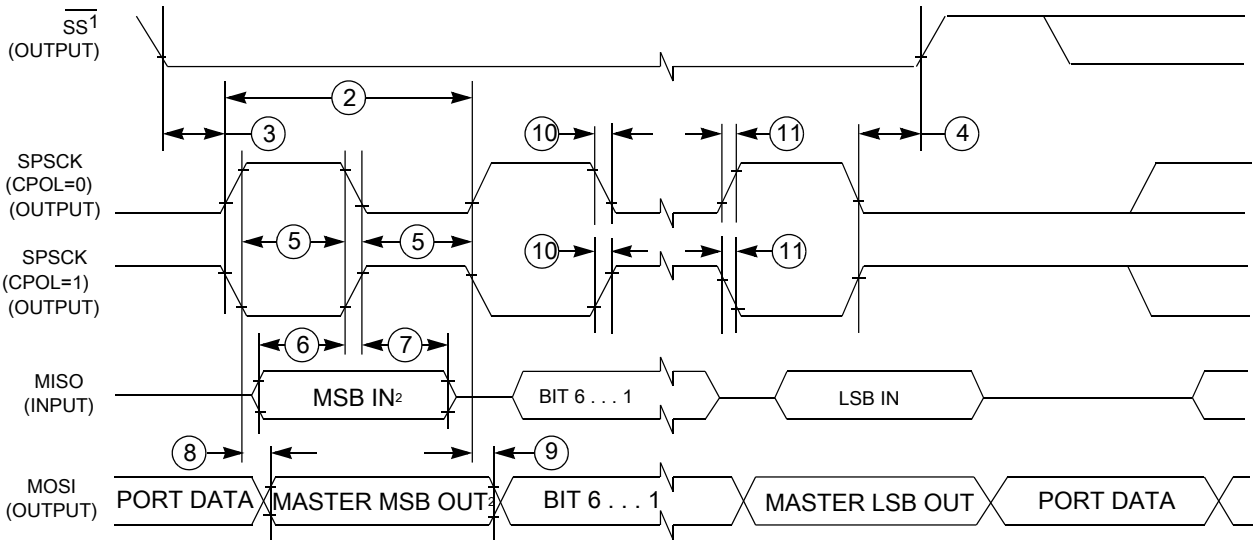
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation: LPSPI0-1 LPSPI2-3	— —	30 60	MHz MHz	1
2	t_{SPSCK}	SPSCK period	$1/f_{periph}$	$1/f_{periph}$	ns	
3	t_{Lead}	Enable lead time	1/2	—	t_{periph}	
4	t_{Lag}	Enable lag time	1/2	—	t_{periph}	2
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{SPSCK}/2 - 3$	$t_{SPSCK}/2$	ns	—
6	t_{SU}	Data setup time (inputs)	4	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	3	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—

1. The frequency of operation is also limited to a minimum of $f_{periph}/2048$ and a max of $f_{periph}/2$, where f_{periph} is the LPSPI peripheral functional clock.
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 28. LPSPI master mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 29. LPSPI master mode timing (CPHA = 1)

Table 44. LPSPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation: LPSPI0-1 LPSPI2-3	— —	15 30	MHz MHz	1

Table continues on the next page...

Table 44. LPSPI slave mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
2	t_{SPSCK}	SPSCK period	$1/f_{periph}$	$1/f_{periph}$	ns	
3	t_{Lead}	Enable lead time	1	—	t_{periph}	
4	t_{Lag}	Enable lag time	1	—	t_{periph}	2
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{SPSCK}/2$ - 5	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	8	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—

1. The frequency of operation is also limited to a minimum of $f_{periph}/2048$ and a max of $f_{periph}/4$, where f_{periph} is the LPSPI peripheral functional clock.
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

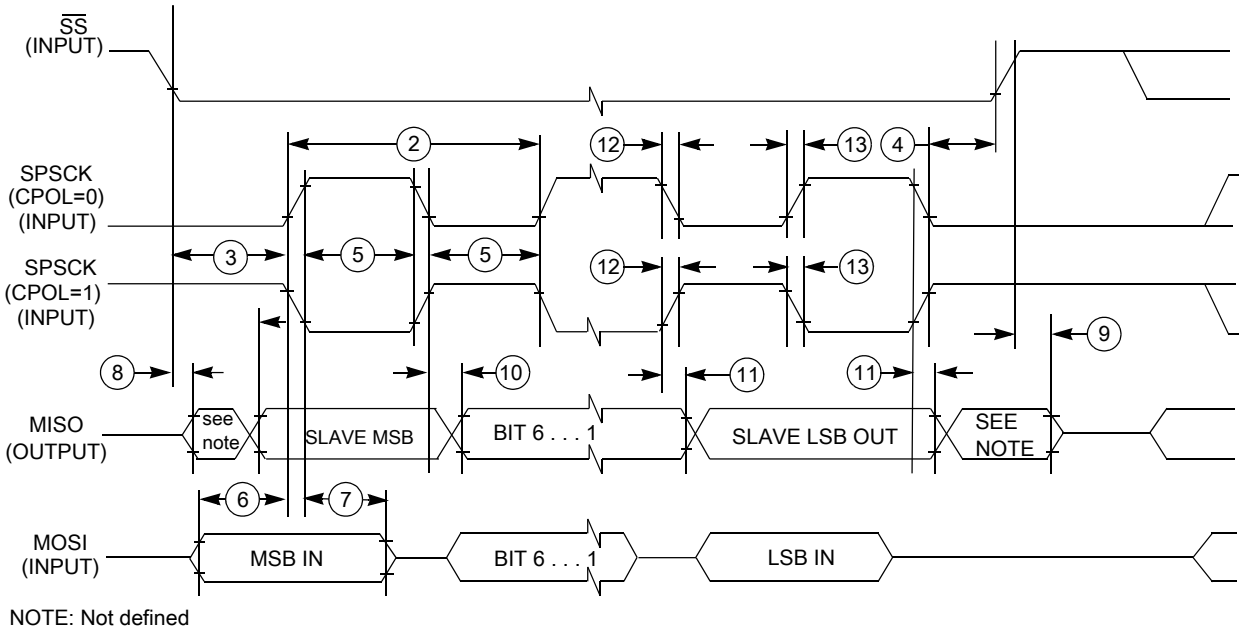


Figure 30. LPSPI slave mode timing (CPHA = 0)

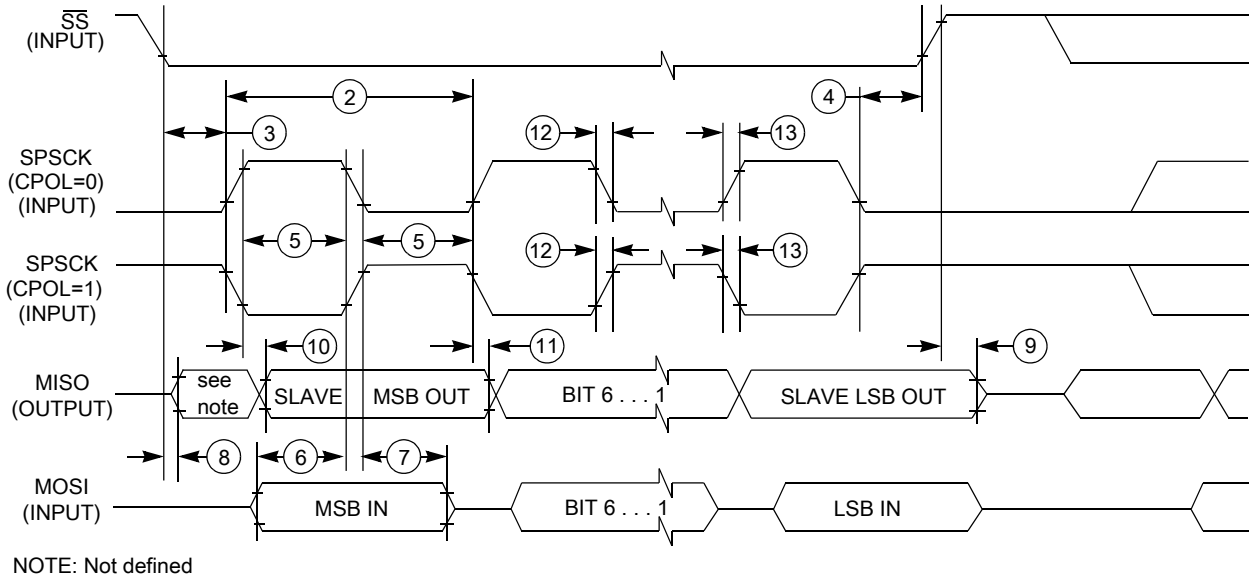


Figure 31. LPSPI slave mode timing (CPHA = 1)

3.6.3 Inter-Integrated Circuit Interface (I^2C) timing (view resource)

Table 45. I^2C timing (Standard, Fast, and Fast Plus modes)

Characteristic	Symbol	Standard Mode		Fast Mode		Fast-mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}	0	100	0	400	0	1000	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	0.26	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	0.5	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	0.26	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	0.26	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0	3.45	0	0.9[1]	0	—	µs
Data set-up time	t_{SU}; DAT	250	—	100[2]	—	50	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[4]	300	20 +0.1C_b[5]	120	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[3]	300	20 +0.1C_b[3]	120	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	0.26	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	0.5	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
4. C_b = total capacitance of the one bus line in pF.
5. C_b = total capacitance of the one bus line in pF.

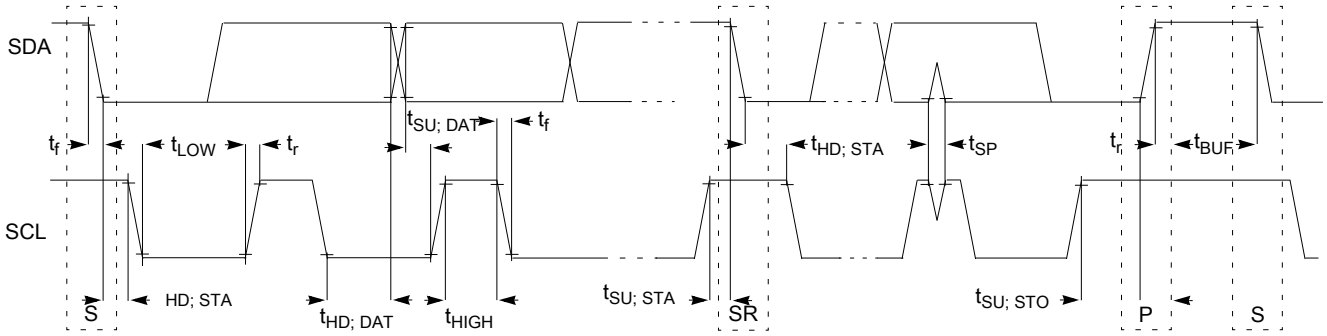


Figure 32. Timing definition for standard, fast, and fast plus devices on the I^2C bus

3.6.4 USB Full Speed Transceiver and High Speed PHY specifications

(view resource)

This section describes the High Speed USB PHY parameters. The high speed PHY is capable of full and low speed signaling as well.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification with the amendments below.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification

  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

USBn_VBUS pins are used as a detector function. Pins are 5V tolerant and complies with the above specifications without needing any external voltage division components.

3.6.5 ULPI timing specifications (view resource)

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in the following table. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB1_ULPI_CLK pin.

Table 46. ULPI timing specifications

Num	Description	Min.	Typ.	Max.	Unit
	USB1_ULPI_CLK operating frequency	—	60	—	MHz
	USB1_ULPI_CLK duty cycle	—	50	—	%
U1	USB1_ULPI_CLK clock period	—	16.67	—	ns
U2	Input setup (control and data)	5	—	—	ns
U3	Input hold (control and data)	1	—	—	ns
U4	Output valid (control and data)	—	—	9.5	ns
U5	Output hold (control and data)	1	—	—	ns

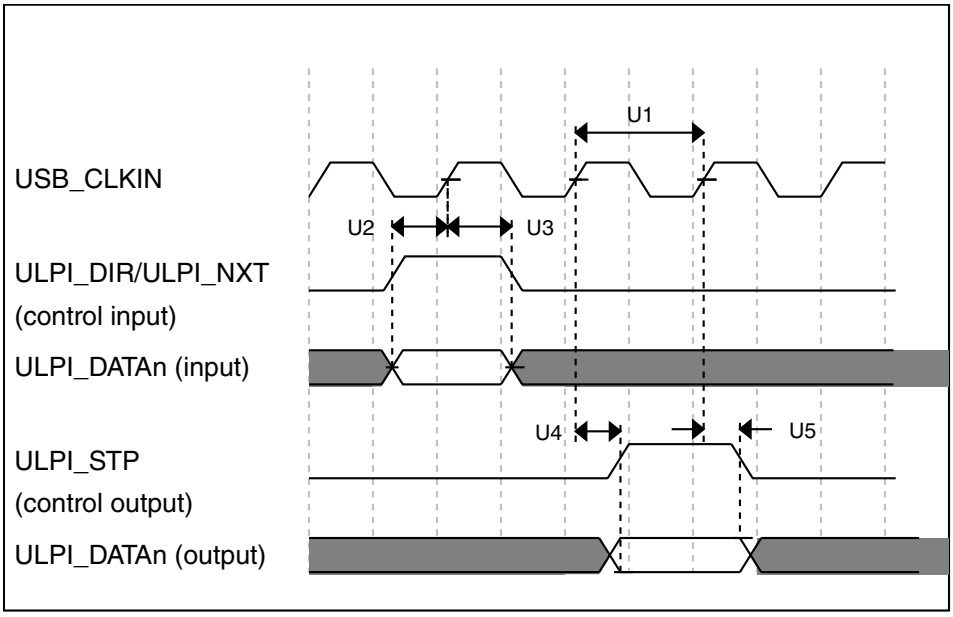


Figure 33. ULPI timing diagram

3.6.6 uSDHC switching specifications (view resource)

See Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) specifications.

3.6.7 Ethernet switching specifications (view resource)

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

These specs are from Pioneer. Is it true that timing is standardized for MII/RMII, so the timing specs should not vary from device to device?

3.6.7.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 47. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	Operating Voltage	2.7	3.6	V
—	RXCLK frequency	—	25	MHz
MII1	[O:] RXCLK pulse width high	35%	65%	RXCLK period
MII2	[O:] RXCLK pulse width low	35%	65%	RXCLK period
MII3	[O:] RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	[O:] RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	[O:] TXCLK frequency	—	25	MHz
MII5	[O:] TXCLK pulse width high	35%	65%	TXCLK period
MII6	[O:] TXCLK pulse width low	35%	65%	TXCLK period
MII7	[O:] TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	[O:] TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

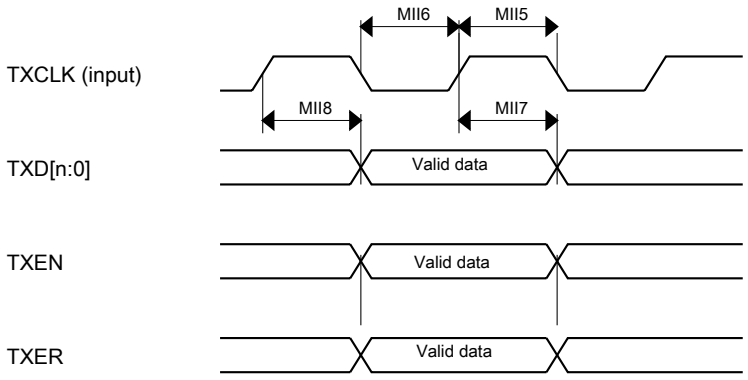


Figure 34. RMII/MII transmit signal timing diagram

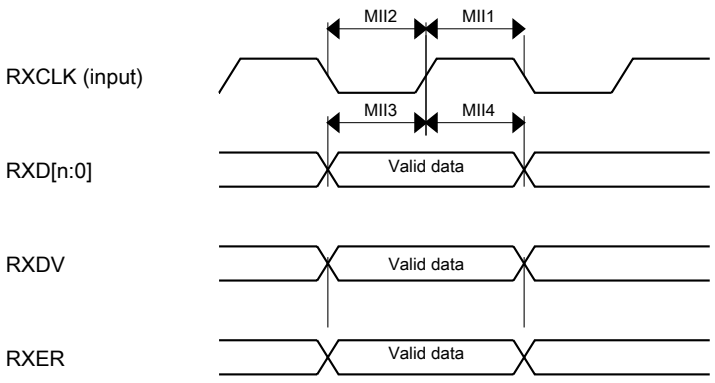


Figure 35. RMII/MII receive signal timing diagram

3.6.7.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 48. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	Operating Voltage	2.7	3.6	
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	[O:] RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	[O:] RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	[O:] RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	[O:] RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	[O:] RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	[O:] RMII_CLK to TXD[1:0], TXEN valid	—	15.4	ns

3.6.8 CAN switching specifications (view resource)

See General switching specifications.

3.6.9 EMV SIM specifications

(view resource)

Each EMV SIM module interface consists of a total of five pins.

The interface is designed to be used with synchronous Smart cards, meaning the EMV SIM module provides the clock used by the Smart card. The clock frequency is typically 372 times the Tx/Rx data rate; however, the EMV SIM module can also work with CLK frequencies of 16 times the Tx/Rx data rate.

There is no timing relationship between the clock and the data. The clock that the EMV SIM module provides to the Smart card is used by the Smart card to recover the clock from the data in the same manner as standard UART data exchanges. All five signals of the EMV SIM module are asynchronous with each other.

There are no required timing relationships between signals in normal mode. The smart card is initiated by the interface device; the Smart card responds with Answer to Reset. Although the EMV SIM interface has no defined requirements, the ISO/IEC 7816 defines reset and power-down sequences (for detailed information see ISO/IEC 7816).

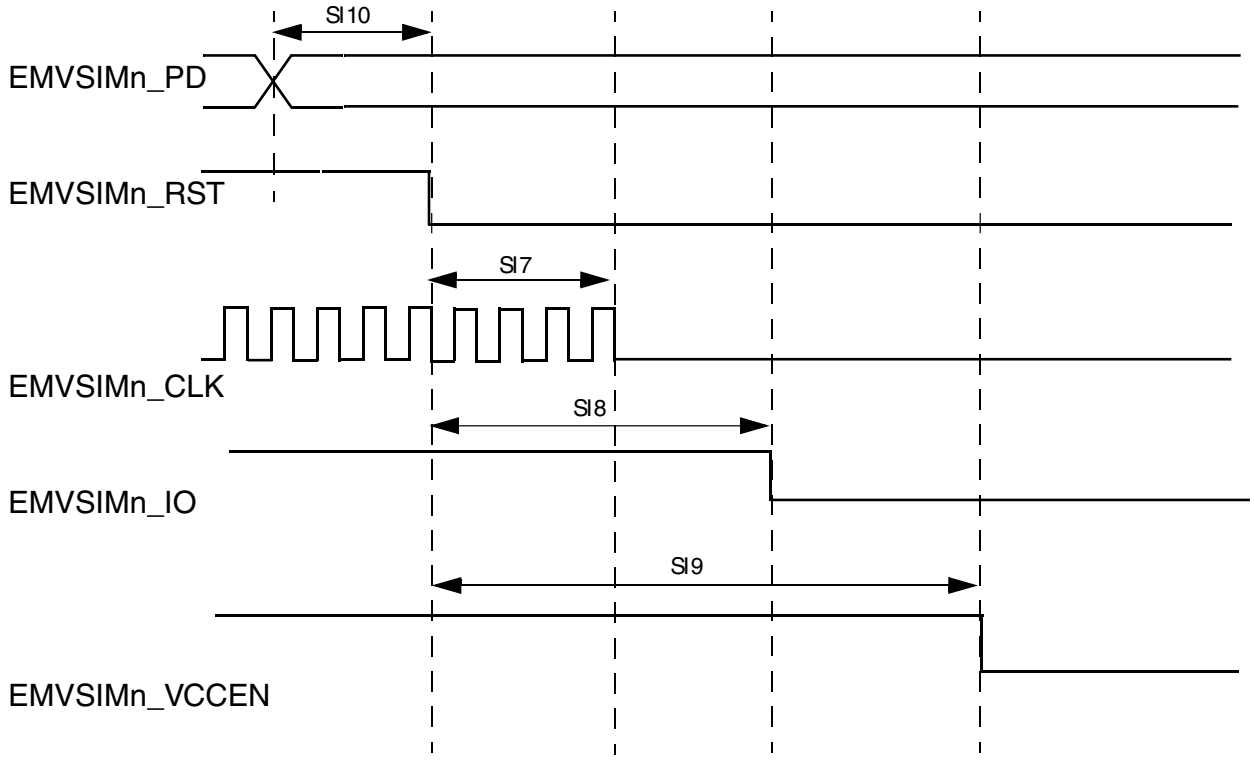


Figure 36. EMV SIM Clock Timing Diagram

The following table defines the general timing requirements for the EMV SIM interface.

Table 49. Timing Specifications, High Drive Strength

ID	Parameter	Symbol	Min	Max	Unit
SI 1	EMV SIM clock frequency (EMVSIMn_CLK)[1]	S_{freq}	1	5	MHz
SI 2	EMV SIM clock rise time (EMVSIMn_CLK)	S_{rise}	—	0.09 × (1/Sfreq)	ns
SI 3	EMV SIM clock fall time (EMVSIMn_CLK)	S_{fall}	—	0.09 × (1/Sfreq)	ns
SI 4	EMV SIM input transition time (EMVSIMn_IO, EMVSIMn_PD)	S_{tran}	20	25	ns
Si 5	EMV SIM I/O rise time / fall time (EMVSIMn_IO)[2]	Tr/Tf	—	1	ns
Si 6	EMV SIM RST rise time / fall time (EMVSIMn_RST)[3]	Tr/Tf	—	1	ns

1. 50% duty cycle clock,
2. With Cin = 30 pF, Cout = 30 pF,
3. With Cin = 30 pF,

3.6.9.1 EMV SIM Reset Sequences
(view resource)

Smart cards may have internal reset or active low reset. The following sections describe the reset sequences in these two cases.

3.6.9.1.1 Smart Cards with Internal Reset
(view resource)

Following figure shows the reset sequence for Smart cards with internal reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on EMVSIMn_CLK (time T0)
- After 200 clock cycles, EMVSIMn_IO must be asserted.
- The card must send a response on EMVSIMn_IO acknowledging the reset between 400–40000 clock cycles after T0.

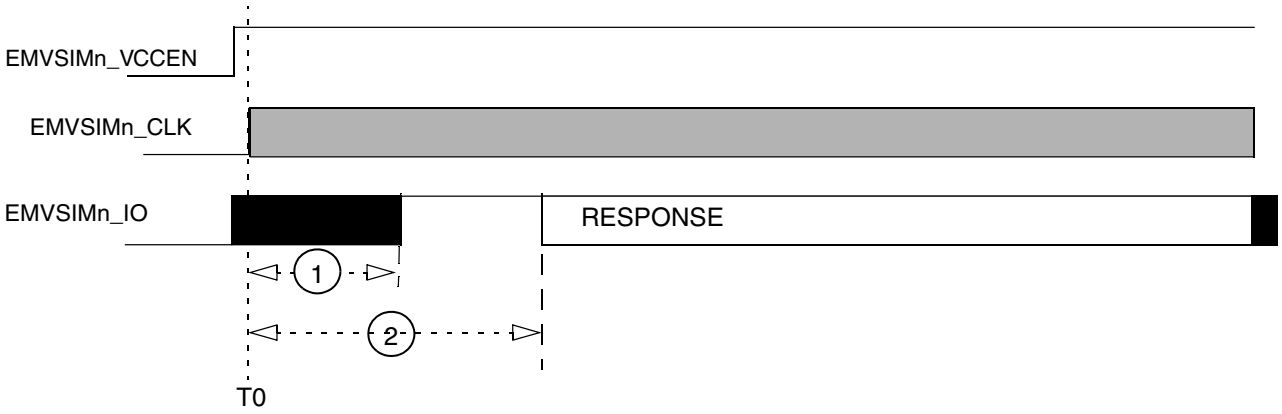


Figure 37. Internal Reset Card Reset Sequence

The following table defines the general timing requirements for the SIM interface.

Table 50. Timing Specifications, Internal Reset Card Reset Sequence

Ref	Min	Max	Units
1	—	200	EMVSIMx_CLK clock cycles
2	400	40,000	EMVSIMx_CLK clock cycles

3.6.9.1.2 Smart Cards with Active Low Reset

(view resource)

Following figure shows the reset sequence for Smart cards with active low reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on EMVSIMn_CLK (time T0)
- After 200 clock cycles, EMVSIMn_IO must be asserted.
- EMVSIMn_RST must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
- EMVSIMn_RST is asserted (at time T1)
- EMVSIMn_RST must remain asserted for at least 40,000 clock cycles after T1, and a response must be received on EMVSIMn_IO between 400 and 40,000 clock cycles after T1.

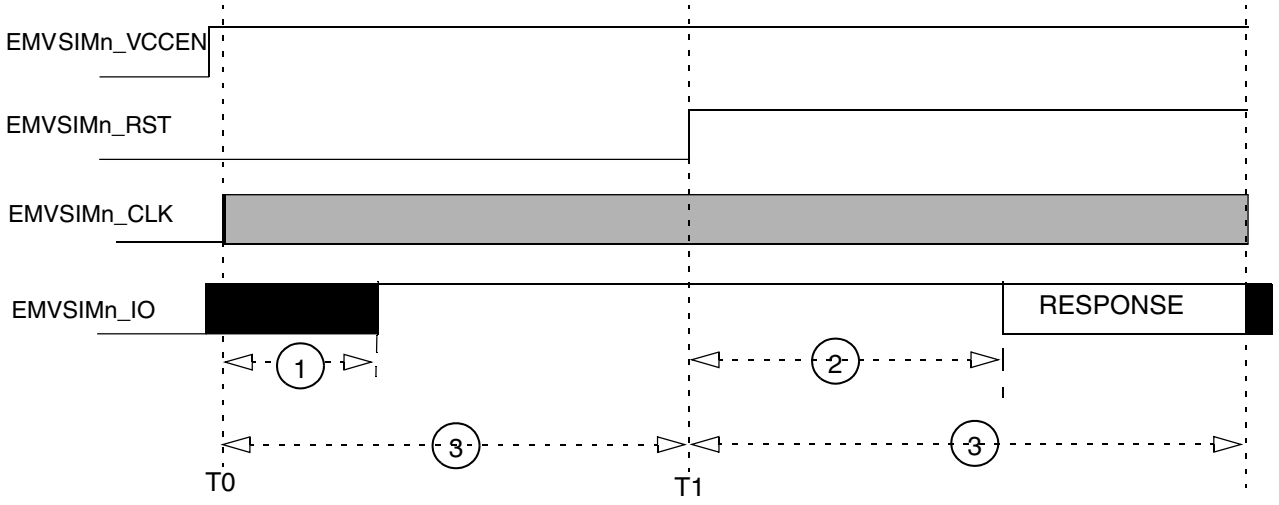


Figure 38. Active-Low-Reset Smart Card Reset Sequence

The following table defines the general timing requirements for the EMVSIM interface.

Table 51. Timing Specifications, Internal Reset Card Reset Sequence

Ref No	Min	Max	Units
1	—	200	EMVSIMx_CLK clock cycles
2	400	40,000	EMVSIMx_CLK clock cycles
3	40,000	—	EMVSIMx_CLK clock cycles

3.6.9.2 EMVSIM Power-Down Sequence

(view resource)

The following figure shows the EMVSIM interface power-down AC timing diagram. Table 52 table shows the timing requirements for parameters (SI7–SI10) shown in the figure. The power-down sequence for the EMVSIM interface is as follows:

- EMVSIMn_PD port detects the removal of the Smart Card
- EMVSIMn_RST is negated
- EMVSIMn_CLK is negated
- EMVSIMn_IO is negated
- EMVSIMn_VCCEN is negated

Each of the above steps requires one F_{RTCCLK} period (usually 32 kHz). Power-down may be initiated by a Smart card removal detection; or it may be launched by the processor.

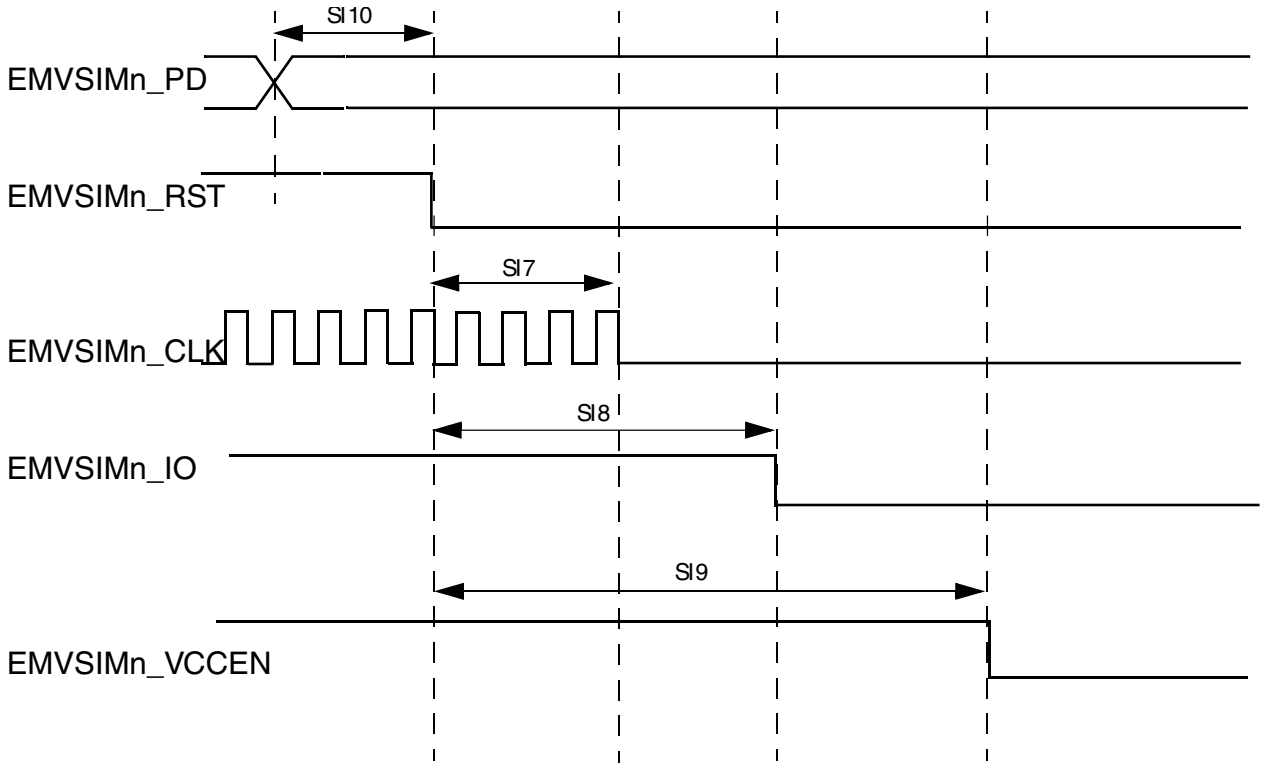


Figure 39. Smart Card Interface Power Down AC Timing

Table 52. Timing Requirements for Power-down Sequence

Ref No	Parameter	Symbol	Min	Max	Units
SI7	EMVSIM reset to SIM clock stop	$S_{RTS2CLK}$	0.9 × 1/ F_{RTCCLK}[1]	1.1 × 1/ $F_{RTCCLK>}$	µs
SI8	EMVSIM reset to SIM Tx data low	$S_{RST2DAT}$	1.8 × 1/ F_{RTCCLK}	2.2 × 1/ F_{RTCCLK}	µs
SI9	EMVSIM reset to SIM voltage enable low	$S_{RST2VEN}$	2.7 × 1/ F_{RTCCLK}	3.3 × 1/ F_{RTCCLK}	µs
SI10	EMVSIM presence detect to SIM reset low	S_{PD2RST}	0.9 × 1/ F_{RTCCLK}	1.1 × 1/ F_{RTCCLK}	µs

1. F_{RTCCLK} is ERCLK32K, and this clock must be enabled during the power down sequence.

NOTE

Same timing is also followed when auto power down is initiated. See Reference Manual for reference.

3.7 Human-machine interfaces (HMI) (view resource)

3.7.1 I2S/SAI switching specifications (view resource)

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and in slave mode (clocks are input). All timing is given for non-inverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a non-inverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

3.7.1.1 Normal Run, Wait and Stop mode performance (view resource)

This section provides the operating performance for the device in Normal Run, Wait and Stop modes.

Table 53. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
S1	I2S_MCLK cycle time	20	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	40	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	7.0	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	10	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	1	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	9	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

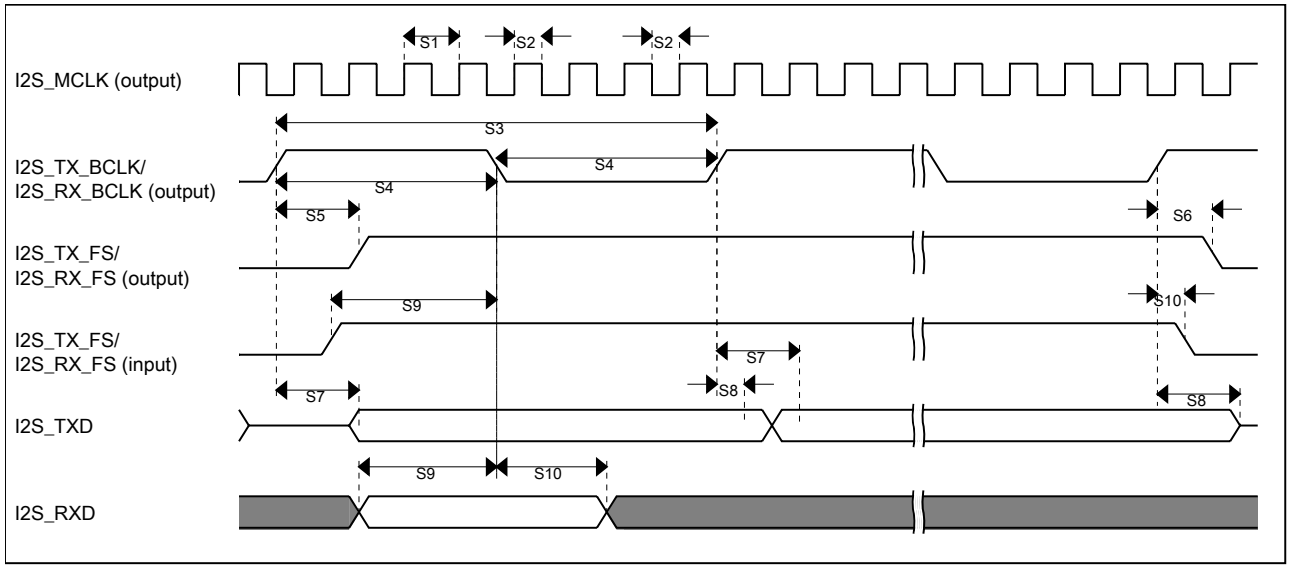


Figure 40. I2S/SAI timing — master modes

Table 54. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	40	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	8	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	1	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	15	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	1	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	1	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	10	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

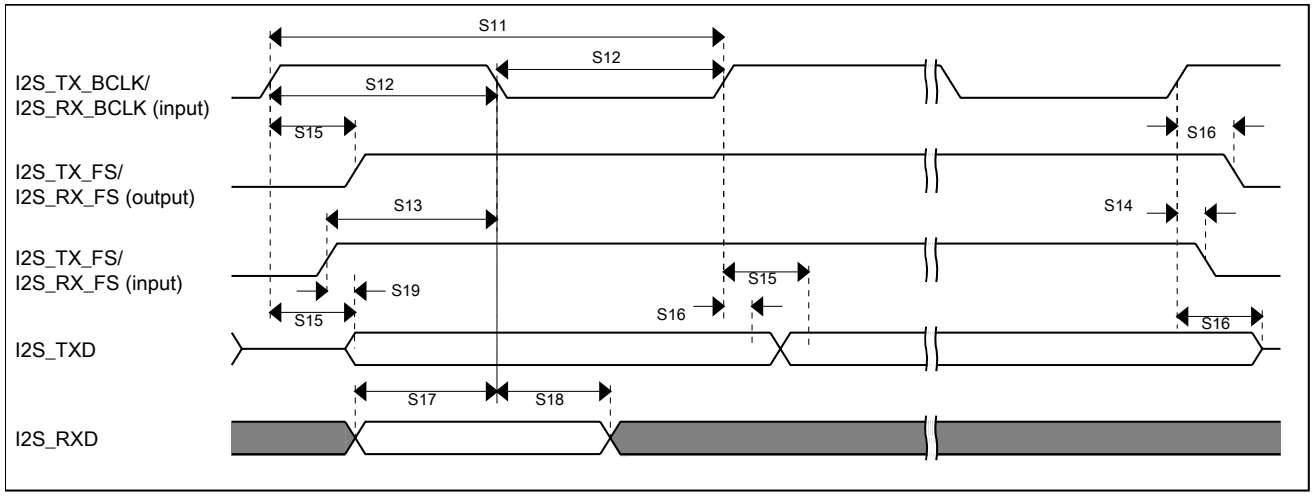


Figure 41. I2S/SAI timing — slave modes

3.7.1.2 VLPR, VLPW, and VLPS mode performance (view resource)

This section provides the operating performance for the device in VLPR, VLPW, and VLPS modes.

Table 55. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes

Num.	Characteristic	Min.	Max.	Unit
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid		—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid		—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK		—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

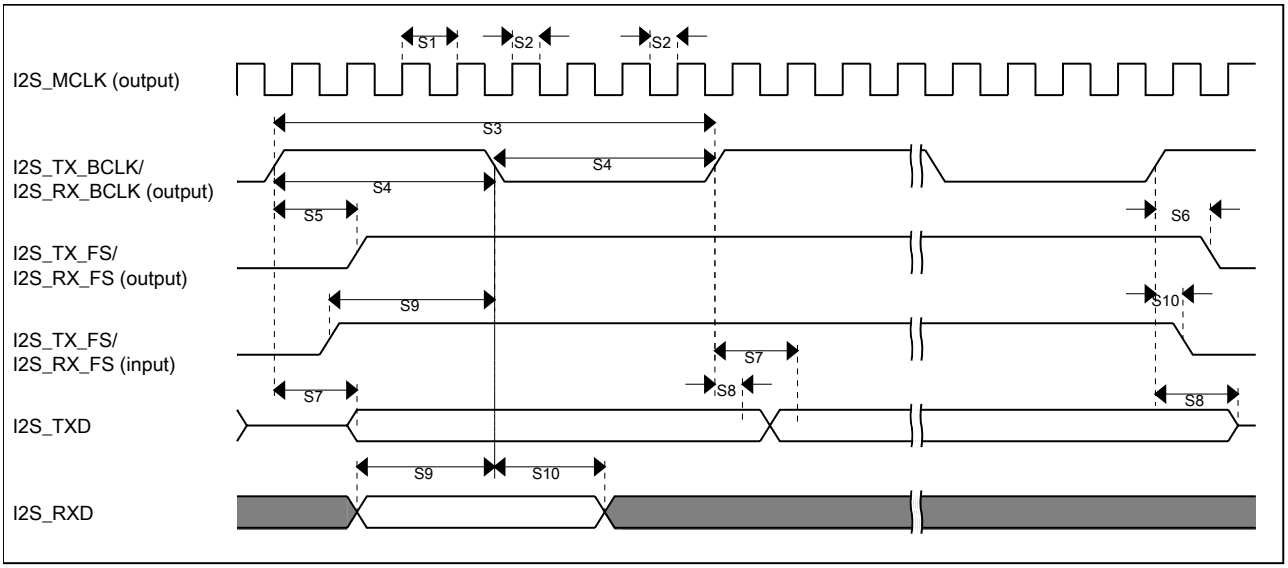


Figure 42. I2S/SAI timing — master modes

Table 56. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes

Num.	Characteristic	Min.	Max.	Unit
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK		—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—		ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK		—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

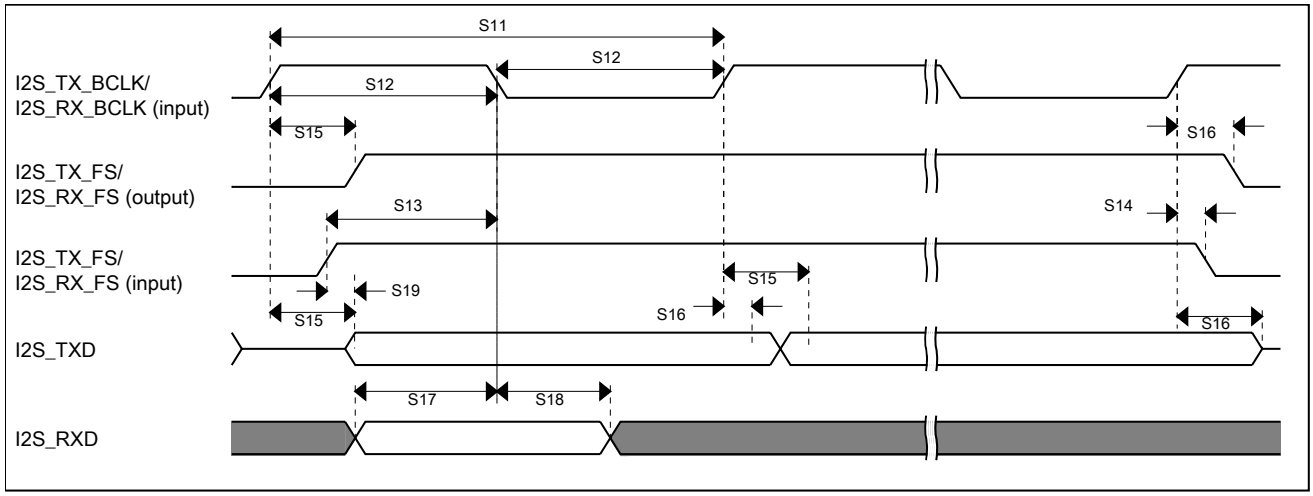


Figure 43. I2S/SAI timing — slave modes

3.7.2 MIC switching specifications (view resource)

What specs, if any, do we need for the microphone interface? Will the general timings work?

See General switching specifications.

3.7.3 SPDIF Timing Parameters (view resource)

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal. Table and Figure below show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 57. SPDIF Timing Parameters

Characteristic	Symbol	Timing Parameter Range		Unit
		Min	Max	
[O:] SPDIFIN Skew: asynchronous inputs, no specs apply			0.7	ns
[O:] SPDIFOUT output (Load = 50pf) • Skew			• 1.5 • 24.2 • 31.3	ns

Table continues on the next page...

Table 57. SPDIF Timing Parameters (continued)

Characteristic	Symbol	Timing Parameter Range		Unit
		Min	Max	
• Transition rising • Transition falling				
[O:] SPDIFOUT output (Load = 30pf) • Skew • Transition rising • Transition falling			• 1.5 • TBD • TBD	ns
[O:] Modulating Rx clock (SRCK) period	srckp	40		ns
[O:] SRCK high period	srckph	16		ns
[O:] SRCK low period	srckpl	16		ns
[O:] Modulating Tx clock (STCLK) period	stclkp	40		ns
[O:] STCLK high period	stclkph	16		ns
[O:] STCLK low period	stclkpl	16		ns

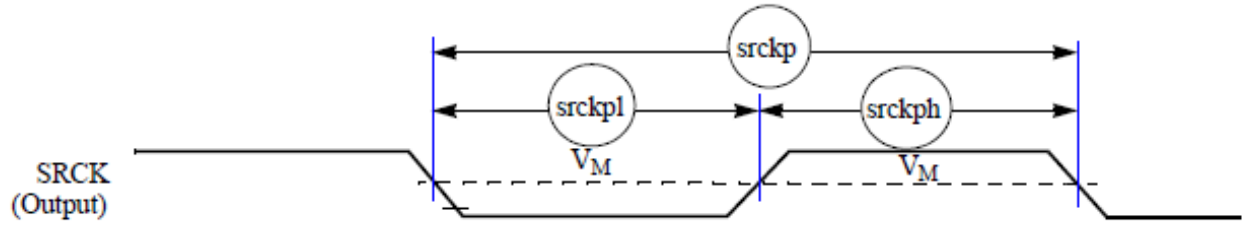


Figure 44. SRCK Timing Diagram

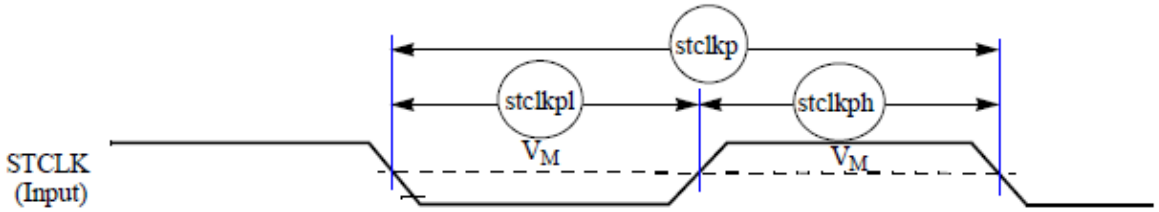


Figure 45. STCLK Timing Diagram

3.7.4 GPIO switching specifications (view resource)

See General switching specifications.

3.7.5 FlexIO switching specifications

(view resource)

See General switching specifications.

3.8 Security and integrity modules
(view resource)

3.8.1 DryIce Tamper Electrical Specifications
(view resource)

Table 58. DryIce Tamper Electrical Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{BAT}	3.3V supply voltage	1.71		3.6	V	
I_{TAM}	[L:] Supply current • voltage tamper enabled (other tampers disabled) • clock tamper enabled (other tampers disabled) • clock and voltage tamper enabled • clock, voltage and temperature tamper enabled		 TBD TBD TBD TBD	 TBD TBD TBD TBD	 µA µA µA µA	
R_{PU_Tamper}	[C:] Internal pullup resistors (per Tamper pin)	170	225	280	kΩ	
R_{PD_Tamper}	[C:] Internal pulldown resistors (per Tamper pin)	170	225	280	kΩ	
	EXTAL32 input clock		32.768		kHz	1
	Operating Temperature (junction)	-40		125	°C	
	[P:] Low Voltage Detect • assertion • negation	 1.545 1.595	 1.60 1.65	 1.655 1.70	 V V	
	[P:] High Voltage Detect • assertion	 3.675	 3.775	 3.875	 V	
	[L:] Voltage Tamper Detect operational temperature • no false alarms • with possible false alarms	 -50 -60		 150 160	 °C °C	
	[L:] Temperature Tamper Detect assertion • low temperature detect • high temperature detect • temperature detect filter delay	 -60	 -45 120 25	 -30 130	 °C °C ms	2, 3
	[L:] Temperature Tamper Detect operational voltage					

Table continues on the next page...

Table 58. DryIce Tamper Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Notes
	• no false alarms	1.5		3.8	V	
	• with possible false alarms	1.4		3.8	V	
	Clock Tamper Detect assertion					4
	• [P:] low frequency			20	kHz	
	• [P:] high frequency	40			kHz	
	• [L:] delay after loss of clock		2		ms	
	[L:] Clock Tamper Detect operational temperature					
	• no false alarms	-50		150	°C	
	• with possible false alarms	-60		160		
	[L:] Clock Tamper Detect operational voltage					
	• no false alarms	1.5		3.8	V	
	• with possible false alarms	1.4		3.8	V	

1. EXTAL32 oscillator must be enabled before enabling DryIce tamper detect.
2. Includes ambient temperature tamper detector assertion/negation is refreshed each 2^8 EXTAL32 clock cycles.
3. Filter delay=f_{clk}*28*3
4. Clock tamper detector assertion/negation is refreshed each 2^8 EXTAL32 clock cycles.

4 Dimensions
(view resource)

4.1 Obtaining package dimensions
(view resource)

Package dimensions are provided in package drawings. To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
13x13 BGA	TBD

5 Pinout
(view resource)

TBD

6 Part identification
(view resource)

6.1 Description
(view resource)

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

6.2 Format
(view resource)

Part numbers for this device have the following format:

Q KBB S FF C ## M R T PPP

6.3 Fields
(view resource)

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow, full reel • P = Prequalification • K = Fully qualified, general market flow, 100 piece reel
KBB	Kinetis brand	• K32
S	Product series	• W = Wireless Connectivity

Table continues on the next page...

Field	Description	Values
		• L = Performance Efficiency • H = High Performance & Integration
FF	Product family	• 84 = Ethernet and CAAM • 24 = No Ethernet and CAAM
C	Core	• Z = M0+ • D = M4 • F = M4F • P = M7 • T = M0+ & M0+ • S = M0+ & M4F • X = M0+ & M7 • U = M4 & M7
##	Special feature	• 05 = Includes tamper • 04 = Baseline • 03 = Includes CAN-FD
M	Flash memory size	• A = 0KB • B = 2KB • C = 4KB • D = 8KB • E = 16KB • F = 32KB • G = 64KB • H = 128KB • I = 256KB • J = 512KB • K = 1MB • L = 1.5MB • M = 2MB • N = 2.5MB
R	Silicon revision	• 0 = initial mask set • 1 = 1st major spin • 2 = 2nd major spin
T	Temperature range (°C)	• C = -40 to 85 • V = –40 to 105 • M = -40 to 125
PP	Package identifier	• VMU = 13x13 MAPBGA (13 mm x 13 mm)

6.4 Example (view resource)

This is an example part number:

MK32H84P04A0VMU

6.5 13 x 13 FBGA part marking

(view resource)

The 13 x 13 BGA package parts follow the part-marking scheme in the following table.

Table 59. 13 x 13 BGA part marking

MK Partnumber	MK Part Marking
K32H84P05A0VPE	TBD
K32H84P04A0VPE	TBD
K32H24P02A0VPE	TBD
K32H84P03A0VPE	TBD

7 Revision History
(view resource)

The following table provides a revision history for this document.

Table 60. Revision History

Rev. No.	Date	Substantial Changes
0.1	02/2016	Preliminary release for internal review

How to Reach Us:

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Revision 0, 02/2016