

# JEDEC STANDARD

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## Low Power Double Data Rate 2 (LPDDR2)

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### JESD209-2F

(Revision of JESD209-2E, April 2011)

JUNE 2013

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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## LOW POWER DOUBLE DATA RATE 2 (LPDDR2)

(From JEDEC Board ballot JCB-13-23, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memory.)

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### **1 Scope**

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This document defines the LPDDR2 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. This standard covers the following technologies: LPDDR2-S2A, LPDDR2-S2B, LPDDR2-S4A, LPDDR2-S4B, LPDDR2-N-A, and LPDDR2-N-B. The purpose of this standard is to define the minimum set of requirements for JEDEC compliant 64 Mb through 8 Gb for x8, x16, and x32 SDRAM devices as well as 64 Mb through 32 Gb for x8, x16, and x32 for NVM devices. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), LPDDR (JESD209), and LPDDR-NVM (N07-NV1A). Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots were then incorporated to prepare the LPDDR2 Standard.

## 2 Package ballout & addressing

### 2.1 LPDDR2 12x12 PoP 2-channel 2x32 package ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	DNU	VSSa/b	VDD2_a	DQ30_a	DQ29_a	VSSQ_	DQ26_a	DQ25_a	VSSQ_	DQS3_c	VSSQ_	DQ14_a	DQ13_a	VSS_a	VDD1_a	VDD2_a	DQ11_a	DQ10_a	DQ9_a	DQS1_t	DM_1_a	VDDQ_	DQS0_t	DQ7_a	DQ6_a	DQ4_a	DQ3_a	VSS_a/	DNU
B	VSSQ_	VACC	DQ31_a	VDDQ_	DQ28_a	DQ27_a	VDDQ_	DQ24_a	VDDQ_	DQS3_t	DM3_a	DQ15_a	VDDQ_	VSSQ_	Vref(DQ	VDD2_a	DQ12_a	VDDQ_	DQ8_a	DQS1_c	VSSQ_	DM_0_a	DQS0_c	VSSQ_	VDDQ_	DQ5_a	DQ2_a	VACC	VSSQ_
C	VDD1_a	DQ16_b																										VDD1_a	VDD2_a
D	DQ17_b	VDDQ_																										DQ1_a	VDDQ_
E	DQ18_b	DQ19_b																										VSSQ_	DQ0_a
F	VSSQ_	DQ20_b																										DM2_a	VDDQ_
G	DQ21_b	VDDQ_																										DQS2_t	DQS2_c
H	DQ22_b	DQ23_b																										VSSQ_	DQ23_a
J	VSSQ_	VDDQ_																										VDDQ_	DQ22_a
K	DQS2_c	DQS2_t																										DQ20_a	DQ21_a
L	DM2_b	DQ0_b																										DQ19_a	VSSQ_
M	DQ1_b	VSSQ_																										VDDQ_	DQ18_a
N	DQ2_b	VDD1_b																										DQ16_a	DQ17_a
P	VSS_b	VSS_b																										VDD2_b	VDD1_b
R	VDD1_b	Vref(DQ																										VSS_b	CA0_b
T	VDD2_b	VDD2_b																										VDDCA	CA1_b
U	VDDQ_	DQ3_b																										Vref(CA	CA2_b
V	DQ4_b	VSSQ_																										VSSCA	CA3_b
W	DQ6_b	DQ5_b																										CA4_b	CSB1_b
Y	VDDQ_	DQ7_b																										CSB0_b	CKE1_b
A	DQS0_t	DQS0_c																										VSSCA	CKE0_b
A	DM0_b	VSSQ_																										CK_t_b	CK_c_b
A	VDDQ_	DM1_b																										VDDCA	CA5_b
A	DQS1_c	DQS1_t																										CA7_b	CA6_b
A	DQ8_b	VSSQ_																										CA8_b	VDDCA
A	DQ9_b	VDDQ_																										VSSCA	CA9_b
A	DQ10_b	DQ11_b																										VDD2_a	ZQ_b
A	VSSQ_	VDD1_a	VDD2_a	DQ13_b	VSSQ_	DQ15_b	DM3_b	DQS3_t	VDDQ_	DQ26_b	DQ27_b	VDDQ_	DQ30_b	VSSQ_	VDD2_a	Vref(CA	CA9_a	VSSCA	CA7_a	CA6_a	CK_c_a	VDDCA	CKE0_a	CSB0_a	CA3_a	CA2_a	CA1_a	VDD1_a	VSSCA
A	DNU	VSS_a/	DQ12_b	VDDQ_	DQ14_b	VDDQ_	VSSQ_	DQS3_c	DQ24_b	DQ25_b	VSSQ_	DQ28_b	DQ29_b	DQ31_b	VDD1_a	VSS_a	ZQ_a	CA8_a	VDDCA	CA5_a	CK_t_a	VSSCA	CKE1_a	CSB1_a	CA4_a	VDDCA	CA0_a	VSS_a/	DNU

NOTE 1: 12x12 mm, 0.4mm pitch, 29 rows

NOTE 2: 216 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.2



2.2 LPDDR2 14x14 PoP 2-channel 2x32 package ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
A	DNU	VSSa/b	VDD2_a/	VSSQ_b	DQ29_b	DQ28_b	VSSQ_b	DQ25_b	DQ24_b	DQS3_c	DM3_b	DQ15_b	VSSQ_b	DQ13_b	DQ11_b	VSSQ_b	DQ9_b	DQS1_c	DM1_b	VSSQ_b	VSS_a/b	VDD2_a/	DQS0_c	DQ7_b	VSSQ_b	VSS_a/b	DNU
B	VDD1_a/	VACC	VDDQ_b	DQ31_b	DQ30_b	VDDQ_b	DQ27_b	DQ26_b	VDDQ_b	DQS3_t	VSSQ_b	VDDQ_b	DQ14_b	DQ12_b	VDDQ_b	DQ10_b	DQ8_b	DQS1_t	VDDQ_b	Vref(DQ)	VDD1_a/	DM0_b	DQS0_t	VDDQ_b	DQ6_b	VACC	VDD2_a/
C	DQ16_a	DQ17_a																								DQ5_b	DQ4_b
D	DQ18_a	VDDQ_a																								VDDQ_b	DQ3_b
E	VSSQ_a	DQ20_a	DQ19_a																						DQ2_b	DQ1_b	VSSQ_b
F	DQ21_a	VDDQ_a																								VDDQ_b	DQ0_b
G	VSSQ_a	DQ22_a	DQ23_a																						DM2_b	DQS2_t	VSSQ_b
H	DQS2_t	DQS2_c																								DQS2_c	DQ23_b
J	VSSQ_a	DM2_a	DQ0_a																						DQ21_b	DQ22_b	VSSQ_b
K	DQ1_a	VDDQ_a																								VDDQ_b	DQ20_b
L	VSSQ_a	DQ2_a	DQ3_a																						DQ19_b	DQ18_b	VSSQ_b
M	DQ4_a	VDDQ_a																								VDD2_a/	DQ17_b
N	VSSQ_a	DQ5_a	DQ6_a																						DQ16_b	VDDQ_b	VSSQ_a
P	DQ7_a	VDDQ_a																								VDDCA	CA0_a
R	VSSQ_a	DQS0_c	DQS0_t																						CA1_a	CA2_a	VSSCA
T	DM0_a	VDDQ_a																								CA3_a	CA4_a
U	VSS_a/b	VSSQ_a	Vref(DQ)																						CS0_n	CS1_n	VSS_a/b
V	VDD2_a/	VDD1_a/																								CKE0_a	CKE1_a
W	VSS_a/b	VDD2_a/	DM1_a																						CK_c_a	CK_t_a	VSSCA
Y	DQS1_c	DQS1_t																								VDDCA	CA5_a
A	VSSQ_a	DQ9_a	DQ10_a																						Vref(CA)	CA6_a	VDD2_a/
A	DQ8_a	VDDQ_a																								CA7_a	VSS_a/b
A	VSSQ_a	DQ11_a	DQ12_a																						CA8_a	CA9_a	VSSCA
A	DQ13_a	DQ14_a																								VDDCA	VDD2_a/
A	VSSQ_a	DQ15_a																								VDD1_a/	ZQ_a
A	VSS_a/b	VDDQ_a	DM3_a	DQS3_t	DQS3_c	DQ25_a	DQ27_a	VDDQ_a	DQ29_a	DQ31_a	VDD2_a/	VDD1_a/	VDDCA	CA9_b	CA7_b	VDD2_a/	Vref(CA)	VDDCA	CK_t_b	CKE1_b	CS0_n	CA4_b	VDDCA	CA2_b	CA0_b	VDD2_a/	VSS_a/b
A	DNU	VDD2_a/	VSSQ_a	VDDQ_a	DQ24_a	DQ26_a	VSSQ_a	DQ28_a	DQ30_a	VSSQ_a	VSS_a/b	ZQ_b	VSSCA	CA8_b	CA6_b	CA5_b	VSS_a/b	VSSCA	CK_c_b	CKE0_b	CS1_n	VSSCA	CA3_b	CA1_b	VSS_a/b	VDD1_a/	DNU

NOTE 1: 14x14 mm, 0.5mm pitch, 27 rows

NOTE 2: 220 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section TBD

## 2.3 LPDDR2 14x14 0.5 mm ball pitch Dualx32 Channel PoP ballout using variation VEEBDC for MO-273

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27		
A	DNU	VSSa/b	VDD2_a	DQ31_a	VDDQ_a	VSSQ_a	DQ26_a	DQ24_a	DQS3_t	DM3_a	DQ15_a	DQ13_a	VSSQ_a	VDDQ_a	DQ8_a	VSSQ_a	Vref(DQ)	VDD1_a	VDDQ_a	VSSQ_a	DQ7_a	DQ5_a	VSSQ_a	VDDQ_a	VDD1_a	VSSQ_a	DNU		
B	VSSQ_b	VACC	VSSQ_a	DQ30_a	DQ29_a	DQ27_a	VDDQ_a	VSSQ_a	DQS3_c	VSSQ_a	DQ14_a	DQ12_a	DQ11_a	DQ9_a	DQS1_c	VDDQ_a	VSS_a/b	VDD2_a	DQS0_c	DM0_a	DQ6_a	DQ4_a	DQ3_a	DQ1_a	DQ0_a	VACC	VSS_a/b		
C	VDD1_a	DQ16_b			DQ28_b		DQ25_a		VDDQ_a		VDDQ_a		DQ10_a		DQS1_t		DM1_a		DQS0_t		VDDQ_a		DQ2_a			DM2_a	VDD2_a		
D	DQ17_b	VDDQ_b																								VDDQ_a	DQS2_c		
E	DQ18_b	DQ19_b	VSSQ_b																							VSSQ_a	DQS2_t	DQ23_a	
F	DQ20_b	DQ21_b																									DQ22_a	VDDQ_a	
G	VDDQ_b	DQ22_b	DQ23_b																							DM21_a	DQ20_a	VSSQ_a	
H	VSSQ_b	DQS2_t																									DM19_a	DQ18_a	
J	DQS2_c	VDDQ_b	DM2_b																							VDDQ_b	DQ17_b	DQ16_a	
K	VSSQ_b	DQ0_b																									VSSQ_a	VDD2_a	
L	DQ1_b	VDDQ_b	DQ2_b																							CA0_b	VDD1_a	VSS_a/b	
M	DQ3_b	VSSQ_b																									CA1_b	VSSCA_a	
N	DQ4_b	DQ5_b	VDDQ_b																								CA3_b	CA2_b	VDDCA_a
P	DQ6_b	DQ7_b																										CA4_b	CSB1_b
R	VDDQ_b	DQS0_t	DQS0_c																								CKE0_b	CSB0_b	CKE1_b
T	VSSQ_b	VSS_a/b																										CK_c_b	CK_t_b
U	Vref(DQ)	VSS_a/b	DM0_b																								VDD2_a	VDDCA_a	VSSCA_a
V	VDD1_a	VDD1_a																										VSS_a/b	Vref(CA)
W	DM1_b	VDD2_a	VDD2_a																								CA5_b	VDDCA_a	VSSCA_a
Y	VDDQ_b	VSSQ_b																										CA7_b	CA6_b
A	DQS1_c	DQS1_t	DQ8_b																								VDD2_a	CA9_b	CA8_b
A	VDDQ_b	DQ9_b																										VSS_a/b	ZQ_b
A	DQ10_b	DQ11_b	VSSQ_b																								DNU	DNU	VDD1_a
A	DQ13_b	DQ12_b																										DNU	DNU
A	VDD1_a	DQ14_b			VSSQ_b		DQ27_b		DQ30_b		VDD2_a		CA6_a		CA5_a		VDD2_a		CA4_a		VSS_a/b		DNU				DNU	DNU	
A	VSSQ_b	VDDQ_b	DQ15_b	VDDQ_b	DQS3_t	DQ25_b	DQ26_b	DQ28_b	VDDQ_b	VSSQ_b	VSS_a/b	CA9_a	CA7_a	VDDCA_a	VSS_a/b	VDDCA_a	CK_t_a	CKE0_a	CSB0_a	CA2_a	VSSCA_a	CA0_a	VDD2_a	DNU	DNU	DNU	DNU		
A	DNU	VSS_a/b	VDD2_a	DM3_b	DQS3_c	DQ24_b	VDDQ_b	VSSQ_b	DQ29_b	DQ31_b	VDD1_a	ZQ_a	CA8_a	VSSCA_a	Vref(CA)	VSSCA_a	CK_c_a	CKE1_a	CSB1_a	CA3_a	VDDCA_a	CA1_a	VDD1_a	DNU	DNU	DNU	DNU		

NOTE 1: 14x14 mm, 0.5mm pitch, 27 rows

NOTE 2: 240 Ball Count, internal row partially populated

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.2

2.4 LPDDR2 12x12 PoP 1-channel x32 package ballout using MO-273

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	DNU	DNU	RDY,R/B_n, WAIT	CLK CLKm	ADQ11 DAT6m	VCCmm	ADQ10 DAT4m	ADQ9 DAT2m	VCCQmm	ADQ8 DAT0m	VDD1	VSSQ	DQ30	DQ29	VSSQ	DQ26	DQ25	VSSQ	DQS3_c	VDD1	VSS	DNU	DNU
B	DNU	DNU	VDD1	ADQ3 DAT7m	VSSmm	ADQ2 DAT5m	ADQ1 DAT3m	VSSmm	ADQ0 DAT1m	VSS	VDD2	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	DQS3_t	VDDQ	DM3	VDD2	DNU	DNU
C	VSS	VDD2																				DQ15	VSSQ
D	ADQ12	ADQ4																				VDDQ	DQ14
E	ADQ13	ADQ5																				DQ12	DQ13
F	VCCQmm VDDImm	VSSmm																				DQ11	VSSQ
G	ADQ14	ADQ6																				VDDQ	DQ10
H	ADQ15	ADQ7																				DQ8	DQ9
J	VCCmm	VSSmm																				DQS1_t	VSSQ
K	WE_n	OE_n/ RE_n																				VDDQ	DQS1_c
L	RP_n, RST_n,	AVD_n, ADV_n,																				VDD2	DM1
M	CE_n	VSS																				Vref(DQ)	VSS
N	INT,WP_n	VDD1																				VDD1	DM0
P	ZQ	Vref(CA)																				DQS0_c	VSSQ
R	VSS	VDD2																				VDDQ	DQS0_t
T	CA9	CA8																				DQ6	DQ7
U	CA7	VDDCA																				DQ5	VSSQ
V	VSSCA	CA6																				VDDQ	DQ4
W	CA5	VDDCA																				DQ2	DQ3
Y	CK_c	CK_t																				DQ1	VSSQ
AA	VSS	VDD2																				VDDQ	DQ0
AB	DNU	DNU	CS0_n	CS1_n	VDD1	CA1	VSSCA	CA3	CA4	VDD2	VSS	DQ16	VDDQ	DQ18	DQ20	VDDQ	DQ22	DQS2_t	VDDQ	DM2	VDD2	DNU	DNU
A C	DNU	DNU	CKE0	CKE1	VSS	CA0	CA2	VDDCA	VSSmm	VDDmm	VACC	VSSQ	DQ17	DQ19	VSSQ	DQ21	DQ23	VSSQ	DQS2_c	VDD1	VSS	DNU	DNU

Ball Location	Mux OneNand	eMMC	Raw NAND	ADD-Mux NOR	Comment
A3	RDY / WAIT_n	CMDm	R/B_n	WAIT	
A4	CLK	CLKm	NC	CLK	
K1	WE_n	NC	WE_n	WE_n	
K2	OE_n	NC	RE_n	OE_n	
L1	RP_n	RST_n (v4.4)	CLE	RST_n / DPD	DPD must be configured active high via
L2	AVD_n	NC	ALE	ADV_n	
N1	INT	NC	WP_n	WP_n	

- NOTE 1: 12x12 mm, 0.5mm pitch, 23 rows
- NOTE 2: 168 Ball Count
- NOTE 3: Top View, A1 in Top Left Corner
- NOTE 4: See JESD21-C, Section 3.12.2

## 2.5 LPDDR2 10x10 PoP 1-channel x32 package ballout using variation VAABCB for MO-273A

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	DNU	DNU	VSS	VSSQ	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	DQS3_c	DM3	VSSQ	DQ14	DQ13	DQ11	VSS	DNU	DNU
B	DNU	DNU	VSS	VDD2	DQ30	DQ29	VSSQ	DQ26	DQ25	VSSQ	DQS3_t	VDDQ	DQ15	VDDQ	DQ12	VDD2	VSS	DNU	DNU
C	ZQ	VDD1																VDD1	DQ10
D	CA9	CA8																DQ9	VDDQ
E	VSSCA	VDDCA																VSSQ	DQ8
F	CA7	CA6																DQS1_t	DQS1_c
G	CA5	VDD2																VDDQ	DM1
H	VDD1	Vref(CA)																VDD2	VSSQ
J	VSS	VDDCA																VSS	VDD2
K	CK_t	CK_c																Vref(DQ )	VSS
L	VSS	VSSCA																VDD1	VDD1
M	CKE1	CKE0																VDD2	VSSQ
N	CS1_n	CS0_n																VDDQ	DM0
P	CA3	CA4																DQS0_t	DQS0_c
R	VDDCA	CA2																VSSQ	DQ7
T	CA1	VSSCA																DQ6	VDDQ
U	CA0	VDD1																VDD1	DQ5
V	DNU	VACC	VSS	VDD2	DQ17	DQ18	VSSQ	DQ21	DQ22	VSSQ	DQS2_t	VDDQ	DQ0	VDDQ	DQ3	VDD2	VSS	DNU	DNU
W	DNU	DNU	VSS	VSSQ	DQ16	VDDQ	DQ19	DQ20	VDDQ	DQ23	DQS2_c	DM2	VSSQ	DQ1	DQ2	DQ4	VSS	DNU	DNU

Legend:

- LPDDR2 DQ
- LPDDR2 CA
- Power
- Ground
- Do Not Use
- ZQ
- Clock

NOTE 1: 10x10 mm, 0.5mm pitch, 19 rows

NOTE 2: 136 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.2

## 2.6 79-ball x16 LPDDR2 0.5mm pitch package ballout (Discrete/MCP)

	1	2	3	4	5	6	7	8	9
A	NC	CA9	VDD2	VDD1	VSSQ	DQ14	DQ12	VDD2	NC
B	CA7	CA8	ZQ	VSS	DQ15	DQ13	VDDQ	VSSQ	DQ11
C	CA5	CA6						DQ10	DQ9
D	VDDCA	VSSCA			CKE2 CS3_n	VSSQ	DQS1_t	DQ8	VDDQ
E	VDD2	Vref(CA)			CKE1	VDDQ	DQS1_c	DM1	VSS
F	VSS	VSSCA			CKE0	VSS	VDD1	VDD2	Vref(DQ)
G	VDDCA	CK_t			CS1_n	VSSQ	DQS0_c	DM0	VDD1
H	CK_c	CS0_n			CS2_n	VDDQ	DQS0_t	DQ7	VDDQ
J	CA4	CA3						DQ5	DQ6
K	CA2	CA1	VACC	VSS	DQ0	DQ2	VDDQ	VSSQ	DQ4
L	NC	CA0	VDD2	VDD1	VSSQ	DQ1	DQ3	VDD2	NC

LPDDR2 DQ

LPDDR2 CA

Power

Ground

Do Not Use/No Connect

ZQ

Clock

NOTE 1: 0.5mm pitch, 11 rows

NOTE 2: 79 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: The ZQ-ball used when operating above 200 MHz is limited to a 5pF load (typically 2 die using CKE0,1 and CS0,1)

NOTE 5: See JESD21-C, Section 3.12.1

**2.7 134-ball x16/x32 LPDDR2 package ballout (Discrete/MCP)**

	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU
B	DNU	NC	VACC	NB	VDD2	VDD1	DQ31 NC	DQ29 NC	DQ26 NC	DNU
C	VDD1	VSS	ZQ1	NB	VSS	VSSQ	VDDQ	DQ25 NC	VSSQ	VDDQ
D	VSS	VDD2	ZQ0	NB	VDDQ	DQ30 NC	DQ27 NC	DQS3_t NC	DQS3_c NC	VSSQ
E	VSSCA	CA9	CA8	NB	DQ28 NC	DQ24 NC	DM3 NC	DQ15	VDDQ	VSSQ
F	VDDCA	CA6	CA7	NB	VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ
G	VDD2	CA5	Vref(CA)	NB	DQS1_c	DQS1_t	DQ10	DQ9	DQ8	VSSQ
H	VDDCA	VSS	CK_c	NB	DM1	VDDQ	NB	NB	NB	NB
J	VSSCA	NC	CK_t	NB	VSSQ	VDDQ	VDD2	VSS	Vref(DQ)	NB
K	CKE0	CKE1	CKE2	NB	DM0	VDDQ	NB	NB	NB	NB
L	CS0_n	CS1_n	CS2_n	NB	DQS0_c	DQS0_t	DQ5	DQ6	DQ7	VSSQ
M	CA4	CA3	CA2	NB	VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ
N	VSSCA	VDDCA	CA1	NB	DQ19 NC	DQ23 NC	DM2 NC	DQ0	VDDQ	VSSQ
P	VSS	VDD2	CA0	NB	VDDQ	DQ17 NC	DQ20 NC	DQS2_t NC	DQS2_c NC	VSSQ
R	VDD1	VSS	VACC	NB	VSS	VSSQ	VDDQ	DQ22 NC	VSSQ	VDDQ
T	DNU	NC	NC	NB	VDD2	VDD1	DQ16 NC	DQ18 NC	DQ21 NC	DNU
U	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU

Ball Definition where 2 labels are present

1st Row	x32 device
2nd Row	x16

Legend:

- LPDDR2 DQ
- LPDDR2 CA
- Power
- Ground
- Do Not Use/NC/No Ball
- ZQ
- Clock

NOTE 1: 0.5mm (x32) or 0.65mm pitch (x32, x16), 17 rows

NOTE 2: 134 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.1

## 2.8 162-ball x16/x32 LPDDR2 and SDR-Flash package ballout

	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	WP_n WP_n DAT0	CLE CLE DAT6	VCCN VCCN VDDIm	IO4 DQ4 DAT5	IO7 DQ7 DAT3	VCCN VCCN VCCm	DNU	DNU
B	DNU	VCCN VCCN VCCm	IO11 DQS DAT1	ALE ALE DAT7	RE_n RE_n CLKm	IO5 DQ5 DAT4	IO14 NC DAT2	IO15 NC VCCQm	VSS	DNU
C	IO10 NC RST_n	IO1 DQ1 NC	IO3 DQ3 VSSQm	WE_n WE_n NC	R/B_n R/B_n CMD	IO6 DQ6 NC	NB	NB	NB	NB
D	IO8 NC NC	IO0 DQ0 NC	IO2 DQ2 NC	CE_n CE_n NC	IO12 NC NC	IO13 NC NC	NB	NB	NB	NB
E	VSS	IO9 NC NC	VACC	NB	VDD2	VDD1	DQ31 NC	DQ29 NC	DQ26 NC	DNU
F	VDD1	VSS	ZQ1	NB	VSS	VSSQ	VDDQ	DQ25 NC	VSSQ	VDDQ
G	VSS	VDD2	ZQ0	NB	VDDQ	DQ30 NC	DQ27 NC	DQS3_t NC	DQS3_c NC	VSSQ
H	VSSCA	CA9	CA8	NB	DQ28 NC	DQ24 NC	DM3 NC	DQ15	VDDQ	VSSQ
J	VDDCA	CA6	CA7	NB	VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ
K	VDD2	CA5	Vref(CA)	NB	DQS1_c	DQS1_t	DQ10	DQ9	DQ8	VSSQ
L	VDDCA	VSS	CK_c	NB	DM1	VDDQ	NB	NB	NB	NB
M	VSSCA	NC	CK_t	NB	VSSQ	VDDQ	VDD2	VSS	Vref(DQ)	NB
N	CKE0	CKE1	CKE2	NB	DM0	VDDQ	NB	NB	NB	NB
P	CS0_n	CS1_n	CS2_n	NB	DQS0_c	DQS0_t	DQ5	DQ6	DQ7	VSSQ
R	CA4	CA3	CA2	NB	VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ
T	VSSCA	VDDCA	CA1	NB	DQ19 NC	DQ23 NC	DM2 NC	DQ0	VDDQ	VSSQ
U	VSS	VDD2	CA0	NB	VDDQ	DQ17 NC	DQ20 NC	DQS2_t NC	DQS2_c NC	VSSQ
V	VDD1	VSS	VACC	NB	VSS	VSSQ	VDDQ	DQ22 NC	VSSQ	VDDQ
W	DNU	NC	NC	NB	VDD2	VDD1	DQ16 NC	DQ18 NC	DQ21 NC	DNU
Y	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU

SDR NVM Ball Definition where 3 labels are present	
1st Row	NVM device
2nd Row	ONFI
3rd Row	device
LPDDR2 Ball Definition where 2 labels are present	
1st Row	x32 device
2nd Row	x16 device

	Flash Memory (eMMC/NVM/ONFI) ADD/CTRL
	LPDDR2 DQ
	LPDDR2 CA
	Power
	Ground
	Do Not Use/NC/No Ball
	ZQ
	Clock

NOTE 1: 0.5mm (x32, x16) or 0.65mm pitch (x32, x16), 20 rows

NOTE 2: 162 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.1

## 2.9 180-ball x16/x32 LPDDR2, SDR-Flash, and e-MMC package ballout

	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	WP_n	CLE	VCCN	IO4 DQ4	IO7 DQ7	VCCN	DNU	DNU
B	DNU	VCCN	IO11 DQS	ALE	RE_n	IO5 DQ5	IO14 NC	IO15 NC	VSS	DNU
C	IO10 NC	IO1 DQ1	IO3 DQ3	WE_n	R/B_n	IO6 DQ6	NB	NB	NB	NB
D	IO8 NC	IO0 DQ0	IO2 DQ2	CE_n	IO12 NC	IO13 NC	NB	NB	NB	NB
E	VSS	IO9 NC	VACC	NB	VDD2	VDD1	DQ31 NC	DQ29 NC	DQ26 NC	DNU
F	VDD1	VSS	ZQ1	NB	VSS	VSSQ	VDDQ	DQ25 NC	VSSQ	VDDQ
G	VSS	VDD2	ZQ0	NB	VDDQ	DQ30 NC	DQ27 NC	DQS3_t NC	DQS3_c NC	VSSQ
H	VSSCA	CA9	CA8	NB	DQ28 NC	DQ24 NC	DM3 NC	DQ15	VDDQ	VSSQ
J	VDDCA	CA6	CA7	NB	VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ
K	VDD2	CA5	Vref(CA)	NB	DQS1_c	DQS1_t	DQ10	DQ9	DQ8	VSSQ
L	VDDCA	VSS	CK_c	NB	DM1	VDDQ	NB	NB	NB	NB
M	VSSCA	NC	CK_t	NB	VSSQ	VDDQ	VDD2	VSS	Vref(DQ)	NB
N	CKE0	CKE1	CKE2	NB	DM0	VDDQ	NB	NB	NB	NB
P	CS0_n	CS1_n	CS2_n	NB	DQS0_c	DQS0_t	DQ5	DQ6	DQ7	VSSQ
R	CA4	CA3	CA2	NB	VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ
T	VSSCA	VDDCA	CA1	NB	DQ19 NC	DQ23 NC	DM2 NC	DQ0	VDDQ	VSSQ
U	VSS	VDD2	CA0	NB	VDDQ	DQ17 NC	DQ20 NC	DQS2_t NC	DQS2_c NC	VSSQ
V	VDD1	VSS	VACC	NB	VSS	VSSQ	VDDQ	DQ22 NC	VSSQ	VDDQ
W	VCCm	VDDIm	NC	NB	VDD2	VDD1	DQ16 NC	DQ18 NC	DQ21 NC	DNU
Y	VSS	DAT2	CMD	DAT6	DAT1	NB	NB	NB	NB	NB
AA	DNU	VCCQm	DAT4	CLKm	DAT0	VCCm	NB	NB	NB	DNU
AB	DNU	DNU	DAT3	DAT5	DAT7	VCCQm	RST_n	VSS	DNU	DNU

SDR NVM Ball Definition where 2 labels are present	
1st Row	NVM device
2nd Row	ONFI device
LPDDR2 Ball Definition where 2 labels are present	
1st Row	x32 device
2nd Row	x16 device

	Flash Memory (eMMC/NVM/ONFI) ADD/CTRL
	LPDDR2 DQ
	LPDDR2 CA
	Power
	Ground
	Do Not Use/NC/No Ball
	ZQ
	Clock

NOTE 1: 0.5mm (x32, x16) or 0.65mm pitch (x32, x16), 22 rows

NOTE 2: 180 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.1



## 2.10 121-ball x16 LPDDR2, SDR Flash-NVM, and e-MMC package ballout

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	DAT2 ADQ9 DQ2	DAT5 ADQ2 DQ5	VDDI VCCQx	VCC	VDD2	VSS	VDDQ	NC	NC
B	NC	VSSx	DAT3 ADQ1 DQ3	DAT6 ADQ11 DQ6	DAT7 ADQ3 DQ7	VSSx	VDD1	DQ15	DQ14	VSSQ	NC
C	VCCQ	DAT0 ADQ8 DQ0	DAT4 ADQ10 DQ4		CLK e CLK o,f DQS i	CMD e RDY o WAIT f	RST_n e,f RP_n o CLE n,i		DQ11	DQ12	DQ13
D	VDD2	DAT1 ADQ0 DQ1								DQ10	VSSQ
E	VSS	ZQ	CA9						DQ8	DQ9	VDDQ
F	VDD1	CA8			VCCx	VSSx	WE_n CLK i		DQS1_t	VSSQ	
G	VSSCA	CA7	CA6		- ADQ12 DQ12	OE_n o,f RE_n n,i W/R_n i	CE_n		DQS1_c	DM1	VDDQ
H	VDDCA	CA5			ADQ13 DQ13	ADQ6 DQ11	ADQ4 DQ9		Vref(DQ)	VDD2	
J	VDD2	Vref(CA)	VSS		ADQ14 DQ14	ADQ7 DQ10	ADQ5 DQ8		DQS0_c	DM0	VDD1
K	CK_t	CK_c			ADQ15 DQ15	VSSx	VCCx		DQS0_t	VDDQ	
L	CS0_n	CS1_n	CS2_n						DQ7	DQ6	VSSQ
M	CA4	CA3							DQ5	VDDQ	
N	VDDCA	CA2	CA1		CKE0	AVD_n o ADV_n f ALE n,i	- INT o WP_n f,n,i		DQ3	DQ2	VSSQ
P	NC	VSSCA	CA0	CKE2	CKE1	VACC VPP	DQ0	DQ1	DQ4	VSSQ	NC
R	NC	NC	VSS	VDD2	VDD1	VSS	VDD2	VSS	VDDQ	NC	NC

SDR NVM Ball Definition where 3 labels are present		
1st Row	eMMC (e)	
2nd Row	OneNAND (o) / AAD Nor (f)	
3rd Row	Raw NAND (n) / ONFI2 (i)	

	Flash Memory (eMMC/Raw NAND/One- NAND)
	LPDDR2 DQ
	LPDDR2 CA
	Power
	Ground
	Do Not Use/NC/No Ball
	ZQ
	Clock

Ball	eMMC (e)	OneNAND (o) AAD NOR (f)	NAND (n)	NAND DDR (i)
-	DAT[7:0]	ADQ[15:0]	DQ[15:0]	DQ[15:0]
C5	CLK	CLK	-	DQS
C6	CMD	RDY / WAIT	R/B_n	R/B_n
C7	RST_n	RP_n/RST_n	CLE	CLE
F7	-	WE_n	WE_n	WE_n, CLK
G6	-	OE_n	RE_n	RE_n, W/R_n
G7	-	CE_n	CE_n	CE_n
N6	-	AVD_n/AVD_n	ALE	ALE
N7	-	INT / WP_n	WP_n	WP_n

VSSx/VCCx represents common Flash VSS/VCC

NOTE 1: 0.5mm pitch, 15 rows

NOTE 2: 121 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.2

## 2.11 LPDDR2 Pad Sequence

### Table 1 — LPDDR2 Pad Sequence

[illegible]

NOTE 1 Pads with (\*1) are optional.

NOTE 2 Ordering of DQ bits shall be maintained in the system, including within the package and on the PCB. DQ byte swapping and DQ bit Swapping are not allowed in the system.

NOTE 3 CA pads and DQ pads shall be separated on opposite sides of die from top of silicon view.

## 2.12 Input/output functional description

### 2.12.1 Pad Definition and Description

**Table 2 — Pad Definition and Description**

Name	Type	Description
CK_t, CK_c	Input	<b>Clock:</b> CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	<b>Clock Enable:</b> CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See <a href="#">Table 60</a> for command code descriptions. CKE is sampled at the positive Clock edge.
CS_n	Input	<b>Chip Select:</b> CS_n is considered part of the command code. See <a href="#">Table 60</a> for command code descriptions. CS_n is sampled at the positive Clock edge.
CA0 - CA9	Input	<b>DDR Command/Address Inputs:</b> Uni-directional command/address bus inputs. CA is considered part of the command code. See <a href="#">Table 60</a> for command code descriptions.
DQ0-DQ7 (x8) DQ0 - DQ15 (x16) DQ0 - DQ31 (x32)	I/O	<b>Data Inputs/Output:</b> Bi-directional data bus
DQS0_t, DQS0_c (x8) DQS0_t, DQS0_c, DQS1_t, DQS1_c (x16) DQS0_t - DQS3_t, DQS0_c - DQS3_c (x32)	I/O	<b>Data Strobe (Bi-directional, Differential):</b> The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data.  For x8, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7. For x16, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7; DQS1_t and DQS1_c to the data on DQ8 - DQ15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31.
DM0 (x8) DM0-DM1 (x16) DM0 - DM3 (x32)	Input	<b>Input Data Mask:</b> For LPDDR2 devices that do not support the DNV feature, DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS_t (or DQS_c).  DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.

Name	Type	Description
DM0/DNV0 (x8) DM0/DNV0-DM1/DNV1 (x16) DM0/DNV0 - DM3/DNV3 (x32)	I/O	<p><b>Input Data Mask/Data Not Valid:</b> For LPDDR2 devices that support the DNV feature, DM/DNV is bidirectional (used for write and read data). It is output with read data, input with write data. DM/DNV is the input mask signal for write data and is an output signal validating a read burst.</p> <p>For data write accesses: Input data is masked when DM/DNV is sampled HIGH coincident with DQ input data during a WRITE access. DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.</p> <p>For data read accesses: See 5.4.2 for detailed description of DNV functionality. DNV0, DNV1, DNV2, and DNV3 are driven coincident with output read data. DNV0, DNV1, DNV2, and DNV3 are driven with the same value and shall be sampled with DQS0, DQS1, DQS2, and DQS3 respectively.</p> <p>The DM/DNV loading shall match the DQ and DQS<sub>t</sub> (or DQS<sub>c</sub>) loading.</p>
V <sub>DD1</sub>	Supply	<b>Core Power Supply 1:</b> Core power supply for LPDDR2-N and LPDDR2-SX devices.
V <sub>DD2</sub>	Supply	<b>Core Power Supply 2:</b> Core power supply for LPDDR2-S2B, LPDDR2-S4 and LPDDR2-N-B devices.
V <sub>DDCA</sub>	Supply	<b>Input Receiver Power Supply:</b> Power supply for CA0-9, CKE, CS <sub>n</sub> , CK <sub>t</sub> , and CK <sub>c</sub> input buffers.
V <sub>DDQ</sub>	Supply	<b>I/O Power Supply:</b> Power supply for Data input/output buffers.
V <sub>ACC</sub>	Supply	<b>NVM Acceleration Supply:</b> NVM device specific embedded operation acceleration. V <sub>ACC</sub> enables some NVM device specific functionality. When not used for NVM device specific functionality, V <sub>ACC</sub> shall be driven to a level of V <sub>DD1</sub> .
V <sub>REF(CA)</sub>	Supply	<b>Reference Voltage for CA Command and Control Input Receiver:</b> Reference voltage for all CA0-9, CKE, CS <sub>n</sub> , CK <sub>t</sub> , and CK <sub>c</sub> input buffers.
V <sub>REF(DQ)</sub>	Supply	<b>Reference Voltage for DQ Input Receiver:</b> Reference voltage for all Data input buffers.
V <sub>SS</sub>	Supply	<b>Ground</b>
V <sub>SSCA</sub>	Supply	<b>Ground for Input Receivers</b>
V <sub>SSQ</sub>	Supply	<b>I/O Ground</b>
ZQ	I/O	<b>Reference Pin for Output Drive Strength Calibration</b>

NOTE 1 Data includes DQ and DM.

## 2.13 LPDDR2 SDRAM Addressing

**Table 3 — LPDDR2 SDRAM Addressing**

Items		64Mb	128Mb	256Mb	512Mb	1Gb		2Gb		4Gb	6Gb	8Gb
Device Type		S2/S4	S2/S4	S2/S4	S2/S4	S2	S4	S2	S4	S2/S4	S2/S4	S2/S4
Number of Banks		4				4	8	4	8	8		
Bank Addresses		BA0-BA1				BA0-BA1	BA0-BA2	BA0-BA1	BA0-BA2	BA0-BA2		
$t_{REFI}(us)^{*2}$		15.6	15.6	7.8	7.8	7.8	7.8	3.9	3.9	3.9	3.9	3.9
x8	Row Addresses	R0-R11	R0-R11	R0-R12	R0-R12	R0-R13	R0-R12	R0-R14	R0-R13	R0-R13	R0-R14 <sup>*4</sup>	R0-R14
	Column Addresses <sup>*1</sup>	C0-C8	C0-C9	C0-C9	C0-C10	C0-C10	C0-C10	C0-C10	C0-C10	C0-C11	C0-C11	C0-C11
x16	Row Addresses	R0-R11	R0-R11	R0-R12	R0-R12	R0-R13	R0-R12	R0-R14	R0-R13	R0-R13	R0-R14 <sup>*4</sup>	R0-R14
	Column Addresses <sup>*1</sup>	C0-C7	C0-C8	C0-C8	C0-C9	C0-C9	C0-C9	C0-C9	C0-C9	C0-C10	C0-C10	C0-C10
x32	Row Addresses	R0-R11	R0-R11	R0-R12	R0-R12	R0-R13	R0-R12	R0-R14	R0-R13	R0-R13	R0-R14 <sup>*4</sup>	R0-R14
	Column Addresses <sup>*1</sup>	C0-C6	C0-C7	C0-C7	C0-C8	C0-C8	C0-C8	C0-C8	C0-C8	C0-C9	C0-C9	C0-C9

NOTE 1 The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

NOTE 2  $t_{REFI}$  values for all bank refresh is  $T_c = -25 \sim 85 \text{ }^{\circ}\text{C}$ ,  $T_c$  means Operating Case Temperature

NOTE 3 Row and Column Address values on the CA bus that are not used are “don’t care.”

NOTE 4 No memory present at addresses with R13=R14=HIGH. ACT command with R13=R14=HIGH is ignored (NOP). Write to R13=R14=HIGH is ignored (NOP).

## 2.14 LPDDR2 NVM Addressing

### 2.14.1 Three-Phase Addressing

The memory controller delivers an array address to the memory in three phases (See [Figure 1](#) and [Figure 2](#)). The [Table 60](#) defines the required assignment of logical address bits to CA pins. Scrambling of the logical address bits in any order different than those described in the Command truth table is prohibited.

During a Preactive command, part of a row address (driven on the CA input pins) is stored in a Row Address Buffer (RAB) selected by BA2-BA0.

During an Activate command, BA2-BA0 select an RAB to retrieve the first part of the row address. Meanwhile, the remainder of the row address is driven on the CA input pins. These two parts of the row address select one row from the memory array. Activate also causes internal sensing circuits to transfer that memory content into a Row Data Buffer (RDB) also selected by BA2-BA0.

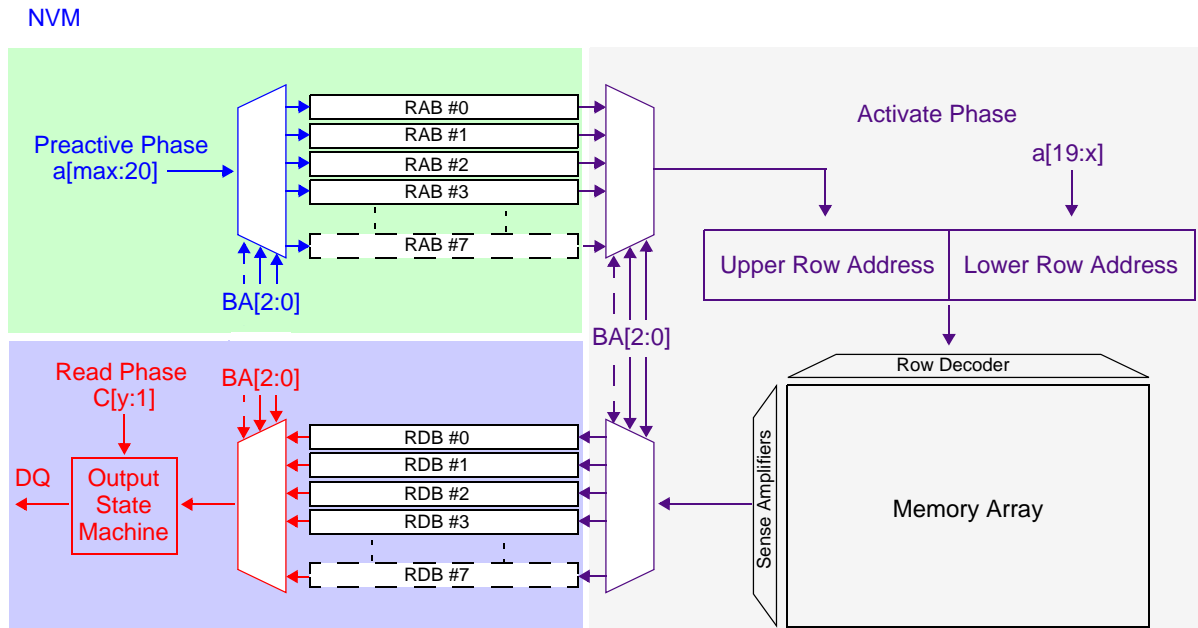
An {RAB, RDB} pair selected by BA2-BA0 is referred to as a Row Buffer (RB). BA2-BA0 do not address any portion of the array and only select an RAB into which address is placed and/or an RDB into which data is placed. The controller may use any value of BA2-BA0 for any array location.

During a Read or Write command BA2-BA0 selects an RDB, and the column address is driven on the CA input pins to choose the starting address of the read or write burst.

The Preactive command is optional when the desired RAB already contains the desired partial row address. The Activate command is optional when the desired RDB already contains the desired memory content.

Upon completion of Device Auto-Initialization, all Row Buffers are in the Idle state, and RABs contain 0x0000 and all RDBs contain indeterminate values.

## 2.5.1 Three-Phase Addressing (cont'd)



**Figure 1 — LPDDR2-N: Three-Phase Address Read**

NOTE 1 In the Preactive phase,  $a[\text{max}]$  is dependent on the density of the NVM device.

NOTE 2 In the Activate phase, the lower order row address bit  $a[x]$  is dependent on the size of the Row Data Buffer (RDB).

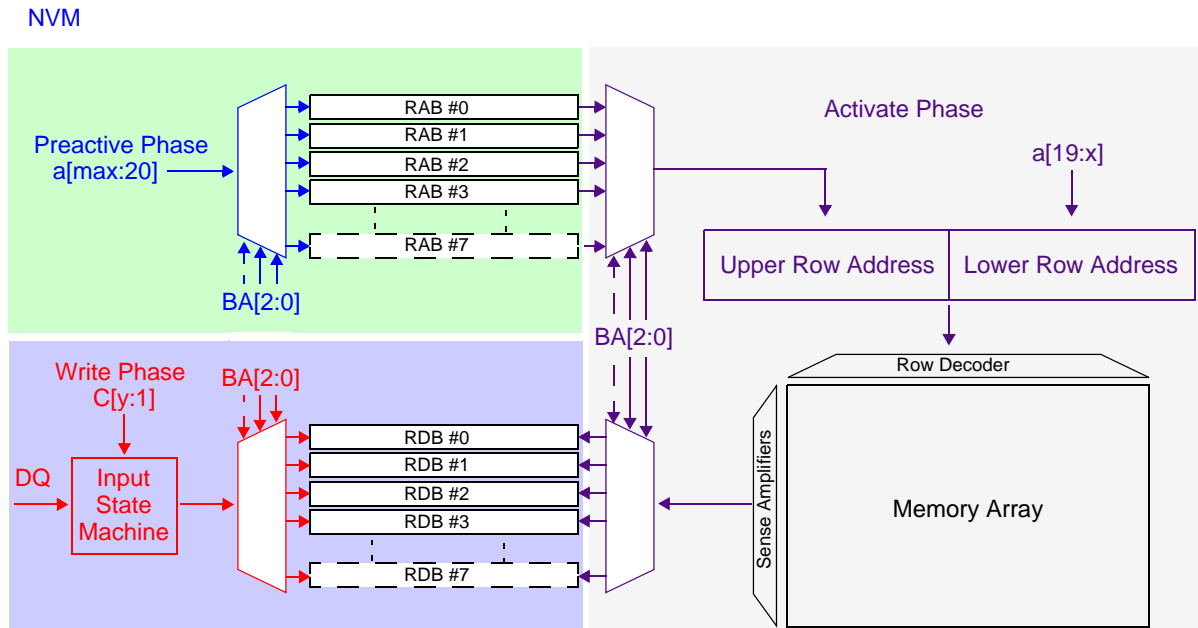
NOTE 3 In the Read phase, column address bit  $C[y]$  is dependent on the size of the Row Data Buffer (RDB) and the data bus width.

NOTE 4 An {RAB, RDB} pair selected by  $BA[2:0]$  is referred to as a Row Buffer (RB).

NOTE 5 The least significant column address  $C0$  is implied to be zero and is not transmitted on the CA bus.

NOTE 6 An {RAB, RDB} pair can be associated with any portion of the memory array.

## 2.5.1 Three-Phase Addressing (cont'd)



**Figure 2 — LPDDR2-N: Three-Phase Address Write**

- NOTE 1 In the Preactive phase,  $a[\max]$  is dependent on the density of the NVM device.
- NOTE 2 In the Activate phase, the lower order row address bit  $a[x]$  is dependent on the size of the Row Data Buffer (RDB).
- NOTE 3 In the Write phase, column address bit  $C[y]$  is dependent on the size of the Row Data Buffer (RDB) and the data bus width.
- NOTE 4 An {RAB, RDB} pair selected by  $BA[2:0]$  is referred to as a Row Buffer (RB).
- NOTE 5 The least significant column address  $C0$  is implied to be zero and is not transmitted on the CA bus.

**Table 4 — 64 Mb Addressing**

Configuration	8 Mb x 8	4 Mb x 16	2 Mb x 32
# of Row Buffers <sup>*2,3</sup>	4	4	4
Upper Row Address (PREACTIVE)	a22-a20	a22-a20	a22-a20
Lower Row Address (ACTIVE) <sup>*1</sup>	a19-A5	a19-a5	a19-a5
Column Address (READ/WRITE) <sup>*1,4</sup>	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size <sup>*1</sup>	32 Bytes	32 Bytes	32 Bytes

**Table 5 — 128 Mb Addressing**

Configuration	16 Mb x 8	8 Mb x 16	4 Mb x 32
# of Row Buffers <sup>*2,3</sup>	4	4	4
Upper Row Address (PREACTIVE)	a23-a20	a23-a20	a23-a20
Lower Row Address (ACTIVE) <sup>*1</sup>	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) <sup>*1,4</sup>	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size <sup>*1</sup>	32 Bytes	32 Bytes	32 Bytes

**2.5.1 Three-Phase Addressing (cont'd)****Table 6 — 256 Mb addressing**

Configuration	32 Mb x 8	16 Mb x 16	8 Mb x 32
# of Row Buffers <sup>*2,3</sup>	4	4	4
Upper Row Address (PREACTIVE)	a24-a20	a24-a20	a24-a20
Lower Row Address (ACTIVE) <sup>*1</sup>	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) <sup>*1,4</sup>	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size <sup>*1</sup>	32 Bytes	32 Bytes	32 Bytes

**Table 7 — 512 Mb addressing**

Configuration	64 Mb x 8	32 Mb x 16	16 Mb x 32
# of Row Buffers <sup>*2,3</sup>	4	4	4
Upper Row Address (PREACTIVE)	a25-a20	a25-a20	a25-a20
Lower Row Address (ACTIVE) <sup>*1</sup>	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) <sup>*1,4</sup>	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size <sup>*1</sup>	32 Bytes	32 Bytes	32 Bytes

**Table 8 — 1 Gb addressing**

Configuration	128 Mb x 8	64 Mb x 16	32 Mb x 32
# of Row Buffers <sup>*2,3</sup>	4	4	4
Upper Row Address (PREACTIVE)	a26-a20	a26-a20	a26-a20
Lower Row Address (ACTIVE) <sup>*1</sup>	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) <sup>*1,4</sup>	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size <sup>*1</sup>	32 Bytes	32 Bytes	32 Bytes

**Table 9 — 2 Gb addressing**

Configuration	256 Mb x 8	128 Mb x 16	64 Mb x 32
# of Row Buffers <sup>*2,3</sup>	4	4	4
Upper Row Address (PREACTIVE)	a27-a20	a27-a20	a27-a20
Lower Row Address (ACTIVE) <sup>*1</sup>	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) <sup>*1,4</sup>	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size <sup>*1</sup>	32 Bytes	32 Bytes	32 Bytes

**Table 10 — 4 Gb addressing**

Configuration	512 Mb x 8	256 Mb x 16	128 Mb x 32
# of Row Buffers <sup>*2,3</sup>	4	4	4
Upper Row Address (PREACTIVE)	a28-a20	a28-a20	a28-a20
Lower Row Address (ACTIVE) <sup>*1</sup>	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) <sup>*1,4</sup>	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size <sup>*1</sup>	32 Bytes	32 Bytes	32 Bytes



## 2.5.1 Three-Phase Addressing (cont'd)

**Table 11 — 8 Gb addressing**

Configuration	1 Gb x 8	512 Mb x 16	256 Mb x 32
# of Row Buffers <sup>*2,3</sup>	4	4	4
Upper Row Address (PREAMBLE)	a29-a20	a29-a20	a29-a20
Lower Row Address (ACTIVE) <sup>*1</sup>	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) <sup>*1,4</sup>	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size <sup>*1</sup>	32 Bytes	32 Bytes	32 Bytes

**Table 12 — 16 Gb addressing**

Configuration	2 Gb x 8	1 Gb x 16	512 Mb x 32
# of Row Buffers <sup>*2,3</sup>	4	4	4
Upper Row Address (PREAMBLE)	a30-a20	a30-a20	a30-a20
Lower Row Address (ACTIVE) <sup>*1</sup>	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) <sup>*1,4</sup>	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size <sup>*1</sup>	32 Bytes	32 Bytes	32 Bytes

**Table 13 — 32 Gb addressing**

Configuration	4 Gb x 8	2 Gb x 16	1 Gb x 32
# of Row Buffers <sup>*2,3</sup>	4	4	4
Upper Row Address (PREAMBLE)	a31-a20	a31-a20	a31-a20
Lower Row Address (ACTIVE) <sup>*1</sup>	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) <sup>*1,4</sup>	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size <sup>*1</sup>	32 Bytes	32 Bytes	32 Bytes

Notes for Tables 4-13

NOTE 1 All tables above show examples using minimum 32 Byte RDB Size, see [Table 14](#) for other RDB sizes.

NOTE 2 The number of Row Buffers can be 4 or 8. A controller may use a smaller number of Row Buffers provided that the appropriate most significant BA addresses are driven to “0”.

NOTE 3 One Row Buffer consists of a pair of one Row Address Buffer (RAB) and one Row Data Buffer (RDB), selected by Buffer Address, BA0-BA2 (CA7r-CA9r).

NOTE 4 The least significant column address C0 is implied to be zero and is not transmitted on the CA bus.

NOTE 5 Row and Column Address values on the CA bus that are not used are “don’t care.”

## 2.5.1 Three-Phase Addressing (cont'd)

**Table 14 — Addressing Dependent on RDB Size**

RDB Size	Configuration	x8	x16	x32
32 Byte	Lower Row Address	a19-a5	a19-a5	a19-a5
	Column Address	a4-a1(C4-C1)	a4-a2(C3-C1)	a4-a3(C2-C1)
64 Byte	Lower Row Address	a19-a6	a19-a6	a19-a6
	Column Address	a5-a1(C5-C1)	a5-a2(C4-C1)	a5-a3(C3-C1)
128 Byte	Lower Row Address	a19-a7	a19-a7	a19-a7
	Column Address	a6-a1(C6-C1)	a6-a2(C5-C1)	a6-a3(C4-C1)
256 Byte	Lower Row Address	a19-a8	a19-a8	a19-a8
	Column Address	a7-a1(C7-C1)	a7-a2(C6-C1)	a7-a3(C5-C1)
512 Byte	Lower Row Address	a19-a9	a19-a9	a19-a9
	Column Address	a8-a1(C8-C1)	a8-a2(C7-C1)	a8-a3(C6-C1)
1 KB	Lower Row Address	a19-a10	a19-a10	a19-a10
	Column Address	a9-a1(C9-C1)	a9-a2(C8-C1)	a9-a3(C7-C1)
2 KB	Lower Row Address	a19-a11	a19-a11	a19-a11
	Column Address	a10-a1(C10-C1)	a10-a2(C9-C1)	a10-a3(C8-C1)
4 KB	Lower Row Address	a19-a12	a19-a12	a19-a12
	Column Address	a11-a1(C11-C1)	a11-a2(C10-C1)	a11-a3(C9-C1)

NOTE 1 The least significant column address C0 is implied to be zero and is not transmitted on the CA bus.

NOTE 2 Row and Column Address values on the CA bus that are not used are “don’t care.”

### 3 Functional description

LPDDR2-S is a high-speed SDRAM device internally configured as a 4 or 8-Bank memory.

LPDDR2-N is a high-speed Non-Volatile Memory device, internally configured to have 4 or 8 Row Buffers.

These devices contain the following number of bits:

64 Mb has 67,108,864 bits  
128 Mb has 134,217,728 bits  
256 Mb has 268,435,456 bits  
512 Mb has 536,870,912 bits  
1 Gb has 1,073,741,824 bits  
2 Gb has 2,147,483,648 bits  
4 Gb has 4,294,967,296 bits  
6 Gb has 6,442,450,944 bits  
8 Gb has 8,589,934,592 bits

The following densities apply to LPDDR2-NVM devices only:

16 Gb has 17,179,869,184 bits  
32 Gb has 34,359,738,368 bits

All LPDDR2 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

LPDDR2-S2 also uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S2 effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal SDRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

LPDDR2-S4 and LPDDR2-N also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 and LPDDR2-N effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM/NVM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For LPDDR2-SX devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

For LPDDR2-N devices, accesses begin with the registration of a Preactive command, followed by an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Preactive and Activate commands are used to select the row and the Row Buffer to be accessed. The address bits registered coincident with the Read or Write command are used to select the Row Buffer and the starting column location for the burst access.

For LPDDR2-NVM devices, operations other than “array reads” are performed by accessing an overlay window that is mapped over the array space of the memory. The Overlay Window Base Address (OWBA) is programmed using the Mode Registers. The overlay window is enabled and disabled by using the Mode Register. When the overlay window is disabled, all array accesses map to the memory array. When the overlay window is enabled, reads and writes to Overlay Window within the array memory space access the Overlay Window.

Prior to normal operation, the LPDDR2 must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

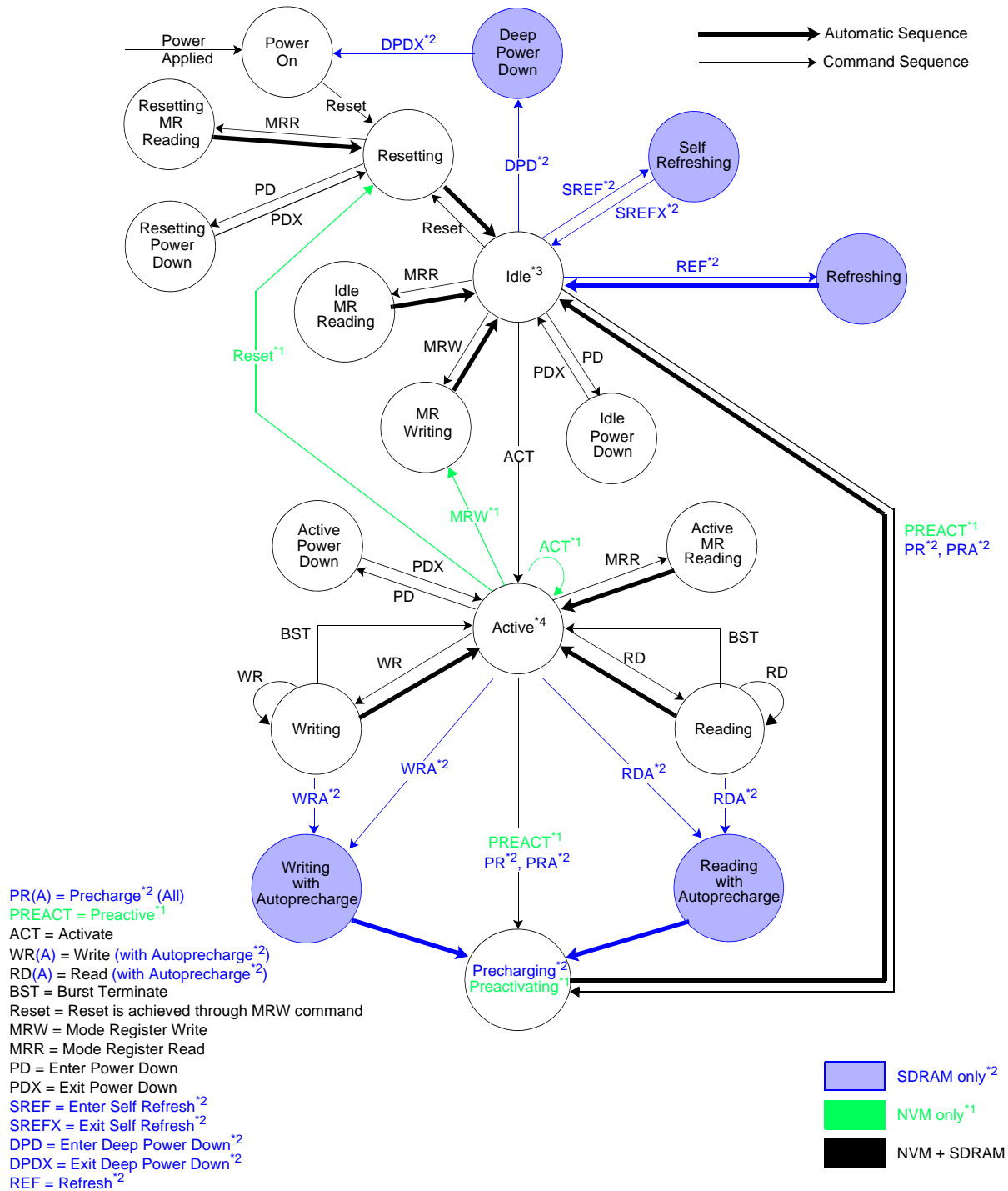
### **3.1 Simplified LPDDR2 Bus Interface State Diagram**

The simplified LPDDR2 bus interface state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see [clause 5](#).

### 3.1 Simplified LPDDR2 Bus Interface State Diagram (cont'd)



### Figure 3 — LPDDR2: Simplified Bus Interface State Diagram

NOTE 1 These transitions apply for LPDDR2-N devices only.

NOTE 2 These transitions apply for LPDDR2-SX devices only.

NOTE 3 For LPDDR2-SDRAM in the Idle state, all banks are precharged.

NOTE 4 For LPDDR2-NVM in the Active state, one or more Row Buffers have been activated.

NOTE 5 Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one Bank/Row Buffer are not captured in full detail.

NOTE 6 Resetting duration is variable. Poll DAI status bit to detect state transition to Idle.

**NOTE 7** Reset command sets all Row Address Buffers to 0x0000.

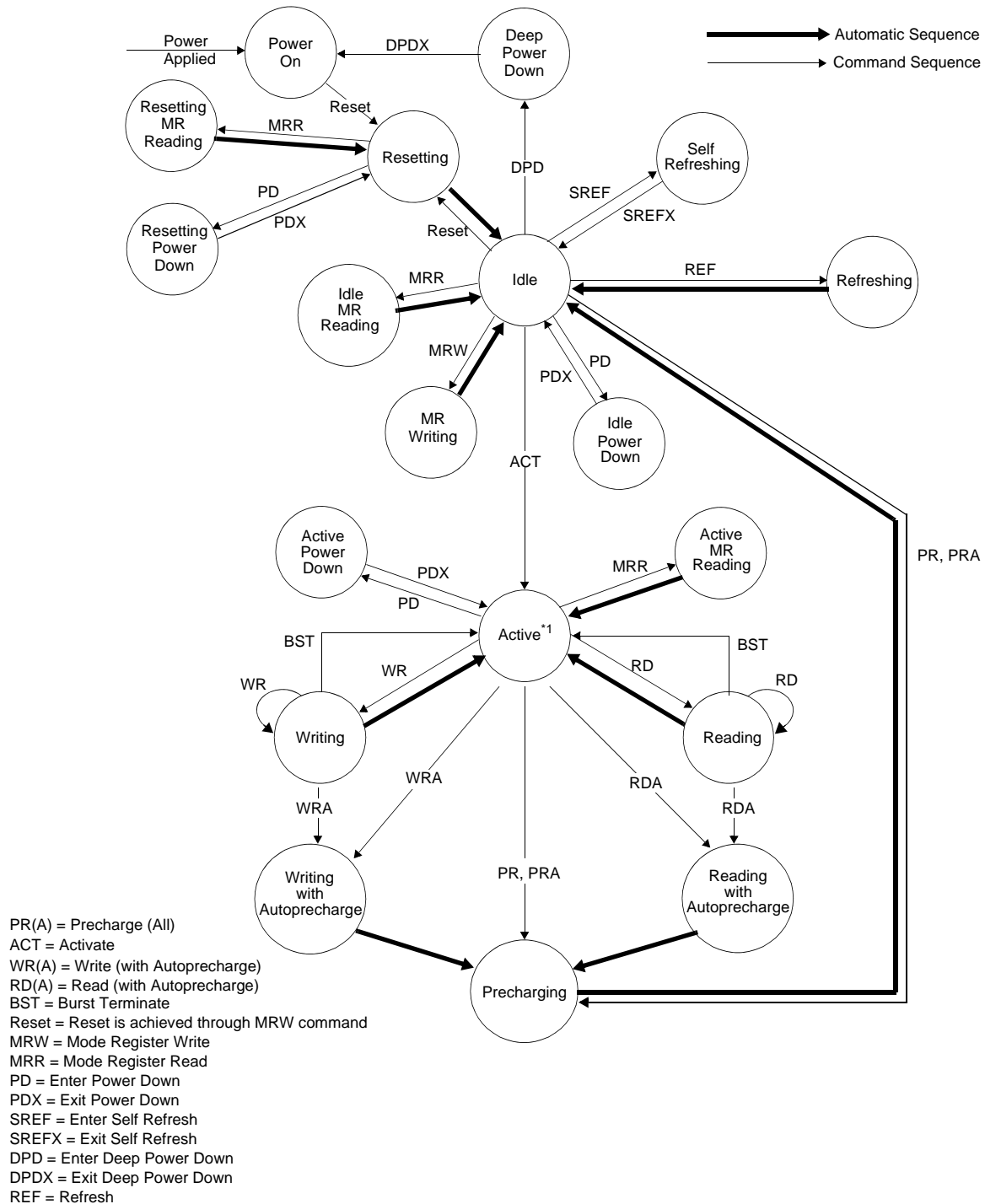
### **3.2 Simplified LPDDR2-SX State Diagram**

LPDDR2-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see [clause 5](#).

### 3.2 Simplified LPDDR2-SX State Diagram (cont'd)



NOTE 1 For LPDDR2-SDRAM in the Idle state, all banks are precharged.

### 3.3 Simplified LPDDR2-N Simplified Bus State Diagram

LPDDR2-NVM simplified bus interface state diagram provides a simplified illustration of allowed bus interface state transitions and the related commands to control them. For a more detailed definition of the device bus interface, the information provided by the state diagram should be integrated with the truth tables and timing specification.

For the command definition see clause 5

LPDDR2-NVM has two types of states: stable states, which are entered and exited with a command, and transitory states, which are entered with a command and exited automatically.

LPDDR2-NVM stable states are: Power-on, Idle, Active, Resetting Power Down, Idle Power Down, and Active Power Down.

LPDDR2-NVM transitory states are: Resetting, Resetting MR Reading, Idle MR Reading, MR Writing, Active MR Reading, Reading, Writing and Preactivating.

LPDDR2-NVM state diagram is shown in Figure 5, where each state transition, due to a command, is represented with a numbered arc.

Follows the description of all the allowed commands for any given state. The arc number of each transition is included in the description in parenthesis.

#### 3.3.1 Power On and Resetting states

- (1) After power up, the device goes in the Power On state.
- (2) The **Reset command is the only command allowed in this state, and when issued, it brings all Row Buffers (RB) into the Resetting state after  $t_{\text{INIT4}}$ .**
- (3) **Mode Register Read (MRR) command can be issued from the Resetting state. MRR allows retrieving useful information such as: memory type, memory characteristics, or the Resetting status through the DAI bit.** The device enters in Resetting Mode Register Reading state when MRR command is registered, and **goes back automatically to Resetting state after  $t_{\text{MRR}}$ .**
- (4) **Enter Power Down command brings all Row Buffers into the Resetting Power Down state.** For the complete description of Power Down entry, see 5.14.
- (5) Exit Power Down command brings all Row Buffers from the Resetting Power Down state back to the Resetting state after  $t_{\text{XP}}$ . For the complete description of Power Down exit, see 5.14.

The duration of Resetting,  $t_{\text{INIT5}}$ , is device specific and it is not defined in this document. **The memory controller shall poll DAI bit to determine the completion of the device initialization. Upon completion of device initialization, all Row Buffers are in the Idle state and all RABs have a default value of 0x0000.**

#### 3.3.2 Idle state

From the Idle state, the following commands are allowed: **Reset, Mode Register Write, Mode Register Read, Preactive, Activate and Enter Power Down.**

- (6) Reset command brings all Row Buffers into the Resetting state after  $t_{\text{INIT4}}$ .
- (7) Mode Register Write command brings all Row Buffers to the MR Writing state. All Row Buffers return to the Idle state after  $t_{\text{MRW}}$ .
- (8) Mode Register Read command brings the Row Buffer to the Idle MR Reading state. The Row Buffer goes automatically back to the Idle state after  $t_{\text{MRR}}$ .
- (9) Preactive command brings the Row Buffer to the Preactivating state. The Row Buffer goes automatically back to the Idle state after  $t_{\text{RP}}$ .



### 3.3.2 Idle state (cont'd)

(10) Activate command brings the Row Buffer from the Idle state to the Row Activating state, which is not explicitly shown in the state diagram. The Row Buffer goes automatically from the Row Activating state to the Active state after  $t_{RCD}$ .

(11) Enter Power Down command brings the Row Buffer into the Idle Power Down state. For the complete description of power down entry see 5.14.

(12) Exit Power Down command brings the Row Buffer from the Idle Power Down state back to the Idle state after  $t_{XP}$ . For the complete description of power down exit see 5.14.

### 3.3.3 Active state

From the Active state, the following commands are allowed: Reset, Mode Register Write, Mode Register Read, Preactive, Activate, Read, Write and Enter Power Down.

(13) Reset command brings all Row Buffers into the Resetting state after  $t_{INIT4}$ .

(14) Mode Register Write command brings all Row Buffers to the MR Writing state. All Row Buffers return to the Idle state after  $t_{MRW}$ .

(15) Mode Register Read command brings the Row Buffer to the Active MR Reading state. The Row Buffer goes automatically back to the Active state after  $t_{MRR}$ .

(16) Preactive command brings the Row Buffer to the Preactivating state. The Row Buffer goes automatically to the Idle state after  $t_{RP}$ .

(17) Activate command brings the Row Buffer from the Active state to the Row Activating state, which is not explicitly shown in the state diagram. The Row Buffer goes automatically back to the Active state after  $t_{RCD}$ .

(18) Read command moves the Row Buffer to the Reading state. The Row Buffer goes automatically back to the Row Active state after BL/2 clock cycles, or after a Burst Terminate command. See 5.4 for timing restrictions to apply between the Read command and a following Read, Write, Mode Register Write, Mode Register Read, Preactive, Activate or Enter Power Down commands that might occur. If a new Read command is issued within BL/2 clock cycles, the Row Buffer remains in the Reading state.

(19) Write command moves the Row Buffer to the Writing state. The Row Buffer goes automatically back to the Row Active state after BL/2 clock cycles, or after a Burst Terminate command. See 5.5 for timing restrictions to apply between the Write command and the following Write, Read, Mode Register Write, Mode Register Read, Preactive, Activate or Enter Power Down commands that might occur. If a new Write command is issued within BL/2 clock cycles, the Row buffer remains in the Writing state.

(20) Enter Power Down command brings the Row Buffer into the Active Power Down state. For the complete description of power down entry see 5.14.

(21) Exit Power Down command brings the Row Buffer from the Active Power Down state back to the Row Active state after  $t_{XP}$ . For the complete description of power down exit see 5.14.

## 3.3.3 Active state (cont'd)

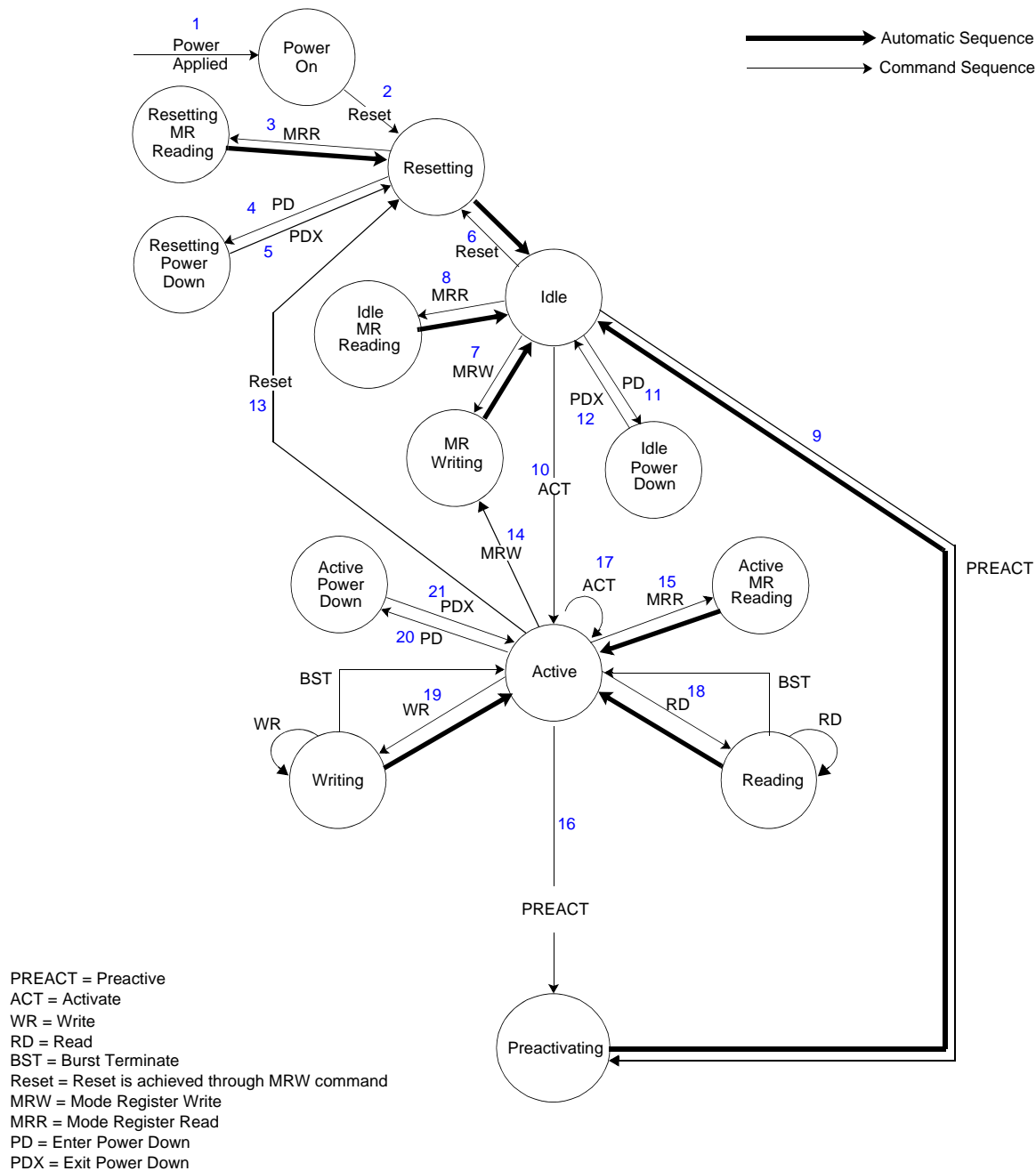


Figure 5 — LPDDR2-N: Simplified Bus Interface State Diagram

- NOTE 1 For LPDDR2-NVM in the Active state, one or more Row Buffers have been activated.
- NOTE 2 Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one Row Buffer are not captured in full detail.
- NOTE 3 Resetting duration is variable. Poll DAI status bit to detect state transition to Idle.
- NOTE 4 Reset command sets all Row Address Buffers to 0x0000.

### 3.4 Power-up, Initialization, and Power-Off

LPDDR2 Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

#### 3.4.1 Power Ramp and Device Initialization

The following sequence shall be used to power up an LPDDR2 device. Unless specified otherwise, these steps are mandatory and apply to S2, S4 and N devices.

##### 1. Power Ramp

While applying power (after  $T_a$ ), CKE shall be held at a logic low level ( $= < 0.2 \times VDDCA$ ), all other inputs shall be between  $VIL_{min}$  and  $VIH_{max}$ . The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

On or before the completion of the power ramp ( $T_b$ ) CKE must be held low.

DQ, DM, DQS<sub>t</sub> and DQS<sub>c</sub> voltage levels must be between  $VSSQ$  and  $VDDQ$  during voltage ramp to avoid latch-up. CK<sub>t</sub>, CK<sub>c</sub>, CS<sub>n</sub>, and CA input levels must be between  $VSSCA$  and  $VDDCA$  during voltage ramp to avoid latch-up.

The following conditions apply:

$T_a$  is the point where *any* power supply first reaches 300 mV.

After  $T_a$  is reached,  $VDD1$  must be greater than  $VDD2 - 200$  mV.

After  $T_a$  is reached,  $VDD1$  and  $VDD2$  must be greater than  $VDDCA - 200$  mV.

After  $T_a$  is reached,  $VDD1$  and  $VDD2$  must be greater than  $VDDQ - 200$  mV.

After  $T_a$  is reached,  $VREF$  must always be less than all other supply voltages.

The voltage difference between any of  $VSS$ ,  $VSSQ$ , and  $VSSCA$  pins may not exceed 100 mV.

The above conditions apply between  $T_a$  and power-off (controlled or uncontrolled).

$T_b$  is the point when all supply voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.

For supply and reference voltage operating conditions, see Table 69, Table 70, and Table 71.

Power ramp duration  $t_{INIT0}$  ( $T_b - T_a$ ) must be no greater than 20 ms.

NOTE  $VDD2$  is not present in some systems. Rules related to  $VDD2$  in those cases do not apply.

##### 2. CKE and clock:

Beginning at  $T_b$ , CKE must remain low for at least  $t_{INIT1} = 100$  ns, after which it may be asserted high. Clock must be stable at least  $t_{INIT2} = 5 \times t_{CK}$  prior to the first low to high transition of CKE ( $T_c$ ). CKE, CS<sub>n</sub> and CA inputs must observe setup and hold time ( $t_{IS}$ ,  $t_{IH}$ ) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

The clock period shall be within the range defined for  $t_{CKb}$  (18 ns to 100 ns), if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met. Furthermore, some AC parameters (e.g.  $t_{DQSCk}$ ) may have relaxed timings (e.g.  $t_{DQSCkb}$ ) before the system is appropriately configured.

While keeping CKE high, issue NOP commands for at least  $t_{INIT3} = 200$  us. ( $T_d$ ).

##### 3. Reset command:

After  $t_{INIT3}$  is satisfied, a MRW(Reset) command shall be issued ( $T_d$ ). The memory controller may optionally issue a Precharge-All command (for LPDDR2-SX) or Preactive (for LPDDR2-N) prior to the MRW Reset command. For LPDDR2-N devices, the subsequent MRW Reset command will set each Row Address Buffers (RAB) to 0x0000 overwriting the value stored by the previous preactive command. Wait for at least  $t_{INIT4} = 1$   $\mu$ s while keeping CKE asserted and issuing NOP commands.

### 3.4.1 Power Ramp and Device Initialization (cont'd)

#### 4. Mode Registers Reads and Device Auto-Initialization (DAI) polling:

After  $t_{\text{INIT4}}$  is satisfied (**Te**) only MRR commands and power-down entry/exit commands are allowed.

Therefore, after **Te**, CKE may go low in accordance to Power-Down entry and exit specification (see 5.14).

The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of  $t_{\text{INIT5}}$  before proceeding.

As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.

After the DAI-bit (MR0, "DAI") is set to zero "DAI complete" by the memory device, the device is in idle state (**Tf**). The state of the DAI status bit can be determined by an MRR command to MR0.

All SDRAM devices will set the DAI-bit no later than  $t_{\text{INIT5}}$  (10 us) after the Reset command. The memory controller shall wait a minimum of  $t_{\text{INIT5}}$  or until the DAI-bit is set before proceeding.

For NVM devices, repetitive polling of the DAI-Bit is required to determine when this bit has internally been set to zero "DAI complete" by the memory device. A Value for  $t_{\text{INIT5}}$  value is not defined for NVMs in this document because it is device dependent. The only way to determine when Device Auto-Initialization is complete is to poll DAI. To obtain the shortest boot up time and ensure compatibility with any future NVM device it is recommended to not rely on any predetermined  $t_{\text{INIT5}}$  value.

After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 "Device Information" etc.).

#### 5. ZQ Calibration:

After  $t_{\text{INIT5}}$  (**Tf**), an MRW ZQ Initialization Calibration command may be issued to the memory (MR10). For LPDDR2 devices which do not support the ZQ Calibration command, this command shall be ignored. This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after  $t_{\text{ZQINIT}}$ .

#### 6. Normal Operation:

After  $t_{\text{ZQINIT}}$  (**Tg**), MRW commands shall be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration.

To support simple boot from the NVM, some Mode Registers are reset to default values during Device Auto-Initialization. See the Mode Register section of this specification for default values.

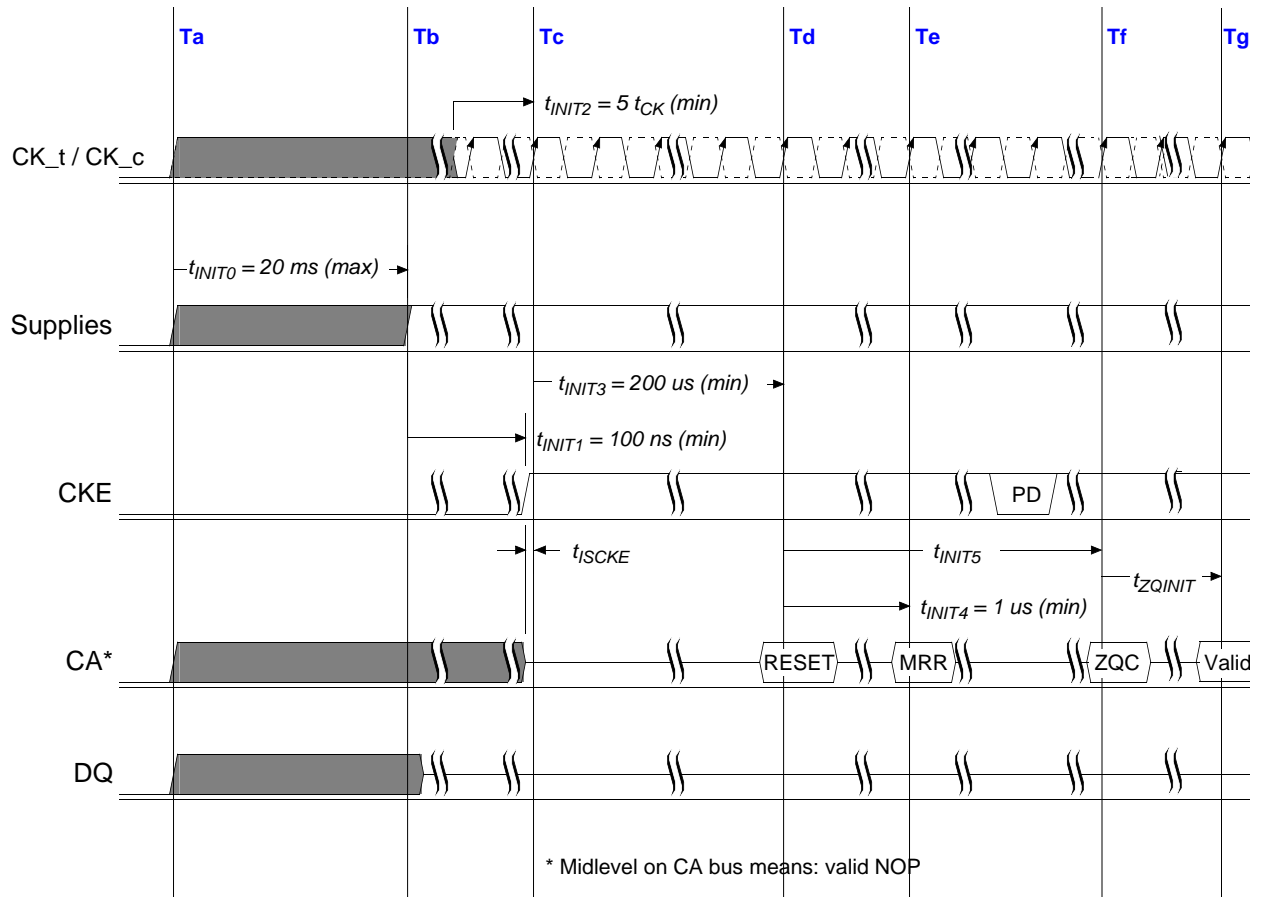
The LPDDR2 device will now be in IDLE state and ready for any valid command.

After **Tg**, the clock frequency may be changed according to the clock frequency change procedure described in 5.16.

### 3.4.1 Power Ramp and Device Initialization (cont'd)

**Table 15 — Timing Parameters for initialization**

Symbol	Value		Unit	Comment
	min	max		
$t_{INIT0}$		20	ms	Maximum Power Ramp Time
$t_{INIT1}$	100		ns	Minimum CKE low time after completion of power ramp
$t_{INIT2}$	5		tCK	Minimum stable clock before first CKE high
$t_{INIT3}$	200		μs	Minimum Idle time after first CKE assertion
$t_{INIT4}$	1		μs	Minimum Idle time after Reset command
$t_{INIT5}$		S: 10	μs	Maximum duration of Device Auto-Initialization
		N: vendor	μs	
$t_{ZQINIT}$	1		μs	ZQ Initial Calibration for LPDDR2-S4 and LPDDR2-N devices
$t_{CKb}$	18	100	ns	Clock cycle time during boot



**Figure 6 — Power Ramp and Initialization Sequence**

### 3.4.2 Initialization after Reset (without Power ramp)

If the RESET command is issued outside the power up initialization sequence, the reinitialization procedure shall begin with step 3 (Td).

### 3.4.3 Power-off Sequence

The following sequence shall be used to power off the LPDDR2 device. Unless specified otherwise, these steps are mandatory and apply to S2, S4 and N devices.

While removing power, CKE shall be held at a logic low level ( $\leq 0.2 \times VDDCA$ ), all other inputs shall be between  $VIL_{min}$  and  $VIH_{max}$ . The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

For LPDDR2-N devices, all embedded operations must be finished or aborted and the device must be in the ready state (Status Register, bit 7 = “1”) prior to Power-off.

DQ, DM, DQS<sub>t</sub>, and DQS<sub>c</sub> voltage levels must be between VSSQ and VDDQ during power off sequence to avoid latch-up. CK<sub>t</sub>, CK<sub>c</sub>, CS<sub>n</sub>, and CA input levels must be between VSSCA and VDDCA during power off sequence to avoid latch-up.

T<sub>x</sub> is the point where any power supply decreases under its minimum value specified in the DC operating condition table, see 7.1.

T<sub>z</sub> is the point where *all* power supplies are below 300 mV. After T<sub>z</sub>, the device is powered off.

The time between T<sub>x</sub> and T<sub>z</sub> (t<sub>POFF</sub>) shall be less than 2s.

The following conditions apply:

Between T<sub>x</sub> and T<sub>z</sub>, VDD1 must be greater than VDD2 - 200 mV.

Between T<sub>x</sub> and T<sub>z</sub>, VDD1 and VDD2 must be greater than VDDCA - 200 mV.

Between T<sub>x</sub> and T<sub>z</sub>, VDD1 and VDD2 must be greater than VDDQ - 200 mV.

Between T<sub>x</sub> and T<sub>z</sub>, VREF must always be less than all other supply voltages.

The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100 mV.

For supply and reference voltage operating conditions, see Table 69, Table 70, and Table 71.

NOTE VDD2 is not present in some systems. Rules related to VDD2 in those cases do not apply.

**Table 16 — Timing Parameters Power-Off**

Symbol	Value		Unit	Comment
	min	max		
t <sub>POFF</sub>	-	2	s	Maximum Power-Off ramp time

### 3.4.4 Uncontrolled Power-Off Sequence

The following sequence shall be used to power off the LPDDR2 device under uncontrolled condition. Unless specified otherwise, these steps are mandatory and apply to S2, S4 and N devices.

T<sub>x</sub> is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.

T<sub>z</sub> is the point where all power supply first reaches 300 mV. After T<sub>z</sub>, the device is powered off.

The time between T<sub>x</sub> and T<sub>z</sub> (t<sub>POFF</sub>) shall be less than 2s. The relative level between supply voltages are uncontrolled during this period.

VDD1 and VDD2 shall decrease with a slope lower than 0.5 V/usec between T<sub>x</sub> and T<sub>z</sub>.

Uncontrolled power off sequence can be applied only up to 400 times in the life of the device.

### 3.5 Mode Register Definition

#### 3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM

**Table 17** shows the 16 common mode registers for LPDDR2 SDRAM and NVM. **Table 18** shows only LPDDR2 SDRAM mode registers and **Table 19** shows only LPDDR2 NVM mode registers. Additionally **Table 20** shows RFU mode registers and Reset Command.

Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written.

Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

**Table 17 — Mode Register Assignment in LPDDR2 SDRAM/NVM(Common part)**

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link	
0	00 <sub>H</sub>	Device Info.	R	(RFU)			RZQI (optional)		DNVI	DI	DAI	<a href="#">go to MR0</a>	
1	01 <sub>H</sub>	Device Feature 1	W	nWR (for AP)			WC	BT	BL			<a href="#">go to MR1</a>	
2	02 <sub>H</sub>	Device Feature 2	W	(RFU)				RL & WL				<a href="#">go to MR2</a>	
3	03 <sub>H</sub>	I/O Config-1	W	(RFU)				DS				<a href="#">go to MR3</a>	
4	04 <sub>H</sub>	SDRAM Refr. R.	R	TUF	(RFU)				Refresh Rate				<a href="#">go to MR4</a>
		NVM Temp. Alert	R	TUF	(RFU)				NVM Temp. Alert				
5	05 <sub>H</sub>	Basic Config-1	R	LPDDR2 Manufacturer ID								<a href="#">go to MR5</a>	
6	06 <sub>H</sub>	Basic Config-2	R	Revision ID1								<a href="#">go to MR6</a>	
7	07 <sub>H</sub>	Basic Config-3	R	Revision ID2								<a href="#">go to MR7</a>	
8	08 <sub>H</sub>	Basic Config-4	R	I/O width		Density				Type			<a href="#">go to MR8</a>
9	09 <sub>H</sub>	Test Mode	W	Vendor-Specific Test Mode								<a href="#">go to MR9</a>	
10	0A <sub>H</sub>	IO Calibration	W	Calibration Code								<a href="#">go to MR10</a>	
11:15	0B <sub>H</sub> ~0F <sub>H</sub>	(reserved)		(RFU)								<a href="#">go to MR11</a>	

**Table 18 — Mode Register Assignment in LPDDR2 SDRAM/NVM (SDRAM part)**

MR#	MA <7:0>	Function	access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
16	10 <sub>H</sub>	PASR_Bank (S4)	W	Bank Mask								go to MR16
		PASR_Bank (S2)		(RFU)						PASR		
17	11 <sub>H</sub>	PASR_Seg	W	Segment Mask (S4 SDRAM only)								go to MR17
18-19	12 <sub>H</sub> -13 <sub>H</sub>	(Reserved)		(RFU)								go to MR18

## 3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

Table 19 — Mode Register Assignment in LPDDR2 SDRAM/NVM (NVM part)

MR#	MA <7:0>	Function	access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
20	14 <sub>H</sub>	NVM Geometry	R	(RFU)		tRCD De-Rating		RB Number	RDB size			<a href="#">go to MR20</a>
21	15 <sub>H</sub>	NVM tRCD	R	tRCD Value (2nd order)				tRCD Value (1st order)				<a href="#">go to MR21</a>
22-23	16 <sub>H</sub> -17 <sub>H</sub>	(Reserved)		(RFU)								<a href="#">go to MR22</a>
24	18 <sub>H</sub>	Overlay Window Enable	R/W	(RFU)						OWD	OWE	<a href="#">go to MR24</a>
25	19 <sub>H</sub>	OW Base-Addr 1	R/W	OW base-addr 31 (a19 ~ a13)							0	<a href="#">go to MR25</a>
26	1A <sub>H</sub>	OW Base-Addr 2	R/W	OW base-addr 2 (a27 ~ a20)								
27	1B <sub>H</sub>	OW Base-Addr 3	R/W	(RFU)				OW base-addr 3 (a31 ~ a28)				
28	1C <sub>H</sub>	(Reserved)		(RFU)								<a href="#">go to MR28</a>
29	1D <sub>H</sub>	DNV Long Delay	R	tDNV Value (2nd order)				tDNV Value (1st order)				<a href="#">go to MR29</a>
30-31	1E <sub>H</sub> -1F <sub>H</sub>	(Reserved)		(RFU)								<a href="#">go to MR30</a>

Table 20 — Mode Register Assignment in LPDDR2 SDRAM/NVM  
(DQ Calibration and Reset Command)

MR#	MA <7:0>	Function	access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
32	20 <sub>H</sub>	DQ Calibration Pattern A	R	See “DQ Calibration” on page 131								<a href="#">go to MR32</a>
33:39	21 <sub>H</sub> -27 <sub>H</sub>	(Do Not Use)										<a href="#">go to MR33</a>
40	28 <sub>H</sub>	DQ Calibration Pattern B	R	See “DQ Calibration” on page 131								<a href="#">go to MR40</a>
41:47	29 <sub>H</sub> -2F <sub>H</sub>	(Do Not Use)										<a href="#">go to MR41</a>
48:62	30 <sub>H</sub> -3E <sub>H</sub>	(Reserved)		(RFU)								<a href="#">go to MR48</a>
63	3F <sub>H</sub>	Reset	W	X								<a href="#">go to MR63</a>
64:126	40 <sub>H</sub> -7E <sub>H</sub>	(Reserved)		(RFU)								<a href="#">go to MR64</a>
127	7F <sub>H</sub>	(Do Not Use)										<a href="#">go to MR127</a>
128:190	80 <sub>H</sub> -BE <sub>H</sub>	(Reserved for Vendor Use)		(RFU)								<a href="#">go to MR128</a>
191	BF <sub>H</sub>	(Do Not Use)										<a href="#">go to MR191</a>
192:254	C0 <sub>H</sub> -FE <sub>H</sub>	(Reserved for Vendor Use)		(RFU)								<a href="#">go to MR192</a>
255	FF <sub>H</sub>	(Do Not Use)										<a href="#">go to MR255</a>

The following notes apply to Tables 17-20:

NOTE 1 RFU bits shall be set to ‘0’ during Mode Register writes.

NOTE 2 RFU bits shall be read as ‘0’ during Mode Register reads.

NOTE 3 All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS<sub>t</sub>, DQS<sub>c</sub> shall be toggled.

NOTE 4 All Mode Registers that are specified as RFU shall not be written.

NOTE 5 See Vendor Device Datasheets for details on Vendor Specific Mode Registers.

NOTE 6 Writes to read-only registers shall have no impact on the functionality of the device.



### 3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

**MR0 Device Information (MA<7:0> = 00<sub>H</sub>):**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)			RZQI (optional)		DNVI	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	<b>0<sub>B</sub></b> : DAI complete <b>1<sub>B</sub></b> : DAI still in progress	
DI (Device Information)	Read-only	OP1	<b>0<sub>B</sub></b> : S2 or S4 SDRAM <b>1<sub>B</sub></b> : NVM	
DNVI (Data Not Valid Information)	Read-only	OP2	<b>0<sub>B</sub></b> : DNV not supported <b>1<sub>B</sub></b> : DNV supported	1,2
RZQI (Built in Self Test for RZQ Information)	Read-only	OP4:OP3	<b>00<sub>B</sub></b> : RZQ self test not supported <b>01<sub>B</sub></b> : ZQ-pin may connect to VDDCA or float <b>10<sub>B</sub></b> : ZQ-pin may short to GND <b>11<sub>B</sub></b> : ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)	3

NOTE 1 LPDDR2 SDRAM will not implement DNV functionality.

NOTE 2 If DNV functionality is not implemented, the device shall not drive the DM/DNV signals.

NOTE 3 RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.

NOTE 4 If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

NOTE 5 In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per NOTE 4), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.

NOTE 6 In the case of the ZQ self-test returning a value of **11<sub>B</sub>**, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240-ohm +/-1%).

**MR1\_Device Feature 1 (MA<7:0> = 01<sub>H</sub>):**

		OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
		nWR (for AP)			WC	BT	BL		
BL	Write-only	OP<2:0>		<b>010<sub>B</sub></b> : BL4 (default) <b>011<sub>B</sub></b> : BL8 <b>100<sub>B</sub></b> : BL16 <b>All others</b> : reserved					
BT	Write-only	OP<3>		<b>0<sub>B</sub></b> : Sequential (default) <b>1<sub>B</sub></b> : Interleaved (allowed for SDRAM only)					1
WC	Write-only	OP<4>		<b>0<sub>B</sub></b> : Wrap (default) <b>1<sub>B</sub></b> : No wrap (allowed for SDRAM BL4 only)					
nWR	Write-only	OP<7:5>		<b>001<sub>B</sub></b> : nWR=3 (default) <b>010<sub>B</sub></b> : nWR=4 <b>011<sub>B</sub></b> : nWR=5 <b>100<sub>B</sub></b> : nWR=6 <b>101<sub>B</sub></b> : nWR=7 <b>110<sub>B</sub></b> : nWR=8 <b>All others</b> : reserved					2

NOTE 1 BL 16, interleaved is not an official combination to be supported.

NOTE 2 Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by  $RU(tWR/tCK)$ .

NOTE 3 BL16 is not supported by LPDDR2-NVM with Row Data Buffer size equal to 32-Byte and Data Bus Width equal to 32-bit.

NOTE 4 OP7:OP5 are reserved for LPDDR2-NVM.

### 3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

**Table 21 — Burst Sequence by BL, BT, and WC**

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence																
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
X	X	0 <sub>B</sub>	0 <sub>B</sub>	wrap	any	4	0	1	2	3													
X	X	1 <sub>B</sub>	0 <sub>B</sub>				2	3	0	1													
X	X	X	0 <sub>B</sub>	nw	any		y	y+1	y+2	y+3													
X	0 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>	wrap	seq	8	0	1	2	3	4	5	6	7									
X	0 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>				2	3	4	5	6	7	0	1									
X	1 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>				4	5	6	7	0	1	2	3									
X	1 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>				6	7	0	1	2	3	4	5									
X	0 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>		int		0	1	2	3	4	5	6	7									
X	0 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>				2	3	0	1	6	7	4	5									
X	1 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>				4	5	6	7	0	1	2	3									
X	1 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>				6	7	4	5	2	3	0	1									
X	X	X	0 <sub>B</sub>	nw	any	illegal (not allowed)																	
0 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0 <sub>B</sub>	0 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	
0 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	
0 <sub>B</sub>	1 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	
1 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	
1 <sub>B</sub>	0 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	
1 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	
1 <sub>B</sub>	1 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	
X	X	X	0 <sub>B</sub>		int	illegal (not allowed)																	
X	X	X	0 <sub>B</sub>	nw	any	illegal (not allowed)																	

1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C1 - C0.
3. For BL=8, the burst address represents C2 - C0.
4. For BL=16, the burst address represents C3 - C0.
5. For no-wrap (nw), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary. The variable y may start at any address with C0 equal to 0 and may not start at any address in [Table 22](#) for the respective density and bus width combinations.

## 3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

Table 22 — LPDDR2-SX Non Wrap Restrictions

	64Mb	128Mb/256Mb	512Mb/1Gb/2Gb	4Gb/6Gb/8Gb
Not across full page boundary				
x8	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001	FFE, FFF, 000, 001
x16	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001
x32	7E, 7F, 00, 01	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001
Not across sub page boundary				
x8	07E, 07F, 080, 081	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401
	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401	7FE, 7FF, 800, 801
	17E, 17F, 180, 181	2FE, 2FF, 300, 301	5FE, 5FF, 600, 601	BFE, BFF, C00, C01
x16	7E, 7F, 80, 81	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401
x32	None	None	None	None

NOTE 1 Non-wrap BL=4 data-orders shown above are prohibited.

**MR2 Device Feature 2 (MA<7:0> = 02<sub>H</sub>):**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

RL & WL	Write-only	OP<3:0>	<b>0001<sub>B</sub></b> : RL = 3 / WL = 1 (default) <b>0010<sub>B</sub></b> : RL = 4 / WL = 2 <b>0011<sub>B</sub></b> : RL = 5 / WL = 2 <b>0100<sub>B</sub></b> : RL = 6 / WL = 3 <b>0101<sub>B</sub></b> : RL = 7 / WL = 4 <b>0110<sub>B</sub></b> : RL = 8 / WL = 4 <b>All others</b> : reserved
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**MR3 I/O Configuration 1 (MA<7:0> = 03<sub>H</sub>):**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP<3:0>	<b>0000<sub>B</sub></b> : reserved <b>0001<sub>B</sub></b> : 34.3-ohm typical <b>0010<sub>B</sub></b> : 40-ohm typical (default) <b>0011<sub>B</sub></b> : 48-ohm typical <b>0100<sub>B</sub></b> : 60-ohm typical <b>0101<sub>B</sub></b> : reserved for 68.6-ohm typical <b>0110<sub>B</sub></b> : 80-ohm typical <b>0111<sub>B</sub></b> : 120-ohm typical (optional) <b>All others</b> : reserved
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### 3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

#### MR4 Device Temperature (MA<7:0> = 04<sub>H</sub>)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF			(RFU)				SDRAM Refresh Rate
TUF			(RFU)				NVM Temperature Alert

SDRAM Refresh Rate	Read-only	OP<2:0>	<b>000<sub>B</sub></b> : SDRAM Low temperature operating limit exceeded <b>001<sub>B</sub></b> : 4x t <sub>REFI</sub> , 4x t <sub>REFIpb</sub> , 4x t <sub>REFW</sub> <b>010<sub>B</sub></b> : 2x t <sub>REFI</sub> , 2x t <sub>REFIpb</sub> , 2x t <sub>REFW</sub> <b>011<sub>B</sub></b> : 1x t <sub>REFI</sub> , 1x t <sub>REFIpb</sub> , 1x t <sub>REFW</sub> (<=85°C) <b>100<sub>B</sub></b> : Reserved <b>101<sub>B</sub></b> : 0.25x t <sub>REFI</sub> , 0.25x t <sub>REFIpb</sub> , 0.25x t <sub>REFW</sub> , do not de-rate SDRAM AC timing <b>110<sub>B</sub></b> : 0.25x t <sub>REFI</sub> , 0.25x t <sub>REFIpb</sub> , 0.25x t <sub>REFW</sub> , de-rate SDRAM AC timing <b>111<sub>B</sub></b> : SDRAM High temperature operating limit exceeded
NVM Temperature Alert	Read-only	OP<2:0>	<b>000<sub>B</sub></b> : NVM Low temperature operating limit exceeded <b>001<sub>B</sub></b> : Reserved <b>010<sub>B</sub></b> : Reserved <b>011<sub>B</sub></b> : Temperature Alert not active, do not de-rate NVM AC timing (<=85°C) <b>100<sub>B</sub></b> : Temperature Alert not active, de-rate NVM AC timing <b>101<sub>B</sub></b> : Temperature Alert active, do not de-rate NVM AC timing <b>110<sub>B</sub></b> : Temperature Alert active, de-rate NVM AC timings <b>111<sub>B</sub></b> : NVM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	<b>0<sub>B</sub></b> : OP<2:0> value has not changed since last read of MR4. <b>1<sub>B</sub></b> : OP<2:0> value has changed since last read of MR4.

NOTE 1 A Mode Register Read from MR4 will reset OP7 to '0'.

NOTE 2 OP7 is reset to '0' at power-up. OP<2:0> bits are undefined after power-up.

NOTE 3 If OP2 equals '1', the device temperature is greater than 85°C.

NOTE 4 OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.

NOTE 5 LPDDR2 might not operate properly when OP[2:0] = 000<sub>B</sub> or 111<sub>B</sub>.

NOTE 6 For specified operating temperature range and maximum operating temperature refer to [Table 72](#).

NOTE 7 LPDDR2-SX devices shall be de-rated by adding 1.875 ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in [Table 103](#). Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.

NOTE 8 LPDDR2-NVM devices shall be de-rated by adding the value found at location OP5:OP4 in MR20 to the following core timing parameters: tRCD, tRC, tRAS, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in [Table 103](#). Prevailing clock frequency spec and related setup and hold timings remain unchanged.

NOTE 9 See [5.12.1](#) for information on the recommended frequency of reading MR4.

**3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)****MR5 Basic Configuration 1 (MA<7:0> = 05<sub>H</sub>):**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							
LPDDR2 Manufacturer ID	Read-only	OP<7:0>	0000 0000B : Reserved				
			0000 0001B : Samsung				
			0000 0010B : Qimonda				
			0000 0011B : Elpida				
			0000 0100B : Etron				
			0000 0101B : Nanya				
			0000 0110B : Hynix				
			0000 0111B : Mosel				
			0000 1000B : Winbond				
			0000 1001B : ESMT				
			0000 1010B : Reserved				
			0000 1011B : Spansion				
			0000 1100B : SST				
			0000 1101B : ZMOS				
			0000 1110B : Intel				
			1111 1110B : Numonyx				
			1111 1111B : Micron				
			All Others : Reserved				

**MR6 Basic Configuration 2 (MA<7:0> = 06<sub>H</sub>):**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							
Revision ID1	Read-only	OP<7:0>	00000000 <sub>B</sub> : A-version				

NOTE 1 MR6 is Vendor Specific.

**MR7 Basic Configuration 3 (MA<7:0> = 07<sub>H</sub>):**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							
Revision ID2	Read-only	OP<7:0>	00000000 <sub>B</sub> : A-version				

NOTE 1 MR7 is Vendor Specific.

### 3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

#### MR8 Basic Configuration 4 (MA<7:0> = 08B<sub>H</sub>):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width			Density			Type	

Type	Read-only	OP<1:0>	<b>00<sub>B</sub></b> : S4 SDRAM <b>01<sub>B</sub></b> : S2 SDRAM <b>10<sub>B</sub></b> : N NVM <b>11<sub>B</sub></b> : Reserved	
Density	Read-only	OP<5:2>	<b>0000<sub>B</sub></b> : 64Mb <b>0001<sub>B</sub></b> : 128Mb <b>0010<sub>B</sub></b> : 256Mb <b>0011<sub>B</sub></b> : 512Mb <b>0100<sub>B</sub></b> : 1Gb <b>0101<sub>B</sub></b> : 2Gb <b>0110<sub>B</sub></b> : 4Gb <b>1110<sub>B</sub></b> : 6Gb <b>0111<sub>B</sub></b> : 8Gb <b>1000<sub>B</sub></b> : 16Gb <b>1001<sub>B</sub></b> : 32Gb <b>all others</b> : reserved	
I/O width	Read-only	OP<7:6>	<b>00<sub>B</sub></b> : x32 <b>01<sub>B</sub></b> : x16 <b>10<sub>B</sub></b> : x8 <b>11<sub>B</sub></b> : not used	

#### MR9 Test Mode (MA<7:0> = 09<sub>H</sub>):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

#### MR10 Calibration (MA<7:0> = 0A<sub>H</sub>):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							
Calibration Code	Write-only	OP<7:0>	<b>0xFF</b> : Calibration command after initialization <b>0xAB</b> : Long calibration <b>0x56</b> : Short calibration <b>0xC3</b> : ZQ Reset <b>others</b> : Reserved				

NOTE 1 Host processor shall not write MR10 with “Reserved” values

NOTE 2 LPDDR2 devices shall ignore calibration command when a “Reserved” value is written into MR10.

NOTE 3 See AC timing table for the calibration latency.

NOTE 4 If ZQ is connected to V<sub>SSCA</sub> through R<sub>ZQ</sub>, either the ZQ calibration function (see 5.13.4) or default calibration (through the ZQreset command) is supported. If ZQ is connected to V<sub>DDCA</sub>, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

NOTE 5 LPDDR2 devices that do not support calibration shall ignore the ZQ Calibration command.

NOTE 6 Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

### 3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

**MR11:15 (Reserved) (MA<7:0> = 0B<sub>H</sub>-0F<sub>H</sub>):**

**MR16\_PASR\_Bank Mask (MA<7:0> = 010<sub>H</sub>): S2 and S4 SDRAM only**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
S2 SDRAM	(RFU)						PASR	
S4 SDRAM	Bank Mask (4-bank or 8-bank)							

#### S2 SDRAM:

PASR Map	Write-only	OP<1:0>	<b>00<sub>B</sub></b> : Full array (default) <b>01<sub>B</sub></b> : 1/2 array - BA1=0 for 4-banks, BA2=0 for 8-banks <b>10<sub>B</sub></b> : 1/4 array - BA1=BA0=0 for 4-banks, BA2=BA1=0 for 8-banks <b>11<sub>B</sub></b> : 1/8 array - Not used for 4-banks, BA2=BA1=BA0=0 for 8-banks	
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#### S4 SDRAM:

Bank <7:0> Mask	Write-only	OP<7:0>	<b>0<sub>B</sub></b> : refresh enable to the bank (=unmasked, default) <b>1<sub>B</sub></b> : refresh blocked (=masked)	1
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1. For 4-bank S4 SDRAM, only OP<3:0> are used.

OP	Bank Mask	4-Bank S4 SDRAM	8-Bank S4 SDRAM
0	XXXXXXX1	<b>Bank 0</b>	<b>Bank 0</b>
1	XXXXXX1X	<b>Bank 1</b>	<b>Bank 1</b>
2	XXXXX1XX	<b>Bank 2</b>	<b>Bank 2</b>
3	XXXX1XXX	<b>Bank 3</b>	<b>Bank 3</b>
4	XXX1XXXX	-	<b>Bank 4</b>
5	XX1XXXXX	-	<b>Bank 5</b>
6	X1XXXXXX	-	<b>Bank 6</b>
7	1XXXXXXX	-	<b>Bank 7</b>



### 3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

#### MR17\_PASR\_Segment Mask (MA<7:0> = 011<sub>H</sub>): 1Gb ~ 8Gb S4 SDRAM only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							
Segment <7:0> Mask	Write-only	OP<7:0>	<b>0<sub>B</sub></b> : refresh enable to the segment (=unmasked, default) <b>1<sub>B</sub></b> : refresh blocked (=masked)				

			1Gb	2Gb,4Gb,6Gb	8Gb
Segment	OP	Segment Mask	R12:10	R13:11	R14:12
0	0	XXXXXXX1	<b>000<sub>B</sub></b>		
1	1	XXXXXX1X	<b>001<sub>B</sub></b>		
2	2	XXXXX1XX	<b>010<sub>B</sub></b>		
3	3	XXXX1XXX	<b>011<sub>B</sub></b>		
4	4	XXX1XXXX	<b>100<sub>B</sub></b>		
5	5	XX1XXXXX	<b>101<sub>B</sub></b>		
6	6	X1XXXXXX	<b>110<sub>B</sub></b>		
7	7	1XXXXXXX	<b>111<sub>B</sub></b>		

NOTE This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment

#### MR18-19\_Reserved (MA<7:0> = 012<sub>H</sub> - 013<sub>H</sub>):

#### MR20\_NVM Geometry (MA<7:0> = 014<sub>H</sub>): NVM only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)		tRCD De-Rating		RB Number	RDB size		

RDB Size	Read-only	OP<2:0>	<b>000<sub>B</sub></b> : 32B <b>001<sub>B</sub></b> : 64B <b>010<sub>B</sub></b> : 128B <b>011<sub>B</sub></b> : 256B <b>100<sub>B</sub></b> : 512B <b>101<sub>B</sub></b> : 1024B <b>110<sub>B</sub></b> : 2048B <b>111<sub>B</sub></b> : 4096B	
RB Number	Read-only	OP<3>	<b>0<sub>B</sub></b> : 4 Row Buffers <b>1<sub>B</sub></b> : 8 Row Buffers	
tRCD De-rating (t <sub>NVMDERATING</sub> )	Read-only	OP<5:4>	<b>00<sub>B</sub></b> : 0 ns <b>01<sub>B</sub></b> : 1.875 ns <b>10<sub>B</sub></b> : 3.75 ns <b>11<sub>B</sub></b> : 7.5 ns	

**3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)****MR21 NVM tRCD (MA<7:0> = 15<sub>H</sub>): NVM only**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
t <sub>RCD</sub> Value (2nd order)				t <sub>RCD</sub> Value (1st order)			

t <sub>RCD</sub> Value (1st order = value ns)	Read-only	OP<3:0>	0000 <sub>B</sub> : 0ns	0001 <sub>B</sub> : 1ns	
			0010 <sub>B</sub> : 2ns	0011 <sub>B</sub> : 3ns	
			0100 <sub>B</sub> : 4ns	0101 <sub>B</sub> : 5ns	
			0110 <sub>B</sub> : 6ns	0111 <sub>B</sub> : 7ns	
			1000 <sub>B</sub> : 8ns	1001 <sub>B</sub> : 9ns	
			1010 <sub>B</sub> : 10ns	1011 <sub>B</sub> : 11ns	
			1100 <sub>B</sub> : 12ns	1101 <sub>B</sub> : 13ns	
			1110 <sub>B</sub> : 14ns	1111 <sub>B</sub> : 15ns	
t <sub>RCD</sub> Value (2nd order = valuex16 ns)	Read-only	OP<7:4>	0000 <sub>B</sub> : 0ns	0001 <sub>B</sub> : 16ns	
			0010 <sub>B</sub> : 32ns	0011 <sub>B</sub> : 48ns	
			0100 <sub>B</sub> : 64ns	0101 <sub>B</sub> : 80ns	
			0110 <sub>B</sub> : 96ns	0111 <sub>B</sub> : 112ns	
			1000 <sub>B</sub> : 128ns	1001 <sub>B</sub> : 144ns	
			1010 <sub>B</sub> : 160ns	1011 <sub>B</sub> : 176ns	
			1100 <sub>B</sub> : 192ns	1101 <sub>B</sub> : 208ns	
			1110 <sub>B</sub> : 224ns	1111 <sub>B</sub> : 240ns	

NOTE 1 t<sub>RCD</sub> value is obtained adding 1st order value to the 2nd order value

**MR22:23 (Reserved) (MA<7:0> = 16<sub>H</sub>:17<sub>H</sub>):**

### 3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

#### **MR24 Overlay Window Enable (MA<7:0> = 18<sub>H</sub>): NVM Only**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)						OWD	OWE

Overlay Window Disable (OWD)	OP<1>	Read	<b>Reserved</b>	
		Write	<b>0<sub>B</sub></b> : Nop <b>1<sub>B</sub></b> : Disable Overlay Window	
Overlay Window Enable (OWE)	OP<0>	Read	<b>0<sub>B</sub></b> : Overlay Window Disabled (Default) <b>1<sub>B</sub></b> : Overlay Window Enabled	
		Write	<b>0<sub>B</sub></b> : Nop <b>1<sub>B</sub></b> : Enable Overlay Window	

NOTE 1 Overlay Window Disable (OP1) shall be set to disable the Overlay Window (See Section on the NVM Overlay Window for more details). OP1 is set by an MRW command with OP1 = “1”. When read, OP1 returns as a reserved value, “0”.

NOTE 2 Overlay Window Enable (OP0) shall be set to enable the Overlay Window (See Section on the NVM Overlay Window for more details). OP0 is set by an MRW command with OP0 = “1”. When read, OP0 returns the status of the Overlay Window. When read, OP0 will reflect whether the Overlay Window is enabled (OP0 = “1”) or disabled (OP0 = “0”).

NOTE 3 All values for MR24 are reset by the device to “0” during Device Auto-Initialization.

NOTE 4 Only one bit is allowed to be set during any single MRW.

#### **MR25:27 OW Base Address 1~3 (MA<7:0> = 19<sub>H</sub>-1B<sub>H</sub>): NVM only**

MR		OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
<b>25</b>	<b>19<sub>H</sub></b>	a19	a18	a17	a16	a15	a14	a13	0
<b>26</b>	<b>1A<sub>H</sub></b>	a27	a26	a25	a24	a23	a22	a21	a20
<b>27</b>	<b>1B<sub>H</sub></b>	(RFU)				a31	a30	a29	a28

NOTE 1 a12 - a0 are implied to be 0. The Overlay Window is aligned on a 8-Kbyte boundary.

NOTE 2 Mode Registers 25-27 are readable and writeable

NOTE 3 Only the value ‘0’ can be written to RFU bit. When read RFU bit shall output ‘0’.

NOTE 4 Only the value ‘0’ can be written to OP0 in MR25.

NOTE 5 Only the value ‘0’ can be written to unused row address bits outside of the device address space.

NOTE 6 When read, unused row address bits outside of the device address space shall return ‘0’.

**3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)****MR28 (Reserved) (MA<7:0> = 1C<sub>H</sub>):****MR29\_NVM tDNV (MA<7:0> = 1D<sub>H</sub>): NVM only**

OP7		OP6	OP5	OP4	OP3	OP2	OP1	OP0
tDNV Value (2nd order)					tDNV Value (1st order)			
tDNV Value (1st order = value ns)	Read-only	OP<3:0>	0000 <sub>B</sub> : 0us		0001 <sub>B</sub> : 1us			
			0010 <sub>B</sub> : 2us		0011 <sub>B</sub> : 3us			
			0100 <sub>B</sub> : 4us		0101 <sub>B</sub> : 5us			
			0110 <sub>B</sub> : 6us		0111 <sub>B</sub> : 7us			
			1000 <sub>B</sub> : 8us		1001 <sub>B</sub> : 9us			
			1010 <sub>B</sub> : 10us		1011 <sub>B</sub> : 11us			
			1100 <sub>B</sub> : 12us		1101 <sub>B</sub> : 13us			
			1110 <sub>B</sub> : 14us		1111 <sub>B</sub> : 15us			
tDNV Value (2nd order = valuex16 us)	Read-only	OP<7:4>	0000 <sub>B</sub> : 0us		0001 <sub>B</sub> : 16us			
			0010 <sub>B</sub> : 32us		0011 <sub>B</sub> : 48us			
			0100 <sub>B</sub> : 64us		0101 <sub>B</sub> : 80us			
			0110 <sub>B</sub> : 96us		0111 <sub>B</sub> : 112us			
			1000 <sub>B</sub> : 128us		1001 <sub>B</sub> : 144us			
			1010 <sub>B</sub> : 160us		1011 <sub>B</sub> : 176us			
			1100 <sub>B</sub> : 192us		1101 <sub>B</sub> : 208us			
			1110 <sub>B</sub> : 224us		1111 <sub>B</sub> : 240us			

**MR30:31 (NVM Reserved) (MA<7:0> = 1E<sub>H</sub>-1F<sub>H</sub>):****MR32 DQ Calibration Pattern A (MA<7:0> = 20<sub>H</sub>):**

Reads to MR32 return DQ Calibration Pattern “A”. See 5.12.2.

**MR33:39 (Do Not Use) (MA<7:0> = 21<sub>H</sub>-27<sub>H</sub>):****MR40 DQ Calibration Pattern B (MA<7:0> = 28<sub>H</sub>):**

Reads to MR40 return DQ Calibration Pattern “B”. See 5.12.2.

**MR41:47 (Do Not Use) (MA<7:0> = 29<sub>H</sub>-2F<sub>H</sub>):****MR48:62 (Reserved) (MA<7:0> = 30<sub>H</sub>-3F<sub>H</sub>):****MR63\_Reset (MA<7:0> = 3F<sub>H</sub>): MRW only**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
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X

NOTE 1 For additional information on MRW RESET see 5.13.

### 3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR64:126 (Reserved) (MA<7:0> = 40<sub>H</sub>-7E<sub>H</sub>):

MR127 (Do Not Use) (MA<7:0> = 7F<sub>H</sub>):

MR128:190 (Reserved for Vendor Use) (MA<7:0> = 80<sub>H</sub>-BE<sub>H</sub>):

MR191 (Do Not Use) (MA<7:0> = BF<sub>H</sub>):

MR192:254 (Reserved for Vendor Use) (MA<7:0> = C0<sub>H</sub>-FE<sub>H</sub>):

MR255 (Do Not Use) (MA<7:0> = FF<sub>H</sub>):

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## 4 LPDDR2-N Software Interface

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### 4.1 Overlay Window

LPDDR2-NVM functions are controlled using memory-mapped registers in an Overlay Window.

System software can locate the Overlay Window within the memory address range of the device by setting Overlay Window Base Address (OWBA) in Mode Registers 25, 26 and 27.

The Overlay Window **can be positioned only at a 8-KByte aligned address** within the address map.

The Overlay Window can be enabled by setting the OWE bit of MR24 to '1', and it can be disabled by setting OWD bit of MR24 to '1'. If OWE bit and OWD bit are set to '0' the Overlay Window status does not change. If OWD bit is set to '1', OWE bit is automatically cleared to '0'.

Once the Overlay Window has been enabled, the address region associated with the overlay window is accessed by the memory controller like any other section of memory in the array. Preactive, Activate, and Read/Write commands are used to access the Overlay Window.

**When the Overlay Window is enabled, read accesses to addresses outside the Overlay Window region will access the memory array.**

**Write commands to addresses outside the Overlay Window may not be allowed.**

Within the Overlay Window, memory-mapped control registers are located at static offsets from the base address (OWBA). The Overlay Window region contains: program buffer, device information, registers to control memory array operation, etc.

While the Overlay Window is enabled, system software can write to (and/or read from) each memory-mapped control register at the address **OWBA+RegisterStaticOffset** according to register definitions shown in [Table 23](#). For LPDDR2-NVM devices, Row Data Buffers are considered to be write through structures and any write issued to an Overlay Window register is completed when the issuing Write command is completed.

While the Overlay Window is disabled, the memory-mapped registers are not available.

#### 4.1.1 Map of Control Registers (offsets and definitions)

Table 23 describes the Overlay Window register map.

**Table 23 — Overlay Window: Control Register Offsets and Definitions**

Byte-Addressing		Type	Register Item	Default Value (hex)	Notes
Offset (hex)	# of bytes (decimal)				
0x001 – 0x000	2	R	Overlay Window Query String “P”	0x00 - 0x50	
0x003 – 0x002	2	R	Overlay Window Query String “F”	0x00 - 0x46	
0x005 – 0x004	2	R	Overlay Window Query String “O”	0x00 - 0x4F	
0x007 – 0x006	2	R	Overlay Window Query String “W”	0x00 - 0x57	
0x009 – 0x008	2	R	Overlay Window ID	0x00 - 0x20	
0x00B – 0x00A	2	R	Overlay Window Revision	Vendor-Specific	
0x00D – 0x00C	2	R	Overlay Window Size	Vendor-Specific	3
0x00F – 0x00E	2		Reserved for JEDEC		1,2
0x011 – 0x010	2	R	Program-Buffer Offset	Vendor-Specific	4
0x013 – 0x012	2	R	Program-Buffer Size	Vendor-Specific	5
0x01F – 0x014	12		Reserved for JEDEC		1,2
0x021 – 0x020	2	R	JEDEC Manufacturer ID	Vendor-Specific	
0x023 – 0x022	2	R	JEDEC Device ID	Vendor-Specific	
0x03D – 0x024	26		Reserved for JEDEC		1,2
0x03F - 0x03E	2	W	Reserved for JEDEC		2,10
0x07F – 0x040	64	Vendor-Specific	Reserved for Vendor Use	Vendor-Specific	
0x081 – 0x080	2	W	Command Code	0x00 - 0x00	6
0x083 – 0x082	2		Reserved for JEDEC		1,2
0x087 – 0x084	4	R/W	Command Data		
0x08B – 0x088	4	W	Command Address		7
0x08F – 0x08C	4		Reserved for JEDEC		1,2
0x093 – 0x090	4	W	Multi-Purpose Register		8
0x0BF - 0x094	44		Reserved for JEDEC		1,2
0x0C1 - 0x0C0	2	W	Command Execute	0x00 - 0x00	
0x0C7 - 0x0C2	6		Reserved for JEDEC		1,2
0x0C9 - 0x0C8	2	R/W	Suspend	0x00 - 0x00	
0x0CB - 0x0CA	2	R/W	Abort	0x00 - 0x00	
0x0CD - 0x0CC	2	R/W	Status Register	0x00 - 0x80	
0x0CF - 0x0CE	2		Reserved for JEDEC		
0x0DF - 0x0D0	16		Reserved for Vendor Use		
0x0FF – 0x0E0	32	-	Reserved for Vendor Use		
Vendor-Specific	Vendor-Specific	Vendor-Specific	Reserved for Vendor Use		
Vendor-Specific	Vendor-Specific	Vendor-Specific	Program-Buffer		

NOTE 1 System Software shall not write to any Reserved register any value other than 0.

NOTE 2 When read, Reserved registers and Write-Only registers will return indeterminate data.

NOTE 3 Number of bytes in this Overlay Window.

NOTE 4 Program-Buffer Offset is the byte-addressing offset of the beginning of the Program-Buffer in this Overlay Window.

NOTE 5 Program-Buffer Size is the number of bytes in the Program-Buffer in this Overlay Window.

NOTE 6 The memory shall reset this register to Default Value after Device Auto-Initialization, and after completion of prior command

NOTE 7 Command Address = a[31:0] of byte-address. System software shall write “0” to any most-significant bits of a[31:23] not used by the memory device.

NOTE 8 Multi-Purpose Register is used as DataCount[31:0] in the buffer-program command. DataCount[31:0] = number of contiguous bytes to be programmed using the Program-Buffer. All products allow, but some products may not require, system software to write to this register. DataCount, in conjunction with Command Address, shall not cause data to wrap beyond the end of the Program-Buffer.

NOTE 9 Only one of the following registers may be written to with a value other than 0x0000 during any Write burst: Command Execute, Suspend, Abort, and the Status Register.

NOTE 10 Overlay Window location 0x03E - 0x03F is a Write-Only register that is reserved. When read, location will return indeterminate data.

#### 4.1.1.1 Command Code Register

Device command codes (e.g., 0x0020 for Block Erase) are written to this register. Command execution occurs only after 0x0001 is written to the Command Execute Register.

See 4.3, for a examples of how the Overlay Window Registers are used.

This register is cleared to its default value after command execution is completed.

**Table 24 — Command Code Register**

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x081 – 0x080	2	W	Command Code	0x00 - 0x00

#### 4.1.1.2 Command Data Register

Command data might be written to this register. Results of queries might be provided through this register.

**Table 25 — Command Data Register**

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x087 – 0x084	4	R/W	Command Data	

#### 4.1.1.3 Command Address Register

The command address (e.g., the first data address for buffered program operation, the block address for erase operation) is written to this registers. The address value (a[31:0]) shall be in byte units.

System software shall write “0” to any most-significant bits of a[31:23] not used by the memory device.

**Table 26 — Command Address Register**

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x08B – 0x088	4	W	Command Address	

#### 4.1.1.4 Multi-Purpose Register

The Multi-Purpose Register is used in several operations. For example, it shall be loaded with the number of contiguous bytes to be programmed during a buffered program operation.

It shall be loaded with the last block address during a block lock/unlock/lock-down operation.

**Table 27 — Multi-Purpose Register**

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x093 – 0x090	4	W	Multi-Purpose Register	



#### 4.1.1.5 Command Execute Register

Command execution begins when “0x0001” is written to this register. It is allowed to write this register only when the device is ready (DRB = “1”). The device executes the current command in the Command Code register. Before writing “0x0001” to the Command Execute register, the user can change the contents of the Command Code register (and any related parameters) any number of times.

It is allowed only to write “0x0001” to this register - writing any another value is prohibited, and may result in undefined operation.

**Table 28 — Command Execute Register**

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x0C1 - 0x0C0	2	W	Command Execute	0x00 - 0x00

#### 4.1.1.6 Suspend Register

When “0x0001” is written to this register, an on-going erase or program operation is suspended. Writing to this register is effective only while the device is busy performing an erase or program operation - writes during other times are ignored.

It is allowed only to write “0x0001” to this register - writing any other value can result in undefined operation.

The Suspend register returns “0x0001” from the time a Suspend command is written until the device is ready (DRB = “1”). The Suspend register returns “0x0000” in all other cases. Once the embedded operation has suspended (or completed), the Suspend register is reset by the device and returns “0x0000” when read.

**Table 29 — Suspend Register**

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x0C9 - 0x0C8	2	R/W	Suspend	0x00 - 0x00

The Status Register shall be read to check if the suspend request was successful: SR.6=1 indicates erase suspend was successful; SR.2=1 indicates program suspend was successful.

Otherwise, if the suspend request was not successful (SR.6=0; SR.2=0), the ongoing program or erase operation may have completed successfully before the suspend could take effect; system software should test all Status Register flags to be certain.

The Suspend Register resets to its default value after suspending the program or erase operation. Also, successful completion of any on-going program or erase operation will clear this register.

Once the device is suspended, the Resume command must be issued in order to continue the program or erase operation. Refer to 4.7.9 for additional details.

Suspend feature is optional. If LPDDR2-NVM does not support suspend feature, Suspend Register can be set only to ‘0x0000’, and when read Suspend Register shall output the value ‘0x0000’.

#### 4.1.1.7 Abort Register

When “0x0001” is written to this register, an on-going embedded operation is aborted. Writing to this register is effective only while the device is busy performing an embedded operation - writes during other times are ignored.

It is allowed only to write “0x0001” to this register - writing any other value can result in undefined operation.

**Table 30 — Abort Register**

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x0CB - 0x0CA	2	R/W	Abort	0x00 - 0x00

The Abort register returns “0x0001” from the time a Abort command is written until the device is ready (DRB = “1”). The Abort register returns “0x0000” in all other cases. Once the embedded operation has aborted (or completed), the Abort register is reset by the device and returns “0x0000” when read.

This register resets to its default value by the device after all embedded operations have ceased and the device becomes ready (SR.7 = “1”). **If any embedded operation is aborted and does not complete due to that abort, one or more error flags will be set in SR (SR.4 and/or SR.5).**

Note that the embedded operation may have completed successfully before the abort could take effect.

Refer to 4.7.11 for additional details.

Abort feature is optional. If LPDDR2-NVM does not support abort feature, Abort Register can be set only to ‘0x0000’, and when read Abort Register shall output the value ‘0x0000’.

#### 4.1.1.8 Status Register

The Status Register (SR) indicates the state (Ready or Busy) of the device, and status of program, erase, and the other embedded operations.

**Table 31 — Status Register**

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x0CD - 0x0CC	2	R/W	Status Register	0x00 - 0x80

In particular, SR.7 indicates the state of the device: **SR.7 = ‘1’ indicates the device is Ready; SR.7 = ‘0’ indicates the device is Busy.**

The following Status Register bits are related to the results of embedded operations: **Control Mode Status Bit (SR.9), Object Mode Status Bit (SR.8), Erase Status (SR.5), Program Status (SR.4), Voltage Supply Error Status (SR.3), and Block Lock Status (SR.1).** These bits are set by the device. These bits are cumulative and can only be cleared by writing a ‘1’ to the Status Register bit to be cleared (W12C is an acronym for “write one to clear”). If these bits are written with a ‘0’, their value will not change.

The following Status Register bits are related to the current state of any in process embedded operation: **Device Busy (SR.7), Erase Suspended (SR.6), and Program Suspended (SR.2).** These bits are set and cleared by the device. Only the value ‘0’ shall be written to this bits, which will be ignored.

**Status Register bit SR.1, SR.2, SR.3, SR.4, SR.5, SR.6, SR. 8, and SR.9 are invalid while SR.7 = ‘0’ (DRB = ‘0’).**

**Once Activated, a Row Data Buffer (RDB) containing the Status Register shall be automatically updated by the LPDDR2-N device and shall reflect the current state for the Status Register.**

#### 4.1.1.8 Status Register (cont'd)

**Table 32 — Status Register details**

Bit	Name	Type	Description
SR.15 : SR.10	(Reserved)	R Only	Reserved for future use.
SR.9	CMSB Control Mode Status Bit	W12C	[CMSB,OMSB] indicates additional error conditions for LPDDR2-NVM devices which support programming operations based on Programming Region. [CMSB,OMSB] = 00 --> Programming successful [CMSB,OMSB] = 01 --> Programming Error: programming attempt to an Object Mode Programming Region [CMSB,OMSB] = 10 --> Programming Error: programming attempt to an invalid Programming Region Element; [CMSB,OMSB] = 11 --> Programming Error: programming attempt using illegal command PSB will also be set along with [CMSB,OMSB] for the above error conditions.
SR.8	OMSB Object Mode Status Bit	W12C	
SR.7	DRB Device Ready Bit	R Only	DRB indicates Erase, Program, or other embedded operation completion in the device. 0 = Embedded controller is Busy 1 = Embedded controller is Ready bit SR.1, SR.2, SR.3, SR.4, SR.5, SR.6, SR. 8, and SR.9 are invalid while DRB = '0'.
SR.6	ESSB Erase Suspend Status Bit	R Only	ESSB indicates whether the device is in Erase Suspend. After issuing a Suspend command, the embedded controller halts and sets to '1' DRB and ESSB. ESSB remains set until the device receives a Resume command. 0 = Operation in progress/completed 1 = Operation suspended
SR.5	ESB Erase Status Bit	W12C	ESB is set to '1' if an attempted Erase failed. A Command Sequence Error is indicated when SR.4, SR.5 and SR.7 are set. 0 = Erase operation successful 1 = Erase Error
SR.4	PSB Program Status Bit	W12C	PSB is set to '1' if an attempted program failed. A Command Sequence Error is indicated when SR.4, SR.5 and SR.7 are set. 0 = Program operation successful 1 = Program Error
SR.3	VSESB Voltage Supply Error Status Bit	W12C	VSESB indicates whether the VACC level is valid voltage. 0 = VACC valid voltage level 1 = VACC invalid voltage level, operation aborted
SR.2	PSSB Program Suspend Status Bit	R Only	PSSB indicates whether the device is in Program Suspend. After receiving a Suspend command, the embedded controller halts execution and sets to '1' DSB and PSSB, which remains set until a Resume command is received. 0 = Operation in progress/completed 1 = Operation suspended
SR.1	BLSB Block Lock Status Bit	W12C	BLSB indicates whether Program or Erase was attempted on a locked block. If the block is locked, the embedded controller sets to '1' BLSB and aborts the operation. 0 = Unlocked 1 = Aborted Write attempt on a locked block
SR.0	(Reserved)	R Only	Reserved for future use.

NOTE 1 The "W12C" Status Register bits type are set by the device and can be cleared by writing '1' to them (W12C is an acronym for "write one to clear")

NOTE 2 The "R only" Status Register bits type can be written only with the value '0' when clearing the status bits.

NOTE 3 ESSB (SR.6) and ESB (SR.5) are reserved if a device does not require Erase features

NOTE 4 PSSB (SR.2) is reserved if a device does not support program suspend.

NOTE 5 ESB (SR.5) is set to '1' if an erase operation is aborted by writing "0x0001" to the Abort Register.

NOTE 6 PSB (SR.4) is set to '1' if a program operation is aborted by writing "0x0001" to the Abort Register.

NOTE 7 **CMSB (SR.9) and OMSB (SR.8) are used to indicate error conditions for LPDDR2-NVM devices which support programming region modes. They are reserved in case programming region modes are not supported.**

NOTE 8 All Reserved bits are driven to '0' by the device, and shall be written with '0'.

NOTE 9 LPDDR2-N devices may implement Vendor Specific features. Refer to Vendor Datasheets for a complete description of the NVM Status Register

#### 4.1.1.9 Program-Buffer

The Program-Buffer is used during Buffered Program operation to input the data to be written in memory array. The Program-Buffer shall be filled prior writing “0x0001” to the Command Execute Register.

Refer to Vendor Datasheets for information about Program-Buffer offset and Program-Buffer size.

**Table 33 — Program-Buffer**

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
Vendor-Specific	Vendor-Specific	Vendor-Specific	Program-Buffer	

## 4.2 Data Byte Lane Assignment for Overlay Window Register

Registers included in the Overlay Window might have various size: 1-byte, 2-byte, 4-byte, etc.

Table 34 describes how each byte of an Overlay Window Register is mapped to data byte lane (DQ[7:0], DQ[15:8], DQ[23:16] and DQ[31:24]) in case of x8, x16 and x32 LPDDR2-NVM.

In particular, examples for 1-byte, 2-byte and 4-byte registers are shown.

To properly access the Overlay Window Register it is necessary to ensure the correct assignment of each data bit.

**Table 34 — Overlay Window Register Byte Lane Assignment**

Byte-Addressing		Register	Data Bus Width					
Offset (hex)	# of bytes (decimal )		x8		x16		x32	
			C1 C0	DQ	C1 C0	DQ	C1 C0	DQ
0x000	1	OneByte_Reg_A[7:0]	0 0	DQ[7:0]	0 0	DQ[7:0]	0 0	DQ[7:0]
0x001	1	OneByte_Reg_B[7:0]	0 1	DQ[7:0]		DQ[15:8]		DQ[15:8]
0x002	1	OneByte_Reg_C[7:0]	1 0	DQ[7:0]	0 1	DQ[7:0]		DQ[23:16]
0x003	1	OneByte_Reg_D[7:0]	1 1	DQ[7:0]		DQ[15:8]		DQ[31:24]
0x001 – 0x000	2	TwoBytes_Reg_A[7:0]	0 0	DQ[7:0]	0 0	DQ[7:0]	0 0	DQ[7:0]
		TwoBytes_Reg_A[15:8]	0 1	DQ[7:0]		DQ[15:8]		DQ[15:8]
0x003 – 0x002	2	TwoBytes_Reg_B[7:0]	1 0	DQ[7:0]	0 1	DQ[7:0]		DQ[23:16]
		TwoBytes_Reg_B[15:8]	1 1	DQ[7:0]		DQ[15:8]		DQ[31:24]
0x003 – 0x000	4	FourBytes_Reg_A[7:0]	0 0	DQ[7:0]	0 0	DQ[7:0]	0 0	DQ[7:0]
		FourBytes_Reg_A[15:8]	0 1	DQ[7:0]		DQ[15:8]		DQ[15:8]
		FourBytes_Reg_A[23:16]	1 0	DQ[7:0]	0 1	DQ[7:0]		DQ[23:16]
		FourBytes_Reg_A[31:24]	1 1	DQ[7:0]		DQ[15:8]		DQ[31:24]

### 4.3 LPDDR2-NVM Operations

LPDDR2-NVM can be produced from a variety of memory array technologies. This section is not intended to describe full details of LPDDR2-NVM operations.

The scope of this section is to provide a standard for some aspects of LPDDR2-NVM software interface, that might be in common among most of NVM technologies.

Based on this standard memory vendors will define their own memory specification, adding all necessary details for the proper use of the device. These details are technology dependant and not easy to predict for emerging or completely new technologies.

Some possible exceptions to the standard are mentioned. It is recommended to refer to the device specification for the complete description.

This section includes the following commands: NOP, Single Word Program, Buffered Program, Block Erase, Block Lock, Block Unlock, Block Lock-Down, Resume, Suspend, Command Execute, and Abort.

Table 35 defines the command code values to be written to the Command Code Register within the Overlay Window (see Overlay Window register map table).

An embedded controller handles all timings and verifies the correct execution of LPDDR2-NVM operations.

The commands can be initiated when the embedded controller is not busy (DRB = “1”). The Device Ready Bit (DRB) is read as part of the Status Register.

VACC shall not change during the period starting from at least 1us prior to the initiation of any embedded operation until that embedded operation is complete.

During the execution of an embedded operation, the device can be placed in Power Down mode by driving CKE low, see Power Down section for detailed description on how to enter and exit Power Down.

**Table 35 — Command Codes**

Operation	Code	Command	Note
NOP	0x0000	No Operation	1
Program	0x0041	Single Word Program	2
	0x0042	Single Word Overwrite	3
	0x00E9	Buffered Program	
	0x00EA	Buffered Overwrite	3
Erase	0x0020	Block Erase	
Block Lock	0x0061	Block Lock	
Block Unlock	0x0062	Block Unlock	
Block Lock-Down	0x0063	Block Lock-Down	
Resume	0x00D0	Resume	

NOTE 1 The Command Code Register default value is 0x0000 (NOP). If the Command Execute Register is set to ‘0x0001’ when Command Code Register is at the default value (0x0000), the device will become busy and then ready without executing any operation (NOP).

NOTE 2 Single Word Program is optional.

NOTE 3 Single Word Overwrite and Buffered Overwrite are optional and are only supported by some NVM technologies and some LPDDR2-NVM devices.

#### 4.4 Nomenclature

### Table 36 — Definition of terms

[illegible]

## 4.5 Acronyms

### Table 37 — Definition of acronyms

[illegible]

## 4.6 Conventions

### Table 38 — Definition of conventions

[illegible]



#### 4.7 Overlay Window Enable and Disable

When the Overlay Window is enabled, it overlaps a portion of the memory array area.

To enable the Overlay Window the value 0x01 shall be written to MR24. To disable the Overlay Window the value 0x02 shall be written to MR24.

The Overlay Window Base Address shall be stored to MR27, MR26 and MR25.

In particular, if OWBA[31:0] is the desired Overlay Window base address, MR27-MR25 shall be set as follows:

MR27[OP7:OP0] = {0,0,0,0,OWBA[31:28]}

MR26[OP7:OP0] = {OWBA[27:20]}

MR25[OP7:OP0] = {OWBA[19:13],0}

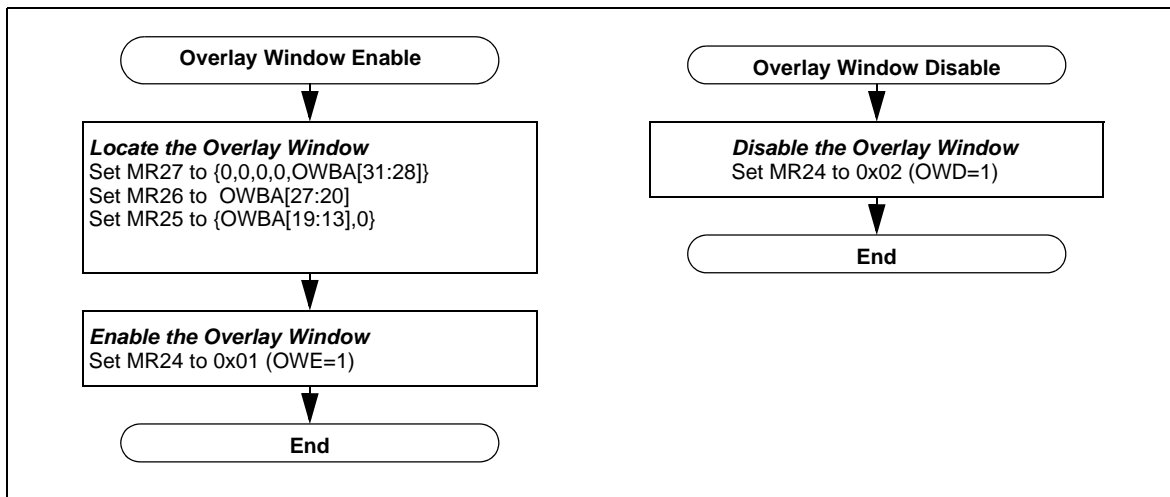
OWBA[12:0] value is assumed to be 0x0000, therefore the Overlay Window can be positioned only at a 8-KByte aligned address.

MR27, MR26 and MR25 shall be written only if the Overlay Window is disabled, OWBA shall be changed only if the MR24.OP0 is '0' (OWE).

Software may open the Overlay Window, and close it immediately after it has accessed it. Alternatively, it may keep the Overlay Window open continuously on a fixed location of the memory map.

If the Overlay Window is enabled and the device is busy (DRB = '0'), write access to the Overlay Window is not allowed expect for the Suspend and Abort registers.

If the Overlay Window is enabled and the device is busy (DRB = '0'), read access to the Overlay Window is allowed. Some OW locations may have valid content only with device ready, refer to device datasheet for complete information.



NOTE OWBA is the byte address of the desired Overlay Window Base Address

Figure 7 — Overlay Window Enable and Disable

#### 4.7.1 Block Lock Command

The Block Lock command is used to lock a block, a consecutive range of blocks, or all blocks and prevents program or erase operations from changing the data within this range. Some LPDDR2-N devices may support locking single blocks or a range of blocks, while other LPDDR2-N devices may only support locking all blocks.

Locked blocks are fully protected from program or erase operations. Any program or erase operations attempted on a locked block will return an error in the Status Register. The status of a locked block can be changed to unlocked using the Block Unlock command.

All blocks are locked after power-up or reset. In LPDDR2 memory, reset is achieved by writing MR63.

Block Lock operation is performed by the embedded processor. Block Lock operation shall not be interrupted by reset or abort (if supported), otherwise the result of this operation is unpredictable.

Block Lock status does not change if an ongoing operation other than Block Lock, Block Unlock and Block Lock-Down is aborted by writing 0x0001 to the Abort Register.

Block Lock operations cannot be suspended.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:

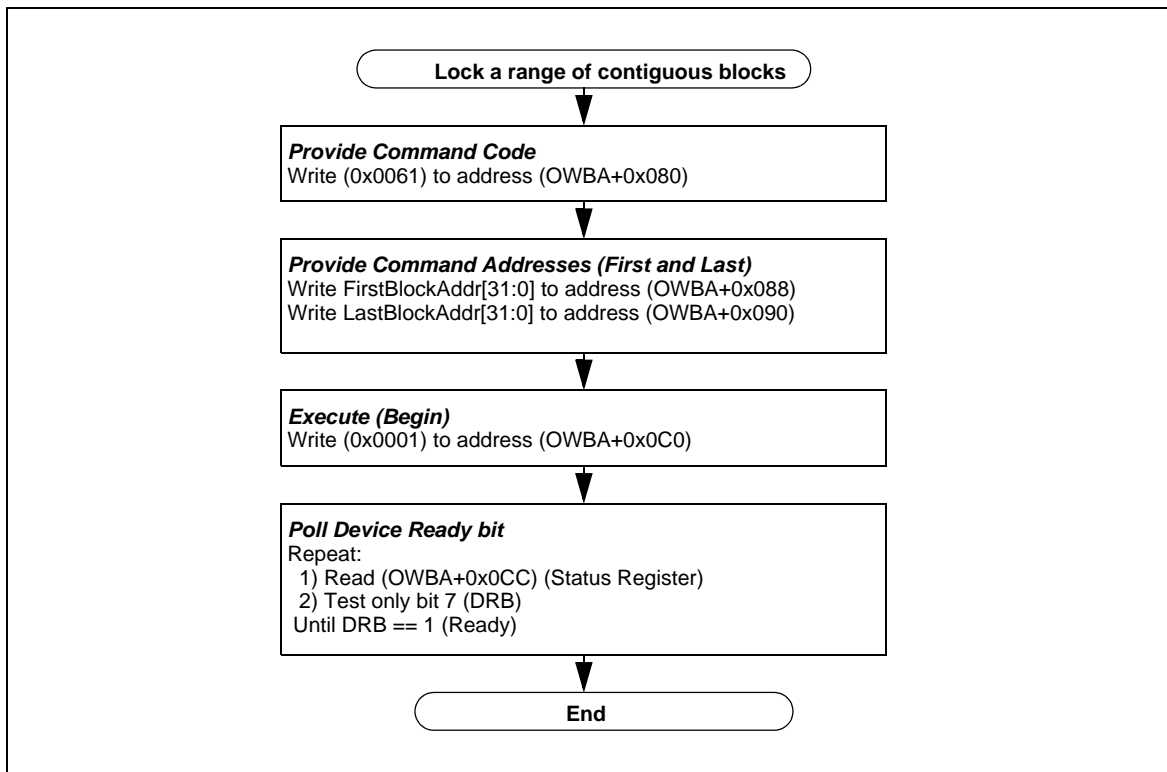
- Write 0x0061 to the Command Code Register,
- Write any address within the desired start block to the Command Address Register,
- Write any address within the desired stop block to the Multi-Purpose Register,
- Write 0x0001 to the Command Execute Register.

For LPDDR2-N devices that only support locking all blocks, the addresses in the Command Address Register and Multi-Purpose Register are not used and are "Do Not Care".

NVM vendors may implement additional security features not described in the JEDEC spec. Users shall refer to the device datasheet for complete information.

Some NVM technologies might not have the notion of block, because they do not require and support the erase operation.

#### 4.7.1 Block Lock Command (cont'd)



NOTE 1 The Overlay Window must be open to issue Block Lock command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 FirstBlockAddr[31:0] is any byte address within the first block being locked. This step is not required for devices that only support locking all blocks with the Block Lock command.

NOTE 5 LastBlockAddr[31:0] is any byte address within the last block being locked. This step is not required for devices that only support locking all blocks with the Block Lock command.

NOTE 6 If the address written at the location OWBA+0x088 (FirstBlockAddr[31:0]) is greater than the address written at the location OWBA+0x090 (LastBlockAddr[31:0]) the block lock status will not change and the Status Register bits PSB and ESB are set. This error check is not required for devices that only support locking all blocks with the Block Lock command.

NOTE 7 Some LPDDR2-N devices will lock all blocks with the Block Lock command. Refer to vendor datasheets for complete information on the Block Lock command.

**Figure 8 — Block Lock Command Flowchart**

#### 4.7.2 Block Unlock Command

The Block Unlock command is used to unlock a block or a consecutive range of blocks, allowing the block to be programmed or erased.

The status of a unlocked block can be changed to locked using the Block Lock command. Some LPDDR2-N devices may only support unlocking a single block or a range of blocks at any given time. For these devices, the blocks not selected by the Block Unlock command will be changed to locked after the completion of the Block Unlock command.

All blocks are locked after power-up or reset. In LPDDR2 memory, reset is achieved by writing MR63.

Block Unlock operation is performed by the embedded processor. Block Unlock operation shall not be interrupted by reset or abort (if supported), otherwise the result of this operation is unpredictable.

Block Lock status does not change if an ongoing operation other than Block Lock, Block Unlock and Block Lock-Down is aborted by writing 0x0001 to the Abort Register.

Block Unlock operations cannot be suspended.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

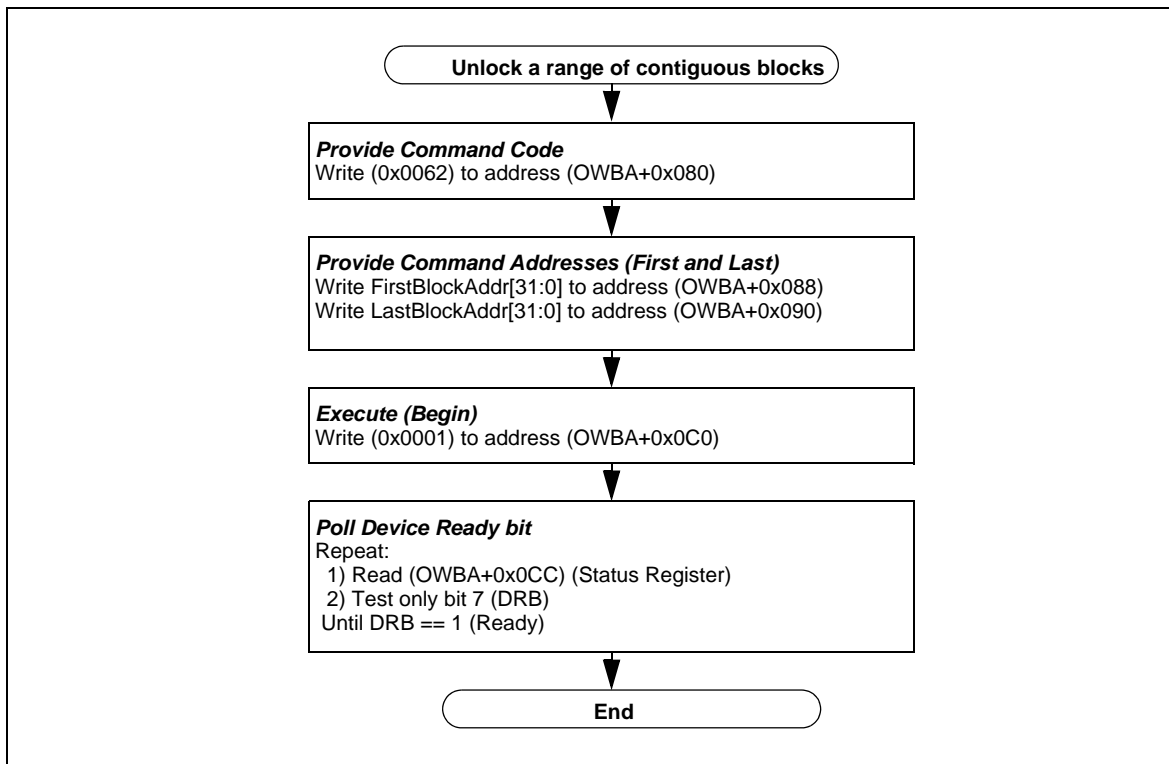
The Command Sequence is:

- Write 0x0062 to the Command Code Register,
- Write any address within the desired start block to the Command Address Registers,
- Write any address within the desired stop block to the Multi-Purpose Registers,
- Write 0x0001 to the Command Execute Register.

NVM vendors may implement additional security features not described in the JEDEC spec. Users shall refer to the device datasheet complete information.

Some NVM technologies might not have the notion of block, because they do not require and support the erase operation.

#### 4.7.2 Block Unlock Command (cont'd)



NOTE 1 The Overlay Window must be open to issue Block Unlock command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 FirstBlockAddr[31:0] is any byte address within the first block being unlocked.

NOTE 5 LastBlockAddr[31:0] is any byte address within the last block being unlocked.

NOTE 6 If the address written at the location OWBA+0x088 (FirstBlockAddr[31:0]) is greater than the address written at the location OWBA+0x090 (LastBlockAddr[31:0]) the block lock status will not change and the Status Register bits PSB and ESB are set.

NOTE 7 Some LPDDR2-N devices will unlock only one block or a range of blocks selected by the Block Unlock command. All other blocks will be locked by these devices. Refer to vendor datasheets for complete information on the Block Unlock command.

**Figure 9 — Block Unlock Flowchart**

### 4.7.3 Block Lock-Down Command

The Block Lock-Down command is used to lock-down a block or a consecutive range of blocks, and prevent program or erase operations from changing the data in it.

Locked-Down blocks are fully protected from program or erase operations. Any program or erase operations attempted on a locked-down block will return an error in the Status Register. **The status of a locked-down block is reset to the default locked state only after removing and applying again the power supply.**

All blocks are locked after power-up or reset. In LPDDR2 memory, reset is achieved by writing MR63.

Block Lock-Down operation is performed by the embedded processor. Block Lock-Down operation shall not be interrupted by reset or abort (if supported), otherwise the result of this operation is unpredictable.

Block Lock status does not change if an ongoing operation other than Block Lock, Block Unlock, and Block Lock-Down is aborted by writing 0x0001 to the Abort Register.

Block Lock-Down operations cannot be suspended.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

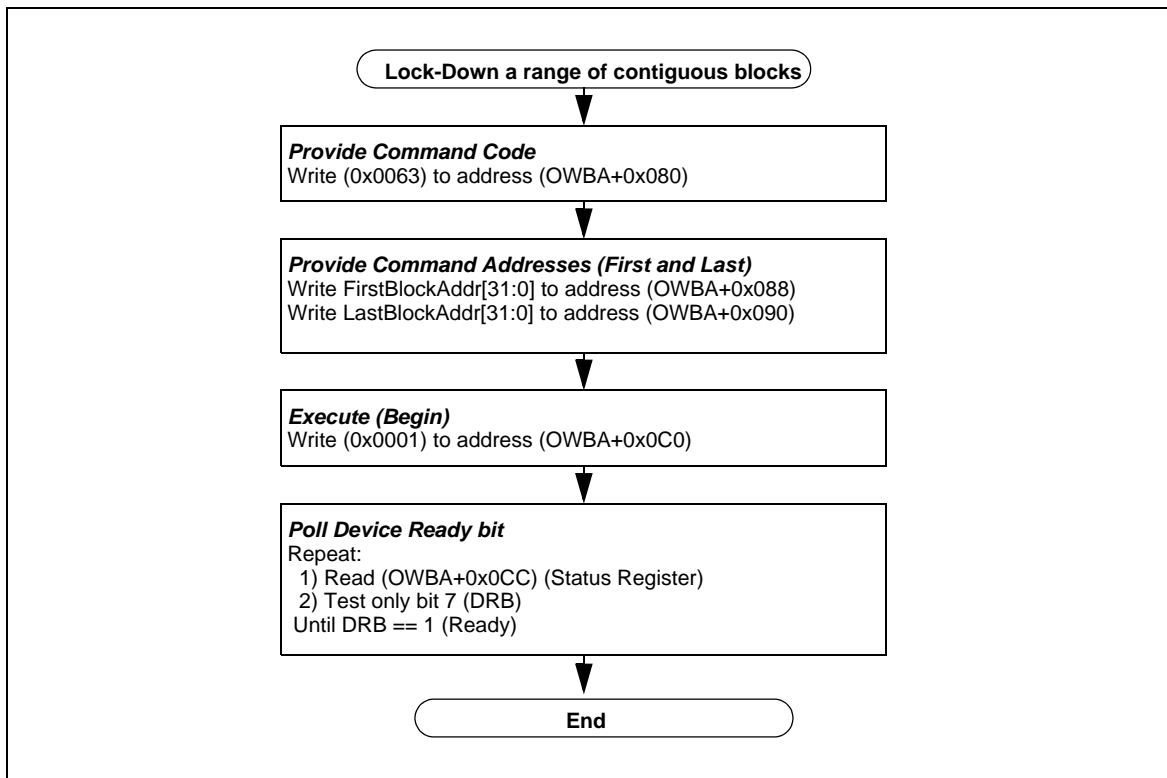
The Command Sequence is:

- Write 0x0063 to the Command Code Register,
- Write any address within the desired start block to the Command Address Registers,
- Write any address within the desired stop block to the Multi-Purpose Registers,
- Write 0x0001 to the Command Execute Register.

NVM vendors may implement additional security features not described in the JEDEC document. Users shall refer to the device datasheet for complete information.

Some NVM technologies might not have the notion of block, because they do not require and support the erase operation.

#### 4.7.3 Block Lock-Down Command (cont'd)



NOTE 1 The Overlay Window must be open to issue Block Lock-Down command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 FirstBlockAddr[31:0] is any byte address within the first block being locked

NOTE 5 LastBlockAddr[31:0] is any byte address within the last block being locked

NOTE 6 If the address written at the location OWBA+0x088 (FirstBlockAddr[31:0]) is greater than the address written at the location OWBA+0x090 (LastBlockAddr[31:0]) the block lock status will not change and the Status Register bits PSB and ESB are set.

**Figure 10 — Block Lock-Down Command Flowchart**

#### 4.7.4 Block Erase Command

The Block Erase command is used to **erase a Block**. It sets all the bits within the selected Block to '1'. All previous data in the Block is lost. If the Block is locked, the erase operation will abort, the data in the Block will not be changed and the Device Status Register will output the error.

The erase operation is performed by the embedded controller.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:

Write 0x0020 to the Command Code Register,

Write any address within the desired block to the Command Address Registers,

Write 0x0001 to the Command Execute Register

**The erase operation can be suspended.**

If a block being erased is locked during an erase suspend, the operation will complete normally when it is resumed.

The erase is aborted by writing MR63, or writing 0x0001 to the Abort Register (if supported).

As data integrity cannot be guaranteed when the Block Erase operation is aborted, the Block must be erased again.

Note that some NVM technologies do not need Erase command, therefore some NVM devices will not support it.

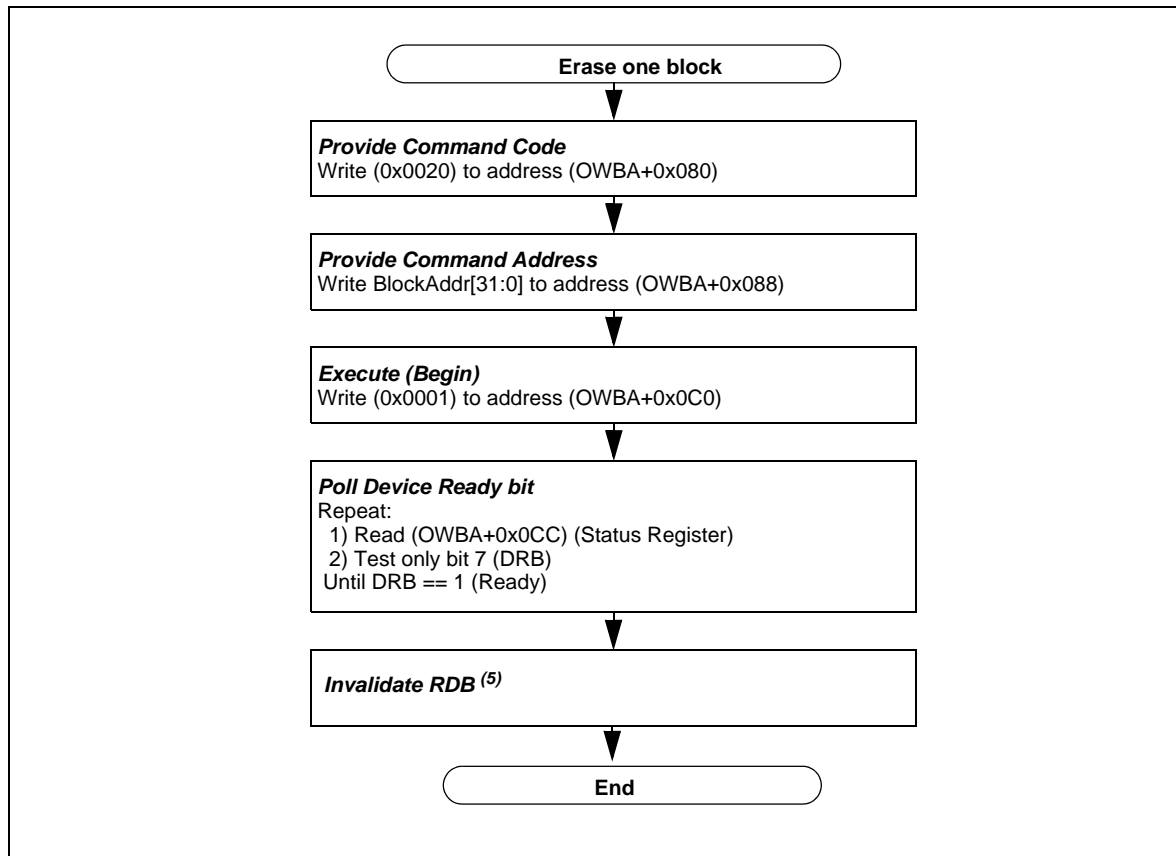
**Table 39 — Block Erase Error Conditions**

7	6	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	1	0	0	0	0	0	Erase operation failure
1	0	1	0	0	0	1	0	Erase operation abort. An erase operation was attempted on a locked block.
1	0	1	0	1	0	0	0	Erase operation abort. VACC not at appropriate level for Erase operation.
1	0	1	1	0	0	0	0	Erase operation abort. Block address outside the LPDDR2-NVM address space.
1	1	1	1	0	0	0	0	Erase operation abort. Attempting to erase a block during Erase Suspend.
1	0	1	1	0	1	0	0	Erase operation abort. Attempting to erase a block during Program Suspend.
1	1	1	1	0	1	0	0	Erase operation abort. Attempting to erase a block during Erase Suspend and Program Suspend.



#### 4.7.4 Block Erase Command (cont'd)

Figure 11 shows the Block Erase Flowchart.



NOTE 1 The Overlay Window must be open to issue Block Erase command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 BlockAddr[31:0] is any byte address within the block being erased

NOTE 5 RDB invalidation may be required to avoid risk of incoherency between memory array content and RDB content. For more details refer to [4.7.12](#).

**Figure 11 — Block Erase Flowchart**

#### 4.7.5 Single Word Program Command

The Single Word Program command is used to program a single word (2-byte data) to the memory array.

This is a legacy command and it is optional.

The program operation is performed by the embedded controller.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:

Write 0x0041 (or 0x0040) to the Command Code Register,

Write desired location address to the Command Address Register,

Write desired program data to the Command Data Register (Command Data[15:0] only),

Write 0x0001 to the Command Execute Register.

Programming can be performed in one block at a time.

The Status Register DRB bit, indicates the progress of the Program operation. It should be read to check whether the operation has completed or not.

After completion of the Program operation (DRB= 1), one of the Status Register error bits (4,3 and 1) going High means that an error was detected: either a failure occurred during programming, VACC is outside the allowed voltage range or an attempt to program a locked Block was made. See Section Device Status Register for detailed information.

The program operation can be suspended.

The program is aborted by writing MR63, or writing 0x0001 to the Abort Register (if supported).

As data integrity cannot be guaranteed when the program operation is aborted, the data must be reprogrammed.

Some NVM technologies support the Single Word Program command only under particular conditions.

For example, for LPDDR2-NVM device that has the notion of program region, Single Word Program Command is supported only by program regions configured in the Control Program mode, and with Command Address value belonging to a particular portion of the program region.

If a Single Word Program command is issued to a Program Region configured in the Object Program mode, the Program operation is aborted and PSB and OMSB Status Register bits are set.

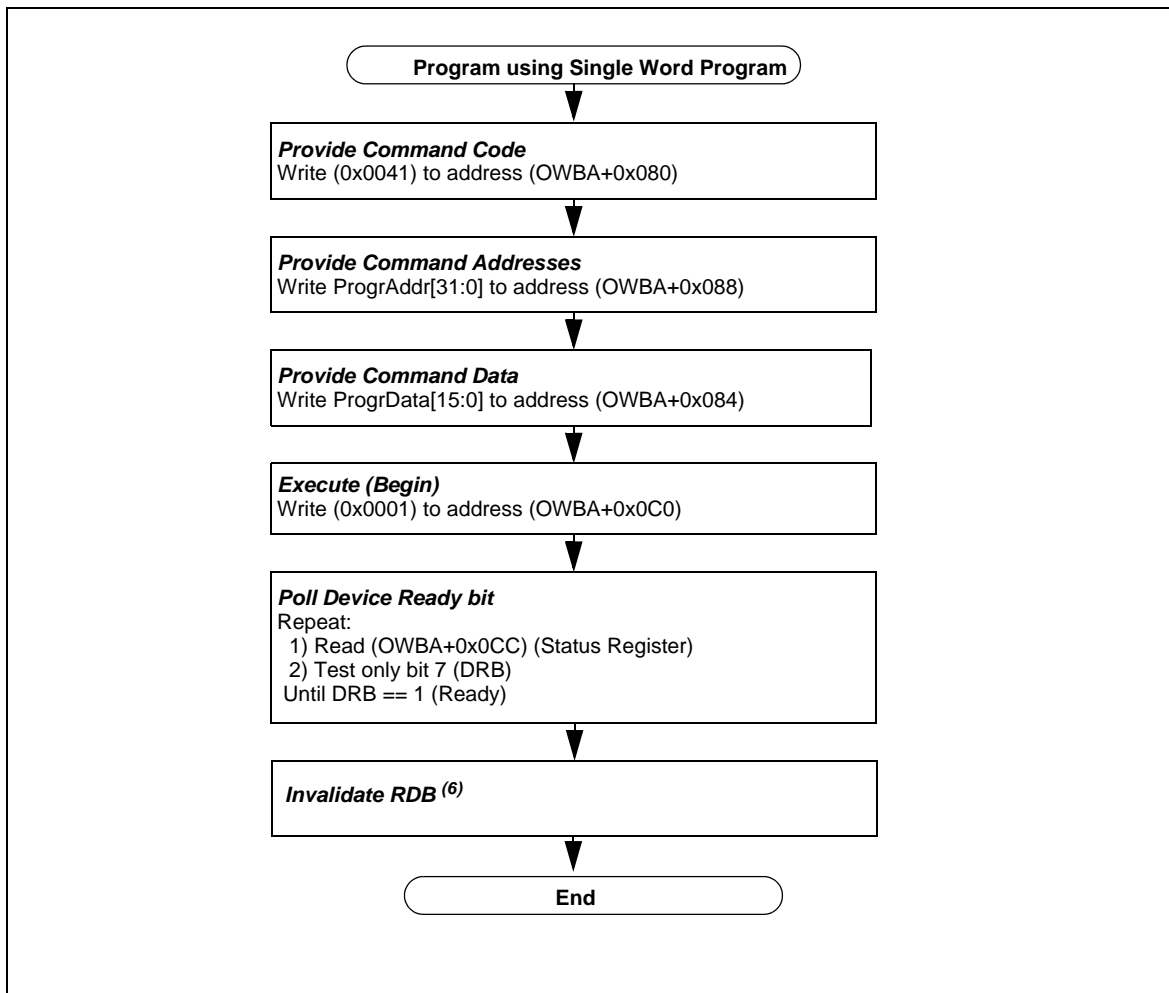
For details about program region and program method see the application note.

**Table 40 — Single Word Program Error Conditions**

7	6 <sup>(1)</sup>	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Single Word Program operation failure.
1	0	0	1	0	0	1	0	Single Word Program operation abort. An program operation was attempted on a locked block.
1	0	0	1	1	0	0	0	Single Word Program operation abort. VACC not at appropriate level for Program operation.
1	0	1	1	0	0	0	0	Single Word Program operation abort. Program address outside the LPDDR2-NVM address space
1	0	1	1	0	1	0	0	Single Word Program operation abort. Attempting to program during Program Suspend.

NOTE 1 ESSB Status Register bit is '1' in case of command issued during Erase Suspend.

#### 4.7.5 Single Word Program Command (cont'd)



NOTE 1 The Overlay Window must be open to issue Single Word Program command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 ProgrAddr[31:0] is the target byte address of the programming operation, and ProgrAddr[0] shall be '0'.

NOTE 5 ProgrData[15:0] is the desired 2-byte data to be programmed.

NOTE 6 RDB invalidation may be required to avoid risk of incoherency between memory array content and RDB content. For more details refer to [4.7.12](#).

**Figure 12 — Single Word Program Flowchart**

#### 4.7.6 Single Word Overwrite Command

Single Word Overwrite is supported only by some NVM technologies and some LPDDR2-NVM devices.

The Single Word Overwrite command is used to write a single word (2-byte data) to the memory array.

The overwrite command allows to change the status of each bit from '1' to '0' or from '0' to '1'.

With the overwrite command the data is written to the memory array allowing to change each bit to '0' or to '1'. With the program command only the data bits equal to '0' are written to the memory array, while the data bits equal to '1' are not.

The overwrite operation is performed by the embedded controller.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:

Write 0x0042 to the Command Code Register,

Write desired location address to the Command Address Register,

Write desired program data to the Command Data Register (Command Data[15:0] only),

Write 0x0001 to the Command Execute Register.

Overwriting can be performed in one block at a time.

The Status Register DRB bit, indicates the progress of the Overwrite operation. It should be read to check whether the operation has completed or not.

After completion of the overwrite operation (DRB= 1), one of the Status Register error bits (4, 3 and 1) going High means that an error was detected: either a failure occurred during overwriting, VACC is outside the allowed voltage range or an attempt to overwrite a locked Block was made. See 4.1.1.8 for detailed information.

The overwrite operation may be suspended.

The overwrite is aborted by writing MR63, or writing 0x0001 to the Abort Register (if supported).

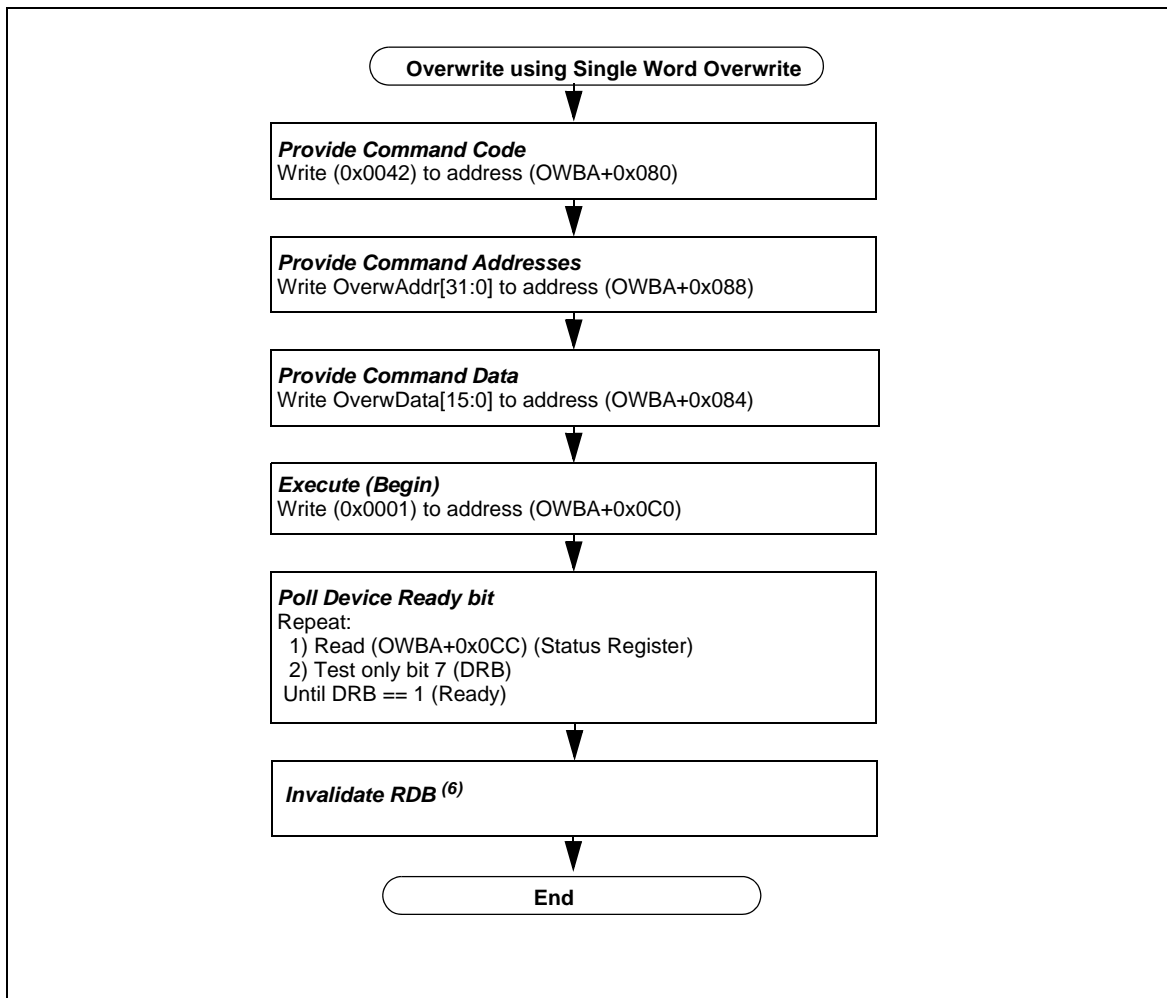
As data integrity cannot be guaranteed when the overwrite operation is aborted, the data must be rewritten.

**Table 41 — Single Word Overwrite Error Conditions**

7	6 <sup>(1)</sup>	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Single Word Overwrite operation failure.
1	0	0	1	0	0	1	0	Single Word Overwrite operation abort. An overwrite operation was attempted on a locked block.
1	0	0	1	1	0	0	0	Single Word Overwrite operation abort. Program voltage violation.
1	0	1	1	0	0	0	0	Single Word Overwrite operation abort. Overwrite address outside the LPDDR2-NVM address space
1	0	1	1	0	1	0	0	Single Word Overwrite operation abort. Attempting to program during Overwrite Suspend or Program Suspend.

NOTE 1: ESSB Status Register bit is '1' in case of command issued during Erase Suspend.

#### 4.7.6 Single Word Overwrite Command (cont'd)



NOTE 1 The Overlay Window must be open to issue Single Word Overwrite command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 OverwAddr[31:0] is the target byte address of the overwriting operation, and OverwAddr[0] shall be '0'.

NOTE 5 OverwData[15:0] is the desired 2-byte data to be overwritten.

NOTE 6 RDB invalidation may be required to avoid risk of incoherency between memory array content and RDB content. For more details refer to [4.7.12](#).

**Figure 13 — Single Word Overwrite Flowchart**

#### 4.7.7 Buffered Program Command

The Buffered Program Command makes use of the device's Program Buffer to speed up programming.

The Buffered Program command dramatically reduces in-system programming time compared to other non-buffered program commands.

If N is the size of the Program Buffer within the Overlay Window, up to N-Bytes can be loaded into the Program Buffer and programmed into the specified N-Byte aligned location in the main array. The region is determined by bit [31: K] of the Command Address Register value, where  $N=2^k$ .

The first word data of the Program Buffer to be programmed depends on bit [K-1:0] of Command Address value. The programming operation proceeds for a contiguous number of bytes equal to the Data Count value. The Data Count value is in units of bytes and written in the Multi-Purpose Registers.

**If the Command Address [K-1:0] value plus the Data Count Register value exceeds the program buffer boundary (N-byte), the programming operation ends without programming the memory array and the Status Register will show an error (0xB0).**

The programming operation doesn't wrap within the program buffer and doesn't cross into the next programming region.

The Overlay Window must be open and the device must be ready (DRB= 1) before starting the command sequence.

The Command Sequence is:

Write the starting address to the Command Address registers,  
Write the Data Count value (number of bytes to be programmed) to the Multi-Purpose Registers,  
Write data into the Program Buffer. The Program Buffer fits within the N-byte aligned array space,  
Write 0x00E9 to the Command Code Register,  
Write 0x0001 to the Command Execute Register.

If the Block being programmed is locked an error will be set in the Status Register and the operation will abort without affecting the data in the memory array.

The Buffered Program operation can be suspended.

The program is aborted by writing MR63, or writing 0x0001 to the Abort Register (if supported). As data integrity cannot be guaranteed when the program operation is aborted, the memory array content must be considered invalid.

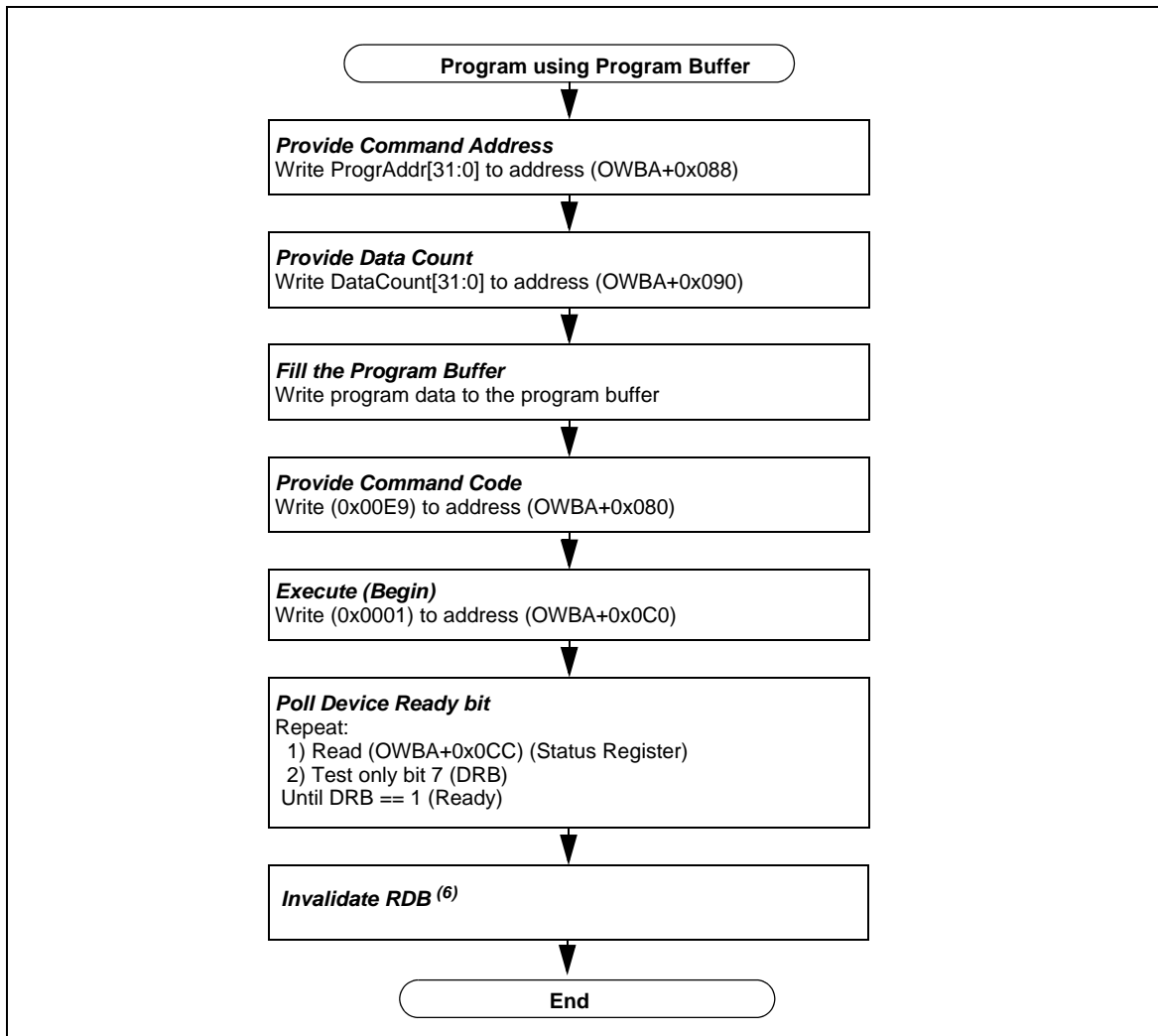
**Table 42 — Buffered Program Error Conditions**

7	6 <sup>(1)</sup>	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Buffered Program operation failure.
1	0	0	1	0	0	1	0	Buffered Program operation abort. An program operation was attempted on a locked block.
1	0	0	1	1	0	0	0	Buffered Program operation abort. Invalid VACC voltage.
1	0	1	1	0	0	0	0	Buffered Program operation abort. Program address outside the LPDDR2-NVM address space
1	0	1	1	0	1	0	0	Buffered Program operation abort. Attempting to program during Program Suspend.
1	0	1	1	0	0	0	0	Buffered Program operation abort. Command Address [K-1:0] value plus the Data Count Register value exceeds the program buffer boundary (it is greater than N byte).

NOTE 1: ESSB Status Register bit is '1' in case of command issued during Erase Suspend.

#### 4.7.7 Buffered Program Command (cont'd)

Figure 14 shows the Buffered Program Flowchart.



NOTE 1 The Overlay Window must be open to issue Buffered Program command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 DataCount[31:0] is amount of byte being programmed

NOTE 5 ProgrAddr[31:0] is the target byte address of the programming operation.

NOTE 6 RDB invalidation may be required to avoid risk of incoherency between memory array content and RDB content. For more details refer to 4.7.12.

Figure 14 — Buffered Program Flowchart

#### 4.7.8 Buffered Overwrite Command

This is a command supported only by some NVM technologies and LPDDR2-NVM devices.

The Buffered Overwrite Command makes use of the device's Program Buffer to speed up overwriting data to the memory array. The Buffered Overwrite command reduces in-system overwriting time compared to other non-buffered overwrite commands.

The overwrite command allows to change the status of each bit from '1' to '0' or from '0' to '1'.

With the overwrite command the data is written to the memory array allowing to change each bit to '0' or to '1'. With the program command only the data bits equal to '0' are written to the memory array, while the data bits equal to '1' are not.

If N is the size of the Program Buffer within the Overlay Window, up to N-Bytes can be loaded into the Program Buffer and overwritten into the specified N-Byte aligned location in the main array. The region is determined by bit [31: K] of the Command Address Register value, where  $N=2^k$ .

The first word data of the Program Buffer to be overwritten depends on bit [K-1:0] of Command Address value. The overwriting operation proceeds for a contiguous number of bytes equal to the Data Count value. **The Data Count value is in units of bytes and written in the Multi-Purpose Registers.**

If the Command Address [K-1:0] value plus the Data Count Register value exceeds the program buffer boundary (N-byte), **the overwriting operation ends without overwriting the memory array and the Status Register will show an error (0xB0).**

**The overwriting operation doesn't wrap within the program buffer and doesn't cross into the next programming region.**

The Overlay Window must be open and the device must be ready (DRB= 1) before starting the command sequence.

The Command Sequence is:

Write the starting address to the Command Address Registers,

Write the Data Count value (number of bytes to be overwritten) to the Multi-Purpose Registers,

Write data into the Program Buffer. The Program Buffer fits within the N-byte aligned array space,

Write 0x00EA to the Command Code Register,

Write 0x0001 to the Command Execute Register.

If the Block being overwritten is locked an error will be set in the Status Register and the operation will abort without affecting the data in the memory array.

The Buffered Overwrite operation can be suspended.

The overwrite is aborted writing MR63, or writing 0x0001 to the Abort Register (if supported). As data integrity cannot be guaranteed when the overwrite operation is aborted, the memory array content must be considered invalid.

**Table 43 — Buffered Overwrite Error Conditions**

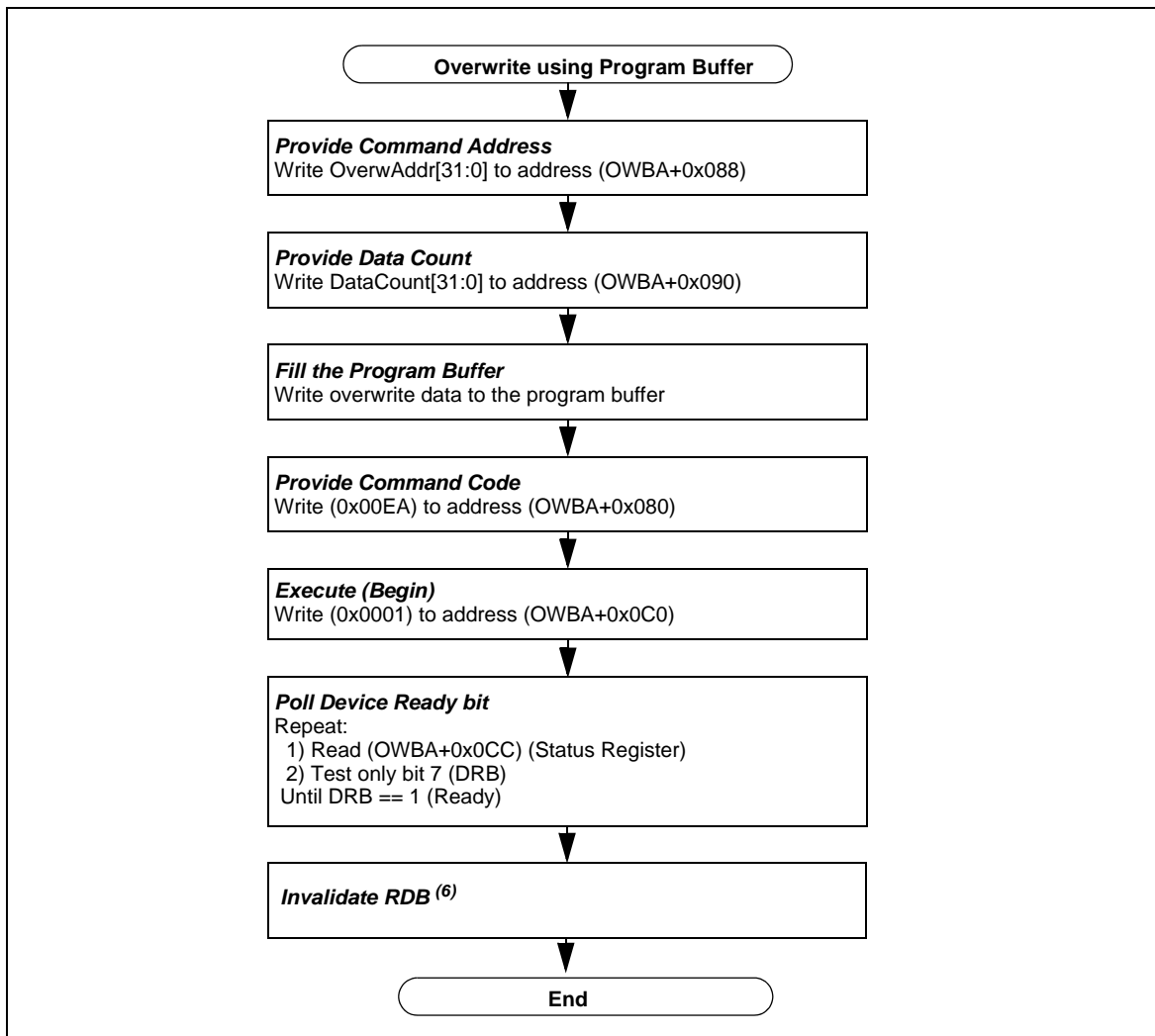
7	6 <sup>(1)</sup>	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Buffered Overwrite operation failure.
1	0	0	1	0	0	1	0	Buffered Overwrite operation abort. An overwrite operation was attempted on a locked block.
1	0	0	1	1	0	0	0	Buffered Overwrite operation abort. Invalid VACC voltage.
1	0	1	1	0	0	0	0	Buffered Overwrite operation abort. Overwrite address outside the LPDDR2-NVM address space
1	0	1	1	0	1	0	0	Buffered Overwrite operation abort. Attempting to overwrite during Overwrite Suspend or Program Suspend.
1	0	1	1	0	0	0	0	Buffered Overwrite operation abort. Command Address [K-1:0] value plus the Data Count Register value exceeds the program buffer boundary (it is greater than N byte).

NOTE 1: ESSB Status Register bit is '1' in case of command issued during Erase Suspend.



#### 4.7.8 Buffered Overwrite Command (cont'd)

Figure 15 shows the Buffered Overwrite Flowchart.



NOTE 1 The Overlay Window must be open to issue Buffered Overwrite command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 DataCount[31:0] is amount of byte being overwritten

NOTE 5 OverwAddr[31:0] is the target byte address of the overwriting operation.

NOTE 6 RDB invalidation may be required to avoid risk of incoherency between memory array content and RDB content. For more details refer to 4.7.12 .

**Figure 15 — Buffered Overwrite Flowchart**

#### 4.7.9 Program/Erase Suspend

The Program/Erase Suspend request pauses a program or block erase operation. The Program/Erase Resume command is required to restart the suspended operation.

Program or erase operations can be suspended. For the complete list of embedded operations that can be suspended, refer to the device datasheet.

The Program/Erase Suspend request is issued by writing '0x0001' to '1' the Suspend Register.

Once the Embedded Controller has paused, bits DRB, ESSB and/or PSSB of the Status Register are set to '1'.

The following operations shall be allowed during Program/Erase Suspend:

- Program/Erase Resume
- Read Array (data from erase-suspended block or program-suspended locations is not valid)

Additionally, if the suspended operation was a Block Erase then the following commands are also accepted:

- Single Word Program (except in erase-suspended Block)
- Buffered Program (except in erase suspended Block)
- Block Lock
- Block Unlock

For the complete list of supported commands during Program or Erase Suspend refer to the device datasheet. Commands not supported during Program or Erase Suspend shall be ignored.

During an erase suspend the Block being erased can be protected by issuing the Block Lock. When the Program/Erase Resume command is issued the operation will complete.

During a program suspend it is not allowed to write the program buffer.

It is possible to accumulate multiple suspend operations. For example: suspend an erase operation, start a program operation, suspend the program operation, then read the array. If a Program command is issued during a Block Erase Suspend, the erase operation cannot be resumed until the program operation has completed.

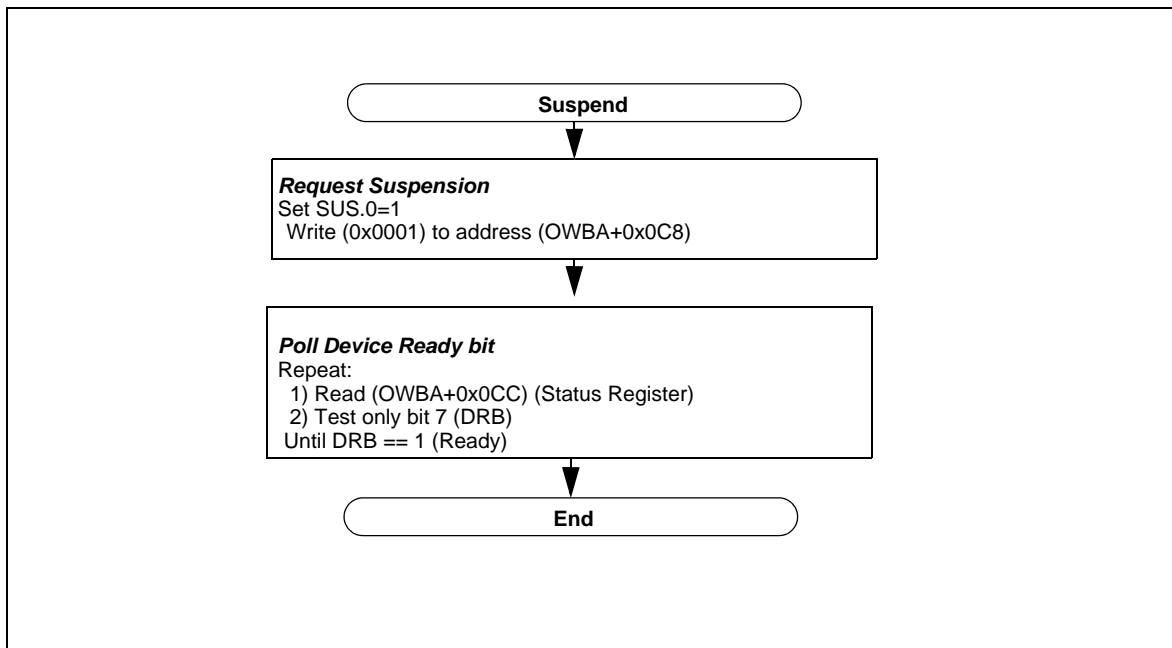
During a Program/Erase Suspend, the device can be placed in Power Down mode by driving CKE low, see Power Down section for detailed description on how to enter and exit Power Down.

Program/Erase is aborted by writing MR63, or writing 0x0001 to the Abort Register (if supported).

Note that some NVM technologies do not need Erase command, therefore some NVM devices will not support it.

#### 4.7.9 Program/Erase Suspend (cont'd)

Figure 16 shows the Program/Erase Suspend Request flowchart.



NOTE 1 The Overlay Window must be open to issue the Program/Erase Suspend command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address.

**Figure 16 — Program/Erase Suspend Request Flowchart**

#### 4.7.10 Program/Erase Resume Command

The Program/Erase Resume command is used to restart a previously suspended program or erase operation.

For the complete list of embedded operations that can be resumed, refer to the device datasheet.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:

**Write 0x00D0 to the Command Code Register**

**Write 0x0001 to the Command Execute Register.**

The command doesn't require to load any value to the Command Address Register within the Overlay Window. It is allowed to issue the Program/Erase resume command only when the embedded controller is in the Ready state and if a program or erase operations has been suspended.

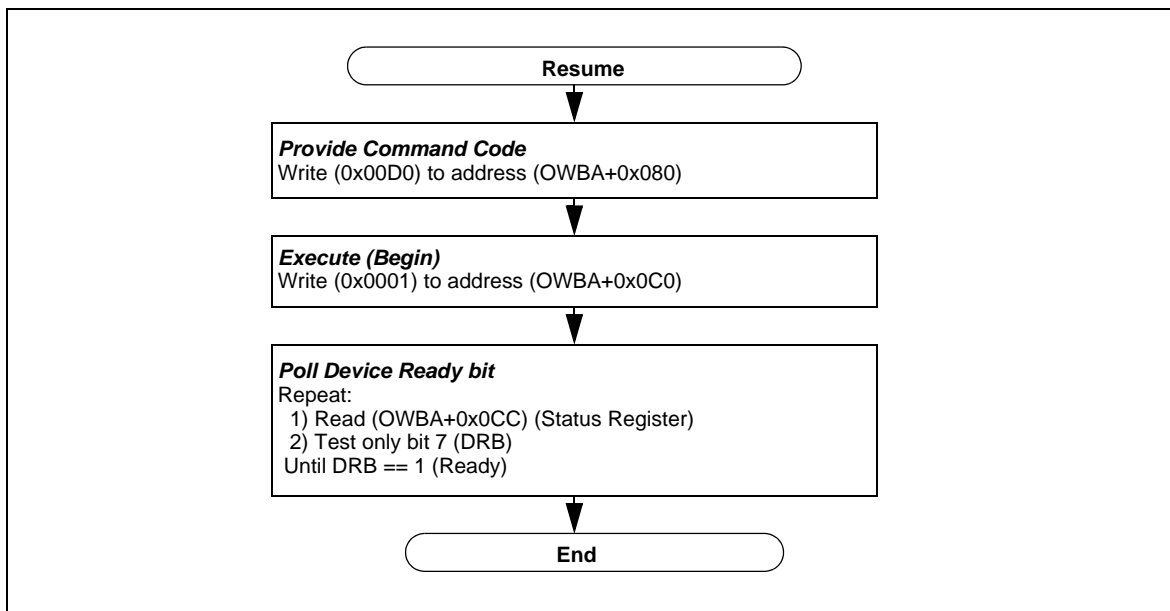
**A Resume command when no operation is suspended will be ignored.**

If a Program command is issued during a Block Erase Suspend, then the erase cannot be resumed until the program operation has completed.

If an Erase and a Program operation are suspended, the Resume command will Resume the Program command.

Note that some NVM technologies do not need Erase command, therefore some NVM devices will not support it.

Figure 17 shows the Program/Erase Resume command flowchart.



NOTE 1 The Overlay Window must be open to issue the Resume command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address.

NOTE 3 The device must be Ready (DRB==1) before starting the command sequence.

**Figure 17 — Program/Erase Resume Command Flowchart**

#### 4.7.11 Abort

The Abort request ends all embedded operations.

If any embedded operation is aborted and does not complete due to an abort request, the operation will fail and one or more Status Register bits will be set.

The Abort request is issued by writing '0x0001' to the Abort Register.

The Abort request is ignored if the Abort Register is written when the device is ready (DRB = "1").

Therefore, if the device is in program or/and erase suspend, the device will remain in the same status.

In particular, if the device is executing a program operation (DRB = "0") while it is in erase suspend, the program will be aborted but the device will remain in erase suspend.

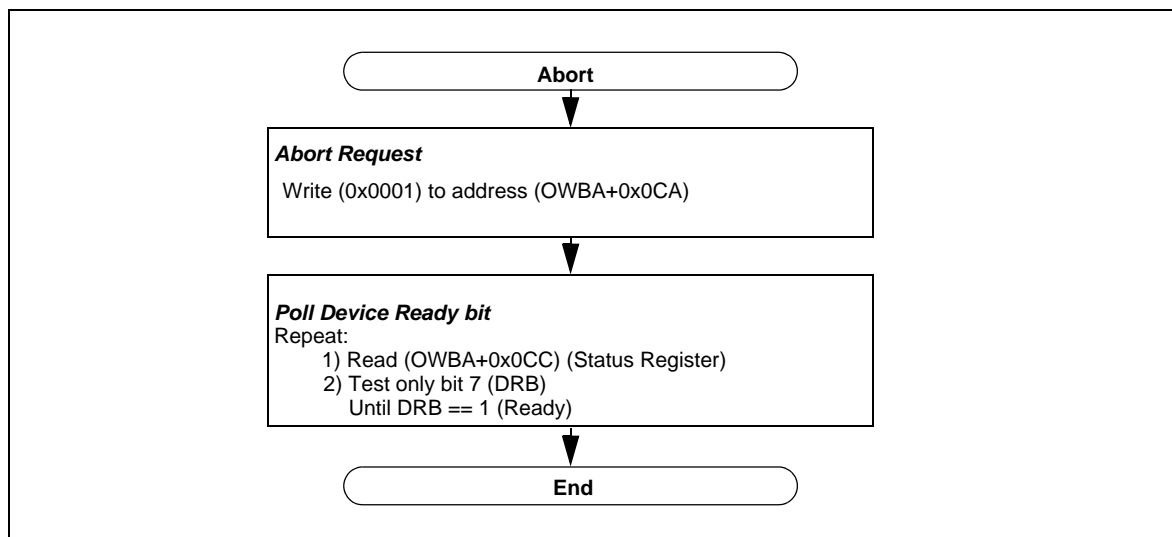
Once the embedded controller has completed the abort request, bit DRB of the Status Register is set to '1' and the Abort Register is set to '0x0000' by the LPDDR2-NVM device.

Abort feature is optional. If LPDDR2-NVM does not support abort feature, Abort Register may be written only with 0x0000, and when read it shall output the value 0x0000.

**Table 44 — Abort Error Conditions**

7	6	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Abort request issued during program operation. Abort request issued while program suspend.
1	0	1	0	0	0	0	0	Abort request issued during erase operation. Abort request issued while erase suspend.
1	0	1	1	0	0	0	0	Abort request issued during erase and program suspend. Abort request issued during program operation and erase suspend.

Figure 18 shows the Abort Request flowchart.



NOTE 1 The Overlay Window must be open to issue the Abort command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address.

**Figure 18 — Abort Request Flowchart**

#### **4.7.12 Row Data Buffer Incoherency**

The ACTIVATE command copies a row content from the memory array to the Row Data Buffer selected by the BA signals. While a row is open in one Row Data Buffer, the host may program, overwrite or erase that particular row.

Once the program, overwrite or erase operation is completed (DRB = '1'), LPDDR2-NVM device will not update the Row Data Buffer with the new row content, generating an incoherency between Row Data Buffer and memory array.

The host shall be aware of this incoherency risk, and manage it in hardware or/and software.

#### 4.8 Dual operations and multiple partition architecture

In some LPDDR2-NVM devices, the memory array may be divided into two or more partitions (multiple partition architecture). Refer to vendor datasheets to determine support for multiple partition architecture.

LPDDR2-NVM devices that support multiple partition architecture provide greater flexibility for software developers to split the code and data spaces within the memory array. The dual operations feature simplifies the software management of the device by allowing code to be executed from one partition while another partition is being programmed or erased.

The dual operations feature means that while programming or erasing in one partition, read operations are possible in another partition with zero latency (only one partition at a time is allowed to be in program or erase mode).

If a read operation is required in a partition, which is programming or erasing, the program or erase operation can be suspended.

Also, if the suspended operation is erase then a program command can be issued to another block, so the device can have one block in erase suspend mode, one programming, and other partitions available for read operations.

For the complete list of dual operations allowed, refer to the device datasheet.

**Table 45 — Simultaneous operations allowed in the same partition**

Status of partition	Operations allowed in the same partition		
	Read <sup>(1)</sup>	Buffered Program	Block Erase
Idle	Yes	Yes	Yes
Programming <sup>(2)</sup>	No	No	No
Erasing	No	No	No
Program suspended	Yes <sup>(3)</sup>	No	No
Erase suspended	Yes <sup>(4)</sup>	Yes <sup>(5)</sup>	No

NOTE 1 Depending on the Overlay Window status and the target read address, data may come from the memory array or from the overlay window.

NOTE 2 Programming may occur during erase suspended.

NOTE 3 LPDDR2-NVM will output invalid data if the read operation occurs in the memory area that is being programmed.

NOTE 4 LPDDR2-NVM will output invalid data if the read operation occurs in the block that is being erased.

NOTE 5 Not allowed in the block that is being erased.

**Table 46 — Simultaneous operations allowed in other partitions**

Status of partition	Operations allowed in another partition		
	Read <sup>(1)</sup>	Buffered Program	Block Erase
Idle	Yes	Yes	Yes
Programming <sup>(2)</sup>	Yes	No	No
Erasing	Yes	No	No
Program suspended	Yes	No	No
Erase suspended	Yes	Yes	No

NOTE 1 Depending on the Overlay Window status and the target read address, data may come from the memory array or from the overlay window.

NOTE 2 Programming may occur during erase suspended.

## 5 LPDDR2 Command Definitions and Timing Diagrams

### 5.1 Activate Command

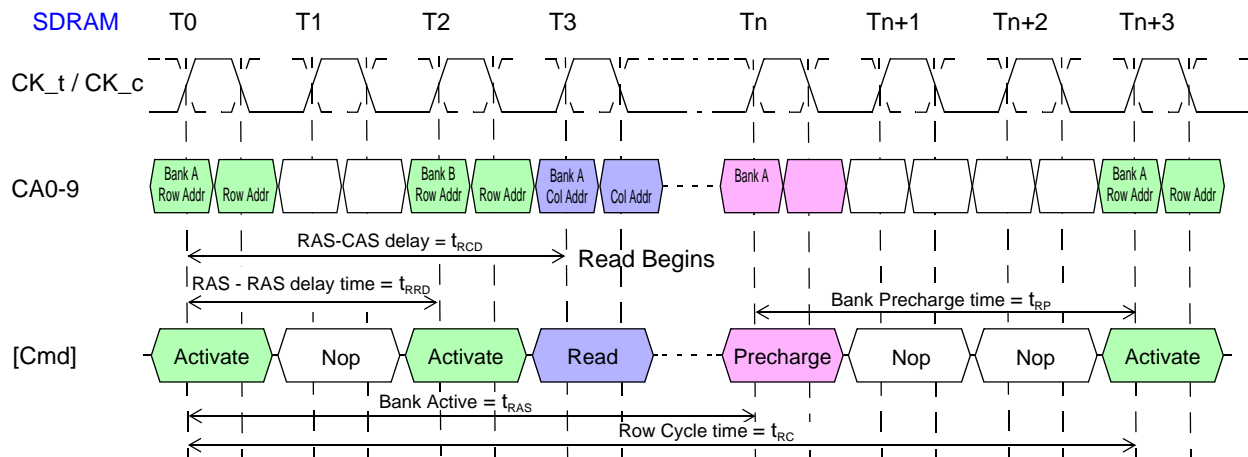
#### 5.1.1 LPDDR2-SX: Activate Command

The SDRAM Activate command is issued by holding CS\_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 - BA2 are used to select the desired bank. The row address R0 through R14 is used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The LPDDR2 SDRAM can accept a read or write command at time  $t_{\text{RCD}}$  after the activate command is sent. Once a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as  $t_{\text{RAS}}$  and  $t_{\text{RP}}$  respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device ( $t_{\text{RC}}$ ). The minimum time interval between Activate commands to different banks is  $t_{\text{RRD}}$ .

Certain restrictions on operation of the 8-bank devices must be observed. There are two rules. One for restricting the number of sequential Activate commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

- 8-bank device Sequential Bank Activation Restriction : No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling  $t_{\text{FAW}}$  window. Converting to clocks is done by dividing  $t_{\text{FAW}}[\text{ns}]$  by  $t_{\text{CK}}[\text{ns}]$ , and rounding up to next integer value. As an example of the rolling window, if  $\text{RU}\{ (t_{\text{FAW}} / t_{\text{CK}}) \}$  is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9. REFpb also counts as bank-activation for the purposes of  $t_{\text{FAW}}$ .

- 8-bank device Precharge All Allowance :  $t_{\text{RP}}$  for a Precharge All command for an 8-bank device shall equal  $t_{\text{RPab}}$ , which is greater than  $t_{\text{RPpb}}$ .



**Figure 19 — LPDDR2-SX: Activate command cycle:  $t_{\text{RCD}} = 3$ ,  $t_{\text{RP}} = 3$ ,  $t_{\text{RRD}} = 2$**

NOTE 1 A Precharge-All command uses  $t_{\text{RPab}}$  timing, while a Single Bank Precharge command uses  $t_{\text{RPpb}}$  timing. In this figure,  $t_{\text{RP}}$  is used to denote either an All-bank Precharge or a Single Bank Precharge.



### 5.1.1 LPDDR2-SX: Activate Command (cont'd)

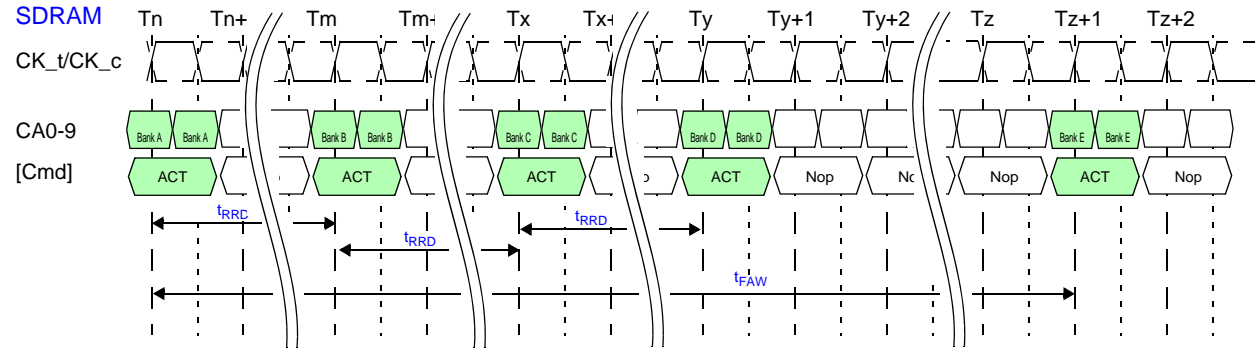


Figure 20 — LPDDR2-SX:  $t_{FAW}$  timing

NOTE 1: For 8-bank devices only. No more than 4 banks may be activated in a rolling  $t_{FAW}$  window.

### 5.1.2 LPDDR2-N: Activate Command

The NVM Activate command is issued by holding CS<sub>n</sub> LOW, CA0 LOW and CA1 HIGH at the rising edge of the clock. The Row Buffer (RB) addresses BA0 - BA2 are used to select the desired {RAB, RDB} pair. Devices may have four or eight Row Buffer pairs. Row Buffers do not correspond directly to any portion of the array; the controller may use any value of BA0 - BA2 for any array location.

Row address a5 through a19 is used in conjunction with the selected RAB contents to determine which row to load into the destination RDB. It is recommended to open any single row in only one Row Buffer. If a memory controller issues an Activate command that causes a single row to be open in more than one RDB, then only the last Row Data Buffer activated for that given row is valid. The Activate command may be issued only after BL/2 clock cycles after a previous Read command, or after WL+BL/2+1+RU(tWRA/tCK) clock cycles after a previous Write command.

The Activate command must be applied before any Read or Write operation can be executed. The LPDDR2 NVM can accept a read or write command at time  $t_{RCD}$  after the activate command is sent. The activate and preactive times are defined as  $t_{RAS}$  and  $t_{RP}$  respectively. The minimum time interval between successive Activate commands to the same Row Buffer pair is determined by the RAS cycle time of the device ( $t_{RC}$ ). The minimum time interval between Activate commands to different Row Buffer pairs is  $t_{RRD}$ .

Table 47 — Row Address Buffer selection for Preactive by BA inputs

BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Selected {RAB, RDB} (4-RB devices)	Selected {RAB, RDB} (8-RB devices)
0	0	0	RB 0	RB 0
0	0	1	RB 1	RB 1
0	1	0	RB 2	RB 2
0	1	1	RB 3	RB 3
1	0	0	RB 0	RB 4
1	0	1	RB 1	RB 5
1	1	0	RB 2	RB 6
1	1	1	RB 3	RB 7

### 5.1.2 LPDDR2-N: Activate Command (cont'd)

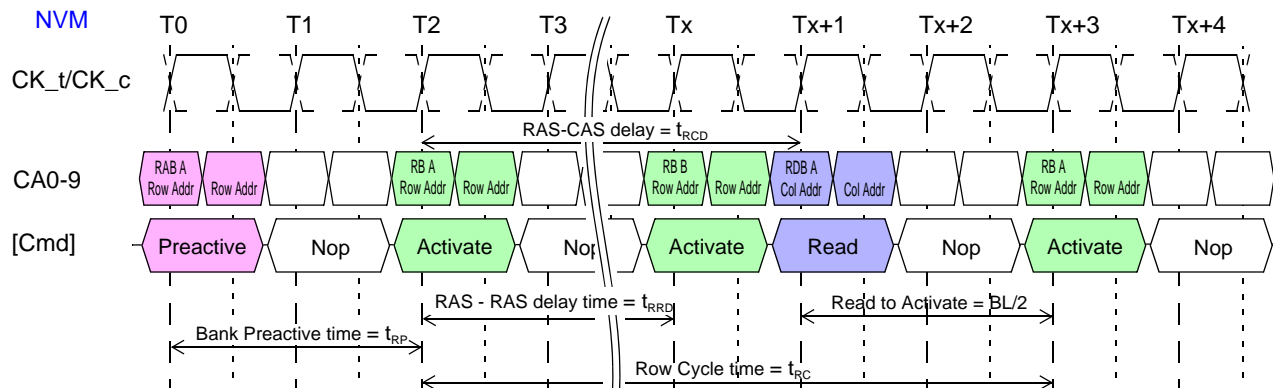
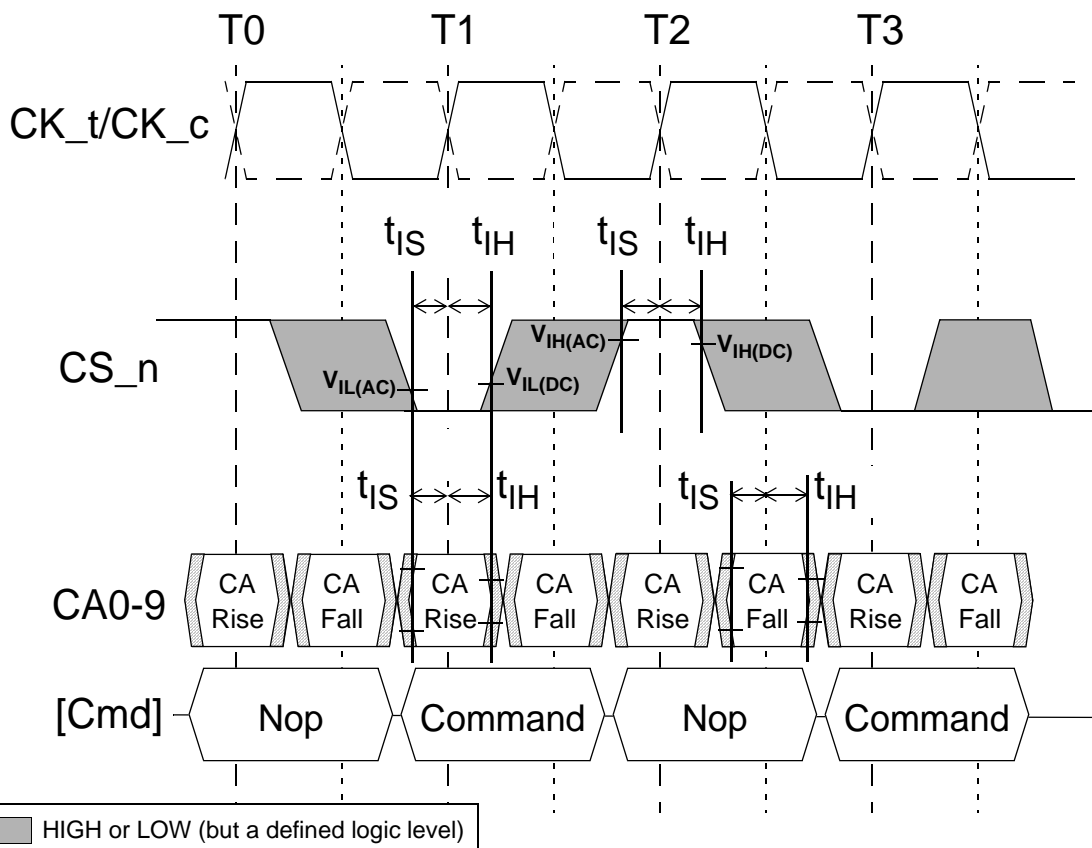


Figure 21 — LPDDR2-N: Activate command cycle:  $t_{RP} = 2$ ,  $BL = 4$

## 5.2 LPDDR2 Command Input Signal Timing Definition

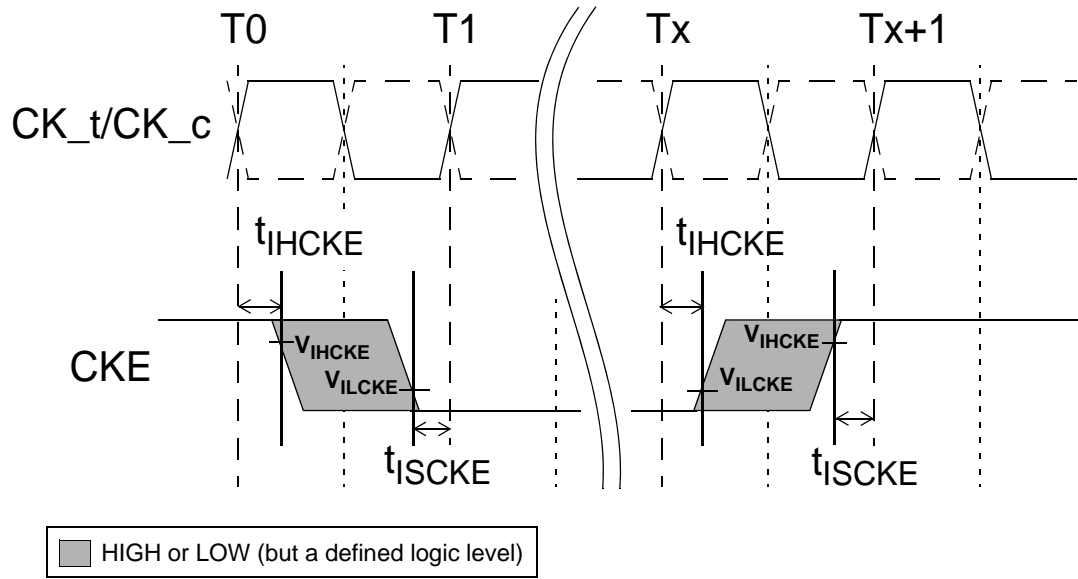
### 5.2.1 LPDDR2 Command Input Setup and Hold Timing



NOTE Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

Figure 22 — LPDDR2: Command Input Setup and Hold Timing

## 5.2.2 LPDDR2 CKE Input Setup and Hold Timing



NOTE 1: After CKE is registered LOW, CKE signal level shall be maintained below  $V_{ILCKE}$  for  $t_{CKE}$  specification (LOW pulse width).

NOTE 2: After CKE is registered HIGH, CKE signal level shall be maintained above  $V_{IHCKE}$  for  $t_{CKE}$  specification (HIGH pulse width).

**Figure 23 — LPDDR2: Command Input Setup and Hold Timing**

### **5.3 Read and Write access modes**

#### **5.3.1 LPDDR2-SX: Read and Write access modes**

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS<sub>n</sub> LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).

The LPDDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles.

For LPDDR2-S4 devices, a new burst access must not interrupt the previous 4-bit burst operation in case of BL = 4 setting. In case of BL = 8 and BL = 16 settings, Reads may be interrupted by Reads and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and  $t_{CCD}$  is met. For LPDDR2-S2 devices, Reads may interrupt Reads and Writes may interrupt Writes, provided that  $t_{CCD}$  is met. The minimum CAS to CAS delay is defined by  $t_{CCD}$ .

#### **5.3.2 LPDDR2-N: Read and Write access modes**

After an RB has been activated, a read or write cycle can be executed. This is accomplished by setting CS<sub>n</sub> LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).

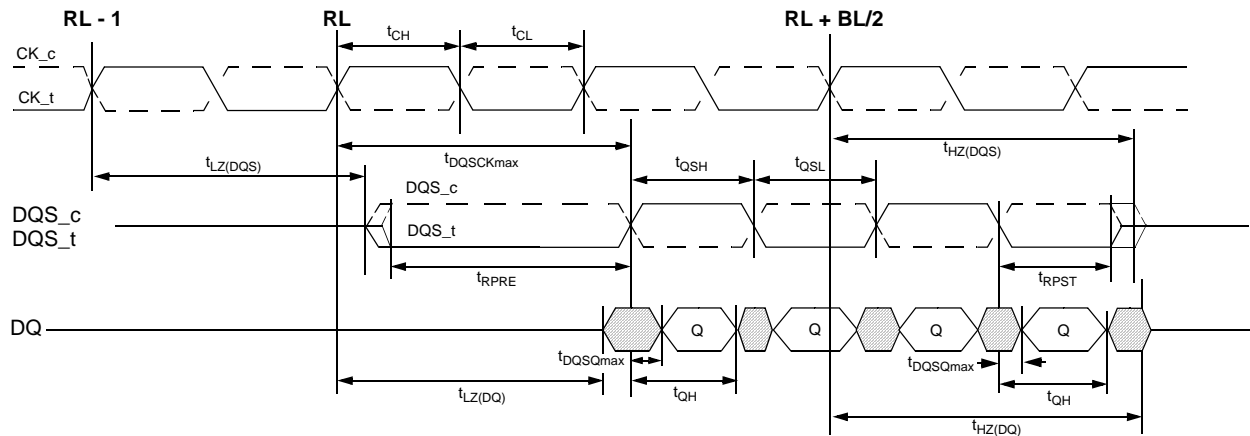
The LPDDR2 NVM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles. The boundary of the burst cycle is restricted to specific segments of the Row Data Buffer (RDB) size. For example, if the size of the RDB is 64 Bytes and the device has a 16 bit data bus interface, the page size of 512 bits is divided into 8, 4, or 2 uniquely addressable boundary segments depending on burst length, 8 for 4 bit burst, 4 for 8 bit burst, and 2 for 16 bit burst respectively. A 4-bit, 8-bit or 16-bit burst operation will occur entirely within one of the 8, 4 or 2 groups beginning with the column address supplied to the device during the Read or Write Command (C1-C4).

For LPDDR2-N devices, a new burst access must not interrupt the previous 4-bit burst operation in case of BL = 4 setting. In case of BL = 8 and BL = 16 settings, Reads may be interrupted by Reads and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and  $t_{CCD}$  is met. The minimum CAS to CAS delay is defined by  $t_{CCD}$ .

## 5.4 Burst Read Command

The Burst Read command is initiated by having CS\_n LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the  $t_{DQSCk}$  delay is measured. The first valid datum is available  $RL * t_{CK} + t_{DQSCk} + t_{DQSQ}$  after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW  $t_{RPRE}$  before the first rising valid strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin edge aligned with the data strobe. The RL is programmed in the mode registers.

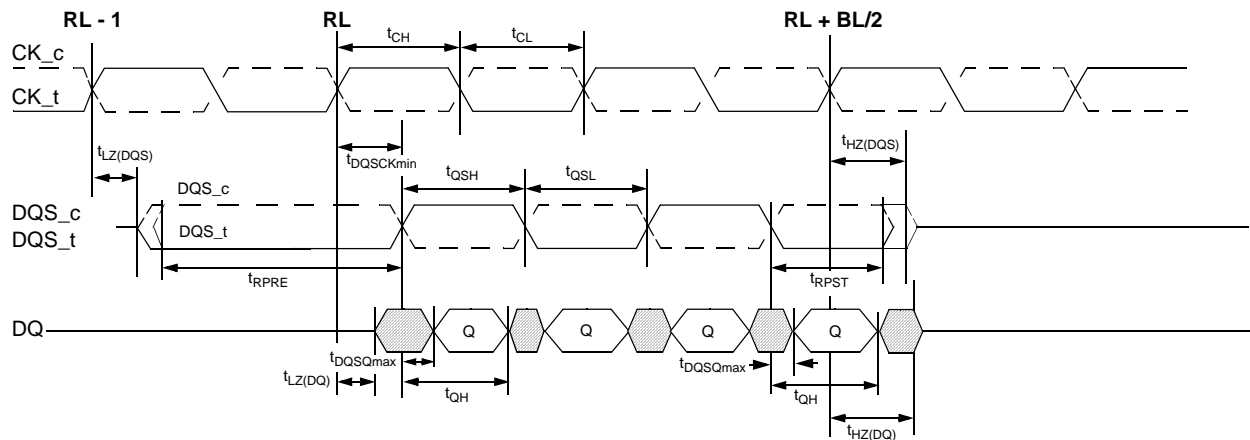
Timings for the data strobe are measured relative to the crosspoint of DQS\_t and its complement, DQS\_c.



**Figure 24 — Data output (read) timing ( $t_{DQSCkmax}$ )**

NOTE 1  $t_{DQSCk}$  may span multiple clock periods.

NOTE 2 An effective Burst Length of 4 is shown.



**Figure 25 — Data output (read) timing ( $t_{DQSCkmin}$ )**

NOTE 1 An effective Burst Length of 4 is shown.

#### 5.4 Burst Read Command (cont'd)

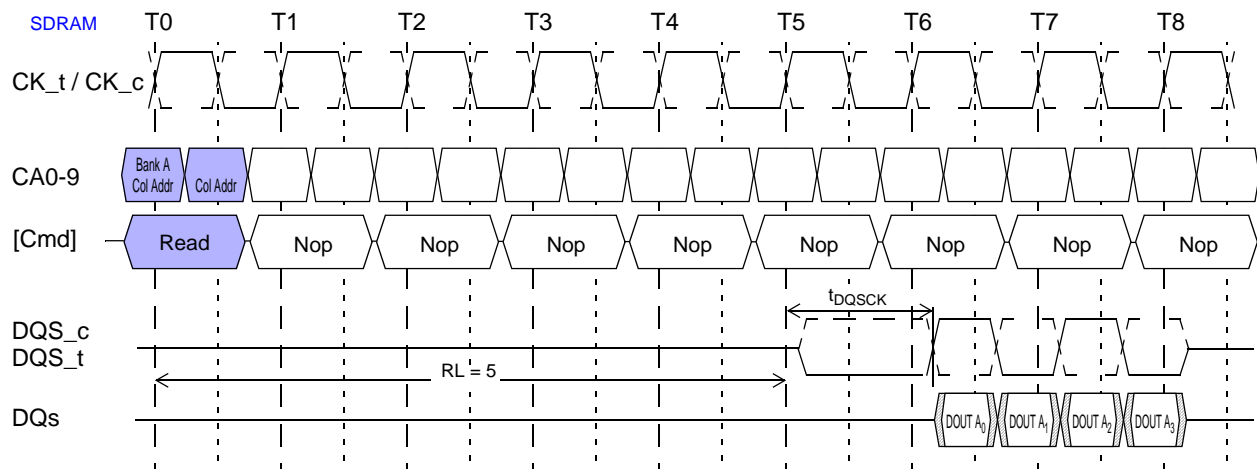


Figure 26 — LPDDR2-SX: Burst read: RL = 5, BL = 4,  $t_{DQsck} > t_{ck}$

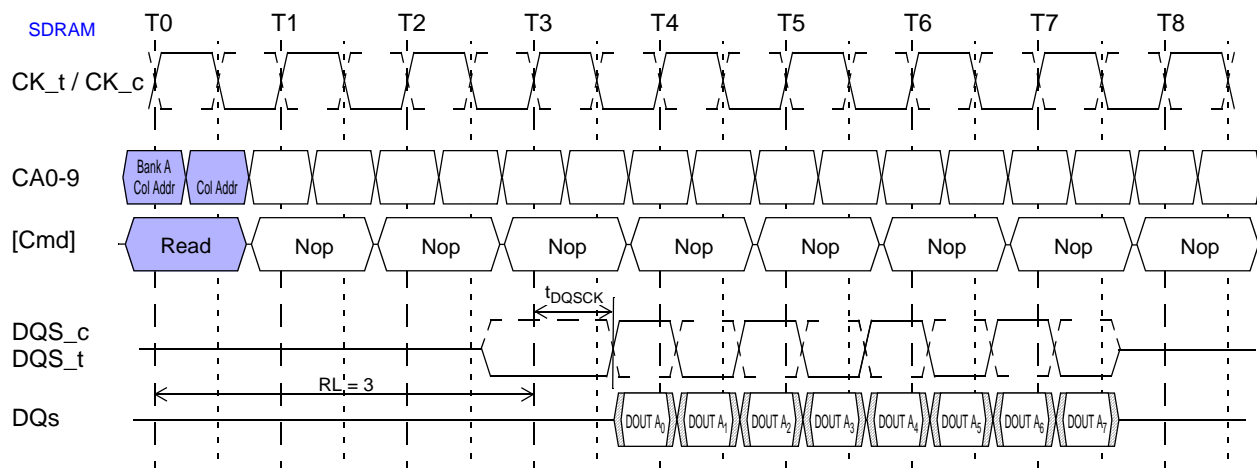


Figure 27 — LPDDR2-SX: Burst read: RL = 3, BL = 8,  $t_{DQsck} < t_{ck}$

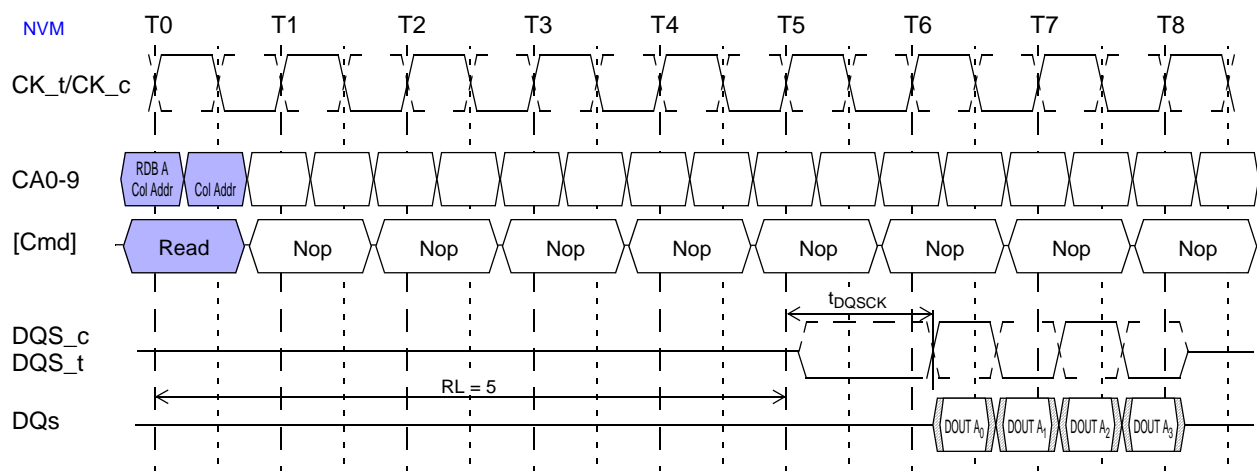


Figure 28 — LPDDR2-N: Burst read: RL = 5, BL = 4,  $t_{DQsck} > t_{ck}$

#### 5.4 Burst Read Command (cont'd)

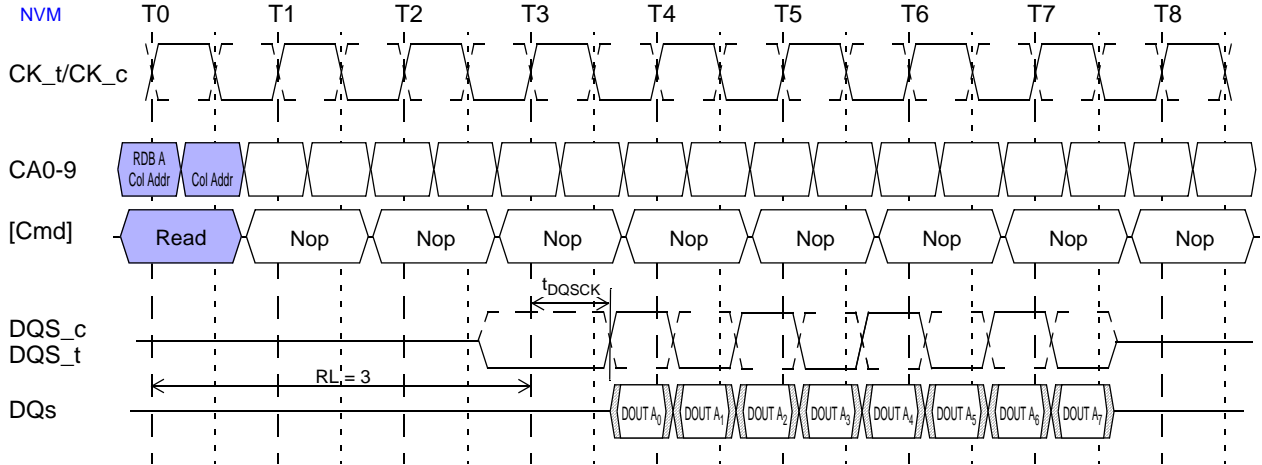
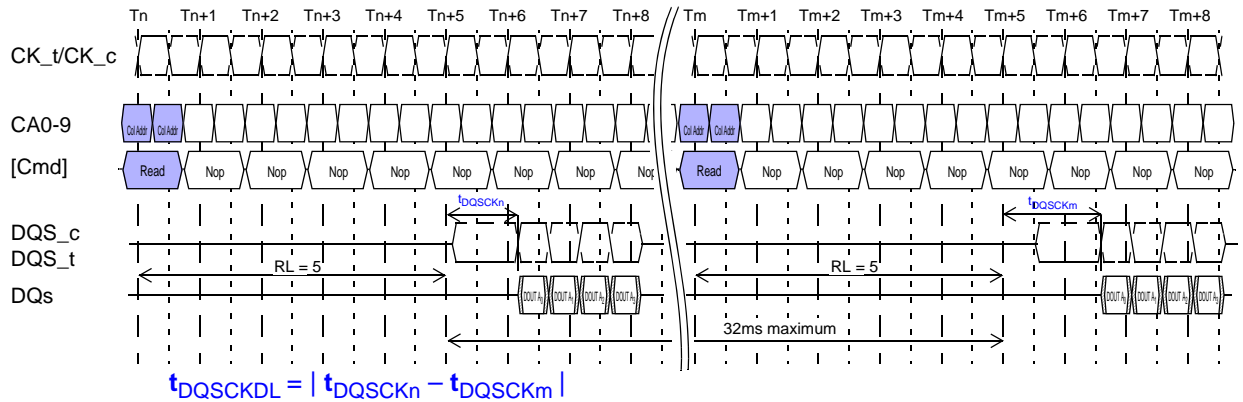


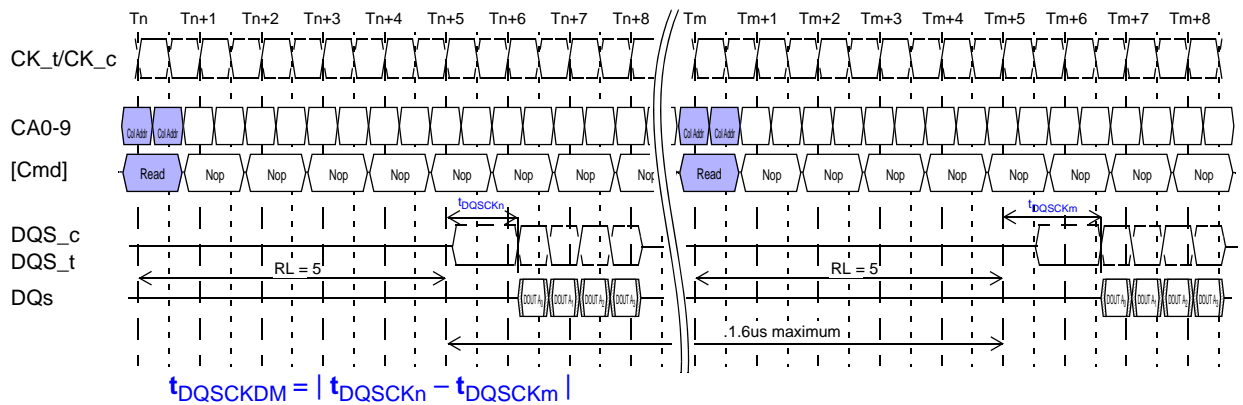
Figure 29 — LPDDR2-N: Burst read:  $RL = 3$ ,  $BL = 8$ ,  $t_{DQsck} < t_{ck}$



$$t_{DQsckDL} = |t_{DQsckn} - t_{DQsckm}|$$

Figure 30 — LPDDR2:  $t_{DQsckDL}$  timing

NOTE 1  $t_{DQsckDLmax}$  is defined as the maximum of  $ABS(t_{DQsckn} - t_{DQsckm})$  for any  $\{t_{DQsckn}, t_{DQsckm}\}$  pair within any 32ms rolling window.

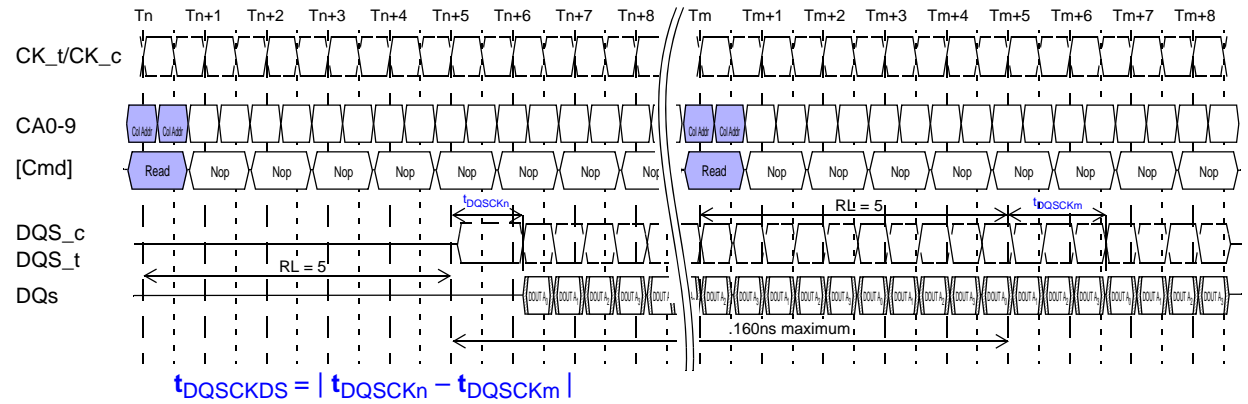


$$t_{DQsckDM} = |t_{DQsckn} - t_{DQsckm}|$$

Figure 31 — LPDDR2:  $t_{DQsckDM}$  timing

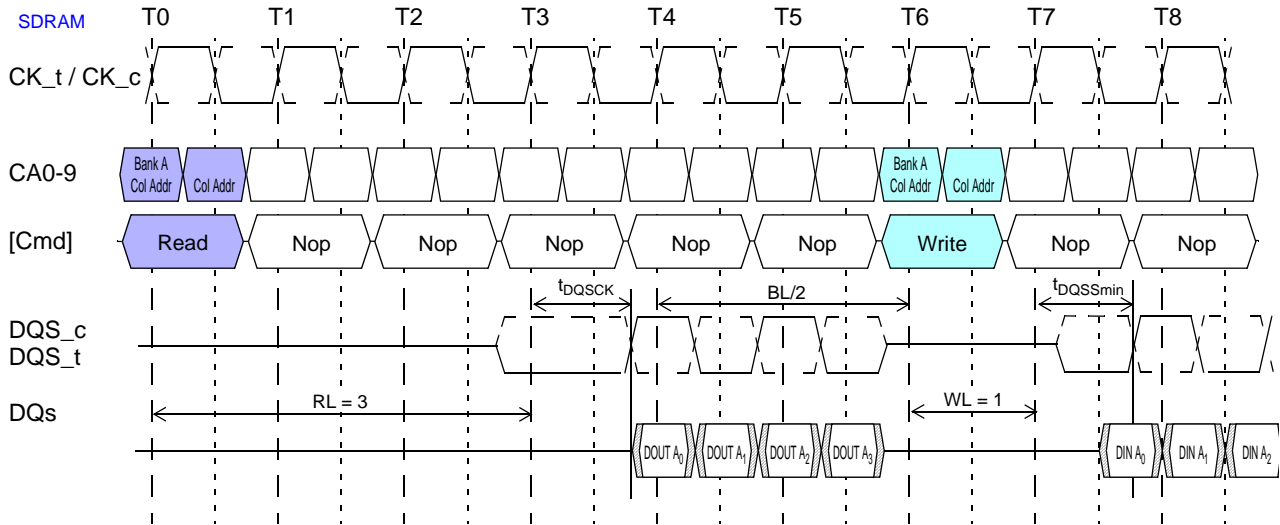
NOTE 1  $t_{DQsckDMmax}$  is defined as the maximum of  $ABS(t_{DQsckn} - t_{DQsckm})$  for any  $\{t_{DQsckn}, t_{DQsckm}\}$  pair within any 1.6us rolling window.

#### 5.4 Burst Read Command (cont'd)



**Figure 32 — LPDDR2:  $t_{DQCKDS}$  timing**

NOTE 1  $t_{DQCKDSmax}$  is defined as the maximum of  $ABS(t_{DQCKn} - t_{DQCKm})$  for any  $\{t_{DQCKn}, t_{DQCKm}\}$  pair for reads within a consecutive burst within any 160ns rolling window.



**Figure 33 — LPDDR2-SX: Burst read followed by burst write: RL = 3, WL = 1, BL = 4**



### 5.4Burst Read Command (cont'd)

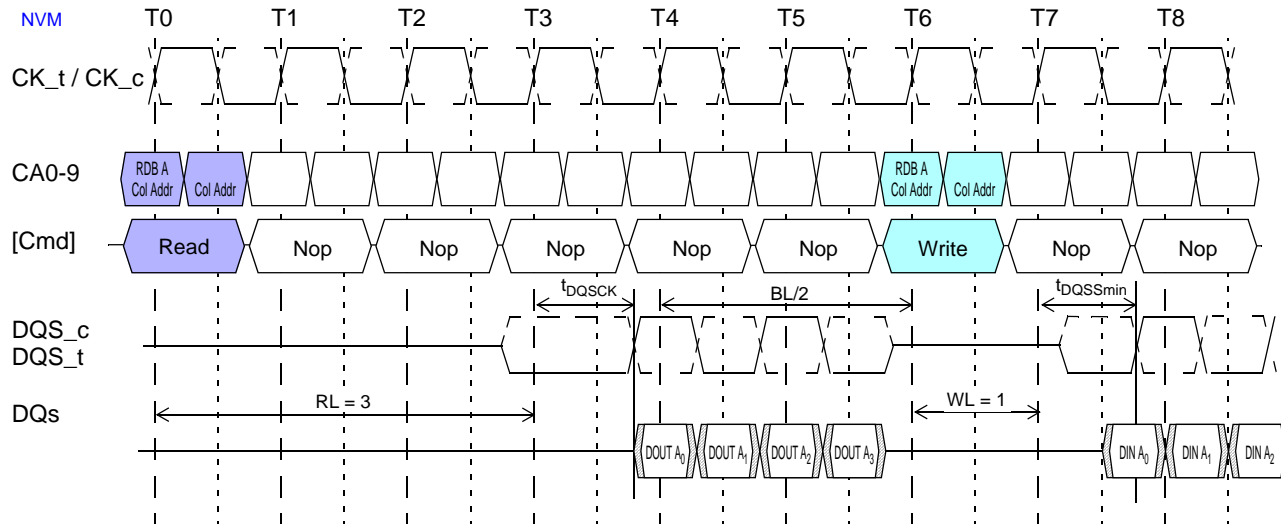


Figure 34 — LPDDR2-N: Burst read followed by burst write: RL = 3, WL = 1, BL = 4

The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum read to write latency is  $RL + RU(t_{DQSCKmax}/t_{CK}) + BL/2 + 1 - WL$  clock cycles. Note that if a read burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated read burst should be used as “BL” to calculate the minimum read to write delay.

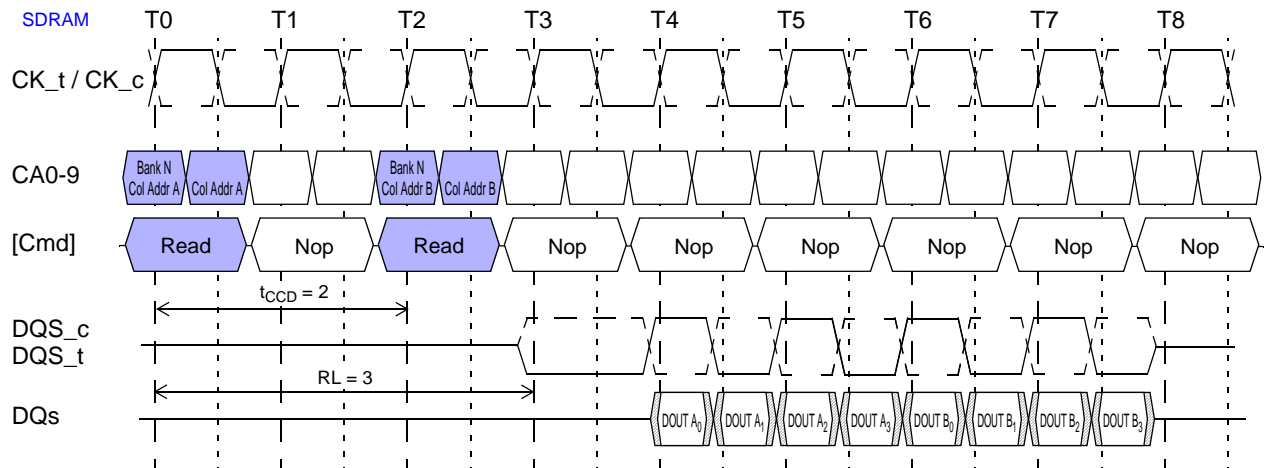
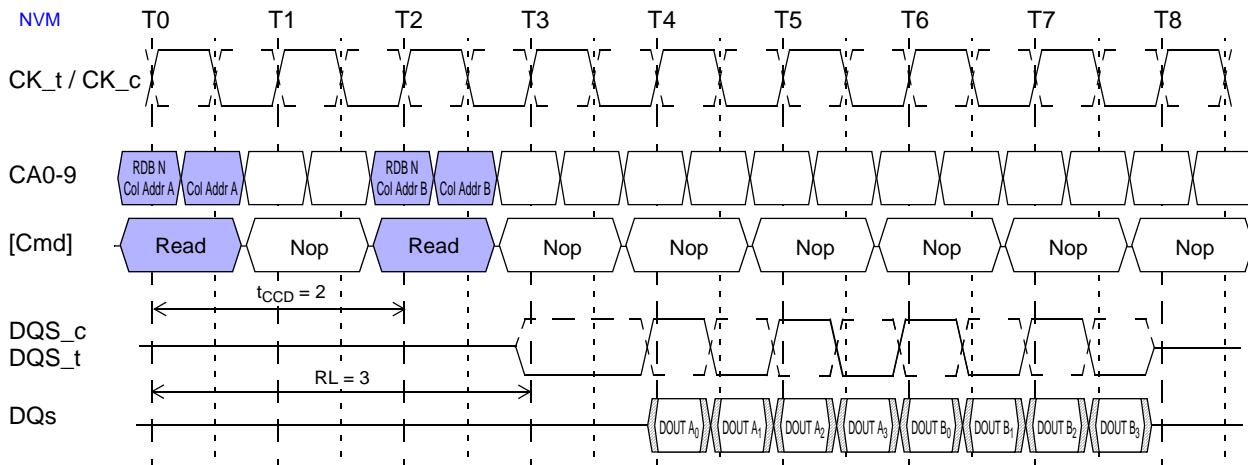


Figure 35 — LPDDR2-SX: Seamless burst read: RL = 3, BL = 4, t<sub>CCD</sub> = 2

## 5.4 Burst Read Command (cont'd)



**Figure 36 — LPDDR2-N: Seamless burst read:  $RL = 3$ ,  $BL = 4$ ,  $t_{CCD} = 2$**

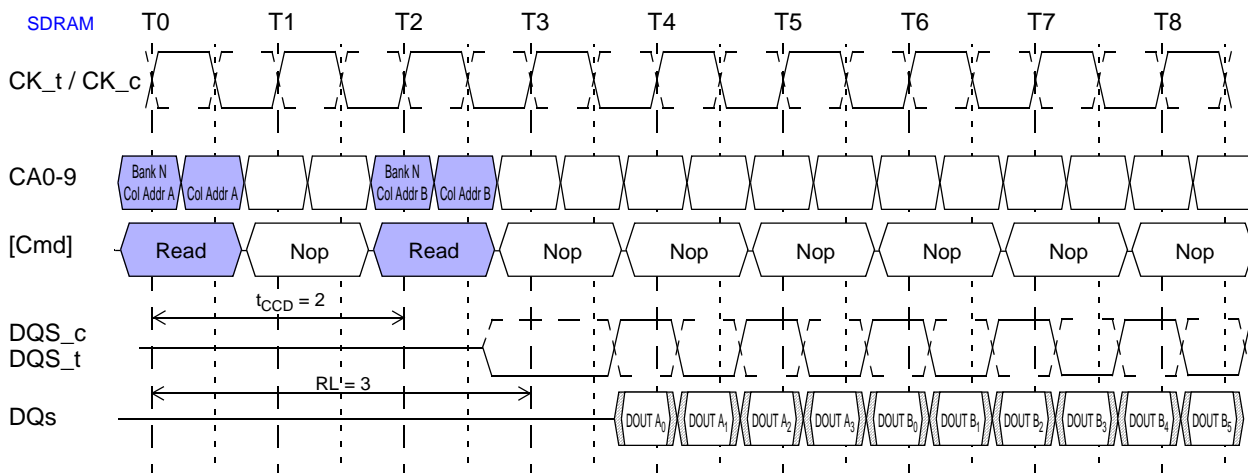
The seamless burst read operation is supported by enabling a read command at every other clock for  $BL = 4$  operation, every 4 clocks for  $BL = 8$  operation, and every 8 clocks for  $BL = 16$  operation.

For LPDDR2-SDRAM, this operation is allowed regardless of whether the accesses read the same or different banks as long as the banks are activated.

For LPDDR2-NVM, this operation is allowed regardless of whether the accesses read the same or different RDBs as long as the RDBs are activated.

### 5.4.1 Reads interrupted by a read

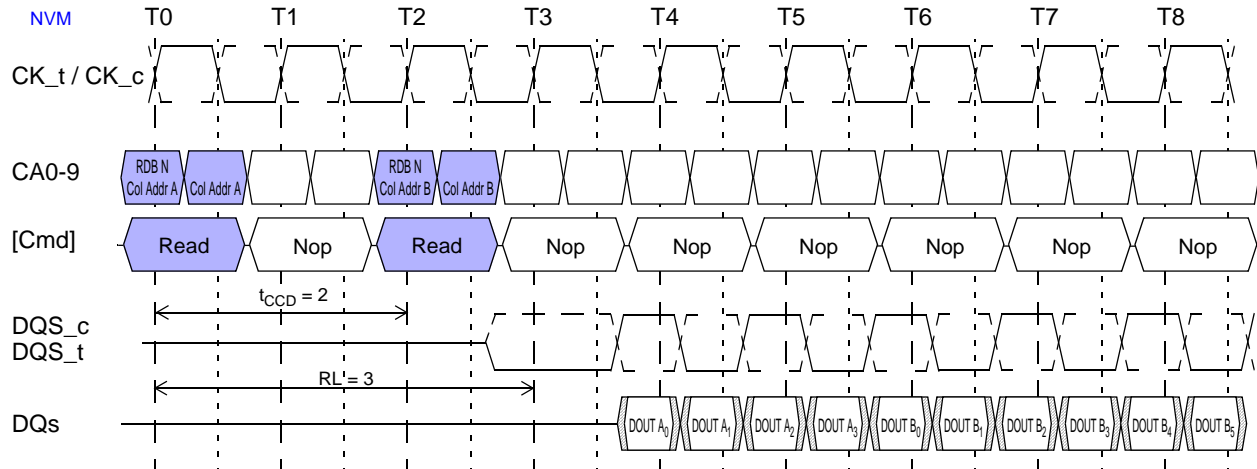
For LPDDR2-S4 and LPDDR2-N devices, burst read can be interrupted by another read on even clock cycles after the Read command, provided that  $t_{CCD}$  is met. For LPDDR2-S2 devices, burst reads may be interrupted by other reads on any subsequent clock, provided that  $t_{CCD}$  is met.



**Figure 37 — LPDDR2-SX: Read burst interrupt example:  $RL = 3$ ,  $BL = 8$ ,  $t_{CCD} = 2$**

- NOTE 1 For LPDDR2-S4 devices, read burst interrupt function is only allowed on burst of 8 and burst of 16.
- NOTE 2 For LPDDR2-S4 devices, read burst interrupt may only occur on even clock cycles after the previous read commands, provided that  $t_{CCD}$  is met.
- NOTE 3 For LPDDR2-S2 devices, read burst interrupt may occur on any clock cycle after the initial read command, provided that  $t_{CCD}$  is met.
- NOTE 4 Reads can only be interrupted by other reads or the BST command.
- NOTE 5 Read burst interruption is allowed to any bank inside DRAM.
- NOTE 6 Read burst with Auto-Precharge is not allowed to be interrupted.
- NOTE 7 The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

### 5.4.1 Reads interrupted by a read (cont'd)



**Figure 38 — LPDDR2-N: Read burst interrupt example: RL = 3, BL = 8,  $t_{CCD} = 2$**

- NOTE 1 For LPDDR2-N devices, read burst interrupt function is only allowed on burst of 8 and burst of 16.
- NOTE 2 For LPDDR2-N devices, read burst interrupt may only occur on even clock cycles after the previous read commands, provided that  $t_{CCD}$  is met.
- NOTE 3 Reads can only be interrupted by other reads or the BST command.
- NOTE 4 Read burst interruption is allowed to any RDB inside the NVM.
- NOTE 5 The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

### 5.4.2 LPDDR2: Data Not Valid

LPDDR2 devices will implement Data Not Valid (DNV) signal if they set MR0 OP2 bit to “1”, and will not implement Data Not Valid signal if they set MR0 OP2 bit to “0”. LPDDR2-SX devices will not implement DNV. DNV signal, when implemented, is outputted from the memory device with DQ data. The DNV signal and the Data Mask signal (DM) share the same pin. For information on the DM signal usage, see “Write data mask” on page 70. DNV signals follow the same timings as the DQ signals for read bursts. DNV0, DNV1, DNV2, and DNV3 timings are referenced to DQS0, DQS1, DQS2, and DQS3 respectively.

LPDDR2 devices that support Data Not Valid shall drive all DNV signal(s) to the same level for each data beat during read bursts. The DNV signal(s) are valid only the first four beats of a read burst. The beat 0 of the DNV signal shall be driven LOW if the data in the burst is valid. Beat 0 of the DNV signal shall be driven HIGH if the data in the burst is invalid. Beat 1 of DNV indicates how the controller may retry the request, (DNV = LOW) for immediate retry or (DNV = HIGH) for retry after a pre-specified time in micro seconds in Mode Register 29 (MR29). Beat 2 for immediate retries indicates whether the immediate retry should be with read command (DNV=LOW) or active command (DNV=HIGH), and for long retry (DNV=LOW). When DNV signal for beats 0, 1, and 2 are driven high, it indicates a currently reserved mode. Beat 3 is not used. Table 48 displays DNV retry options.

For devices that implement Data Not Valid, DNV shall be driven to zero during the first data beat during MRR operations.

**Table 48 — LPDDR2: Data Not Valid**

DNV, beat 0	DNV, beat 1	DNV, beat 2	DNV, beat 3	Read Burst	Notes
0	X	X	X	Valid	3
1	0	0	X	Immediate Retry with Read	1
1	0	1	X	Immediate Retry with Activate	1
1	1	0	X	Retry Long with Read	2
1	1	1	X	Reserved	

- NOTE 1 Immediate Retry indicates the controller may retry the request immediately with read or active command as specified.
- NOTE 2 Retry Long indicates that the controller should wait for the pre-specified time before retrying the Read. An Active must be issued before the retry Read command. Optionally, a Preactive command may be issued before the Active command. A retry earlier than the pre-specified time may result in receiving another DNV signal.
- NOTE 3 In case of Mode Register Read (MRR) command, DNV shall be driven to zero during the first data beat.

## 5.4.2 LPDDR2: Data Not Valid (cont'd)

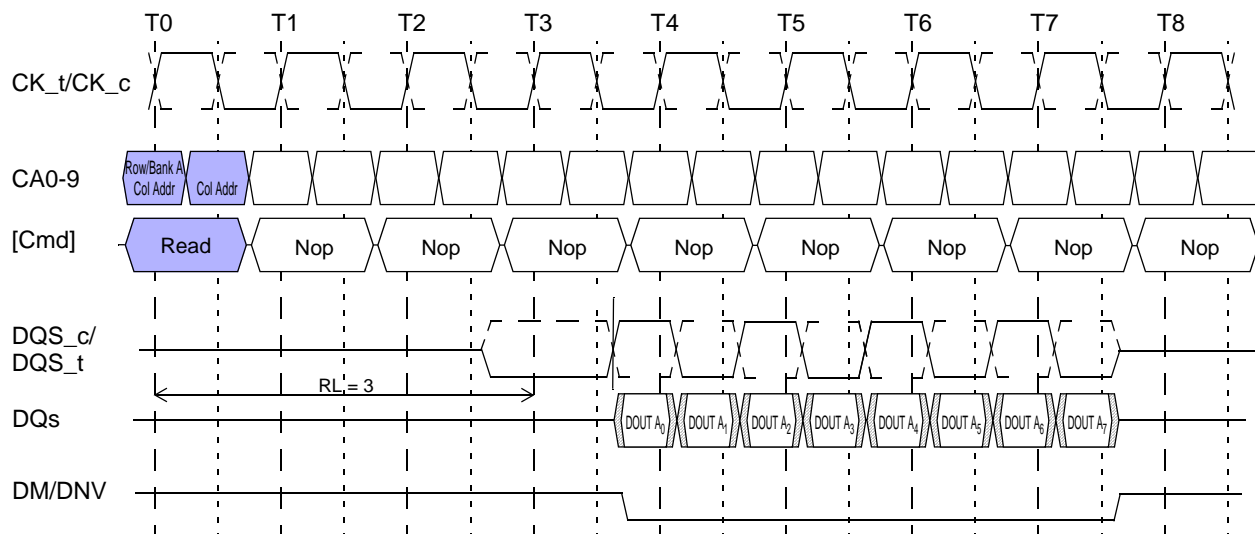


Figure 39 — LPDDR2: DNV with valid data: RL = 3, BL = 8

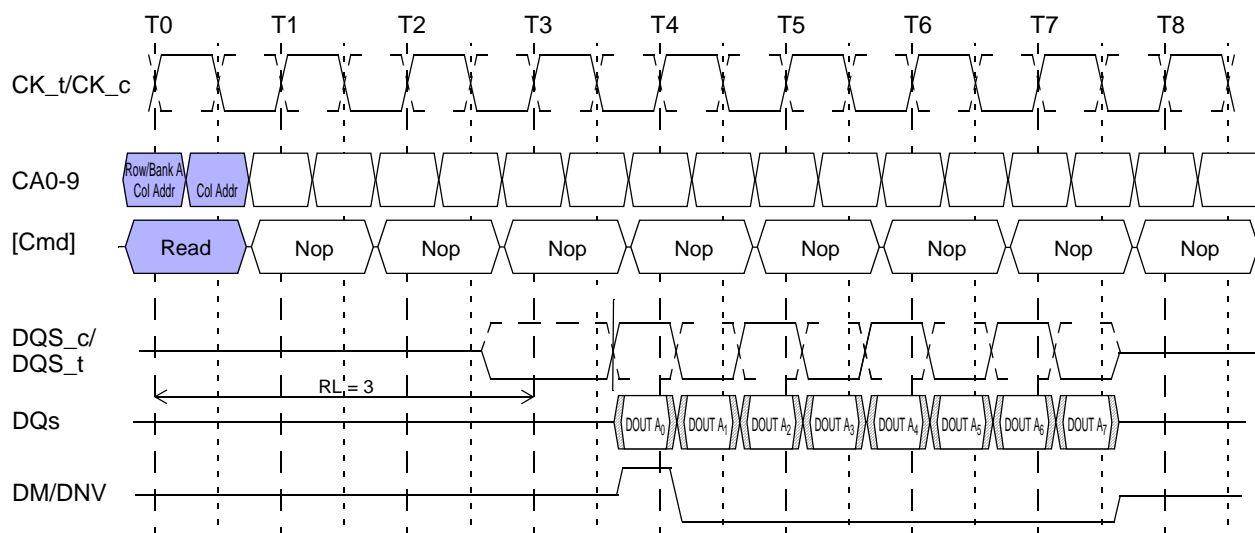


Figure 40 — LPDDR2: DNV with invalid data, retry with Read: RL = 3, BL = 8

## 5.5 Burst Write Operation

The Burst Write command is initiated by having CS\_n LOW, CA0 HIGH, CA1 LOW and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Write Latency (WL) is defined from the rising edge of the clock on which the Write Command is issued to the rising edge of the clock from which the  $t_{DQSS}$  delay is measured. The first valid datum shall be driven  $WL * t_{CK} + t_{DQSS}$  from the rising edge of the clock from which the Write command is issued. The data strobe signal (DQS) should be driven LOW  $t_{WPST}$  prior to the data input. The data bits of the burst cycle must be applied to the DQ pins  $t_{DS}$  prior to the respective edge of the DQS\_t, DQS\_c and held valid until  $t_{DH}$  after that edge. The burst data are sampled on successive edges of the DQS\_t, DQS\_c until the burst length is completed, which is 4, 8, or 16 bit burst.

For LPDDR2-SDRAM devices,  $t_{WR}$  must be satisfied before a precharge command to the same bank may be issued after a burst write operation.

For LPDDR2-N devices,  $t_{WRA}$  must be satisfied before an Activate command to the same RDB may be issued after a burst write operation. A Preactive command may be sent at any time after a Write command.

Input timings are measured relative to the crosspoint of DQS\_t and its complement, DQS\_c.

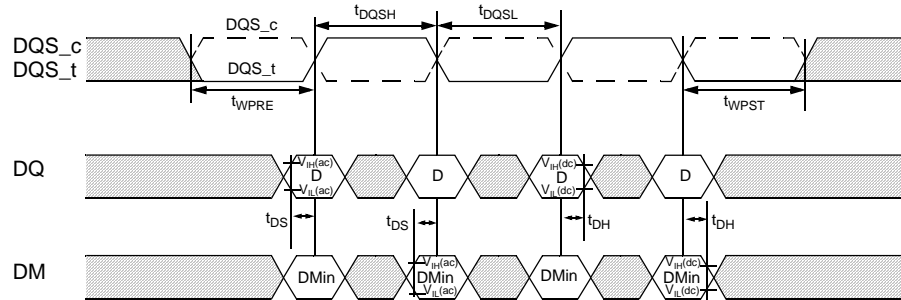


Figure 41 — Data input (write) timing

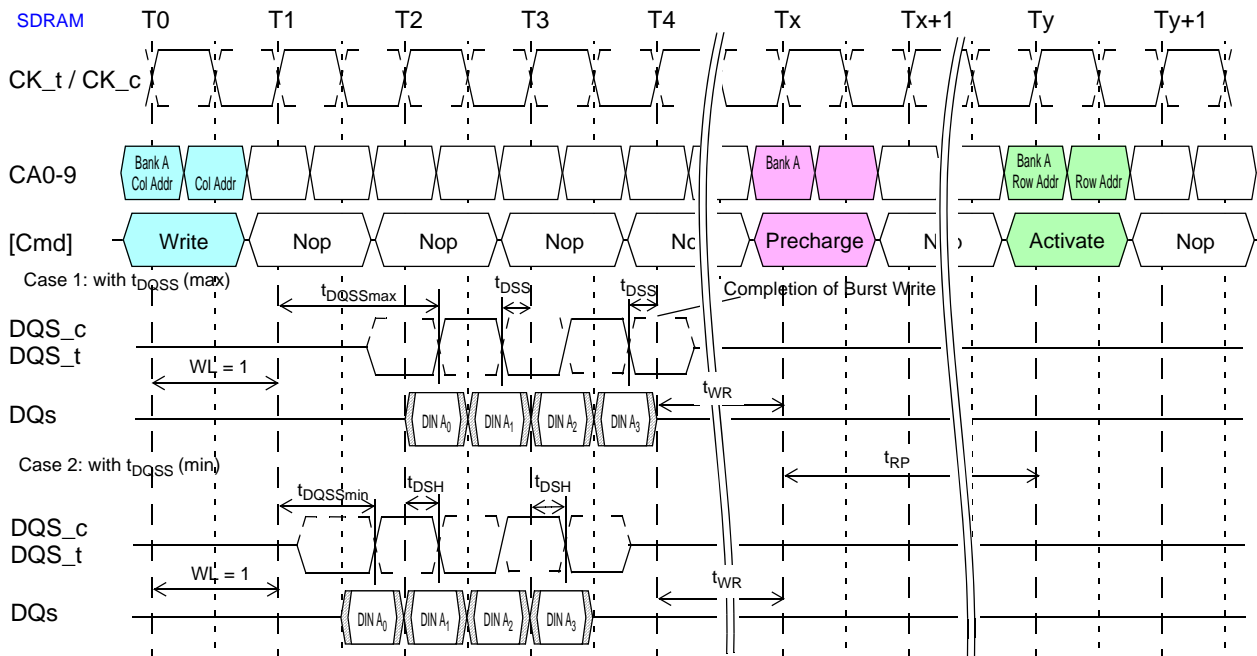
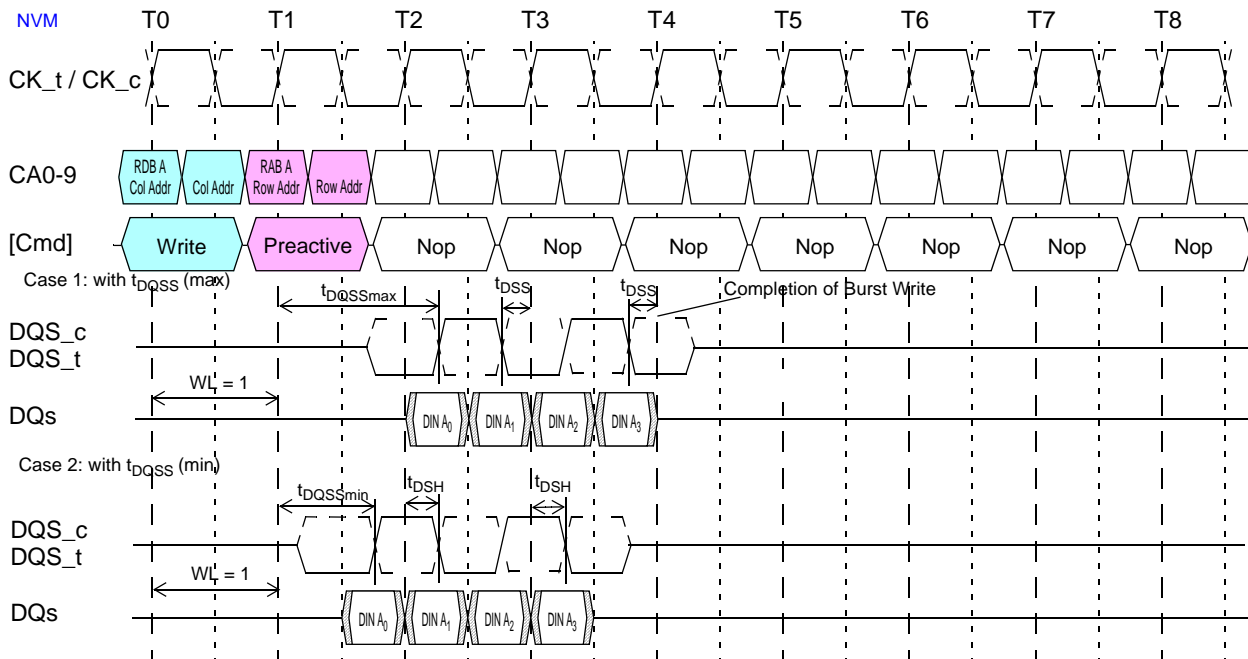
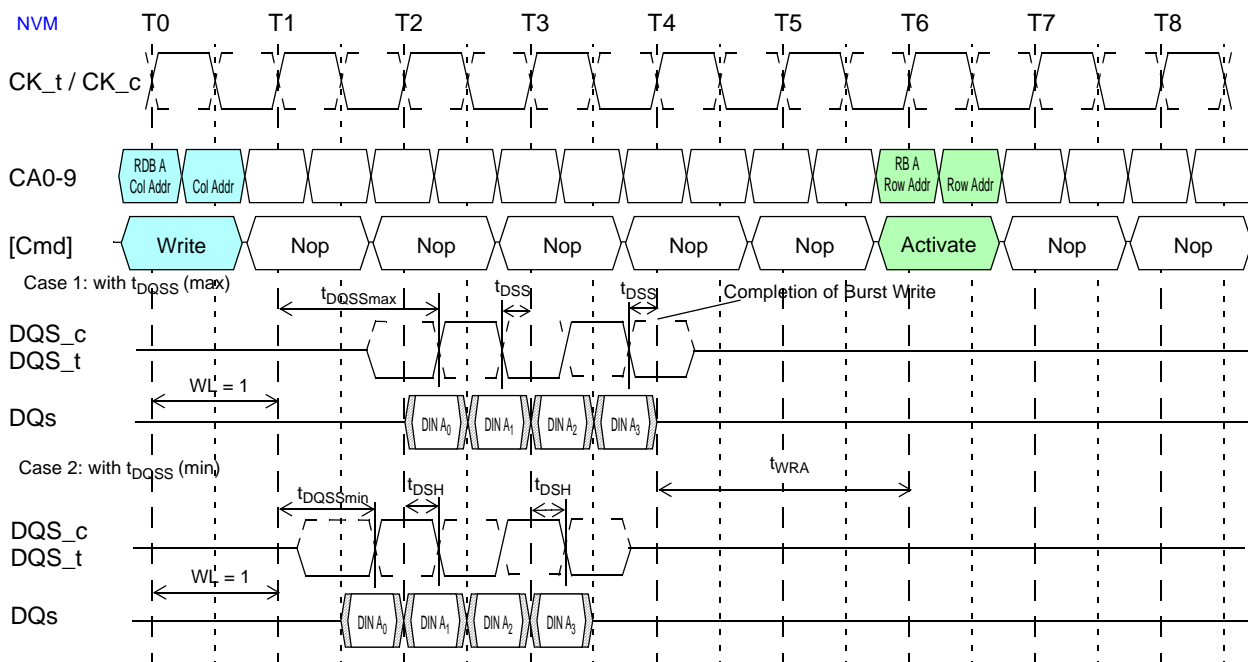


Figure 42 — LPDDR2-SX: Burst write : WL = 1, BL = 4

## 5.5 Burst Write Operation (cont'd)



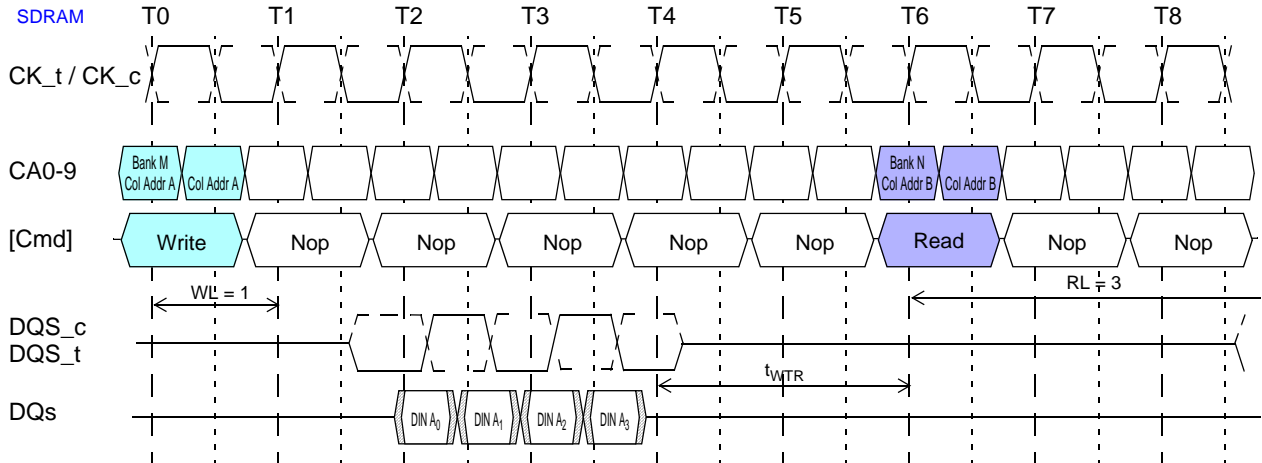
NOTE 1 A Preactive command may be issued on any clock cycle after a Write command and does not affect the ongoing burst.



NOTE 1 The minimum number of clock cycles from the burst write command to the Activate command is  $[WL + 1 + BL/2 + RU(t_{WRA}/t_{CK})]$ .

NOTE 2 If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst shall be used as “BL” to calculate the minimum write to Activate delay.

## 5.5 Burst Write Operation (cont'd)

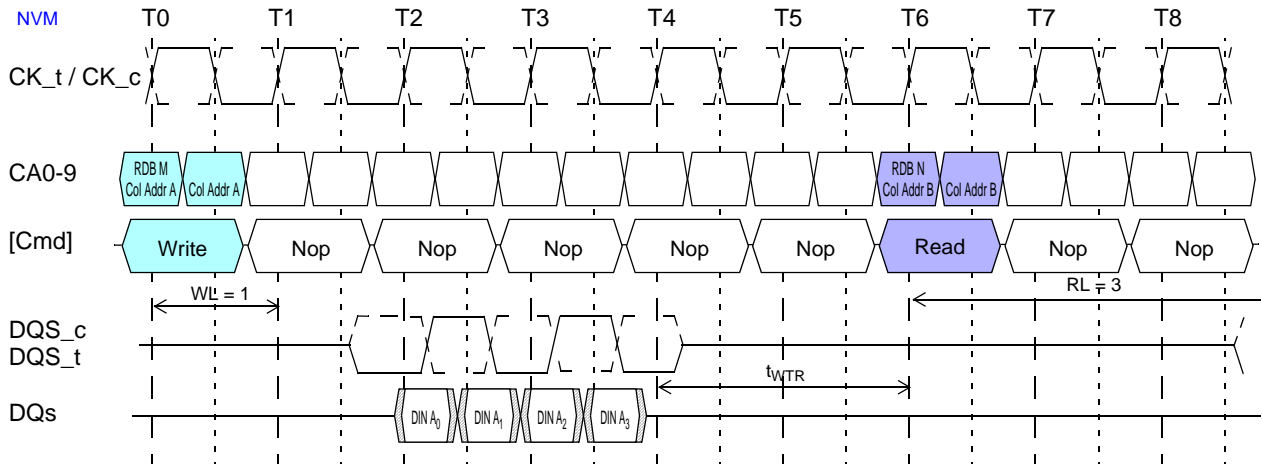


**Figure 45 — LPDDR2-SX: Burst write followed by burst read:  $RL=3$ ,  $WL = 1$ ,  $BL = 4$**

NOTE 1 The minimum number of clock cycles from the burst write command to the burst read command for any bank is  $[WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})]$ .

NOTE 2  $t_{WTR}$  starts at the rising edge of the clock after the last valid input datum.

NOTE 3 If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as “BL” to calculate the minimum write to read delay.



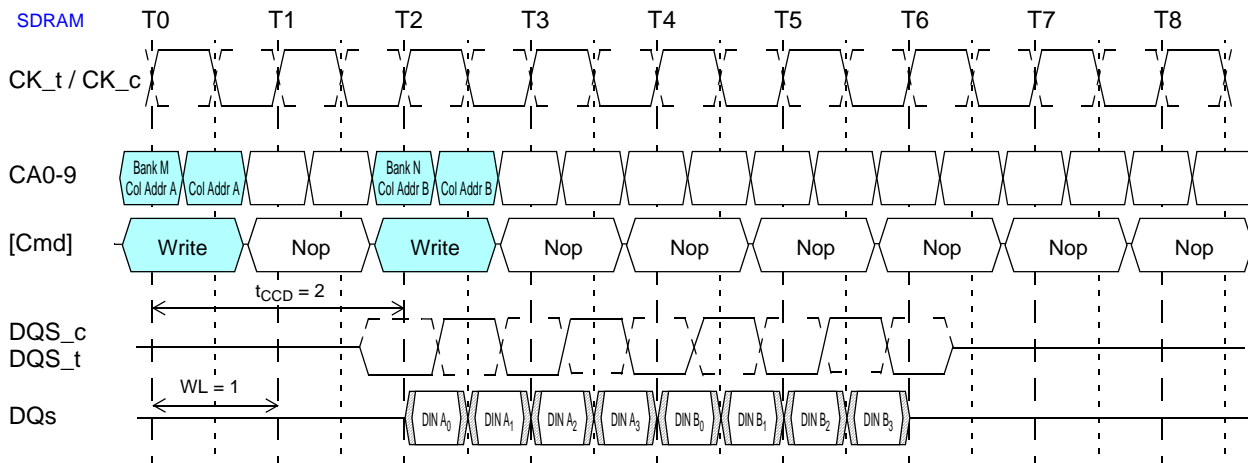
**Figure 46 — LPDDR2-N: Burst write followed by burst read:  $RL=3$ ,  $WL = 1$ ,  $BL = 4$**

NOTE 1 The minimum number of clock cycles from the burst write command to the burst read command for any RDB is  $[WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})]$ .

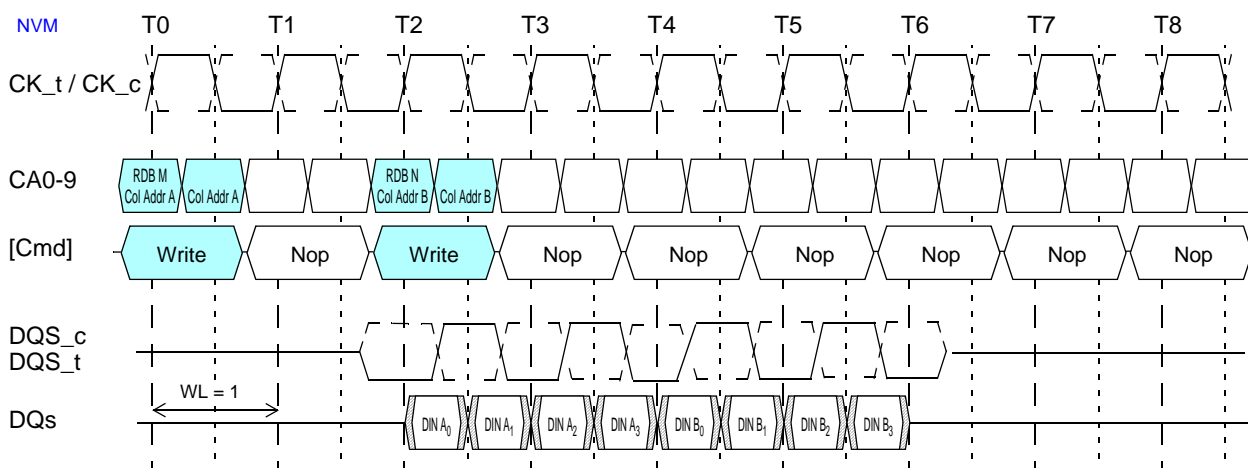
NOTE 2  $t_{WTR}$  starts at the rising edge of the clock after the last valid input datum.

NOTE 3 If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as “BL” to calculate the minimum write to read delay.

## 5.5 Burst Write Operation (cont'd)



NOTE 1: The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL=16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.



NOTE 1: The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL=16 operation. This operation is allowed regardless of same or different Row Buffers as long as the Row Buffers are activated.

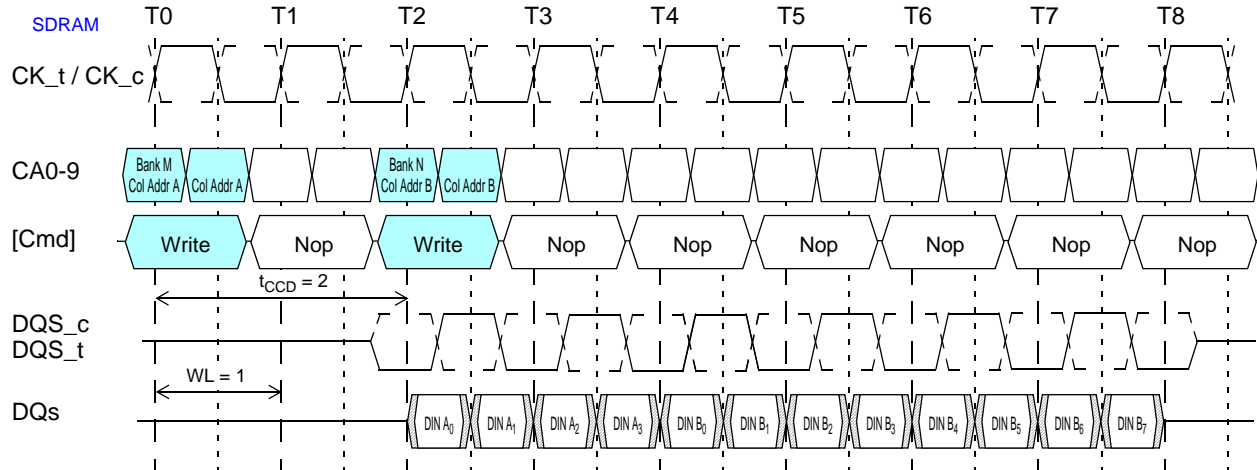
### 5.5.1 Writes interrupted by a write

For LPDDR2-S4 and LPDDR2-N devices, burst write can only be interrupted by another write on even clock cycles after the Write command, provided that  $t_{CCD}(\text{min})$  is met.

For LPDDR2-S2 devices, burst writes may be interrupted on any subsequent clock, provided that  $t_{CCD}(\text{min})$  is met.



### 5.5.1 Writes interrupted by a write (cont'd)



**Figure 49 — LPDDR2-SX: Write burst interrupt timing: WL = 1, BL = 8, t<sub>CCD</sub> = 2**

NOTE 1 For LPDDR2-S4 devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.

NOTE 2 For LPDDR2-S4 devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that t<sub>CCD</sub>(min) is met.

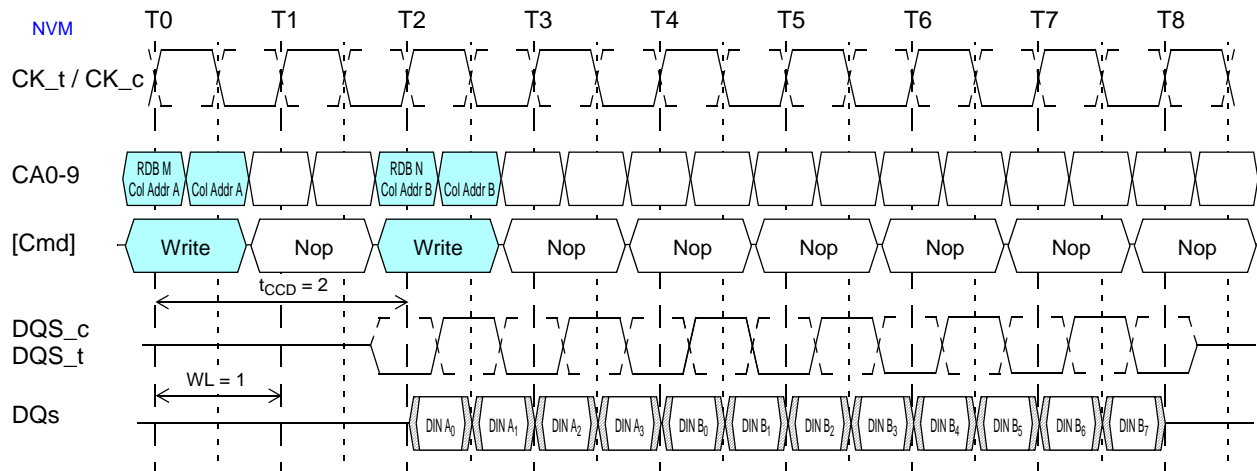
NOTE 3 For LPDDR2-S2 devices, write burst interrupt may occur on any clock after the initial write command, provided that t<sub>CCD</sub>(min) is met.

NOTE 4 Writes can only be interrupted by other writes or the BST command.

NOTE 5 Write burst interruption is allowed to any bank inside DRAM.

NOTE 6 Write burst with Auto-Precharge is not allowed to be interrupted.

NOTE 7 The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.



**Figure 50 — LPDDR2-N: Write burst interrupt timing: WL = 1, BL = 8, t<sub>CCD</sub> = 2**

NOTE 1 For LPDDR2-N devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.

NOTE 2 For LPDDR2-N devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that t<sub>CCD</sub>(min) is met.

NOTE 3 Writes can only be interrupted by other writes or the BST command.

NOTE 4 Write burst interruption is allowed to any RDB inside the NVM.

NOTE 5 The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.

## 5.6 Burst Terminate

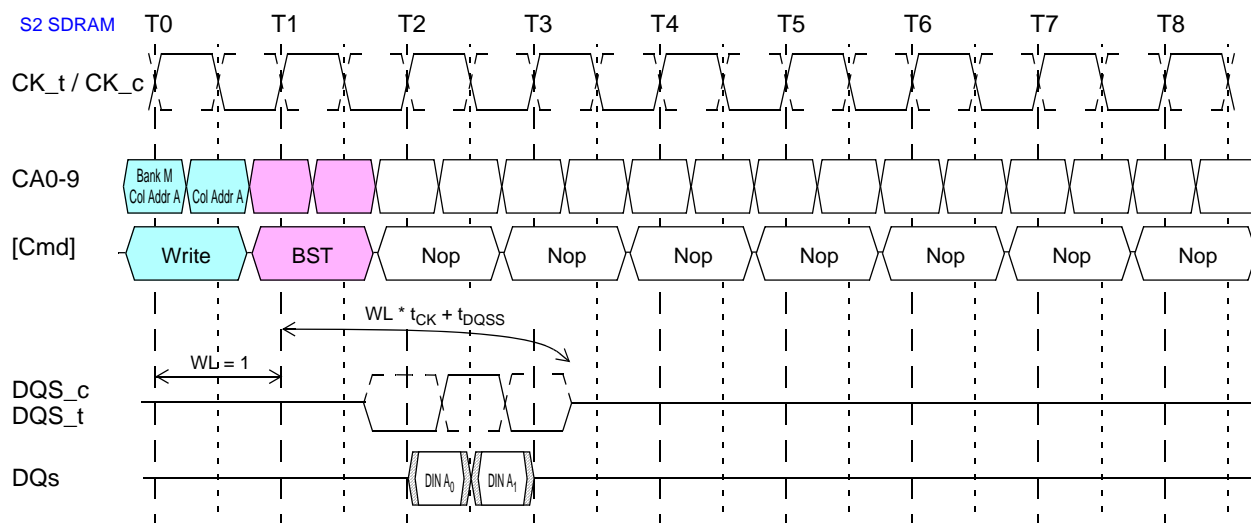
The Burst Terminate (BST) command is initiated by having CS<sub>n</sub> LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of clock. A Burst Terminate command may only be issued to terminate an active Read or Write burst. Therefore, a Burst Terminate command may only be issued up to and including BL/2 - 1 clock cycles after a Read or Write command. The effective burst length of a Read or Write command truncated by a BST command is as follows:

$$\text{Effective burst length} = 2 \times \{\text{Number of clock cycles from the Read or Write Command to the BST command}\}$$

Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL” to calculate the minimum read to write or write to read delay.

The BST command only affects the most recent read or write command. The BST command truncates an ongoing read burst  $RL \times t_{CK} + t_{DQSQ}$  after the rising edge of the clock where the Burst Terminate command is issued. The BST command truncates an ongoing write burst  $WL \times t_{CK} + t_{DQSS}$  after the rising edge of the clock where the Burst Terminate command is issued.

For LPDDR2-S2 devices, the 2-bit prefetch architecture allows the BST command to be issued in any cycle after a Write or Read command.

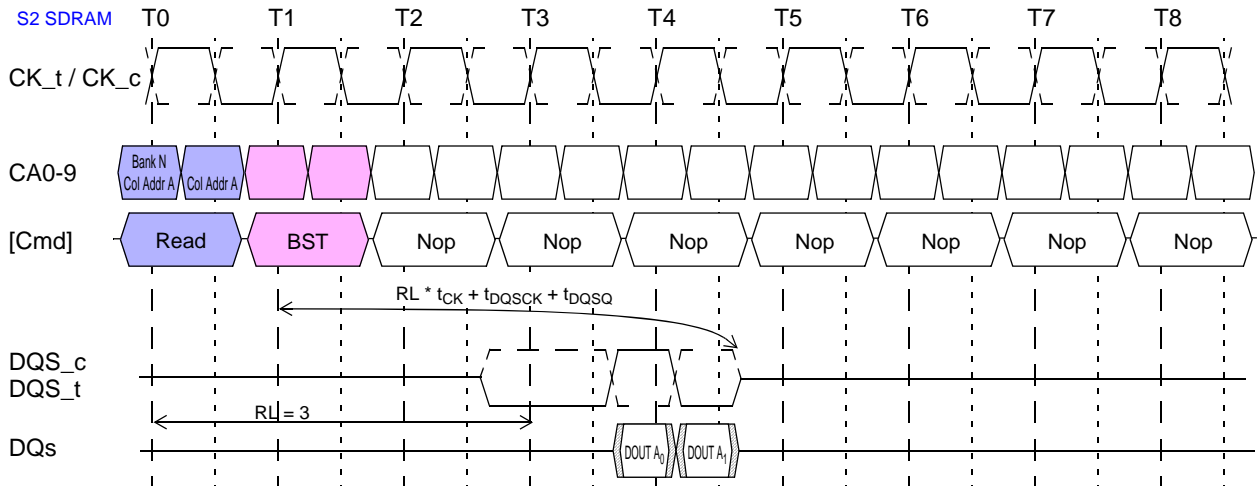


**Figure 51 — LPDDR2-S2: Write burst truncated by BST: WL = 1, BL = 16**

NOTE 1 The BST command truncates an ongoing write burst  $WL \times t_{CK} + t_{DQSS}$  after the rising edge of the clock where the Burst Terminate command is issued.

NOTE 2 Additional BST commands are not allowed after T1 and may not be issued until after the next Read or Write command.

## 5.6 Burst Terminate (cont'd)

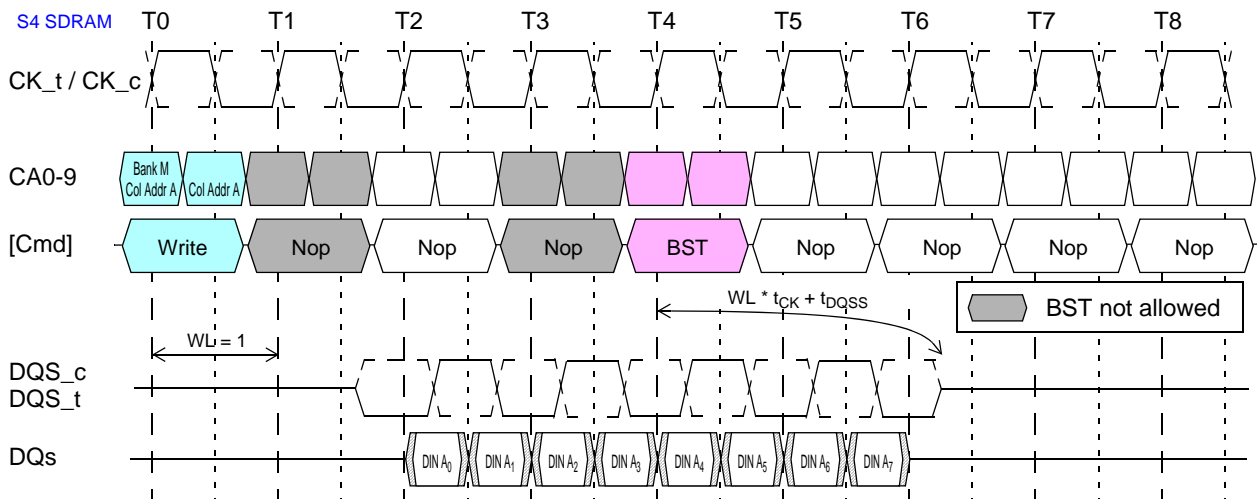


**Figure 52 — LPDDR2-S2: Read burst truncated by BST: RL = 3, BL = 4**

NOTE 1 The BST command truncates an ongoing read burst  $RL * t_{CK} + t_{DQSCK} + t_{DQSQ}$  after the rising edge of the clock where the Burst Terminate command is issued.

NOTE 2 Additional BST commands are not allowed after T1 and may not be issued until after the next Read or Write command.

For LPDDR2-S4 and LPDDR2-N devices, the 4-bit prefetch architecture allows the BST command to be issued on an even number of clock cycles after a Write or Read command. Therefore, the effective burst length of a Read or Write command truncated by a BST command is an integer multiple of 4.



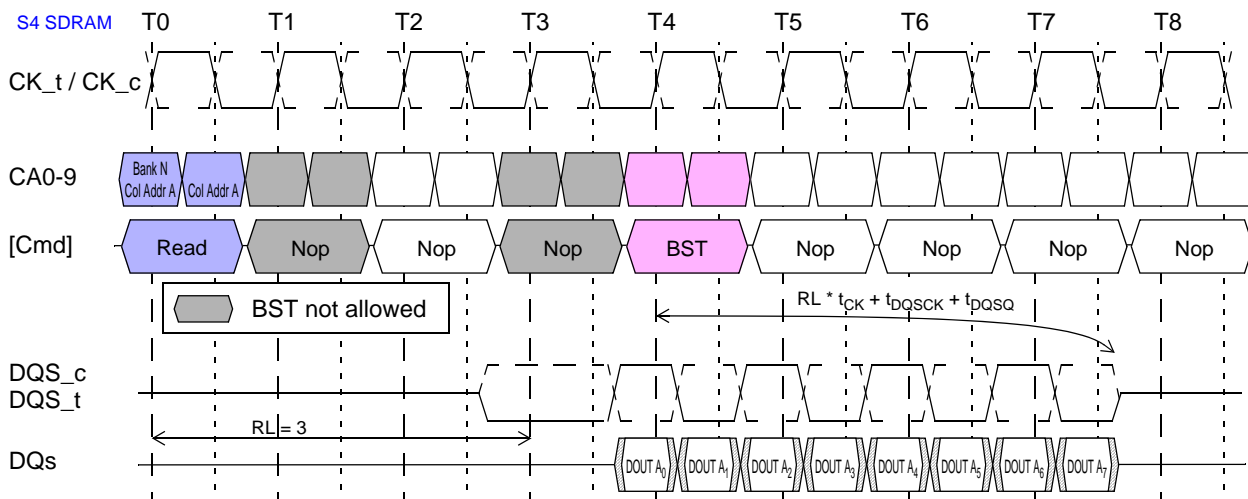
**Figure 53 — LPDDR2-S4: Burst Write truncated by BST: WL = 1, BL = 16**

NOTE 1 The BST command truncates an ongoing write burst  $WL * t_{CK} + t_{DQSS}$  after the rising edge of the clock where the Burst Terminate command is issued.

NOTE 2 For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Write command.

NOTE 3 Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

## 5.6 Burst Terminate (cont'd)

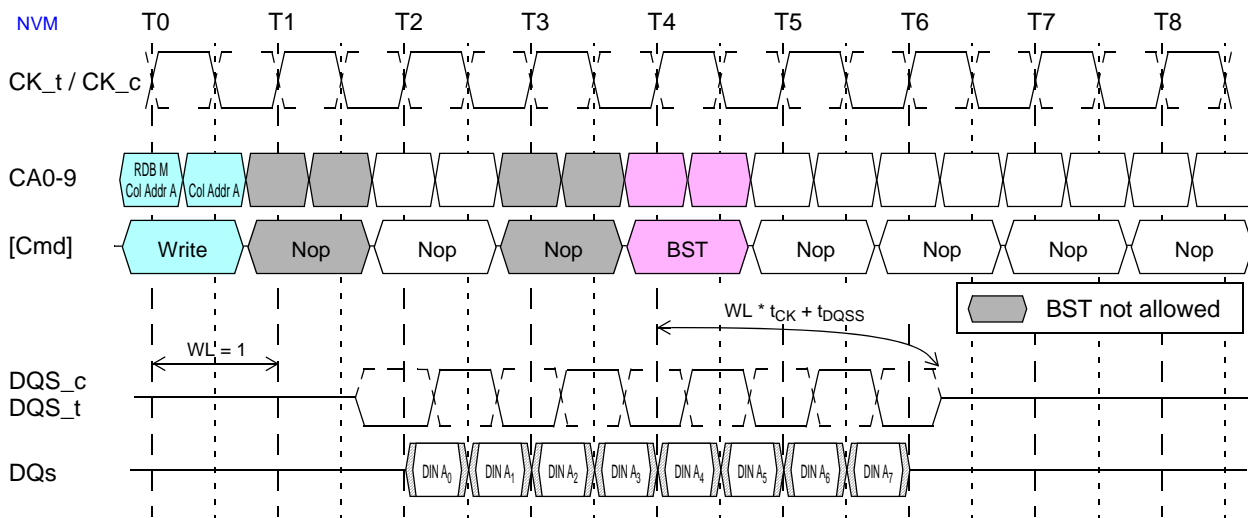


**Figure 54 — LPDDR2-S4: Burst Read truncated by BST: RL=3, BL = 16**

NOTE 1 The BST command truncates an ongoing read burst  $RL * t_{CK} + t_{DQsck} + t_{DQsq}$  after the rising edge of the clock where the Burst Terminate command is issued.

NOTE 2 For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Read command.

NOTE 3 Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.



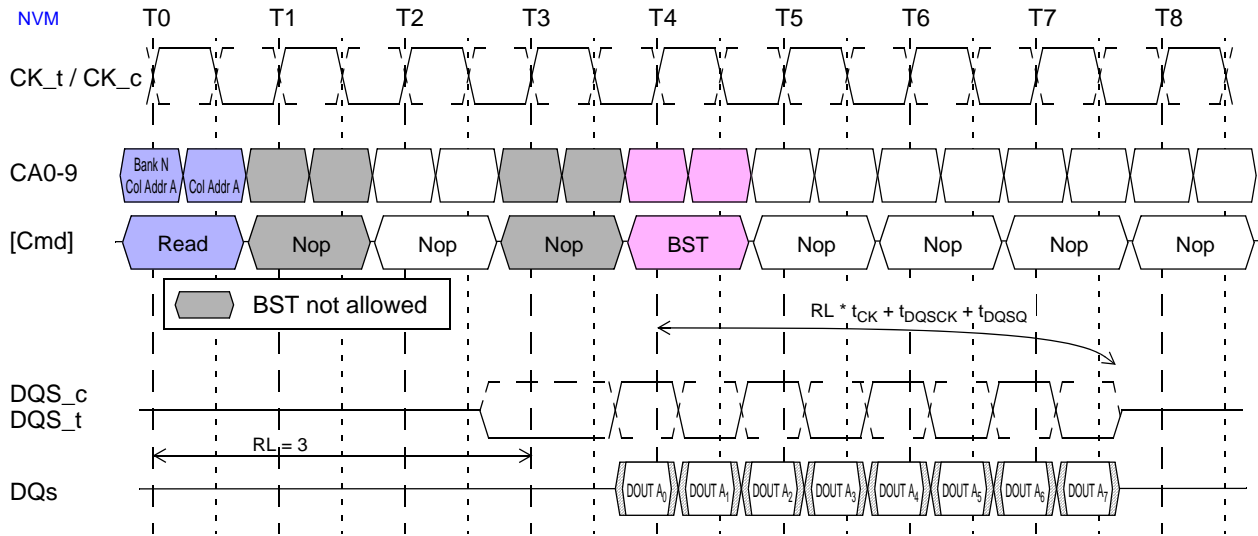
**Figure 55 — LPDDR2-N: Burst Write truncated by BST: WL = 1, BL = 16**

NOTE 1 The BST command truncates an ongoing write burst  $WL * t_{CK} + t_{DQss}$  after the rising edge of the clock where the Burst Terminate command is issued.

NOTE 2 For LPDDR2-N devices, BST can only be issued an even number of clock cycles after the Write command.

NOTE 3 Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

## 5.6 Burst Terminate (cont'd)



**Figure 56 — LPDDR2-N: Burst Read truncated by BST: RL=3, BL = 16**

NOTE 1 The BST command truncates an ongoing read burst  $RL * t_{CK} + t_{DQSCK} + t_{DQSQ}$  after the rising edge of the clock where the Burst Terminate command is issued.

NOTE 2 For LPDDR2-N devices, BST can only be issued an even number of clock cycles after the Read command.

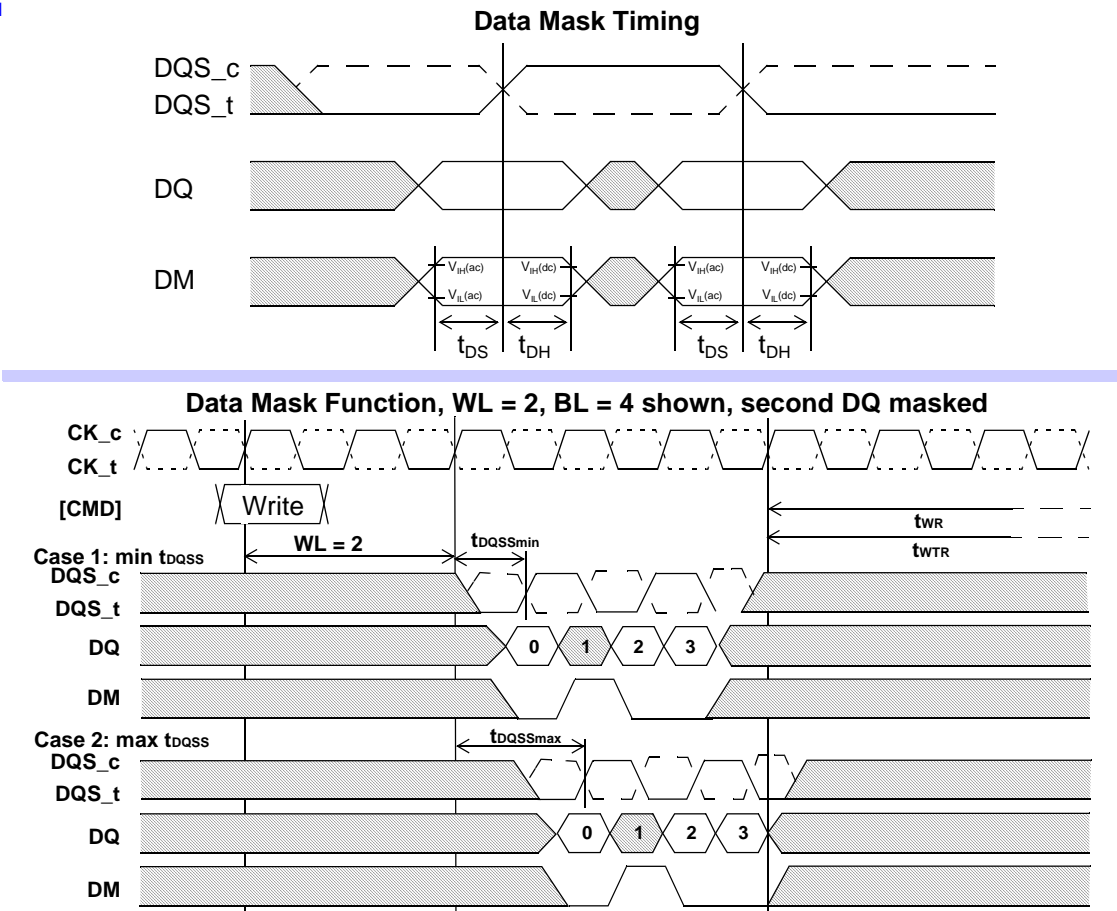
NOTE 3 Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

5.7 Write Data Mask

One write data mask (DM) pin for each data byte (DQ) will be supported on LPDDR2 devices, consistent with the implementation on LPDDR SDRAMs. Each data mask (DM) may mask its respective data byte (DQ) for any given cycle of the burst. Data mask has identical timings on write operations as the data bits, though used as input only, is internally loaded identically to data bits to insure matched system timing.

See [Table 51](#) for Write to Precharge timings for LPDDR2-S4 and [Table 52](#) for Write to Precharge timings for LPDDR2-S2.

SDRAM





## 5.8 LPDDR2-N: Preactive operation

The Preactive command is initiated by having CS<sub>n</sub> LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of clock. After issuing a Preactive command, the target Row Buffer will return to the Idle state once the minimum Preactive latency ( $t_{RP}$ ) is satisfied and any ongoing Read or Write operation is complete. The Preactive command addresses one Row Address Buffer (RAB). Each RAB is coupled with one specific Row Data Buffer (RDB) selected by BA0 - BA2. An {RAB, RDB} pair is referred to as a Row Buffer (RB).

The Preactive command is used to load the upper part of a row address into one RAB selected by BA0 - BA2. The address subset stored in an RAB will later be combined with the lower portion of the row address sent with the Activate command to load one row of the memory array or Overlay Window content into an RDB. Note that the row size of the NVM device may differ from the row size for an SDRAM.

Devices may have four or eight RABs. Each RAB is not restricted to any portion of the device address space, therefore the controller may use any RAB for any partial row address, including storing the same partial row address value in multiple RABs concurrently. Each RAB is persistent until a MRW Reset command is issued or power loss occurs, or until a new Preactive command is issued to that RAB. Therefore, Preactive is optional when the desired RAB already holds the desired partial row-address value.

The Preactive command does not invoke internal sensing. Therefore, after issuing a Preactive command to any RAB and then satisfying  $t_{RP}$ , the memory controller shall issue an Activate command to the corresponding RB before issuing a Read or Write command to the respective RDB.

All RABs shall be reset to 0x0000 by the memory during the initialization procedure.

**Table 49 — Row Address Buffer selection for Preactive by BA inputs**

BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Selected RAB (4-RB devices)	Selected RAB (8-RB devices)
0	0	0	RAB 0	RAB 0
0	0	1	RAB 1	RAB 1
0	1	0	RAB 2	RAB 2
0	1	1	RAB 3	RAB 3
1	0	0	RAB 0	RAB 4
1	0	1	RAB 1	RAB 5
1	1	0	RAB 2	RAB 6
1	1	1	RAB 3	RAB 7



### 5.8.1 LPDDR2-N: Burst Read operation followed by Activate or Preactive

For LPDDR2-N devices, a Read burst may be followed by a Preactive or Activate command to the same Row Buffer pair. An Activate command to the same Row Buffer pair may not be issued earlier than  $BL/2$  cycles after the Read command. For an untruncated burst,  $BL$  is the complete burst length selected in the Mode Registers. For a truncated burst,  $BL$  is the effective burst length. A Preactive command may be issued at any time following a Read command. Following the Preactive command, only BST may be issued to the same Row Buffer until  $t_{RP}$  is met. Following the Activate command, a subsequent command to the same Row Buffer shall not be issued until  $t_{RCD}$  is met. Read bursts are not impacted by Preactive or Activate commands to different Row Buffer pairs.

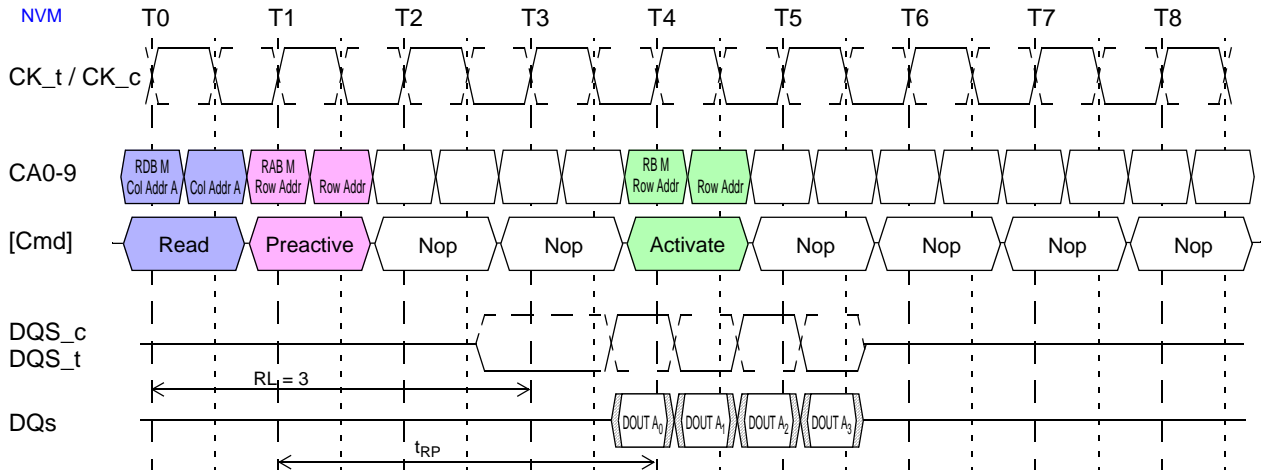


Figure 59 — LPDDR2-N: Burst read operation followed by Preactive:  $RL = 3$ ,  $BL = 4$

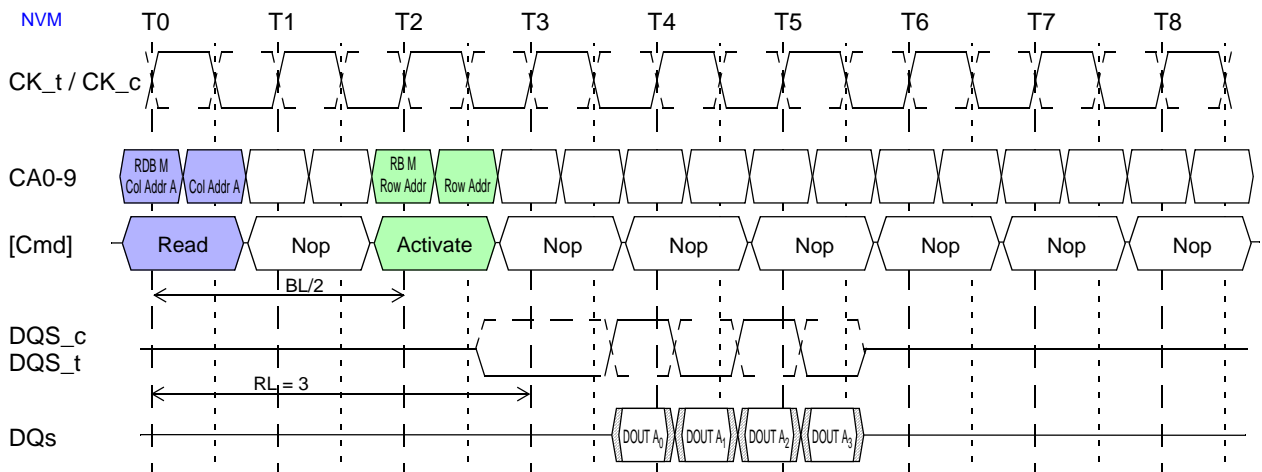


Figure 60 — LPDDR2-N: Burst read operation followed by Activate:  $RL = 3$ ,  $BL = 4$

NOTE 1 If a read burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated read burst shall be used as “BL” to calculate the minimum Read to Activate delay

### 5.8.2 LPDDR2-N: Burst Write operation followed by Activate or Preactive

A Preactive command may be issued at any time after a Write command. An Activate command to the same RDB may be issued  $t_{WRA}$  after the completion of the last burst write cycle. No Activate command to the same RDB should be issued prior to the  $t_{WRA}$  delay.

Minimum Write to Activate command spacing to the same Row Buffer equals  $WL + BL/2 + 1 + RU(t_{WRA}/t_{CK})$  clock cycles. For an untruncated burst, BL is the value from the Mode Register. For an truncated burst, BL is the effective burst length.

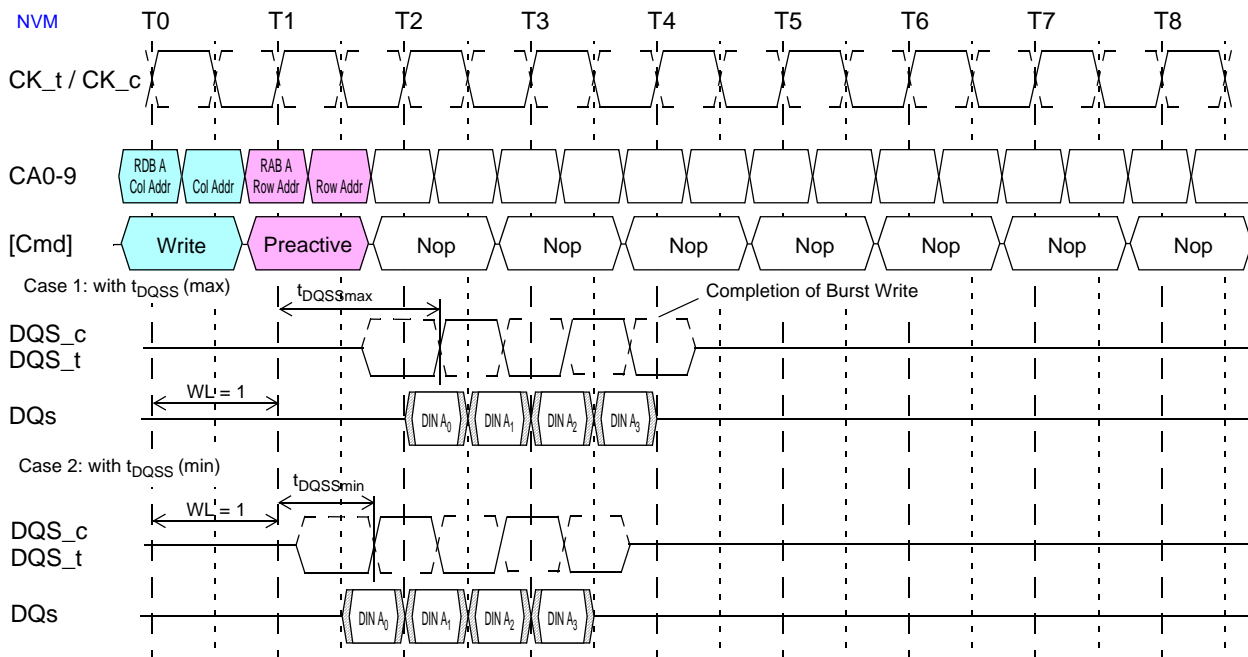
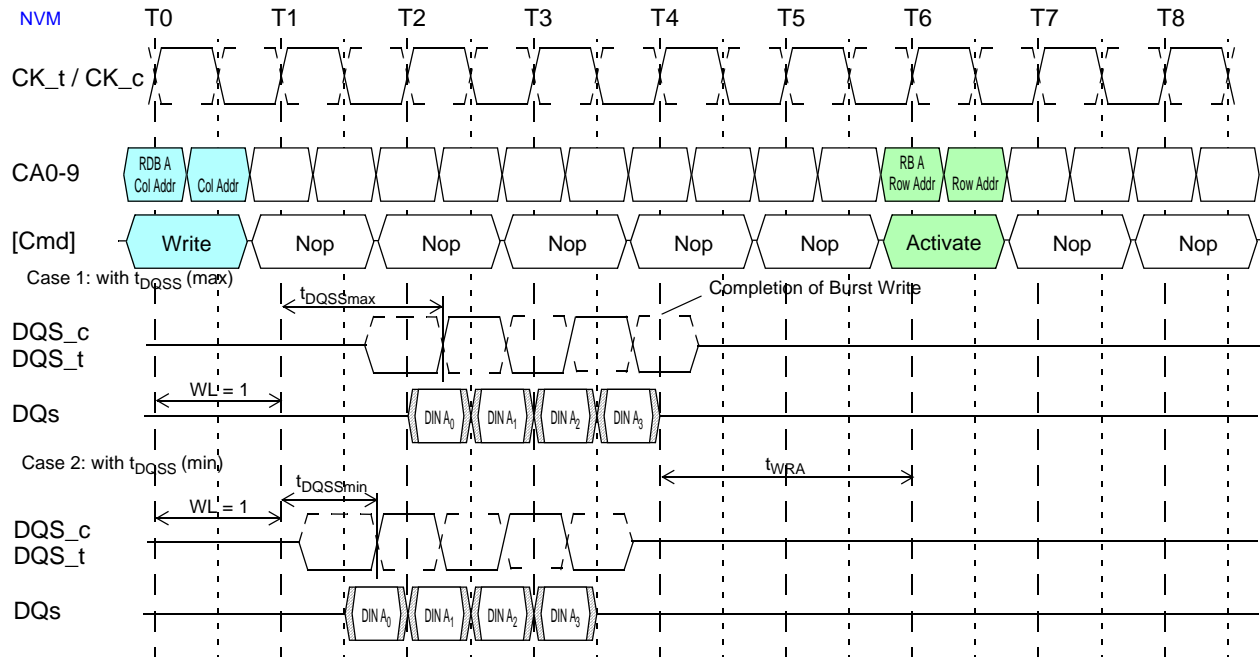


Figure 61 — LPDDR2-N: Burst write followed by Preactive:  $WL = 1$ ,  $BL = 4$



**Figure 62 — LPDDR2-N: Burst write followed by Activate: WL = 1, BL = 4**

NOTE 1 The minimum number of clock cycles from the burst write command to the Activate command is  $[WL + 1 + BL/2 + RU(t_{WRA}/t_{CK})]$ .

NOTE 2 If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst shall be used as "BL" to calculate the minimum write to Activate delay.

### 5.8.3 LPDDR2-N: Auto Precharge (AP) bit

The AP bit (CA0f) is ignored during READ and WRITE commands.

### 5.9 LPDDR2-SX: Precharge operation

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated by having CS<sub>n</sub> LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices, the AB flag, and the bank address bits, BA0 and BA1, are used to determine which bank(s) to precharge. For 8-bank devices, the AB flag, and the bank address bits, BA0, BA1, and BA2, are used to determine which bank(s) to precharge. The bank(s) will be available for a subsequent row access  $t_{RPab}$  after an All-Bank Precharge command is issued and  $t_{RPpb}$  after a Single-Bank Precharge command is issued.

In order to ensure that 8-bank devices do not exceed the instantaneous current supplying capability of 4-bank devices, the Row Precharge time ( $t_{RP}$ ) for an All-Bank Precharge for 8-bank devices ( $t_{RPab}$ ) will be longer than the Row Precharge time for a Single-Bank Precharge ( $t_{RPpb}$ ). For 4-bank devices, the Row Precharge time ( $t_{RP}$ ) for an All-Bank Precharge ( $t_{RPab}$ ) is equal to the Row Precharge time for a Single-Bank Precharge ( $t_{RPpb}$ ).

Figure 19 shows Activate to Precharge timing.

**Table 50 — Bank selection for Precharge by address bits**

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 4-bank device	Precharged Bank(s) 8-bank device
0	0	0	0	Bank 0 only	Bank 0 only
0	0	0	1	Bank 1 only	Bank 1 only
0	0	1	0	Bank 2 only	Bank 2 only
0	0	1	1	Bank 3 only	Bank 3 only
0	1	0	0	Bank 0 only	Bank 4 only
0	1	0	1	Bank 1 only	Bank 5 only
0	1	1	0	Bank 2 only	Bank 6 only
0	1	1	1	Bank 3 only	Bank 7 only
1	DON'T CARE	DON'T CARE	DON'T CARE	All Banks	All Banks

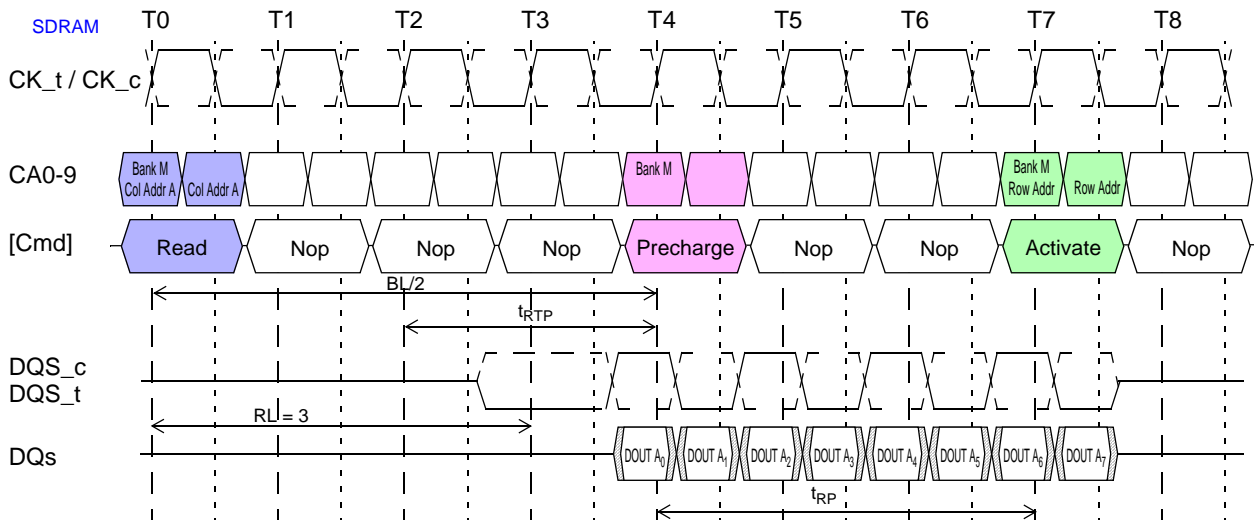
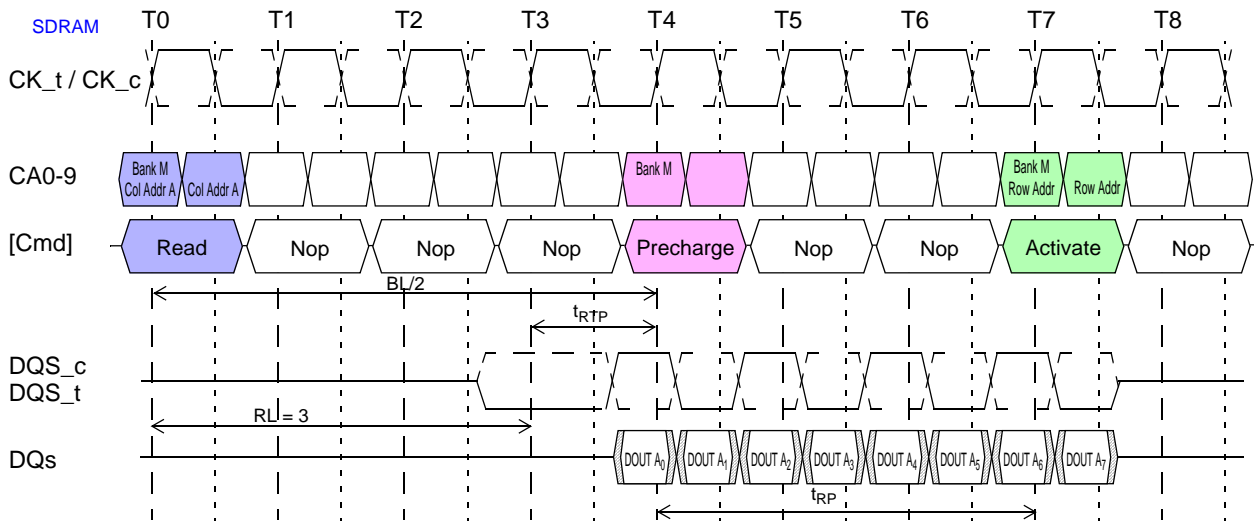
### 5.9.1 LPDDR2-SX: Burst Read operation followed by Precharge

For the earliest possible precharge, the precharge command may be issued BL/2 clock cycles after a Read command. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length. A new bank active (command) may be issued to the same bank after the Row Precharge time ( $t_{RP}$ ). A precharge command cannot be issued until after  $t_{RAS}$  is satisfied.

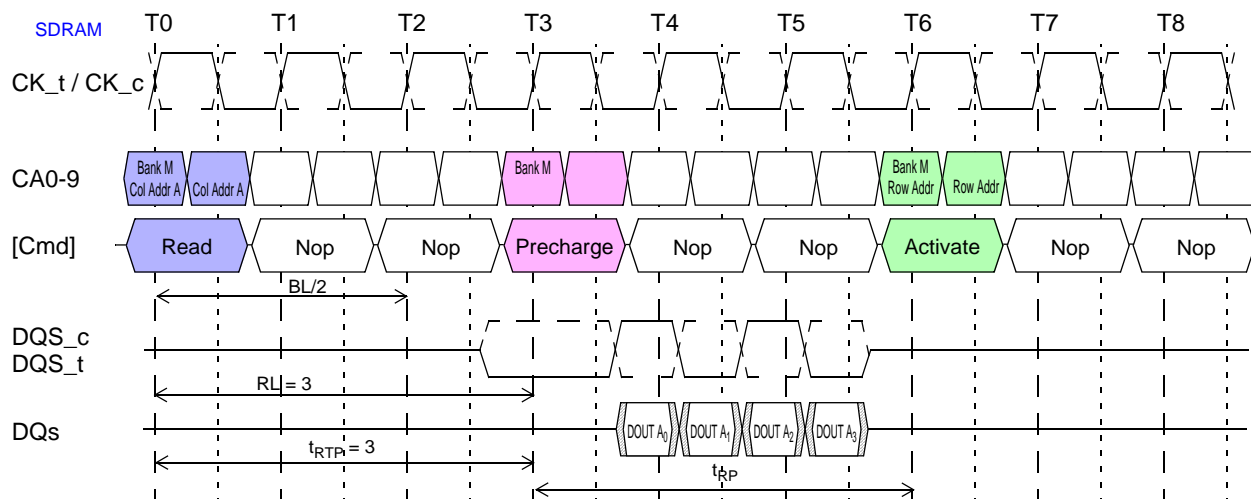
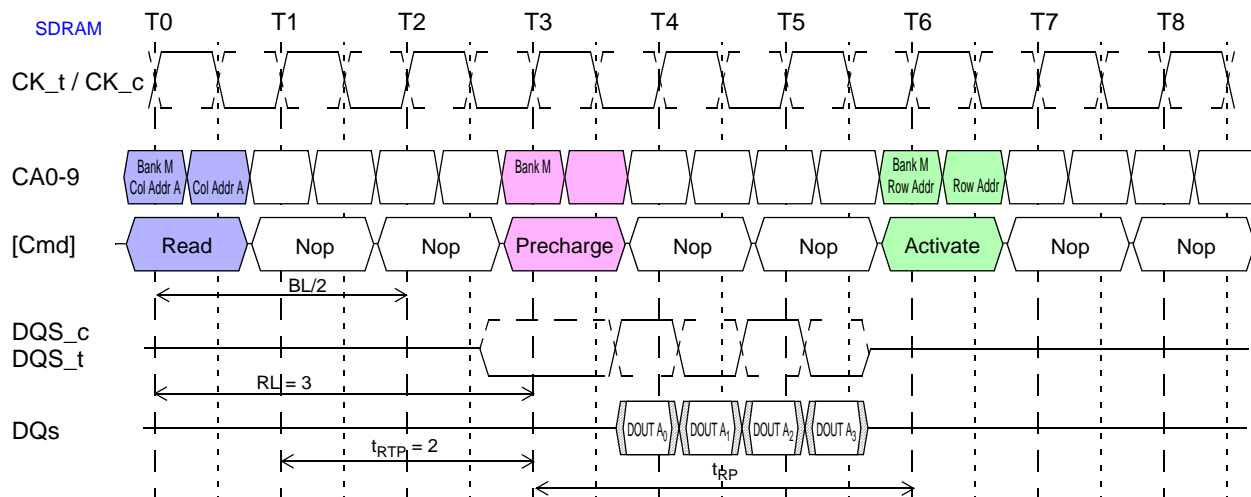
For LPDDR2-S4 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read command. For LPDDR2-S2 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 2-bit prefetch of a Read command. This time is called  $t_{RTP}$  (Read to Precharge).

For LPDDR2-S2 devices,  $t_{RTP}$  begins BL/2 - 1 clock cycles after the Read command. For LPDDR2-S4 devices,  $t_{RTP}$  begins BL/2 - 2 clock cycles after the Read command. If the burst is truncated by a BST command or a Read command to a different bank, the effective “BL” shall be used to calculate when  $t_{RTP}$  begins.

See Table 51 for Read to Precharge timings for LPDDR2-S4 and Table 52 for Read to Precharge timings for LPDDR2-S2.



### 5.9.1 LPDDR2-SX: Burst Read operation followed by Precharge 9cont'd)



### 5.9.2 LPDDR2-SX: Burst Write followed by Precharge

For write cycles, a delay must be satisfied from the time of the last valid burst input data until the Precharge command may be issued. This delay is known as the write recovery time ( $t_{WR}$ ) referenced from the completion of the burst write to the precharge command. No Precharge command to the same bank should be issued prior to the  $t_{WR}$  delay.

LPDDR2-S2 devices write data to the array in prefetch pairs (prefetch = 2) and LPDDR2-S4 devices write data to the array in prefetch quadruples (prefetch = 4). The beginning of an internal write operation may only begin after a prefetch group has been latched completely. Therefore, the write recovery time ( $t_{WR}$ ) starts at different boundaries for LPDDR2-S2 and LPDDR2-S4 devices.

For LPDDR2-S2 devices, minimum Write to Precharge command spacing to the same bank is  $WL + RU(BL/2) + 1 + RU(t_{WR}/t_{CK})$  clock cycles. For LPDDR2-S4 devices, minimum Write to Precharge command spacing to the same bank is  $WL + BL/2 + 1 + RU(t_{WR}/t_{CK})$  clock cycles. For an untruncated burst, BL is the value from the Mode Register. For an truncated burst, BL is the effective burst length.

See Table 51 for Write to Precharge timings for LPDDR2-S4 and Table 52 for Write to Precharge timings for LPDDR2-S2.

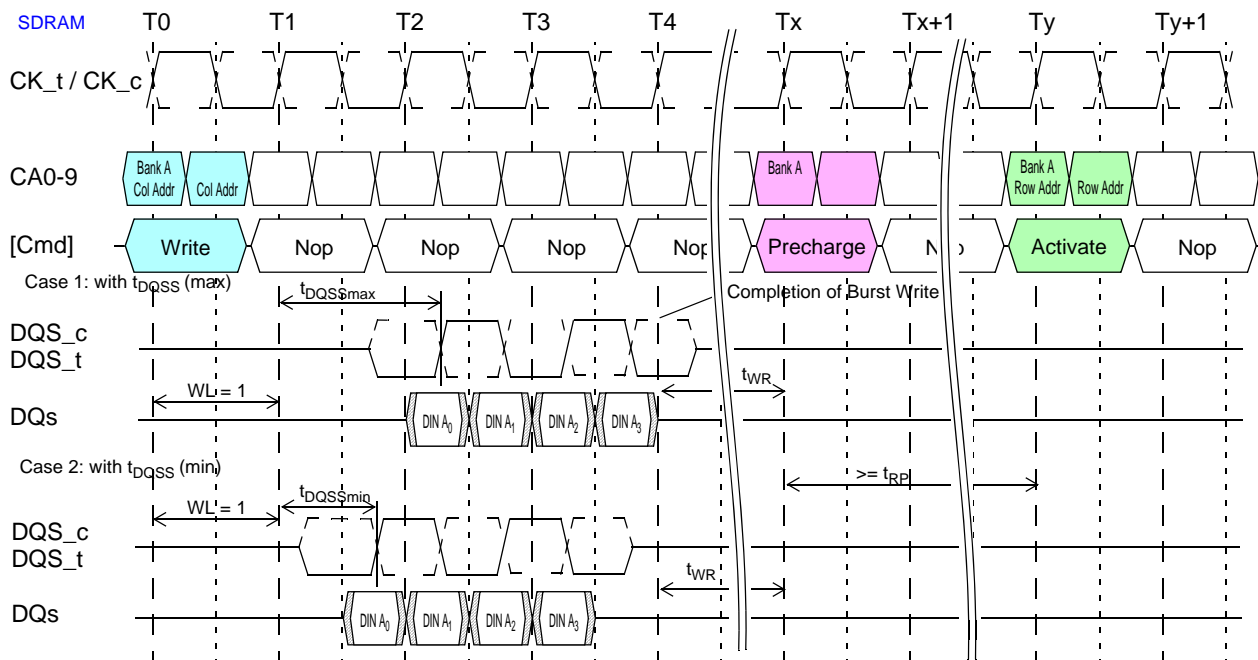


Figure 67 — LPDDR2-SX: Burst write followed by precharge: WL = 1, BL = 4

### 5.9.3 LPDDR2-SX: Auto Precharge operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the LPDDR2 SDRAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle.

If AP is LOW when the Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency) thus improving system performance for random data access.

### 5.9.3.1 LPDDR2-SX: Burst Read with Auto-Precharge

If AP (CA0f) is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged.

LPDDR2-S2 devices start an Auto-Precharge operation on the rising edge of the clock  $BL/2 - 1 + RU(t_{RTP}/t_{CK})$  clock cycles later than the Read with AP command. Refer to Table 52 for equations related to Auto-Precharge for LPDDR2-S2.

LPDDR2-S4 devices start an Auto-Precharge operation on the rising edge of the clock  $BL/2$  or  $BL/2 - 2 + RU(t_{RTP}/t_{CK})$  clock cycles later than the Read with AP command, whichever is greater. Refer to Table 51 for equations related to Auto-Precharge for LPDDR2-S4.

A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied simultaneously.

The RAS precharge time ( $t_{RP}$ ) has been satisfied from the clock at which the auto precharge begins.

The RAS cycle time ( $t_{RC}$ ) from the previous bank activation has been satisfied.

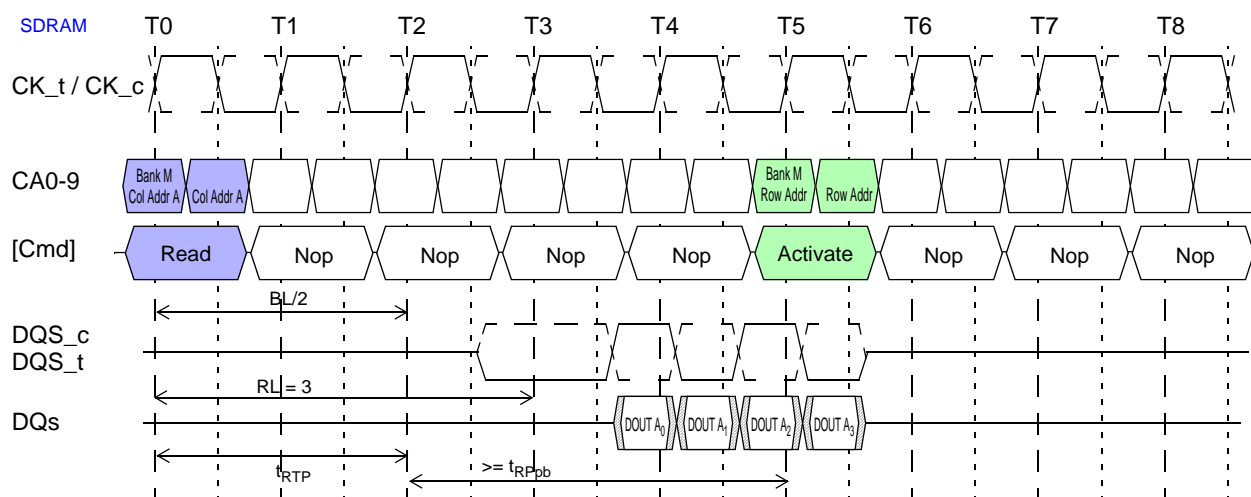


Figure 68 — LPDDR2-S4: Burst read with Auto-Precharge:

RL = 3, BL = 4,  $RU(t_{RTP(min)}/t_{CK}) = 2$

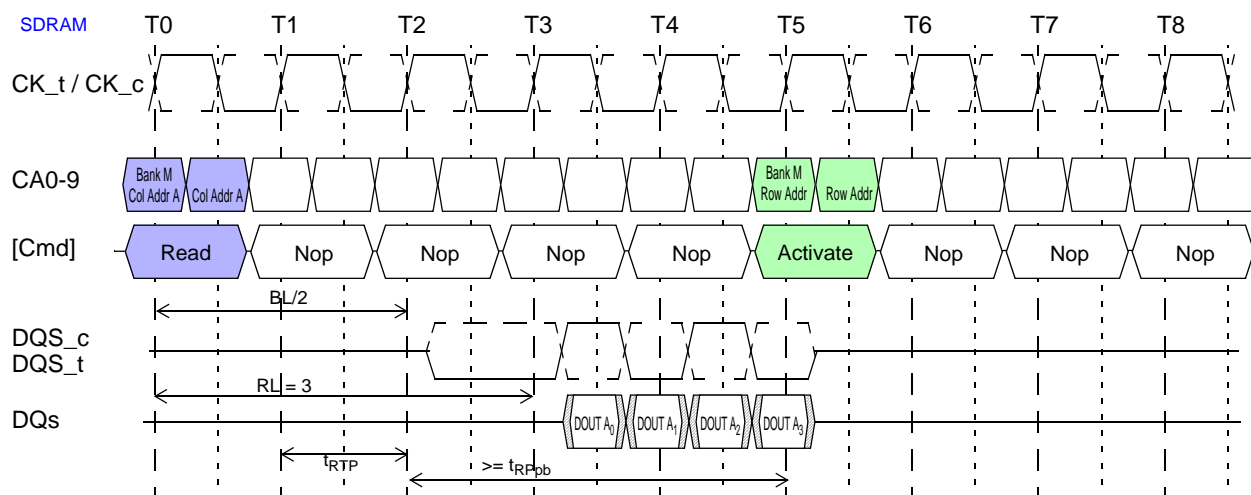


Figure 69 — LPDDR2-S2: Burst read with Auto-Precharge:

RL = 3, BL = 4,  $RU(t_{RTP(min)}/t_{CK}) = 1$



### 5.9.3.2 LPDDR2-SX: Burst write with Auto-Precharge

If AP (CA0f) is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The LPDDR2 SDRAM starts an Auto Precharge operation on the rising edge which is  $t_{WR}$  cycles after the completion of the burst write.

A new bank activate (command) may be issued to the same bank if both of the following two conditions are satisfied.

The RAS precharge time ( $t_{RP}$ ) has been satisfied from the clock at which the auto precharge begins.

The RAS cycle time ( $t_{RC}$ ) from the previous bank activation has been satisfied.

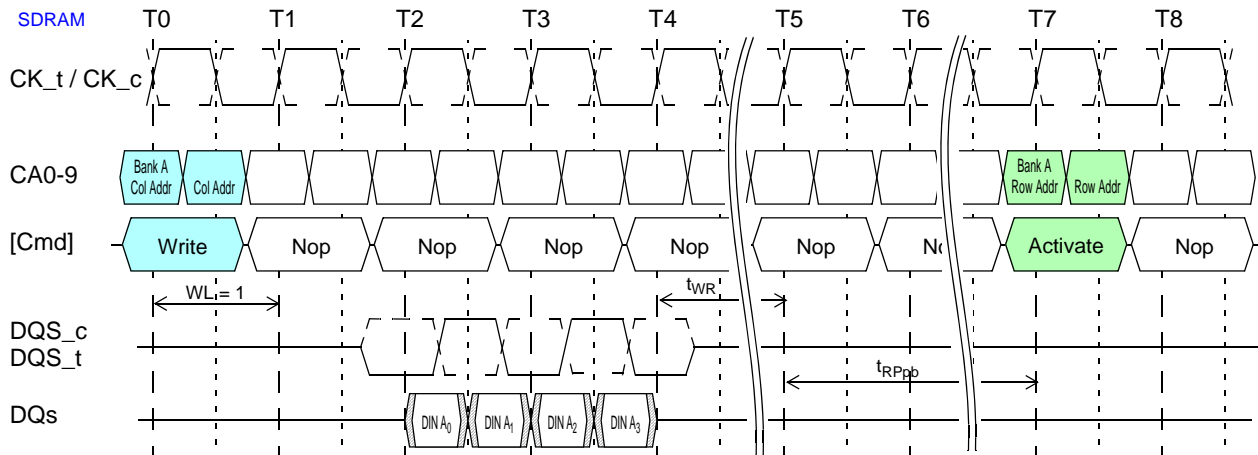


Figure 70 — LPDDR2-SX: Burst write w/Auto Precharge: WL = 1, BL = 4

## 5.9.3.2 LPDDR2-SX: Burst write with Auto-Precharge (cont'd)

Table 51 — LPDDR-S4: Precharge &amp; Auto Precharge clarification

From Command	To Command	Minimum Delay between “From Command” to “To Command”	Unit	Notes
Read	Precharge (to same Bank as Read)	$BL/2 + \max(2, RU(t_{RTP}/t_{CK})) - 2$	clks	1
	Precharge All	$BL/2 + \max(2, RU(t_{RTP}/t_{CK})) - 2$	clks	1
BST (for Reads)	Precharge (to same Bank as Read)	1	clks	1
	Precharge All	1	clks	1
Read w/AP	Precharge (to same Bank as Read w/AP)	$BL/2 + \max(2, RU(t_{RTP}/t_{CK})) - 2$	clks	1,2
	Precharge All	$BL/2 + \max(2, RU(t_{RTP}/t_{CK})) - 2$	clks	1
	Activate (to same Bank as Read w/AP)	$BL/2 + \max(2, RU(t_{RTP}/t_{CK})) - 2 + RU(t_{RPpb}/t_{CK})$	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	$RL + BL/2 + RU(t_{DQSCkmax}/t_{CK}) - WL + 1$	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	$BL/2$	clks	3
Write	Precharge (to same Bank as Write)	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	clks	1
	Precharge All	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	clks	1
BST (for Writes)	Precharge (to same Bank as Write)	$WL + RU(t_{WR}/t_{CK}) + 1$	clks	1
	Precharge All	$WL + RU(t_{WR}/t_{CK}) + 1$	clks	1
Write w/AP	Precharge (to same Bank as Write w/AP)	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	clks	1
	Precharge All	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	clks	1
	Activate (to same Bank as Write w/AP)	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1 + RU(t_{RPpb}/t_{CK})$	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	$BL/2$	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	$WL + BL/2 + RU(t_{WTR}/t_{CK}) + 1$	clks	3
Precharge	Precharge (to same Bank as Precharge)	1	clks	1
	Precharge All	1	clks	1
Precharge All	Precharge	1	clks	1
	Precharge All	1	clks	1
<p>NOTE 1 For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after <math>t_{RP}</math> depending on the latest precharge command issued to that bank.</p> <p>NOTE 2 Any command issued during the minimum delay time as specified in Table 51 is illegal.</p> <p>NOTE 3 After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write w/AP may not be interrupted or truncated.</p>				

### 5.9.3.2 LPDDR2-SX: Burst write with Auto-Precharge (cont'd)

**Table 52 — LPDDR-S2: Precharge & Auto Precharge clarification**

From Command	To Command	Minimum Delay between “From Command” to “To Command”	Unit	Notes
Read	Precharge (to same Bank as Read)	$BL/2 + RU(t_{RTP}/t_{CK}) - 1$	clks	1
	Precharge All	$BL/2 + RU(t_{RTP}/t_{CK}) - 1$	clks	1
BST (for Reads)	Precharge (to same Bank as Read)	1	clks	1
	Precharge All	1	clks	1
Read w/AP	Precharge (to same Bank as Read w/AP)	$BL/2 + RU(t_{RTP}/t_{CK}) - 1$	clks	1
	Precharge All	$BL/2 + RU(t_{RTP}/t_{CK}) - 1$	clks	1
	Activate (to same Bank as Read w/AP)	$BL/2 + RU(t_{RTP}/t_{CK}) - 1 + RU(t_{RPpb}/t_{CK})$	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	$RL + BL/2 + RU(t_{DQSCkmax}/t_{CK}) - WL + 1$	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	$BL/2$	clks	3
Write	Precharge (to same Bank as Write)	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	clks	1
	Precharge All	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	clks	1
BST (for Writes)	Precharge (to same Bank as Write)	$WL + RU(t_{WR}/t_{CK}) + 1$	clks	1
	Precharge All	$WL + RU(t_{WR}/t_{CK}) + 1$	clks	1
Write w/AP	Precharge (to same Bank as Write w/AP)	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	clks	1
	Precharge All	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	clks	1
	Activate (to same Bank as Write w/AP)	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1 + RU(t_{RPpb}/t_{CK})$	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	$BL/2$	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	$WL + BL/2 + RU(t_{WTR}/t_{CK}) + 1$	clks	3
Precharge	Precharge (to same Bank as Precharge)	1	clks	1
	Precharge All	1	clks	1
Precharge All	Precharge	1	clks	1
	Precharge All	1	clks	1

NOTE 1 For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after  $t_{RP}$  depending on the latest precharge command issued to that bank.

NOTE 2 Any command issued during the minimum delay time as specified in Table 52 is illegal.

NOTE 3 After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write w/AP may not be interrupted or truncated.

### 5.10 LPDDR2-SX: Refresh command

The Refresh command is initiated by having CS<sub>n</sub> LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of clock. Per Bank Refresh is initiated by having CA3 LOW at the rising edge of clock and All Bank Refresh is initiated by having CA3 HIGH at the rising edge of clock. Per Bank Refresh is only allowed in devices with 8 banks.

A Per Bank Refresh command, REFpb performs a refresh operation to the bank which is scheduled by the bank counter in the memory device. The bank sequence of Per Bank Refresh is fixed to be a sequential round-robin: “0-1-2-3-4-5-6-7-0-1-...”. The bank count is synchronized between the controller and the SDRAM upon issuing a RESET command or at every exit from self refresh, by resetting bank count to zero. The bank addressing for the Per Bank Refresh count is the same as established in the single-bank Precharge command (see Table 50).

A bank must be idle before it can be refreshed. It is the responsibility of the controller to track the bank being refreshed by the Per Bank Refresh command.

As shown in Table 53, the REFpb command may not be issued to the memory until the following conditions are met:

- a)  $t_{RFCab}$  has been satisfied after the prior REFab command
- b)  $t_{RFCpb}$  has been satisfied after the prior REFpb command
- c)  $t_{RP}$  has been satisfied after the prior Precharge command to that given bank

$t_{RRD}$  has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than affected by the REFpb command).

The target bank is inaccessible during the Per Bank Refresh cycle time ( $t_{RFCpb}$ ), however other banks within the device are accessible and may be addressed during the Per Bank Refresh cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in active state or accessed by a read or a write command.

When the Per Bank refresh cycle has completed, the affected bank will be in the Idle state.

As shown in Table 53, after issuing REFpb:

- a)  $t_{RFCpb}$  must be satisfied before issuing a REFab command
- b)  $t_{RFCpb}$  must be satisfied before issuing an ACTIVATE command to the same bank
- c)  $t_{RRD}$  must be satisfied before issuing an ACTIVATE command to a different bank
- d)  $t_{RFCpb}$  must be satisfied before issuing another REFpb command

An All Bank Refresh command, REFab performs a refresh operation to all banks. All banks have to be in Idle state when REFab is issued (for instance, by Precharge all-bank command). REFab also synchronizes the bank count between the controller and the SDRAM to zero.

As shown in Table 53, the REFab command may not be issued to the memory until the following conditions have been met:

- a)  $t_{RFCab}$  has been satisfied after the prior REFab command
- b)  $t_{RFCpb}$  has been satisfied after the prior REFpb command
- c)  $t_{RP}$  has been satisfied after prior Precharge commands

When the All Bank refresh cycle has completed, all banks will be in the Idle state.

As shown in Table 53, after issuing REFab:

- a) the  $t_{RFCab}$  latency must be satisfied before issuing an ACTIVATE command
- b) the  $t_{RFCab}$  latency must be satisfied before issuing a REFab or REFpb command.

## 5.10 LPDDR2-SX: Refresh command (cont'd)

**Table 53 — Command Scheduling Separations related to Refresh**

Symbol	minimum delay from	to		Notes
$t_{RFCab}$	REFab	REFab		
		Activate cmd to <i>any</i> bank		
		REFpb		
$t_{RFCpb}$	REFpb	REFab		
		Activate cmd to <i>same</i> bank as REFpb		
		REFpb		
$t_{RRD}$	REFpb	Activate cmd to <i>different</i> bank than REFpb		
	Activate	REFpb affecting an idle bank ( <i>different</i> bank than Activate)		1
		Activate cmd to <i>different</i> bank than prior Activate		
NOTE 1 A bank must be in the Idle state before it is refreshed. Therefore, after Activate, REFab is not allowed and REFpb is allowed only if it affects a bank which is in the Idle state.				

### 5.10.1 LPDDR2 SDRAM Refresh Requirements

(1) Minimum number of Refresh commands:

The LPDDR2 SDRAM requires a minimum number of R Refresh (REFab) commands within any rolling Refresh Window ( $t_{REFW} = 32 \text{ ms @ MR4}[2:0] = "011"$  or  $T_{case} \leq 85^\circ \text{C}$ ). See [Table 101](#) and [Table 102](#) for actual numbers per density. The resulting average refresh interval ( $t_{REFI}$ ) is given in [Table 102](#) and [Table 101](#).

See Mode Register 4 ([MR4](#)) for  $t_{REFW}$  and  $t_{REFI}$  refresh multipliers at different MR4 settings.

For LPDDR2-SDRAM devices supporting Per-Bank-Refresh, a REFab command may be replaced by a full cycle of eight REFpb commands.

(2) Burst Refresh limitation:

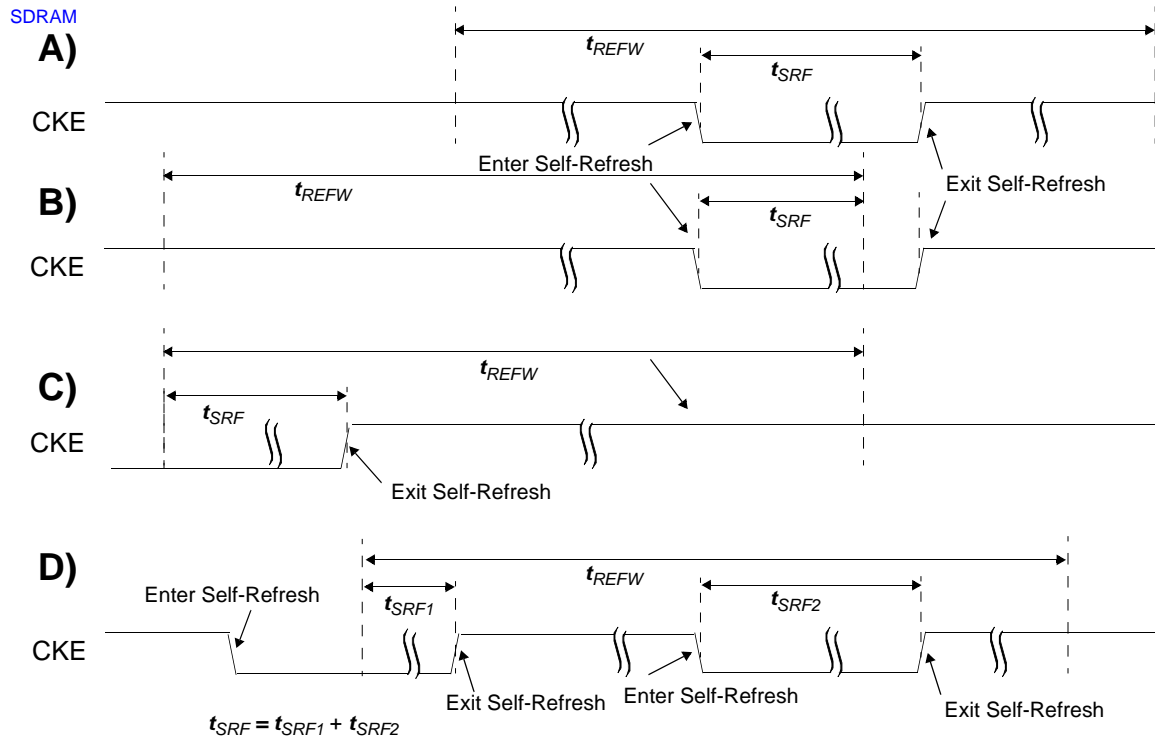
To limit maximum current consumption, a maximum of 8 REFab commands may be issued in any rolling  $t_{REFBW}$  ( $t_{REFBW} = 4 \times 8 \times t_{RFCab}$ ). This condition does not apply if REFpb commands are used.

(3) Refresh Requirements and Self-Refresh:

If any time within a refresh window is spent in Self-Refresh Mode, the number of required Refresh commands in this particular window is reduced to:

$$R^* = R - RU\{t_{SRF} / t_{REFI}\} = R - RU\{R * t_{SRF} / t_{REFW}\}; \text{ where RU stands for the round-up function.}$$

## 5.10.1 LPDDR2 SDRAM Refresh Requirements (cont'd)

Figure 71 — LPDDR2-SX: Definition of  $t_{SRF}$ 

Several examples on how  $t_{SRF}$  is calculated:

A: with the time spent in Self-Refresh Mode fully enclosed in the Refresh Window ( $t_{REFW}$ ),

B: at Self-Refresh entry

C: at Self-Refresh exit

D: with several different intervals spent in Self Refresh during one  $t_{REFW}$  interval

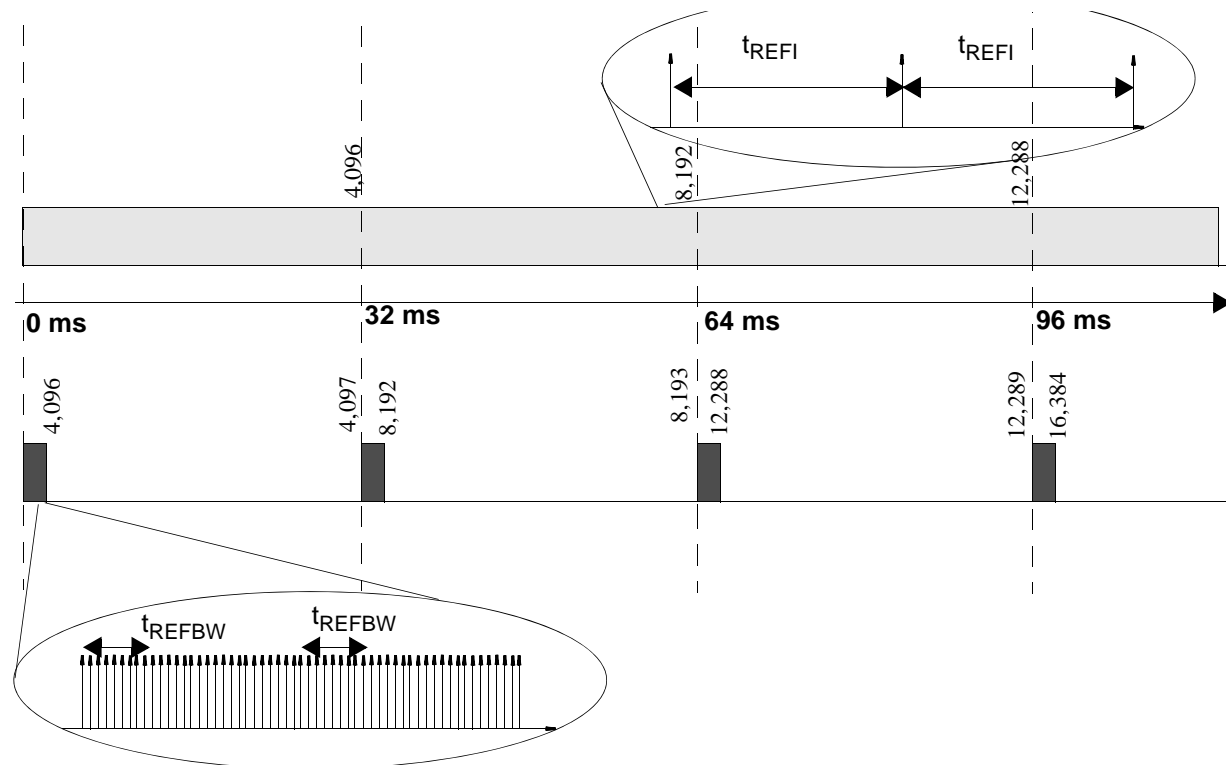
In contrast to JESD79 and JESD79-2 and JESD79-3 compliant SDRAM devices, LPDDR2-SX devices allow significant flexibility in scheduling REFRESH commands, as long as the boundary conditions above are met.

In the most straight forward case a REFRESH command should be scheduled every  $t_{REFI}$ . In this case Self-Refresh may be entered at any time.

The users may choose to deviate from this regular refresh pattern e.g., to enable a period where no refreshes are required. In the extreme (e.g., LPDDR2-S4 1Gb) the user may choose to issue a refresh burst of 4096 REFRESH commands with the maximum allowable rate (limited by  $t_{REFBW}$ ) followed by a long time without any REFRESH commands, until the refresh window is complete, then repeating this sequence. The achievable time without REFRESH commands is given by  $t_{REFW} - (R / 8) * t_{REFBW} = t_{REFW} - R * 4 * t_{RFCab}$ . (e.g., for a LPDDR2-S4 1Gb device @  $T_{case} \leq 85^{\circ}\text{C}$  this can be up to 32 ms - 4096 \* 4 \* 130 ns ~ 30 ms).

While both - the regular and the burst/pause - patterns can satisfy the refresh requirements per rolling refresh interval, if they are repeated in every subsequent 32 ms window, extreme care must be taken when transitioning from one pattern to another to satisfy the refresh requirement in every rolling refresh window during the transition. Figure 73 shows an example of an allowable transition from a burst pattern to a regular, distributed pattern. If this transition happens directly after the burst refresh phase, all rolling  $t_{REFW}$  intervals will have at least the required number of refreshes. Figure 74 shows an example of a non-allowable transition. In this case the regular refresh pattern starts after the completion of the pause-phase of the burst/pause refresh pattern. For several rolling  $t_{REFW}$  intervals the minimum number of REFRESH commands is not satisfied. The understanding of the pattern transition is extremely relevant (even if in normal operation only one pattern is employed), as in Self-Refresh-Mode a regular, distributed refresh pattern has to be assumed, which is reflected in the equation for  $R^*$  above. Therefore it is recommended to enter Self-Refresh-Mode ONLY directly after the burst-phase of a burst/pause refresh pattern as indicated in Figure 75 and begin with the burst phase upon exit from Self-Refresh.

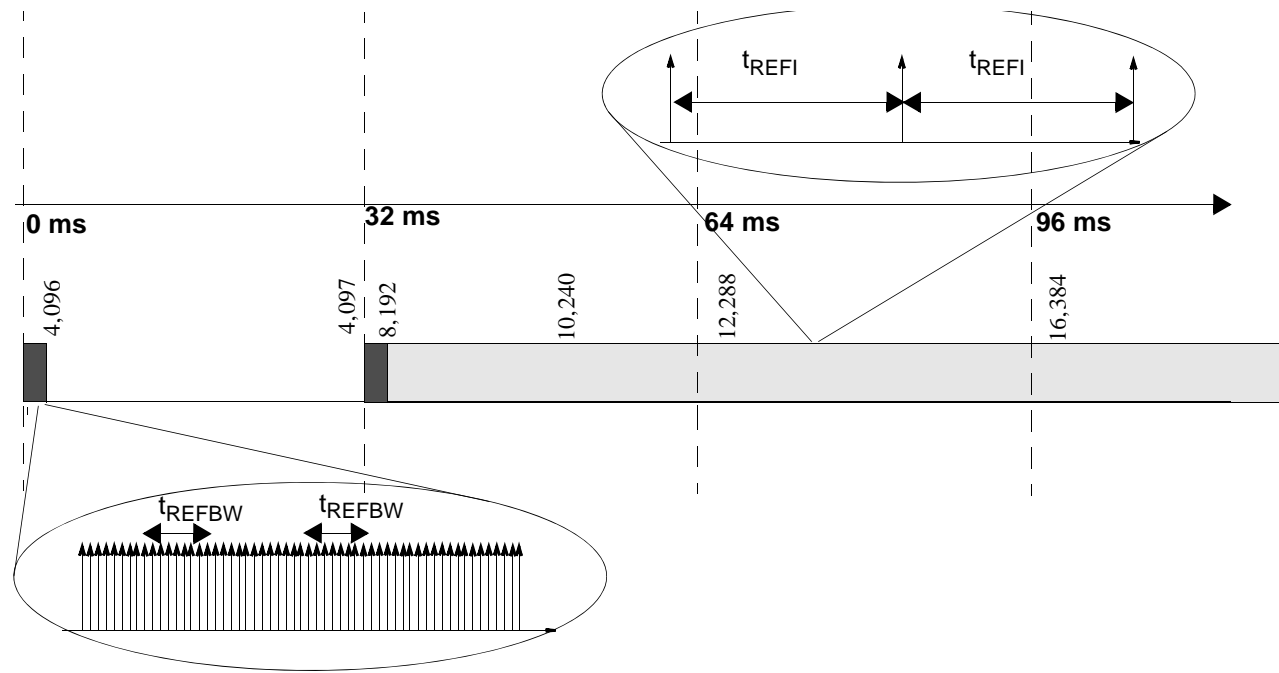
### 5.10.1 LPDDR2 SDRAM Refresh Requirements (cont'd)



**Figure 72 — LPDDR2-SX: Regular, Distributed Refresh Pattern vs. Repetitive Burst Refresh with Subsequent Refresh Pause**

NOTE 1 For a (e.g.) LPDDR2-S4 1 Gb device @ Tcase less than or equal to 85C the distributed refresh pattern would have one REFRESH command per 7.8 us; the burst refresh pattern would have an average of one refresh command per 0.52 us followed by ~30 ms without any REFRESH command.

### 5.10.1 LPDDR2 SDRAM Refresh Requirements (cont'd)

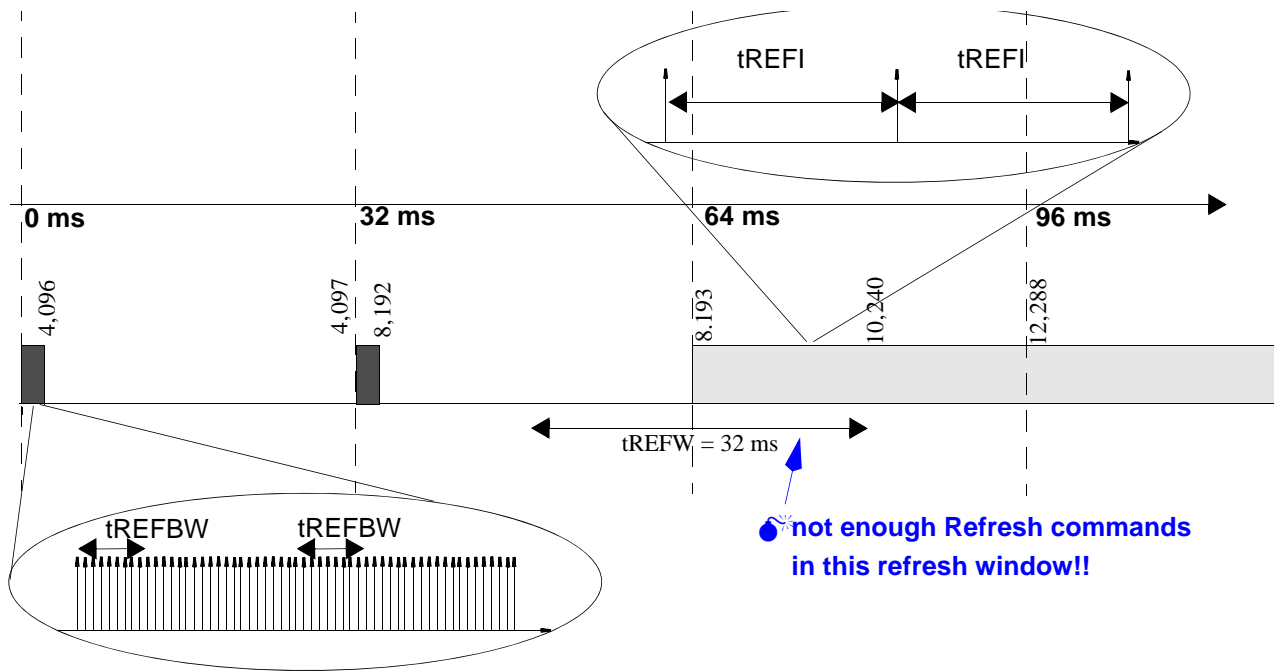


**Figure 73 — LPDDR2-SX: Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern**

NOTE 1 For a (e.g.) LPDDR2-S4 1 Gb device @ Tcase less than or equal to 85 C the distributed refresh pattern would have one REFRESH command per 7.8 us; the burst refresh pattern would have an average of one refresh command per 0.52 us followed by ~30 ms without any REFRESH command.

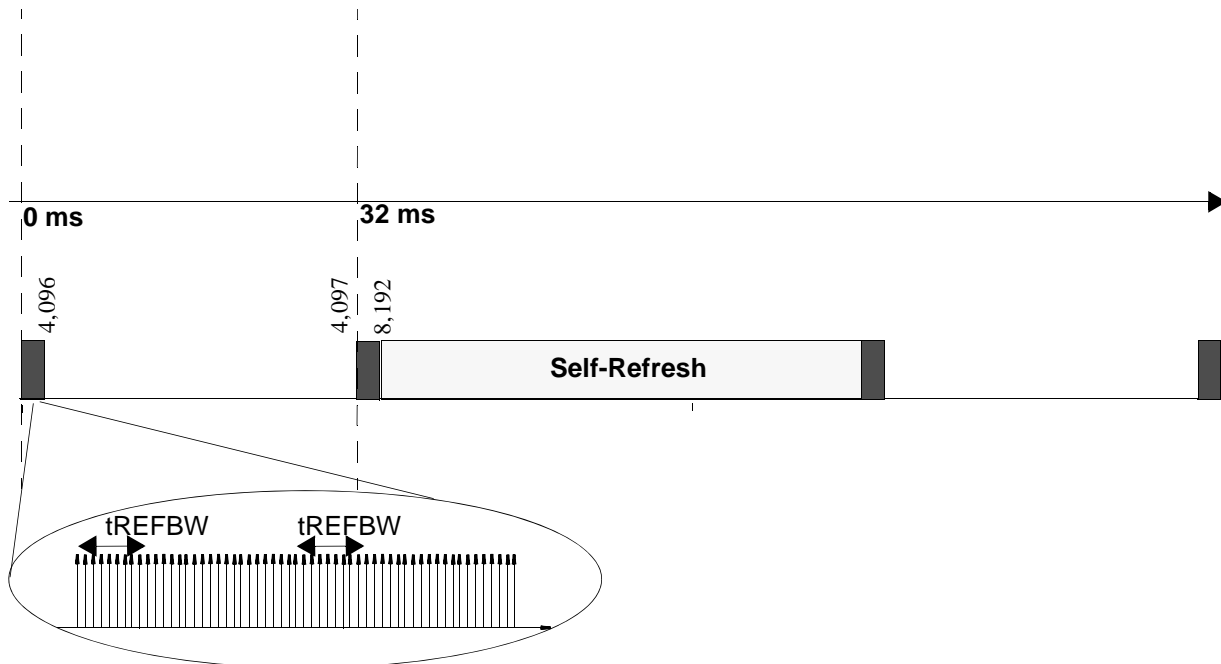


### 5.10.1 LPDDR2 SDRAM Refresh Requirements (cont'd)



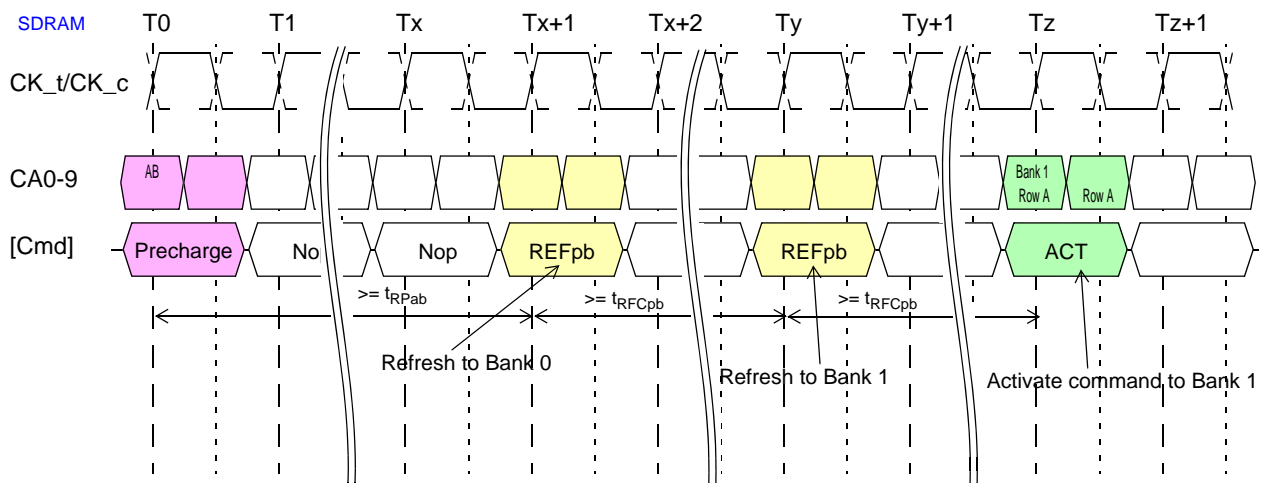
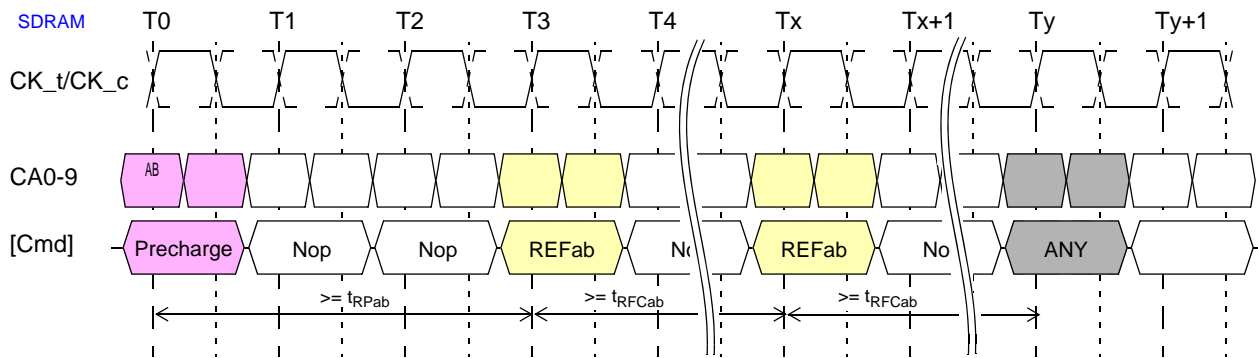
**Figure 74 — LPDDR2-SX: NOT-Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern**

NOTE 1 Only ~2048 REFRESH commands (<R!!) in the indicated  $t_{REFW}$  win-



**Figure 75 — LPDDR2-SX: Recommended Self-refresh entry and exit in conjunction with a Burst/Pause Refresh patterns.**

### 5.10.1 LPDDR2 SDRAM Refresh Requirements (cont'd)



NOTE 1 In the beginning of this example, the REFpb bank is pointing to Bank 0.

NOTE 2 Operations to other banks than the bank being refreshed are allowed during the  $t_{RFCpb}$  period.

**Figure 77 — LPDDR2-SX: Per Bank Refresh Operation**

### 5.11 LPDDR2-SX: Self Refresh operation

The Self Refresh command can be used to retain data in the LPDDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the LPDDR2 SDRAM retains data without external clocking. The LPDDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS\_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

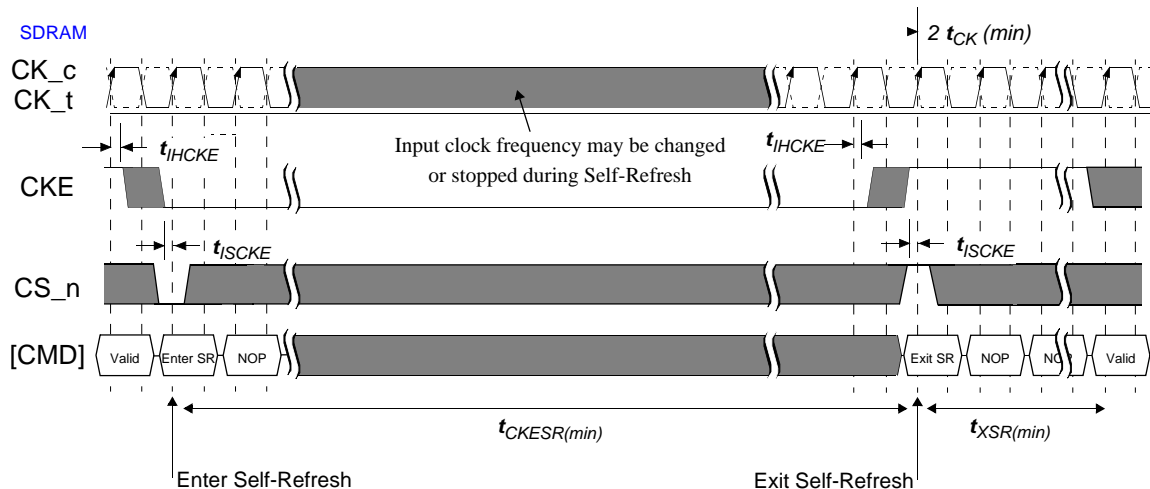
LPDDR2-SX devices can operate in Self Refresh in both the Standard or Extended Temperature Ranges. LPDDR2-SX devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher at high temperatures. See [Table 98](#) for details.

Once the LPDDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pins (VDD1, VDD2, and VDDCA) must be at valid levels. VDDQ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, VDDQ must be within specified limits. VrefDQ and VrefCA may be at any level within minimum and maximum levels (see [6.1](#)). However prior to exiting Self-Refresh, VrefDQ and VrefCA must be within specified limits (see [7.1](#)). The SDRAM initiates a minimum of one all-bank refresh command internally within  $t_{CKESR}$  period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the LPDDR2 SDRAM must remain in Self Refresh mode is  $t_{CKESR}$ . The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 tCK prior to the positive clock edge that registers CKE HIGH. Once Self Refresh Exit is registered, a delay of at least  $t_{XSR}$  must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period  $t_{XSR}$  for proper operation except for self refresh re-entry. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval  $t_{XSR}$ .

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in 5.10.1, since no refresh operations are performed in power-down mode.



### Figure 78 — LPDDR2-SX: Self-Refresh Operation

NOTE 4 A valid command may be issued only after  $t_{XSR}$  is satisfied. NOPs shall be issued during  $t_{XSR}$ .

### 5.11.1 LPDDR2-S2: Partial Array Self-Refresh: Bank Masking

LPDDR2-S2 SDRAM keeps the same PASR mapping of LPDDR SDRAM (JESD209). The choice of partial array to be refreshed in self refresh mode allows to reduce the range into lower numbered banks. MR16 has to be properly programmed to choose the PASR range (See Mode Register 16 ([MR16](#))). The PASR range becomes effective when the device goes into self refresh mode and determines which bank or banks to be refreshed.

**Table 54 — Bank Masking in LPDDR2-S2 4-Bank devices (64mb-2Gb)**

PASR Choice	Bank 0	Bank 1	Bank 2	Bank 3
Full Array				
1/2 Array			No Self-Refresh	
1/4 Array		No Self-Refresh		

**Table 55 — Bank Masking in LPDDR2-S2 8-Bank devices (4Gb-8Gb)**

PASR Choice	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Full Array								
1/2 Array					No Self-Refresh			
1/4 Array			No Self-Refresh					
1/8 Array		No Self-Refresh						

### 5.11.2 LPDDR2-S4: Partial Array Self-Refresh: Bank Masking

LPDDR2-S4 SDRAM has 4 or 8 banks. For LPDDR2-S4 devices, 64Mb to 512Mb LPDDR2 SDRAM has 4 banks, while 1Gb and higher density has 8. Each bank of LPDDR2 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16 (MR16).

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, “unmasked”. When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is described in the following chapter.

### 5.11.3 LPDDR2-S4: Partial Array Self-Refresh: Segment Masking

Segment masking scheme may be used in lieu of or in combination with bank masking scheme in LPDDR2-S4 SDRAM. The number of segments differ by the density and the setting of each segment mask bit is applied across all the banks. For segment masking bit assignments, see Mode Register 17 (MR17).

For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, “masked”. Programming of segment mask bits is similar to the one of bank mask bits. LPDDR2 SDRAM whose density is 64Mb, 128Mb, 256Mb, or 512Mb does not support segment masking. Only bank masking scheme is available. For 1Gb and larger densities, 8 segments are used as listed in Mode Register 17 (MR17). One mode register unit is used for the programming of segment mask bits up to 8 bits. One more mode register unit may be reserved for future use. These 2 mode register units are noted as “not used” for low-density LPDDR2-S4 SDRAM and a programming of mask bits has no effect on the device operation.

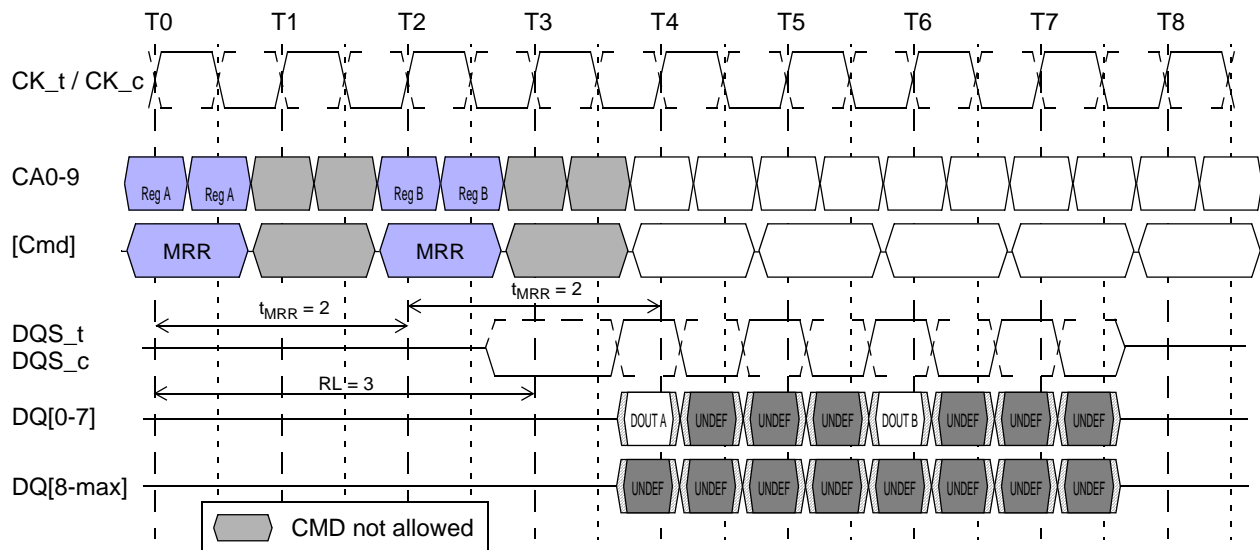
**Table 56 — Example of Bank and Segment Masking use in LPDDR2-S4 devices**

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0		M						M
Segment 1	0		M						M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0		M						M
Segment 4	0		M						M
Segment 5	0		M						M
Segment 6	0		M						M
Segment 7	1	M	M	M	M	M	M	M	M

NOTE 1 This table illustrates an example of an 8-bank LPDDR2-S4 device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

## 5.12 Mode Register Read Command

The Mode Register Read command is used to read configuration and status data from mode registers for both NVM and SDRAM. The Mode Register Read (MRR) command is initiated by having CS\_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The mode register contents are available on the first data beat of DQ0-DQ7,  $RL * t_{CK} + t_{DQSCk} + t_{DQSQ}$  after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in 5.12.2. All DQS\_t, DQS\_c shall be toggled for the duration of the Mode Register Read burst. The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period ( $t_{MRR}$ ) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS\_t, DQS\_c shall be toggled.



**Figure 79 — Mode Register Read timing example:  $RL = 3$ ,  $t_{MRR} = 2$**

NOTE 1 Mode Register Read has a burst length of four.

NOTE 2 Mode Register Read operation shall not be interrupted.

NOTE 3 Mode Register data is valid only on DQ[0-7] on the first beat. Subsequent beats contain valid, but undefined data. DQ[8-max] contain valid, but undefined data for the duration of the MRR burst.

NOTE 4 The Mode Register Command period is  $t_{MRR}$ . No command (other than Nop) is allowed during this period.

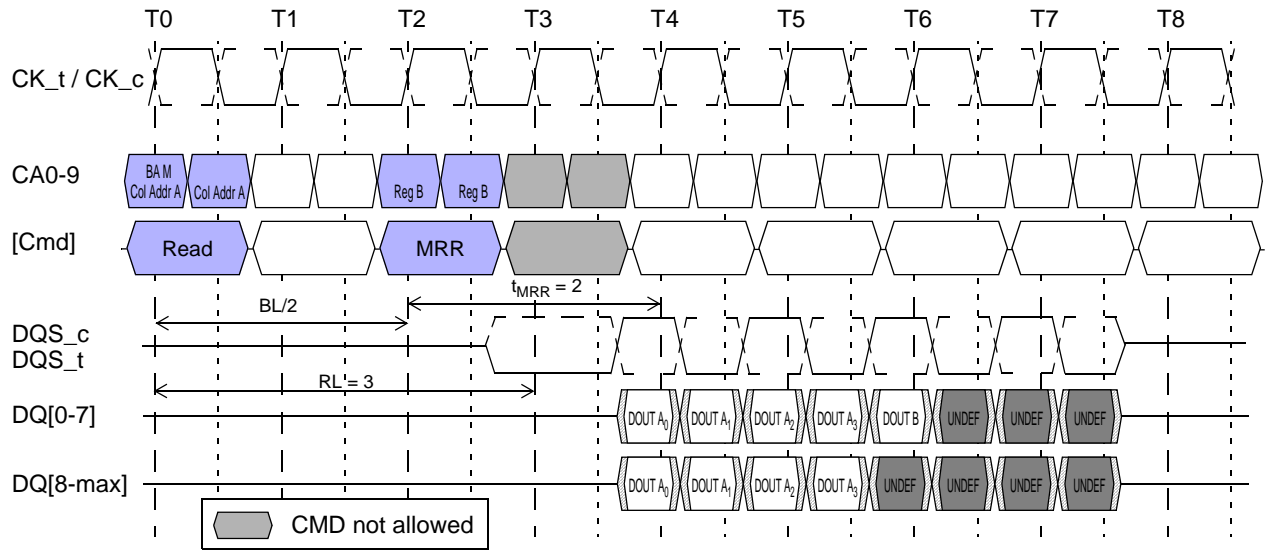
NOTE 5 Mode Register Reads to DQ Calibration registers MR32 and MR40 are described in the section on DQ Calibration.

NOTE 6 Minimum Mode Register Read to write latency is  $RL + RU(t_{DQSCkmax}/t_{CK}) + 4/2 + 1 - WL$  clock cycles.

NOTE 7 Minimum Mode Register Read to Mode Register Write latency is  $RL + RU(t_{DQSCkmax}/t_{CK}) + 4/2 + 1$  clock cycles.

The MRR command shall not be issued earlier than  $BL/2$  clock cycles after a prior Read command and  $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$  clock cycles after a prior Write command, because read-bursts and write-bursts shall not be truncated by MRR. Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL.”

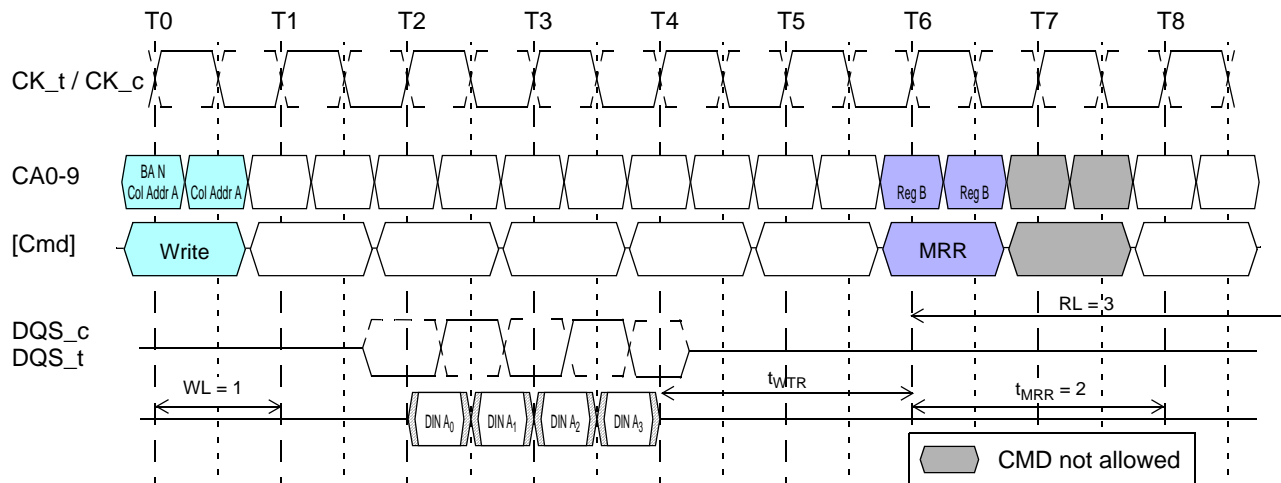
## 5.12 Mode Register Read Command (cont'd)



**Figure 80 — LPDDR2: Read to MRR timing example:  $RL = 3$ ,  $t_{MRR} = 2$**

NOTE 1: The minimum number of clocks from the burst read command to the Mode Register Read command is  $BL/2$ .

NOTE 2: The Mode Register Read Command period is  $t_{MRR}$ . No command (other than Nop) is allowed during this period.



**Figure 81 — LPDDR2: Burst Write Followed by MRR:  $RL = 3$ ,  $WL = 1$ ,  $BL = 4$**

NOTE 1 The minimum number of clock cycles from the burst write command to the Mode Register Read command is  $[WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})]$ .

NOTE 2 The Mode Register Read Command period is  $t_{MRR}$ . No command (other than Nop) is allowed during this period.

### 5.12.1 Temperature Sensor

LPDDR2-SX and LPDDR2-N devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate (SDRAM), determine whether AC timing de-rating is required in the Extended Temperature Range (SDRAM and NVM), and/or monitor the operating temperature (SDRAM and NVM). Either the temperature sensor or the device TOPER (See Table 73) may be used to determine whether operating temperature requirements are being met.

LPDDR2 devices shall monitor device temperature and update MR4 according to tTSI. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than tTSI.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification (See Table 73) that applies for the Standard or Extended Temperature Ranges. For example, TCASE may be above 85 °C when MR4[2:0] equals 011B.

To assure proper operation using the temperature sensor, applications should consider the following factors:

TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2 °C.

ReadInterval is the time period between MR4 reads from the system.

TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.

SysRespDelay is the maximum time between a read of MR4 and the response by the system.

LPDDR2 devices shall allow for a 2° C temperature margin between the point at which the device temperature enters the Extended Temperature Range and point at which the controller re-configures the system accordingly.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$TempGradient \times (ReadInterval + tTSI + SysRespDelay) \leq 2C$$

**Table 57 — Temperature Sensor**

Parameter	Symbol	Max/Min	Value	Unit	Notes
System Temperature Gradient	TempGradient	Max	System Dependent	°C/s	
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	
Temperature Sensor Interval	tTSI	Max	32	ms	
System Response Delay	SysRespDelay	Max	System Dependent	ms	
Device Temperature Margin	TempMargin	Max	2	°C	

For example, if TempGradient is 10°C/s and the SysRespDelay is 1 ms:

$$\frac{10C}{s} \times (ReadInterval + 32ms + 1ms) \leq 2C$$

In this case, ReadInterval shall be no greater than 167 ms.



### 5.12.1 Temperature Sensor (cont'd)

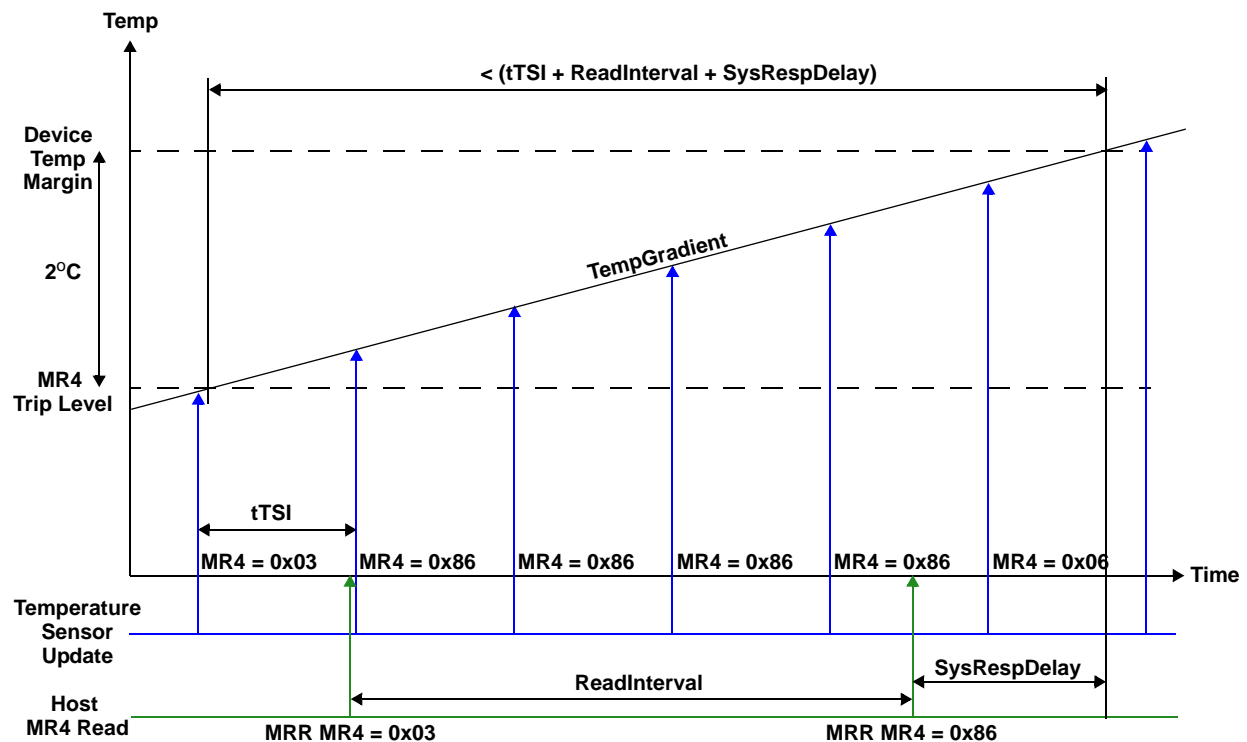


Figure 82 — Temp Sensor Timing

### 5.12.2 DQ Calibration

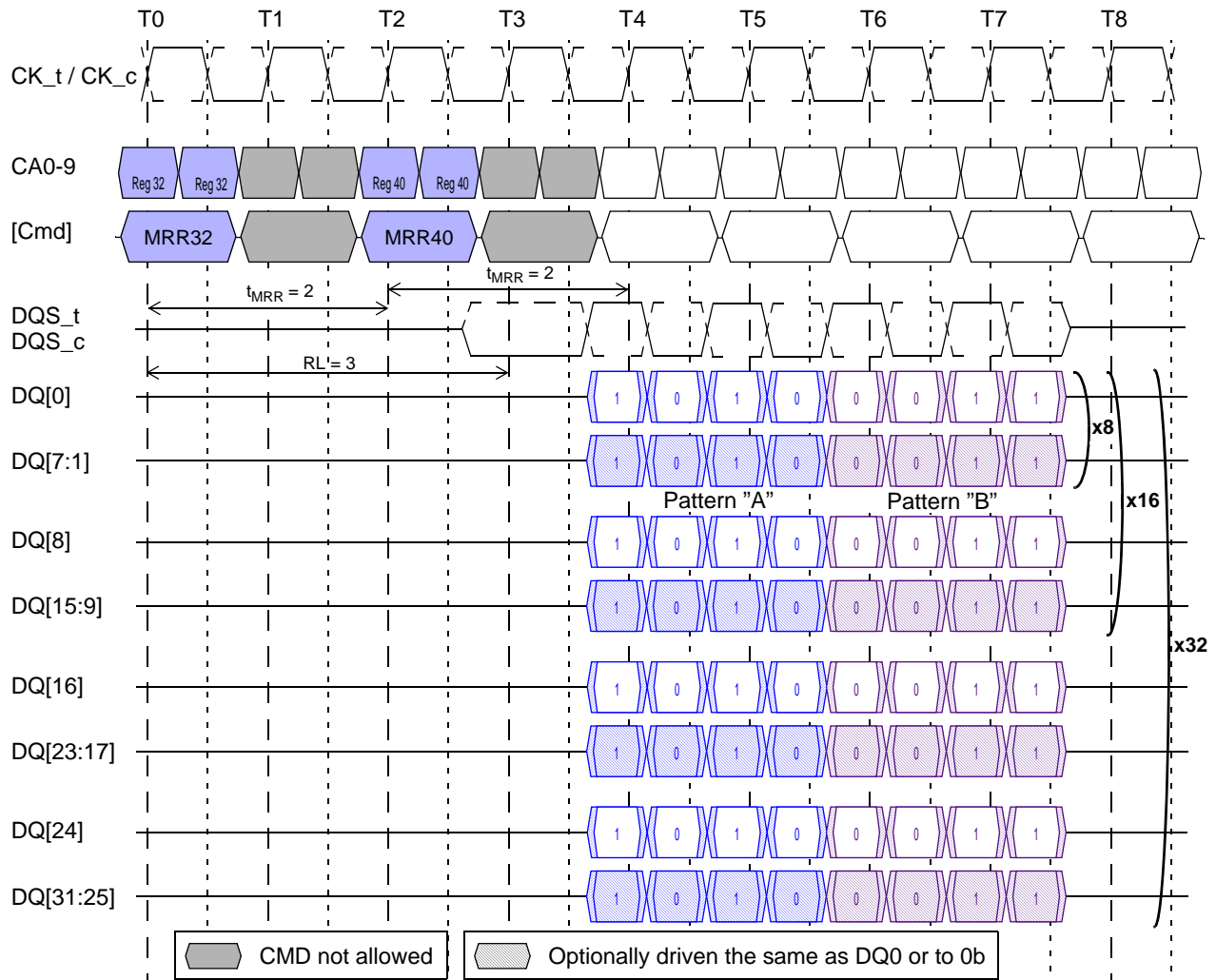
LPDDR2-SX and LPDDR2-N devices feature a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern “A”) or MR40 (Pattern “B”) will return the specified pattern on DQ[0] for x8 devices, DQ[0] and DQ[8] for x16 devices, and DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices. For x8 devices, DQ[7:1] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For x16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst.

For LPDDR2-SX devices, MRR DQ Calibration commands may only occur in the Idle state.

Table 58 — Data Calibration Pattern Description

	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
Pattern “A” (MR32)	1	0	1	0
Pattern “B” (MR40)	0	0	1	1

### 5.12.2 DQ Calibration (cont'd)



**Figure 83 — MR32 and MR40 DQ Calibration timing example: RL = 3,  $t_{MRR} = 2$**

NOTE 1 Mode Register Read has a burst length of four.

NOTE 2 Mode Register Read operation shall not be interrupted.

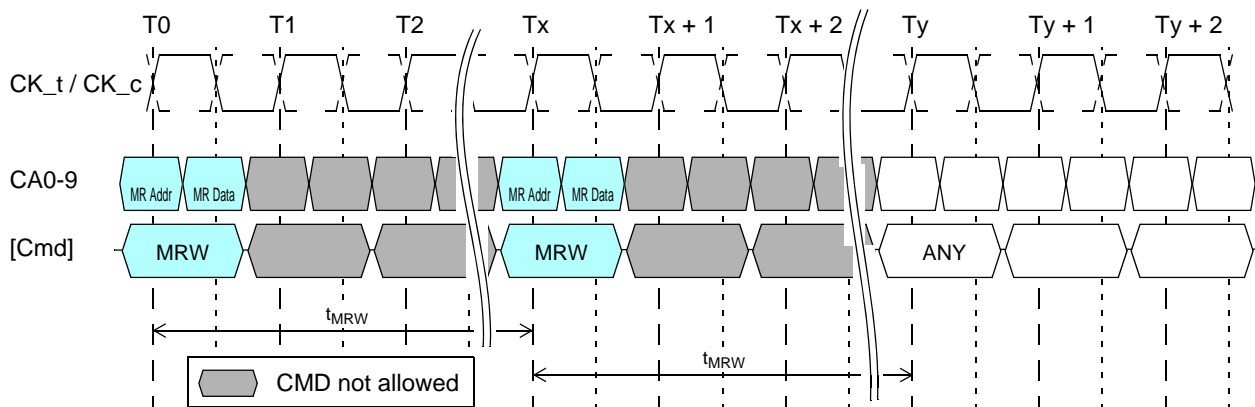
NOTE 3 Mode Register Reads to MR32 and MR40 drive valid data on DQ[0] during the entire burst. For x16 devices, DQ[8] shall drive the same information as DQ[0] during the burst. For x32 devices, DQ[8], DQ[16], and DQ[24] shall drive the same information as DQ[0] during the burst.

NOTE 4 For x8 devices, DQ[7:1] may optionally drive the same information as DQ[0] or they may drive 0b during the burst. For x16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or they may drive 0b during the burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or they may drive 0b during the burst.

NOTE 5 The Mode Register Command period is  $t_{MRR}$ . No command (other than Nop) is allowed during this period.

### 5.13 Mode Register Write Command

The Mode Register Write command is used to write configuration data to mode registers for both NVM and SDRAM. The Mode Register Write (MRW) command is initiated by having CS<sub>n</sub> LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by  $t_{MRW}$ . Mode Register Writes to read-only registers shall have no impact on the functionality of the device.



**Figure 84 — Mode Register Write timing example: RL = 3,  $t_{MRW}$  = 5**

NOTE 1 The Mode Register Write Command period is  $t_{MRW}$ . No command (other than Nop) is allowed during this period.

NOTE 2 At time Ty, the device is in the idle state.

#### 5.13.1 LPDDR2-SX: Mode Register Write

For LPDDR2-S devices, the MRW may only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in the idle precharge state is to issue a Precharge-All command.

#### 5.13.2 LPDDR2-N: Mode Register Write

For LPDDR2-N devices, the MRW may be issued from the Row Active or Idle states. If the MRW command is issued from the Row Active state, all row buffer contents are invalidated and the device returns to the Idle state.

The minimum time from the burst read command to the MRW command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum Read to MRW latency is  $RL + RU(t_{DQSCkmax}/t_{CK}) + BL/2$  clock cycles. The minimum time from the burst write command to the MRW command is defined by the Write Latency (WL) and the Burst Length (BL). Minimum Write to MRW latency is  $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$  clock cycles. Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL.”

## 5.13.2 LPDDR2-N: Mode Register Write (cont'd)

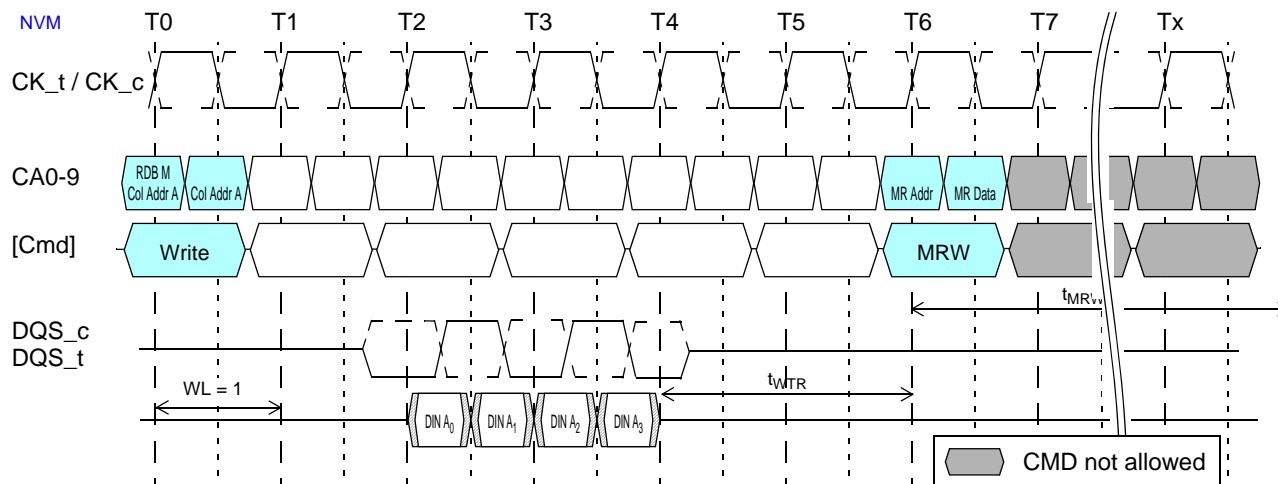


Figure 85 — LPDDR2-N: Burst Write Followed by MRW: WL = 1, BL = 4

NOTE 1 The minimum number of clock cycles from the burst write command to the Mode Register Write command is  $[WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})]$ .

NOTE 2 The Mode Register Write Command period is  $t_{MRW}$ . No command (other than Nop) is allowed during this period.

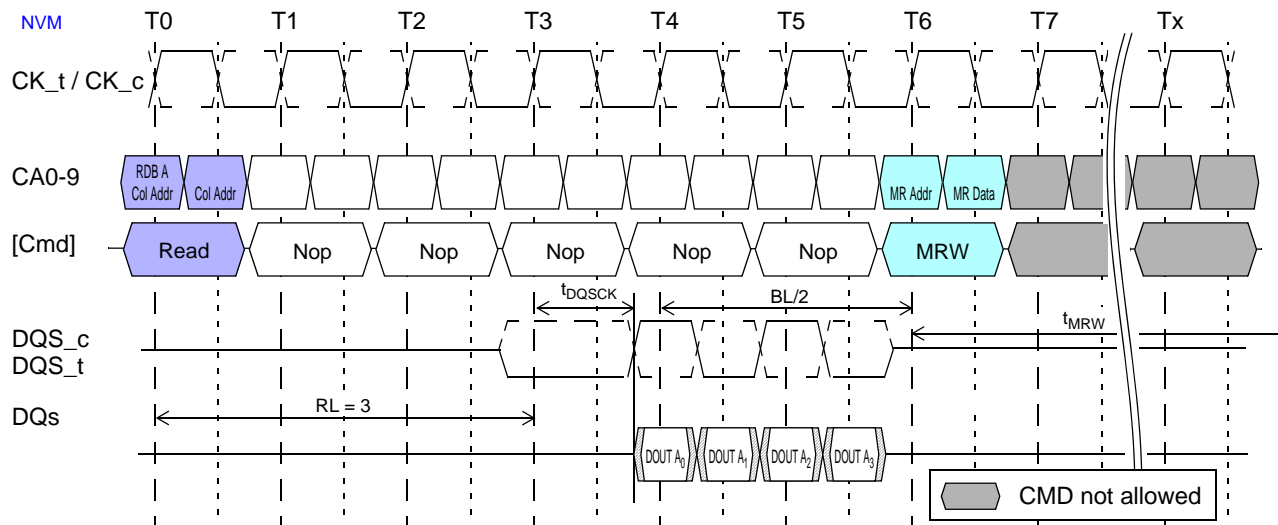


Figure 86 — LPDDR2-N: Burst Read followed by MRW: RL = 3, BL = 4

NOTE 1 The minimum number of clock cycles from the burst read command to the Mode Register Write command is  $[RL + RU(t_{DQSCk}/t_{CK}) + BL/2]$ .

NOTE 2 The Mode Register Write Command period is  $t_{MRW}$ . No command (other than Nop) is allowed during this period.

### 5.13.2 LPDDR2-N: Mode Register Write (cont'd)

**Table 59 — Truth Table for Mode Register Read (MRR)  
and Mode Register Write (MRW)**

Current State		Command	Intermediate State		Next State	
SDRAM	NVM		SDRAM	NVM	SDRAM	NVM
All Banks Idle	All RBs idle	MRR	Mode Register Reading (All Banks Idle)	Mode Register Reading (All RBs Idle)	All Banks Idle	All RBs Idle
		MRW	Mode Register Writing (All Banks Idle)	Mode Register Writing (All RBs Idle)	All Banks Idle	All RBs Idle
		MRW (RESET)	Resetting (Device Auto-Init)	Device Auto-Init (Resetting)	All Banks Idle	All RBs Idle
Bank(s) Active	RB(s) Active	MRR	Mode Register Reading (Bank(s) Active)	Mode Register Reading (RB(s) Active)	Bank(s) Active	RB(s) Active
		MRW	Not Allowed	Mode Register Writing (RB(s) Active)	Not Allowed	All RBs Idle
		MRW (RESET)	Not Allowed	Device Auto-Init (Resetting)	Not Allowed	All RBs Idle

### 5.13.3 Mode Register Write Reset (MRW Reset)

Any MRW command issued to MRW63 initiates an MRW Reset. The MRW Reset command brings the device to the Device Auto-Initialization (Resetting) State in the Power-On Initialization sequence (step 3 in 3.4.1). The MRW Reset command may be issued from the Idle state for LPDDR2-SX devices and the Idle or Active states for LPDDR2-N devices. This command resets all Mode Registers to their default values. In addition, for LPDDR2-N devices, this command ends all embedded operations and resets all Overlay Window registers to their default values. No commands other than NOP may be issued to the LPDDR2 device during the MRW Reset period ( $t_{INIT4}$ ). After MRW Reset, boot timings must be observed until the device initialization sequence is complete and the device is in the Idle state. Array data for LPDDR2-SX devices are undefined after the MRW Reset command.

For the timing diagram related to MRW Reset, refer to [Figure 6](#).

#### 5.13.4 Mode Register Write ZQ Calibration Command

The MRW command is also used to initiate the ZQ Calibration command. The ZQ Calibration command is used to calibrate the LPDDR2 output drivers (RON) over process, temperature, and voltage. LPDDR2-S2 devices do not support ZQ Calibration and the ZQ Calibration command shall be ignored by these devices. LPDDR2-S4 and LPDDR2-N devices support ZQ Calibration.

There are four ZQ Calibration commands and related timings, tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT corresponds to the initialization calibration, tZQRESET for resetting ZQ setting to default, tZQCL is for long calibration, and tZQCS is for short calibration. See Mode Register 10 ([MR10](#)) for description on the command codes for the different ZQ Calibration commands.

The Initialization ZQ Calibration (ZQINIT) shall be performed for LPDDR2-S4 and LPDDR2-N devices. This Initialization Calibration achieves a RON accuracy of +/-15%. After initialization, the ZQ Long Calibration may be used to re-calibrate the system to a RON accuracy of +/-15%. A ZQ Short Calibration may be used periodically to compensate for temperature and voltage drift in the system.

The ZQReset Command resets the RON calibration to a default accuracy of +/-30% across process, voltage, and temperature. This command is used to ensure RON accuracy to +/-30% when ZQCS and ZQCL are not used.

One ZQCS command can effectively correct a minimum of 1.5% (ZQCorrection) of RON impedance error within tZQCS for all speed bins assuming the maximum sensitivities specified in the ‘Output Driver Voltage and Temperature Sensitivity’. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdribrate) and voltage (Vdribrate) drift rates that the LPDDR2 is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdribrate) + (VSens \times Vdribrate)}$$

where TSens = max(dRONdT) and VSens = max(dRONdV) define the LPDDR2 temperature and voltage sensitivities.

For example, if TSens = 0.75% / °C, VSens = 0.20% / mV, Tdribrate = 1 °C / sec and Vdribrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

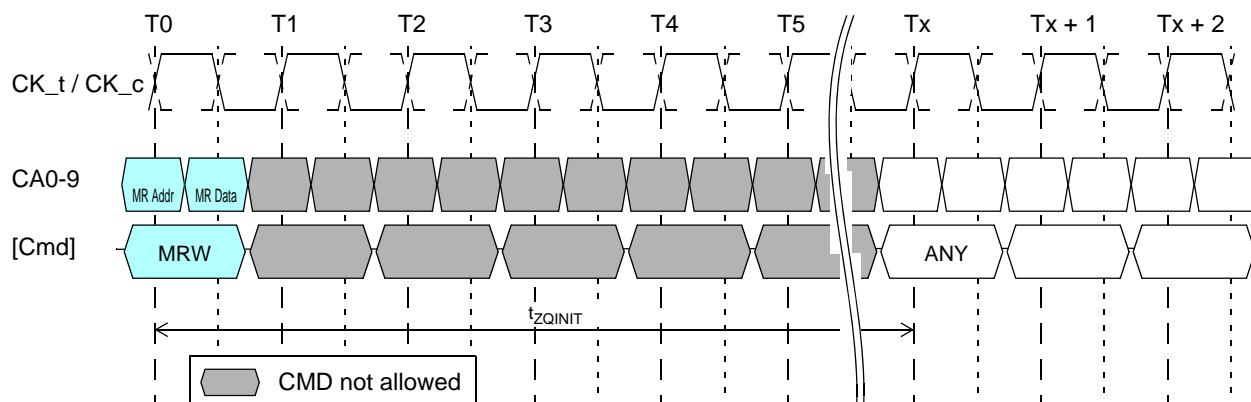
$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

For LPDDR2-S4 devices, a ZQ Calibration command may only be issued when the device is in Idle state with all banks precharged. For LPDDR2-N devices, a ZQ Calibration command may only be issued when the device is in the Idle or Active states.

No other activities can be performed on the LPDDR2 data bus during the calibration period (tZQINIT, tZQCL, tZQCS). The quiet time on the LPDDR2 data bus helps to accurately calibrate RON. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ Resistor, only one device may be calibrating at any given time. After calibration is achieved, the LPDDR2 device shall disable the ZQ ball's current consumption path to reduce power.

In systems that share the ZQ resistor between devices, the controller must not allow overlap of tZQINIT, tZQCS, or tZQCL between the devices. ZQ Reset overlap is allowed. If the ZQ resistor is absent from the system, ZQ shall be connected permanently to VDDCA. In this case, the LPDDR2 device shall ignore ZQ calibration commands and the device will use the default calibration settings (See [Table 92](#))

### 5.13.4 Mode Register Write ZQ Calibration Command (cont'd)

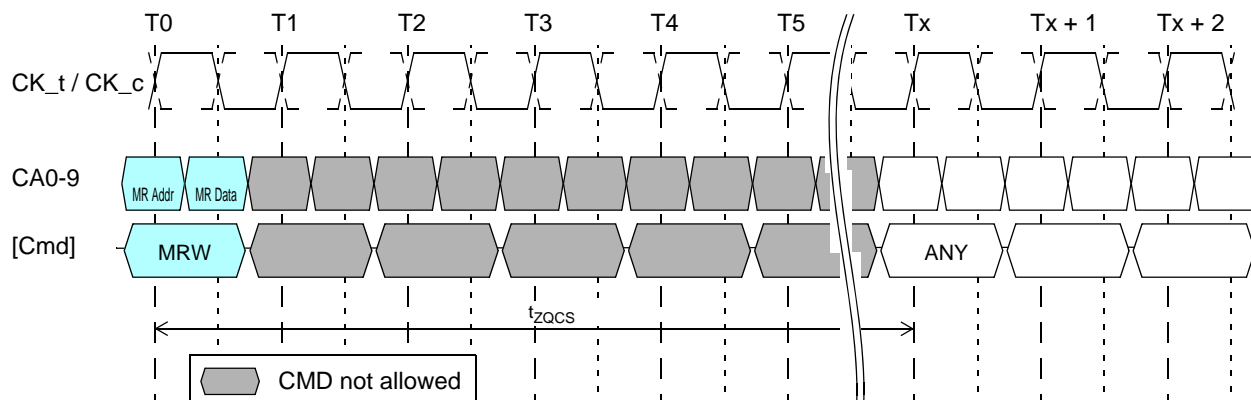


**Figure 87 — ZQ Calibration Initialization timing example**

NOTE 1: The ZQ Calibration Initialization period is  $t_{ZQINIT}$ . No command (other than Nop) is allowed during this period.

NOTE 2: CKE must be continuously registered HIGH during the calibration period.

NOTE 3: All devices connected to the DQ bus should be high impedance during the calibration process.

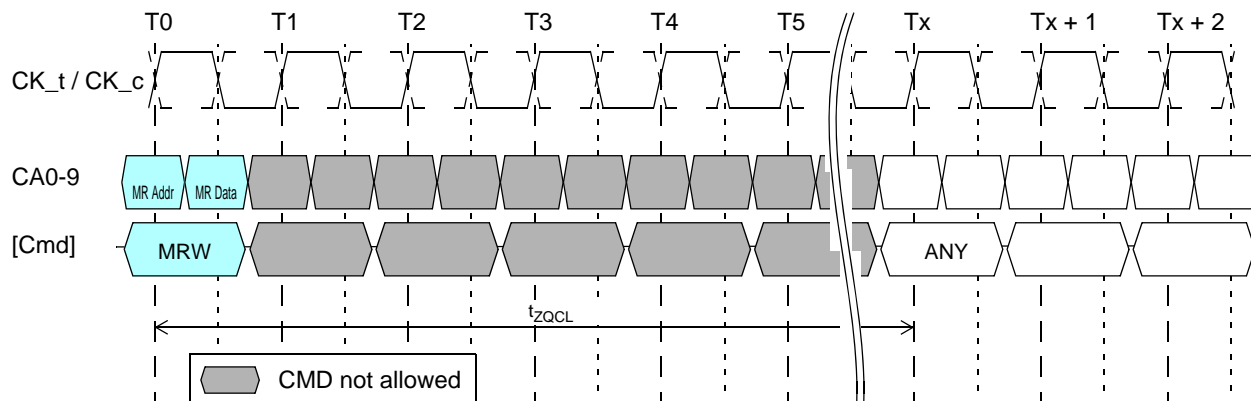


**Figure 88 — ZQ Calibration Short timing example**

NOTE 1: The ZQ Calibration Short period is  $t_{ZQCS}$ . No command (other than Nop) is allowed during this period.

NOTE 2: CKE must be continuously registered HIGH during the calibration period.

NOTE 3: All devices connected to the DQ bus should be high impedance during the calibration process.



**Figure 89 — ZQ Calibration Long timing example**

NOTE 1 The ZQ Calibration Long period is  $t_{ZQCL}$ . No command (other than Nop) is allowed during this period.

NOTE 2 CKE must be continuously registered HIGH during the calibration period.

NOTE 3 All devices connected to the DQ bus should be high impedance during the calibration process.

5.13.4 Mode Register Write ZQ Calibration Command (cont'd)

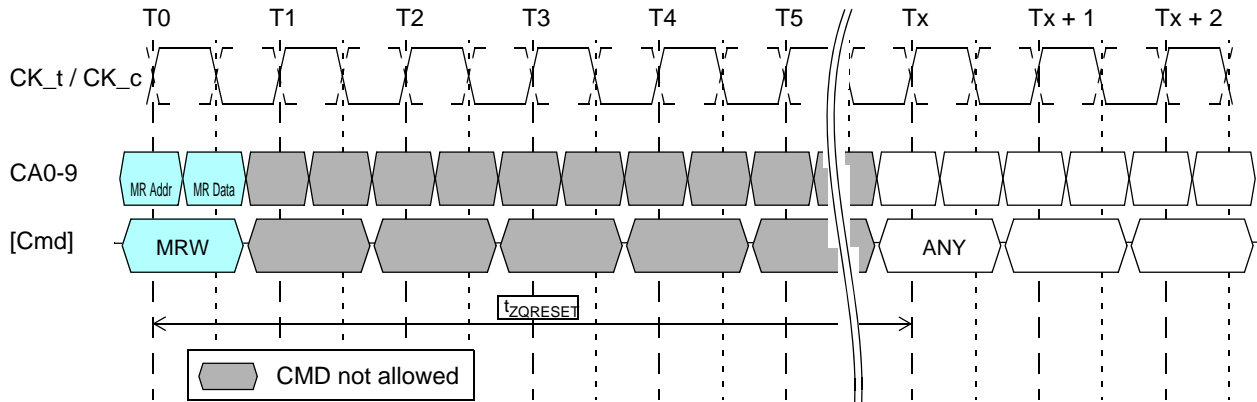


Figure 90 — ZQ Calibration Reset timing example

- NOTE 1 The ZQ Calibration Reset period is  $t_{ZQRESET}$ . No command (other than Nop) is allowed during this period.
- NOTE 2 CKE must be continuously registered HIGH during the calibration period.
- NOTE 3 All devices connected to the DQ bus should be high impedance during the calibration process.

5.13.4.1 ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ Calibration function, a 240 Ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each LPDDR2 device or one resistor can be shared between multiple LPDDR2 devices if the ZQ calibration timings for each LPDDR2 device do not overlap. The total capacitive loading on the ZQ pin must be limited (See [Table 94](#)).



## 5.14 Power-down

For LPDDR2 SDRAM, power-down is synchronously entered when CKE is registered LOW and CS\_n HIGH at the rising edge of clock. For LPDDR2 NVM, power-down is synchronously entered when CKE is registered LOW at the rising edge of clock. CKE must be registered HIGH in the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. CKE is allowed to go LOW while any of other operations such as row activation, preactive, precharge, autoprecharge, or refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power down.

For LPDDR2 SDRAM, if power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

For LPDDR2 NVM, if power-down occurs when all row buffers are idle, this mode is referred to as idle power-down; if power-down occurs when any row buffer is in the active state, this mode is referred to as active power-down.

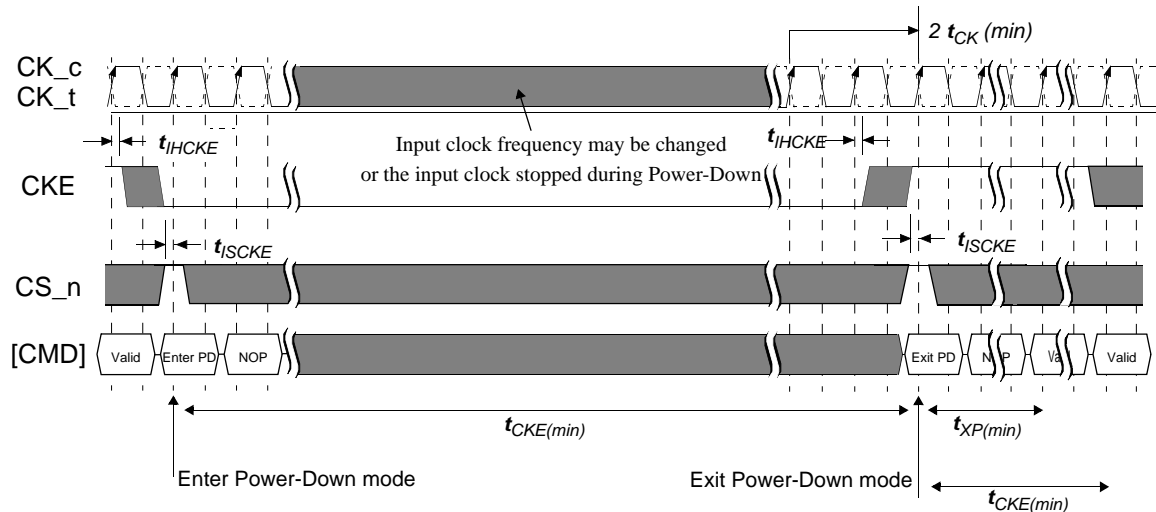
Entering power-down deactivates the input and output buffers, excluding CK\_t, CK\_c, and CKE. In power-down mode, CKE must be maintained LOW while all other input signals are “Don’t Care”. CKE LOW must be maintained until  $t_{CKE}$  has been satisfied.  $V_{REF}$  must be maintained at a valid level during power down.

VDDQ may be turned off during power down. If VDDQ is turned off, then VREFDQ must also be turned off. Prior to exiting power down, both VDDQ and VREFDQ must be within their respective min/max operating ranges (See 7.1).

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in 5.10.1, as no refresh operations are performed in power-down mode.

The power-down state is exited when CKE is registered HIGH. The controller shall drive CS\_n HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until  $t_{CKE}$  has been satisfied. A valid, executable command can be applied with power-down exit latency,  $t_{XP}$  after CKE goes HIGH. Power-down exit latency is defined in the timing parameter table of this standard.

### SDRAM

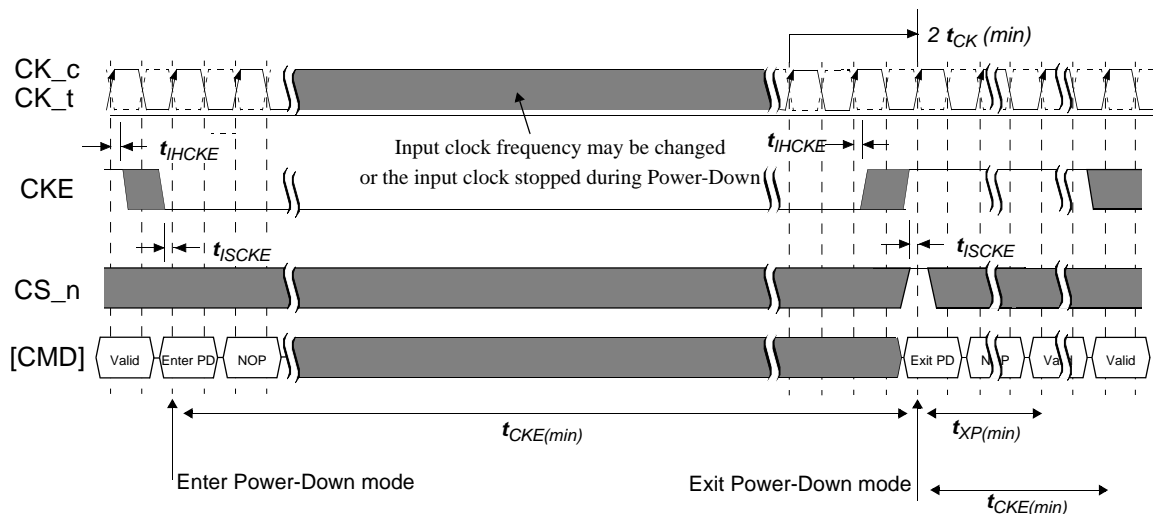


**Figure 91 — LPDDR2-SX: Basic power down entry and exit timing diagram**

NOTE 1 Input clock frequency may be changed or the input clock stopped during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

## 5.14 Power-down (cont'd)

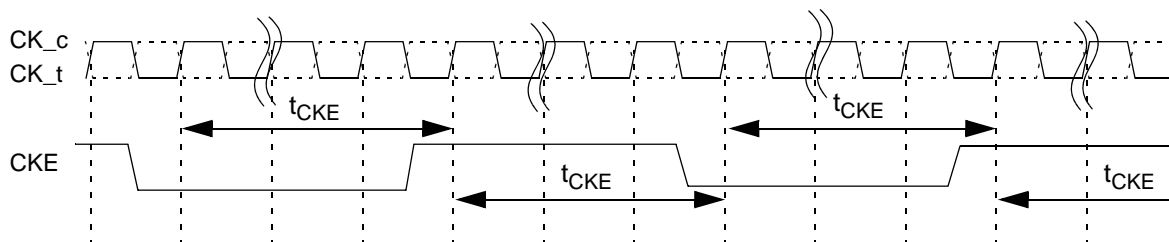
NVM



**Figure 92 — LPDDR2-N: Basic power down entry and exit timing diagram**

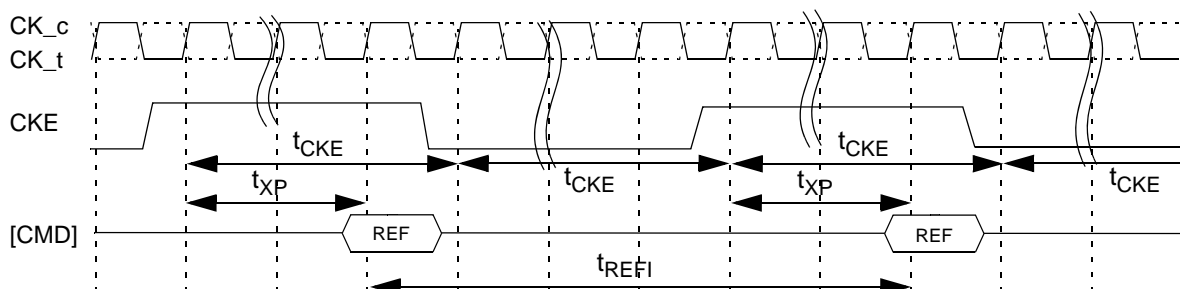
NOTE 1 Input clock frequency may be changed or the input clock stopped during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

NOTE 2 CS\_n is “do not care” for entry into power-down for NVM.



**Figure 93 — Example of CKE intensive environment**

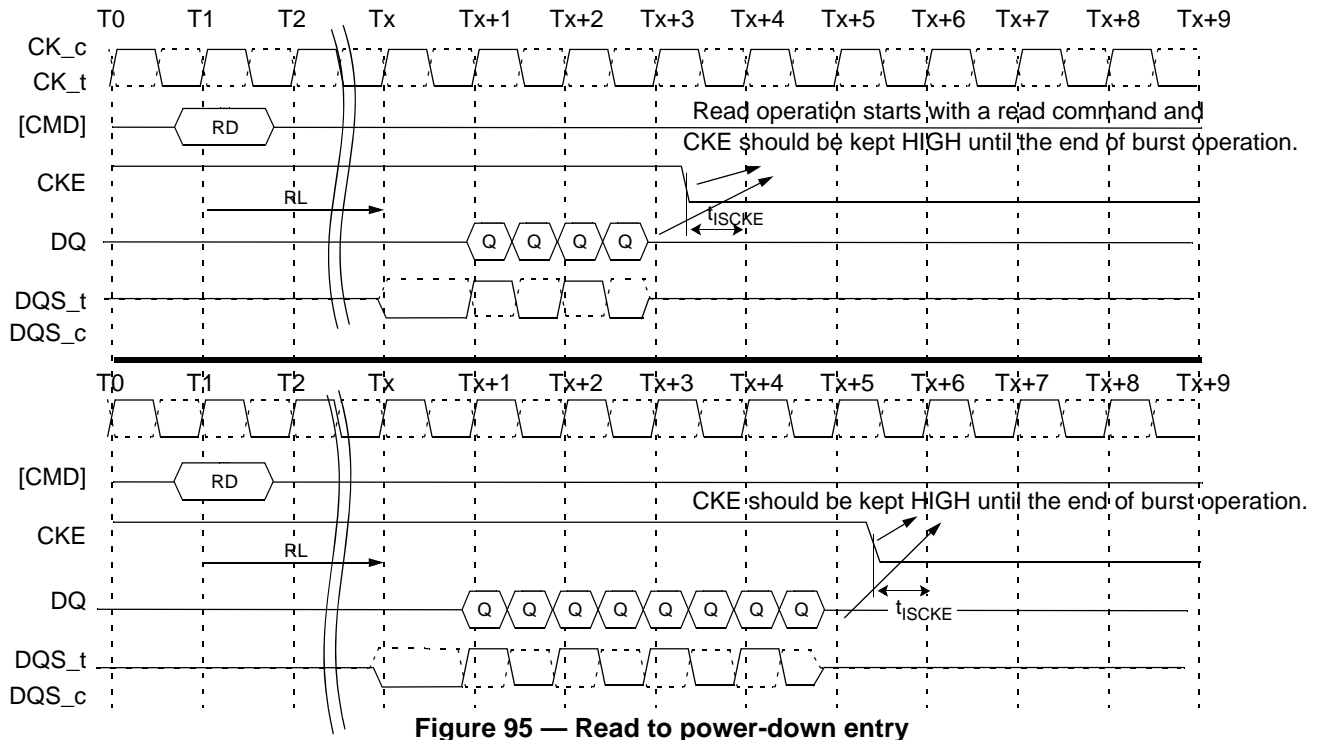
SDRAM



NOTE 1 The pattern shown above can repeat over a long period of time. With this pattern, LPDDR2 SDRAM guarantees all AC and DC timing & voltage specifications with temperature and voltage drift

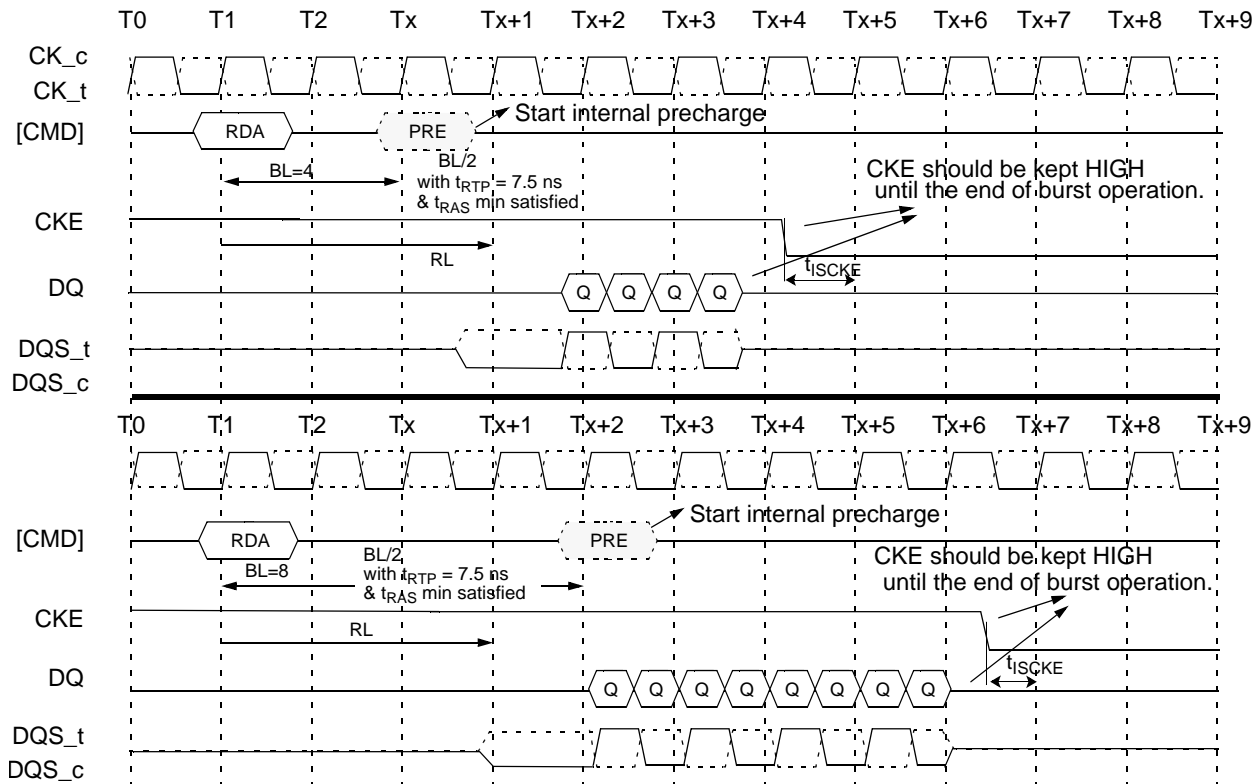
**Figure 94 — REF to REF timing with CKE intensive environment for LPDDR2 SDRAM**

#### 5.14 Power-down (cont'd)



NOTE 1 CKE may be registered LOW  $RL + RU(t_{DQSCK(MAX)}/t_{CK}) + BL/2 + 1$  clock cycles after the clock on which the Read command is registered.

#### SDRAM



NOTE 1 CKE may be registered LOW  $RL + RU(t_{DQSCK(MAX)}/t_{CK}) + BL/2 + 1$  clock cycles after the clock on which the Read command is registered.

### 5.14 Power-down (cont'd)

#### SDRAM

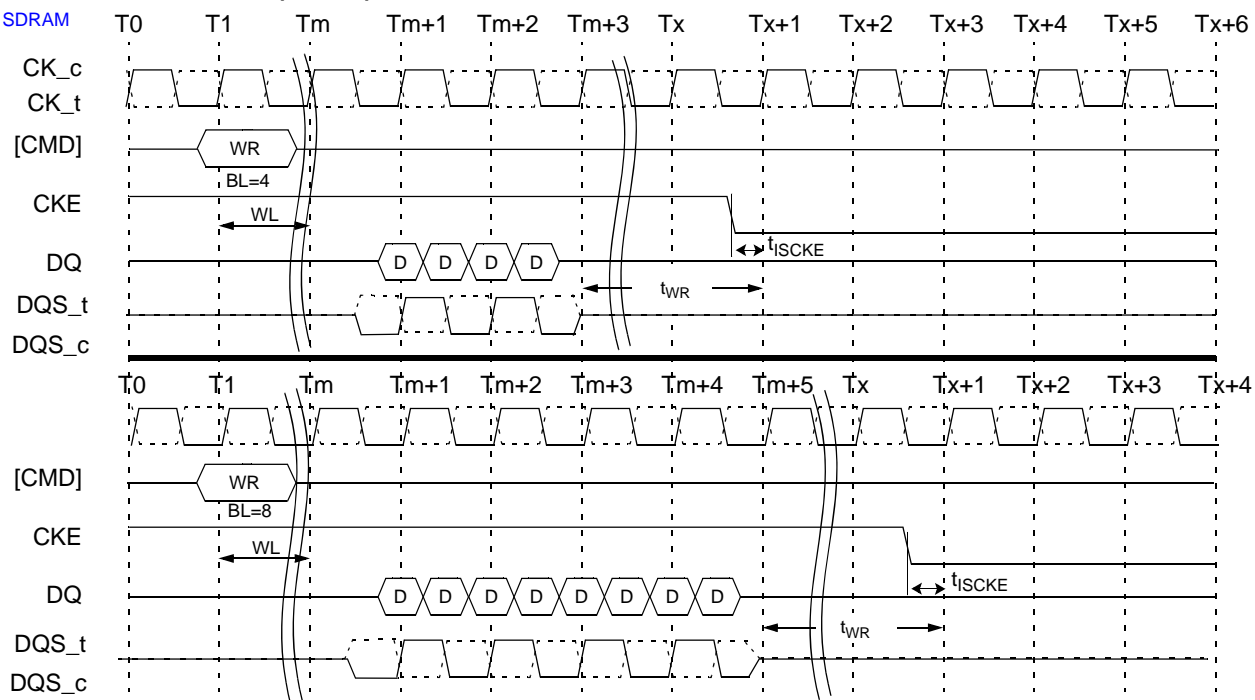


Figure 97 — Write to power-down entry

NOTE 1 CKE may be registered LOW  $WL + 1 + BL/2 + RU(t_{WR}/t_{CK})$  clock cycles after the clock on which the Write command is registered.

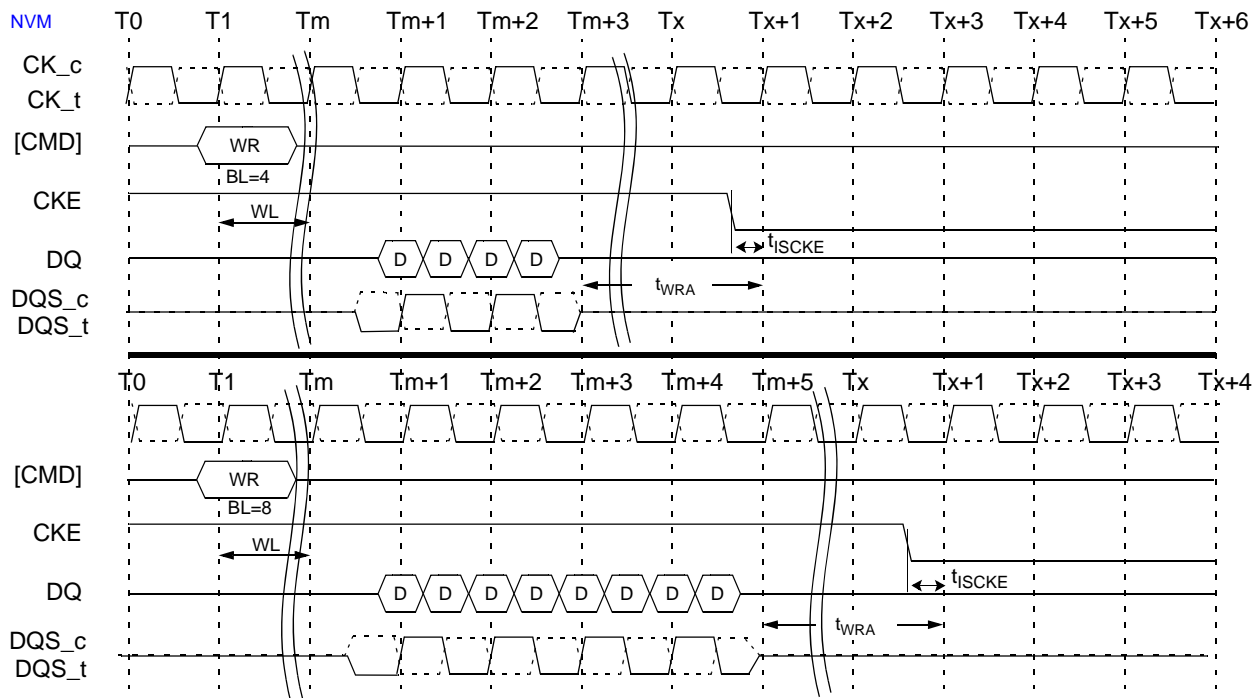
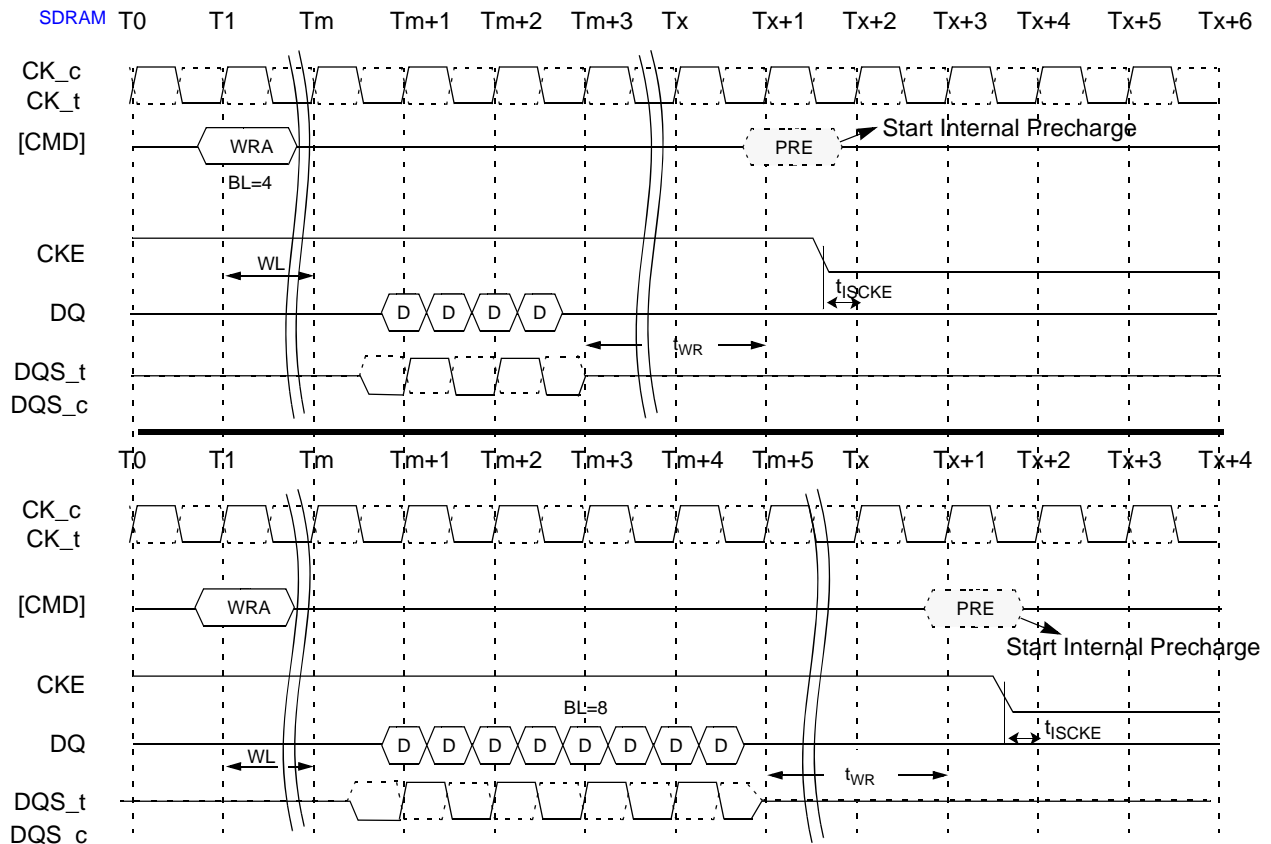


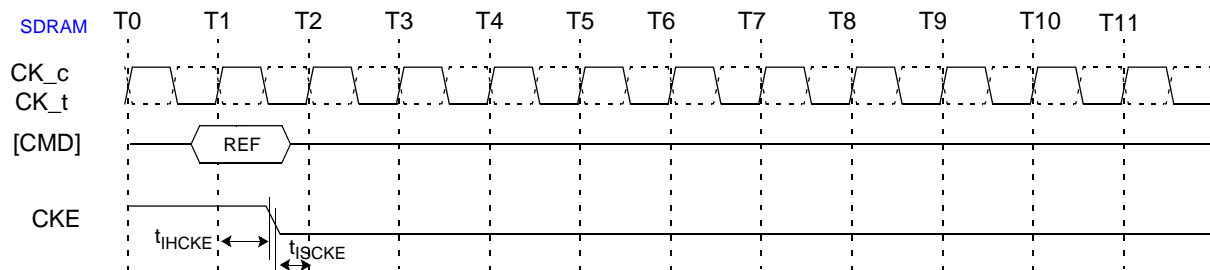
Figure 98 — Write to power-down entry

NOTE 1 CKE may be registered LOW  $WL + 1 + BL/2 + RU(t_{WRA}/t_{CK})$  clock cycles after the clock on which the Write command is registered.

## 5.14 Power-down (cont'd)



NOTE 1 CKE may be registered LOW  $WL + 1 + BL/2 + RU(t_{WR}/t_{CK}) + 1$  clock cycles after the Write command is registered.



NOTE 1 CKE may go LOW  $t_{IHCKE}$  after the clock on which the Refresh command is registered.

## 5.14 Power-down (cont'd)

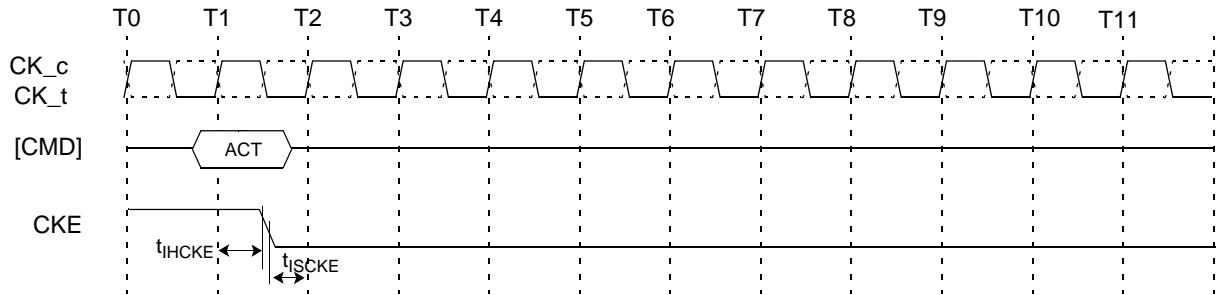


Figure 101 — Activate command to power-down entry

NOTE 1 CKE may go LOW  $t_{IHCKE}$  after the clock on which the Activate command is registered.

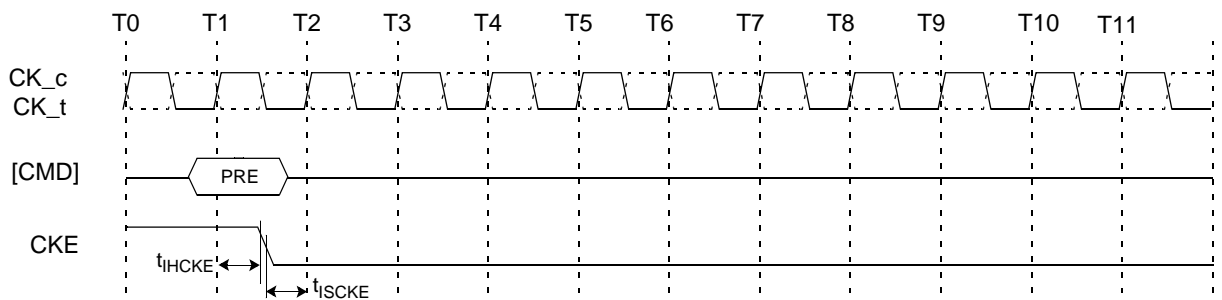


Figure 102 — Preactive/Precharge/Precharge-all command to power-down entry

NOTE 1 CKE may go LOW  $t_{IHCKE}$  after the clock on which the Preactive/Precharge/Precharge-All command is registered.

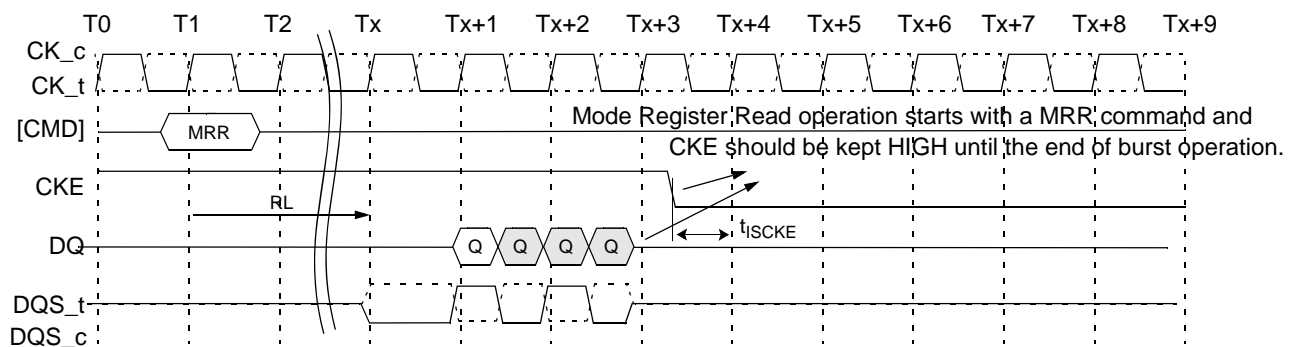
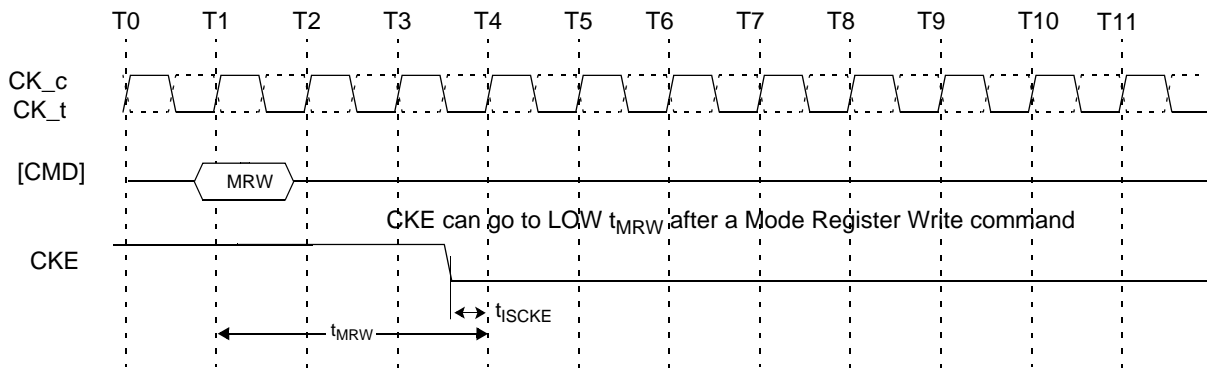


Figure 103 — Mode Register Read to power-down entry

NOTE 1 CKE may be registered LOW  $RL + RU(t_{DQSCK(MAX)}/t_{CK}) + 4/2 + 1$  clock cycles after the clock on which the Mode Register Read command is registered.

## 5.14 Power-down (cont'd)



**Figure 104 — MRW command to power-down entry**

NOTE 1 CKE may be registered LOW  $t_{MRW}$  after the clock on which the Mode Register Write command is

## 5.15 LPDDR2-SX: Deep Power-Down

Deep Power-Down is entered when CKE is registered LOW with CS\_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress.

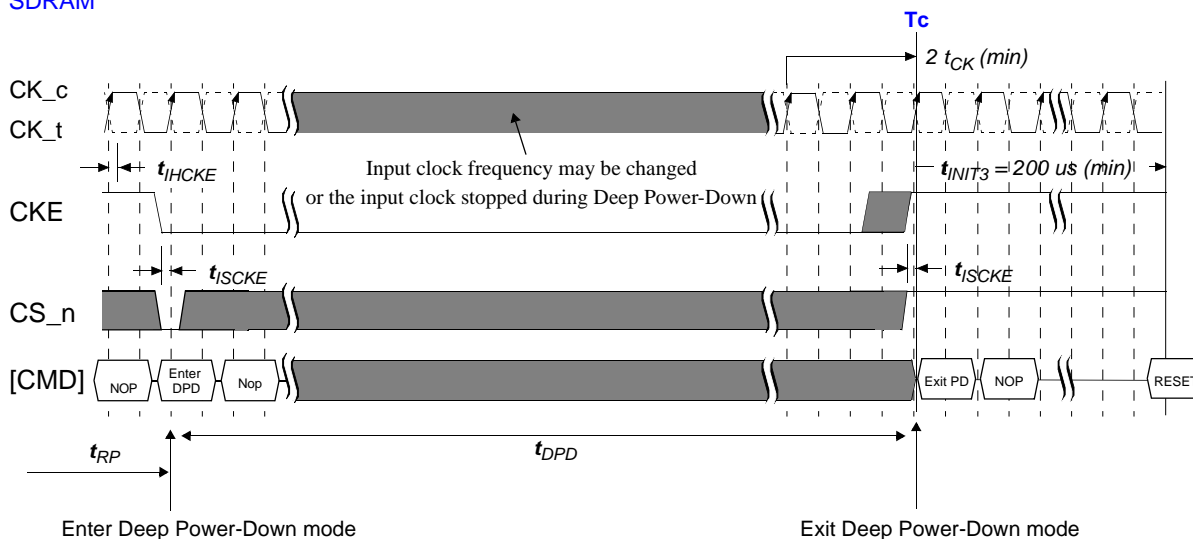
All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power-Down, CKE must be held LOW.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. All power supplies must be within specified limits prior to exiting Deep Power-Down. VrefDQ and VrefCA may be at any level within minimum and maximum levels (see 6.1). However prior to exiting Deep Power-Down, Vref must be within specified limits (see 7.1).

The contents of the SDRAM may be lost upon entry into Deep Power-Down mode.

The Deep Power-Down state is exited when CKE is registered HIGH, while meeting  $t_{ISCKE}$  with a stable clock input. The SDRAM must be fully re-initialized as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence.

### SDRAM



**Figure 105 — LPDDR2-SX: Deep power down entry and exit timing diagram**

NOTE 1 Initialization sequence may start at any time after  $T_c$ .

NOTE 2  $t_{INIT3}$  and  $T_c$  refer to timings in the LPDDR2 initialization sequence. For more detail, see 3.4.

NOTE 3 Input clock frequency may be changed or the input clock stopped during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.



## 5.16 Input clock stop and frequency change

LPDDR2 devices support input clock frequency change during CKE LOW under the following conditions:

- $t_{CK(ABS)min}$  is met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate, Preactive, or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions ( $t_{RCD}$ ,  $t_{RP}$ ) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE LOW under the following conditions:

- CK<sub>t</sub> is held LOW and CK<sub>c</sub> is held HIGH during clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Preactive, or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions ( $t_{RCD}$ ,  $t_{RP}$ ) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR2 devices support input clock frequency change during CKE HIGH under the following conditions:

- $t_{CK(ABS)min}$  is met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- Any Activate, Read, Write, Preactive, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions ( $t_{RCD}$ ,  $t_{WR}$ ,  $t_{WRA}$ ,  $t_{RP}$ ,  $t_{MRW}$ ,  $t_{MRR}$ , etc.) have been met prior to changing the frequency;
- CS<sub>n</sub> shall be held HIGH during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- The LPDDR2 device is ready for normal operation after the clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of  $2t_{CK} + t_{XP}$ .

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE HIGH under the following conditions:

- CK<sub>t</sub> is held LOW and CK<sub>c</sub> is held HIGH during clock stop;
- CS<sub>n</sub> shall be held HIGH during clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Read, Write, Preactive, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions ( $t_{RCD}$ ,  $t_{WR}$ ,  $t_{WRA}$ ,  $t_{RP}$ ,  $t_{MRW}$ ,  $t_{MRR}$ , etc.) have been met prior to stopping the clock;
- The LPDDR2 device is ready for normal operation after the clock is restarted and satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of  $2t_{CK} + t_{XP}$ .

### **5.17 No Operation command**

The purpose of the No Operation command (NOP) is to prevent the LPDDR2 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. CS\_n HIGH at the clock rising edge N.
2. CS\_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

### **5.18 Truth tables**

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

## 5.18.1 Command Truth Table

Table 60 — Command Truth Table

		SDR Command Pins			DDR CA pins (10)										
SDRAM Command	NVM Command	CKE		CS_N	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK_t EDGE
		CK_t(n-1)	CK_t(n)												
MRW	MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	
				X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	
MRR	MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	
				X	MA6	MA7	X								
Refresh (per bank) <sup>11</sup>	-	H	H	L	L	L	H	L	X						
				X	X										
Refresh (all bank)	-	H	H	L	L	L	H	H	X						
				X	X										
Enter Self Refresh	Enter Power Down	H	L	L	L	L	H	X							
		X		X											
Activate (bank)	Activate (row buffer)	H	H	L	L	H	R8/a15	R9/a16	R10/a17	R11/a18	R12/a19	BA0	BA1	BA2	
				X	R0/a5	R1/a6	R2/a7	R3/a8	R4/a9	R5/a10	R6/a11	R7/a12	R13/a13	R14/a14	
Write (bank)	Write (RDB)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	
				X	AP <sup>3,4</sup>	C3	C4	C5	C6	C7	C8	C9	C10	C11	
Read (bank)	Read (RDB)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	
				X	AP <sup>3,4</sup>	C3	C4	C5	C6	C7	C8	C9	C10	C11	
Precharge (pre bank, all bank)	Preactive (RAB)	H	H	L	H	H	L	H	AB/a30	X/a31	X/a32	BA0	BA1	BA2	
				X	X/a20	X/a21	X/a22	X/a23	X/a24	X/a25	X/a26	X/a27	X/a28	X/a29	
BST	BST	H	H	L	H	H	L	L	X						
				X	X										
Enter Deep Power Down	Enter Power Down	H	L	L	H	H	L	X							
		X		X											
NOP	NOP	H	H	L	H	H	H	X							
				X	X										
Maintain PD, SREF, DPD (NOP)	Maintain Power Down (NOP)	L	L	L	H	H	H	X							
				X	X										
NOP	NOP	H	H	H	X										
				X	X										
Maintain PD, SREF, DPD (NOP)	Maintain Power Down (NOP)	L	L	H	X										
				X	X										
Enter Power Down	Enter Power Down	H	L	H	X										
		X		X											
Exit PD, SREF, DPD	Exit Power Down	L	H	H	X										
		X		X											

**5.18.1 Command Truth Table (cont'd)**

Notes to [Table 60](#)

NOTE 1 All LPDDR2 commands are defined by states of CS<sub>n</sub>, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.

NOTE 2 For LPDDR2 SDRAM, Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For LPDDR2 NVM, BA0, BA1, BA2 determine a row buffer.

NOTE 3 AP is significant only to SDRAM. AP is do-not-care for NVM.

NOTE 4 AP “high” during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.

NOTE 5 “X” means “H or L (but a defined logic level)”

NOTE 6 Self refresh exit and Deep Power Down exit are asynchronous.

NOTE 7 VREF must be between 0 and VDDQ during Self Refresh and Deep Power Down operation.

NOTE 8 CA<sub>xr</sub> refers to command/address bit “x” on the rising edge of clock.

NOTE 9 CA<sub>xf</sub> refers to command/address bit “x” on the falling edge of clock.

NOTE 10 CS<sub>n</sub> and CKE are sampled at the rising edge of clock.

NOTE 11 Per Bank Refresh is only allowed in devices with 8 banks.

NOTE 12 The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

NOTE 13 AB “high” during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

## 5.19 LPDDR2-SDRAM Truth Tables

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the Banks.

**Table 61 — LPDDR2-SX: CKE Table**

Device Current State <sup>*3</sup>	CKE <sub>n-1</sub> <sup>*1</sup>	CKE <sub>n</sub> <sup>*1</sup>	CS <sub>n</sub> <sup>*2</sup>	Command n <sup>*4</sup>	Operation n <sup>*4</sup>	Device Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6, 9
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6, 9
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6, 9, 12
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7, 10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	
	H	L	L	Enter Self-Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Deep Power Down	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
	H	H	Refer to the Command Truth Table				

NOTE 1 “CKE<sub>n</sub>” is the logic state of CKE at clock rising edge n; “CKE<sub>n-1</sub>” was the state of CKE at the previous clock edge.

NOTE 2 “CS<sub>n</sub>” is the logic state of CS<sub>n</sub> at the clock rising edge n;

NOTE 3 “Current state” is the state of the LPDDR2 device immediately prior to clock edge n.

NOTE 4 “Command n” is the command registered at clock edge N, and “Operation n” is a result of “Command n”.

NOTE 5 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 6 Power Down exit time (t<sub>XP</sub>) should elapse before a command other than NOP is issued.

NOTE 7 Self-Refresh exit time (t<sub>XSR</sub>) should elapse before a command other than NOP is issued.

NOTE 8 The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.

NOTE 9 The clock must toggle at least twice during the t<sub>XP</sub> period.

NOTE 10 The clock must toggle at least twice during the t<sub>XSR</sub> time.

NOTE 11 ‘X’ means ‘Don’t care’.

NOTE 12 Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.

## 5.19 LPDDR2-SDRAM Truth Tables (cont'd)

**Table 62 — Current State Bank n - Command to Bank n**

Current State	Command	Operation	Next State	NOTES
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing(All Bank)	7
	MRW	Load value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	7, 8
	Precharge	Deactivate row in bank or banks	Precharging	9, 15
Row Active	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10, 11
	Write	Select column, and start write burst	Writing	10, 11, 12
	BST	Read burst terminate	Active	13
Writing	Write	Select column, and start new write burst	Writing	10, 11
	Read	Select column, and start read burst	Reading	10, 11, 14
	BST	Write burst terminate	Active	13
Power On	Reset	Begin Device Auto-Initialization	Resetting	7, 9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE 1 The table applies when both CKEn-1 and CKEn are HIGH, and after  $t_{XSR}$  or  $t_{XP}$  has been met if the previous state was Power Down.

NOTE 2 All states and sequences not shown are illegal or reserved.

NOTE 3 Current State Definitions:

Idle: The bank or banks have been precharged, and  $t_{RP}$  has been met.

Active: A row in the bank has been activated, and  $t_{RCD}$  has been met. No data bursts / accesses and no register accesses are in progress.

Reading: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

Writing: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

NOTE 4 The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and Table 2, and according to Table 3.

Precharging: starts with the registration of a Precharge command and ends when  $t_{RP}$  is met. Once  $t_{RP}$  is met, the bank will be in the idle state.

Row Activating: starts with registration of an Activate command and ends when  $t_{RCD}$  is met. Once  $t_{RCD}$  is met, the bank will be in the 'Active' state.

Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when  $t_{RP}$  has been met. Once  $t_{RP}$  has been met, the bank will be in the idle state.

Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when  $t_{RP}$  has been met. Once  $t_{RP}$  is met, the bank will be in the idle state.

## 5.19 LPDDR2-SDRAM Truth Tables (cont'd)

Notes (cont'd) to [Table 62](#)

NOTE 5 The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.

Refreshing (Per Bank): starts with registration of an Refresh (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.

Refreshing (All Bank): starts with registration of an Refresh (All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.

Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.

Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.

Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.

MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.

Precharging All: starts with the registration of a Precharge-All command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

NOTE 6 Bank-specific; requires that the bank is idle and no bursts are in progress.

NOTE 7 Not bank-specific; requires that all banks are idle and no bursts are in progress.

NOTE 8 Not bank-specific reset command is achieved through Mode Register Write command.

NOTE 9 This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.

NOTE 10 A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.

NOTE 11 The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.

NOTE 12 A Write command may be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.

NOTE 13 Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank.

NOTE 14 A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.

NOTE 15 If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

## 5.19 LPDDR2-SDRAM Truth Tables (cont'd)

**Table 63 — Current State Bank n - Command to Bank m**

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	NOTES
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	7
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	10, 11, 13
Reading (Autoprecharge disabled)	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8, 14
	Activate	Select and activate row in Bank m	Active	
Writing (Autoprecharge disabled)	Precharge	Deactivate row in bank or banks	Precharging	9
	Read	Select column, and start read burst from Bank m	Reading	8, 16
	Write	Select column, and start write burst to Bank m	Writing	8
	Activate	Select and activate row in Bank m	Active	
Reading with Autoprecharge	Precharge	Deactivate row in bank or banks	Precharging	9
	Read	Select column, and start read burst from Bank m	Reading	8, 15
	Write	Select column, and start write burst to Bank m	Writing	8, 14, 15
	Activate	Select and activate row in Bank m	Active	
Writing with Autoprecharge	Precharge	Deactivate row in bank or banks	Precharging	9
	Read	Select column, and start read burst from Bank m	Reading	8, 15, 16
	Write	Select column, and start write burst to Bank m	Writing	8, 15
	Activate	Select and activate row in Bank m	Active	
Power On	Reset	Begin Device Auto-Initialization	Resetting	12, 17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE 1 The table applies when both CKEn-1 and CKEn are HIGH, and after  $t_{XSR}$  or  $t_{XP}$  has been met if the previous state was Self Refresh or Power Down.

NOTE 2 All states and sequences not shown are illegal or reserved.

NOTE 3 Current State Definitions:

Idle: the bank has been precharged, and  $t_{RP}$  has been met.

Active: a row in the bank has been activated, and  $t_{RCD}$  has been met. No data bursts/accesses and no register accesses are in progress.

Reading: a Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

Writing: a Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

NOTE 4 Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.

NOTE 5 A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.



## 5.19 LPDDR2-SDRAM Truth Tables (cont'd)

Notes (cont'd) to [Table 63](#)

NOTE 6 The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:

Idle MR Reading: starts with the registration of a MRR command and ends when  $t_{MRR}$  has been met. Once  $t_{MRR}$  has been met, the bank will be in the Idle state.

Resetting MR Reading: starts with the registration of a MRR command and ends when  $t_{MRR}$  has been met. Once  $t_{MRR}$  has been met, the bank will be in the Resetting state.

Active MR Reading: starts with the registration of a MRR command and ends when  $t_{MRR}$  has been met. Once  $t_{MRR}$  has been met, the bank will be in the Active state.

MR Writing: starts with the registration of a MRW command and ends when  $t_{MRW}$  has been met. Once  $t_{MRW}$  has been met, the bank will be in the Idle state.

NOTE 7  $t_{RRD}$  must be met between Activate command to Bank n and a subsequent Activate command to Bank m.

NOTE 8 Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.

NOTE 9 This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.

NOTE 10 MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when  $t_{RCD}$  is met.)

NOTE 11 MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when  $t_{RP}$  is met.)

NOTE 12 Not bank-specific; requires that all banks are idle and no bursts are in progress.

NOTE 13 The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon  $t_{RCD}$  and  $t_{RP}$  respectively.

NOTE 14 A Write command may be applied after the completion of the Read burst, otherwise a BST must be issued to end the Read prior to asserting a Write command.

NOTE 15 Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions in [Table 51 on page 116](#) and [Table 52 on page 117](#) are followed.

NOTE 16 A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.

NOTE 17 Reset command is achieved through Mode Register Write command.

NOTE 18 BST is allowed only if a Read or Write burst is ongoing.

## 5.20 LPDDR2-N: Truth Tables

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the Row Buffers.

Table 64 describes Power Down transitions for a LPDDR2-NVM. If the Enter Power Down command is issued when all Row Buffers are Idle the device goes into the Idle Power Down state. However, if the Enter Power Down command is issued when one or more Row Buffers are Active, the device goes into the Active Power Down state. CKE shall be held low to maintain the Power Down state. When CKE is driven high with CS\_n high the device exits the Power Down State. For additional details on entering and exiting power down, please refer to 5.14.

**Table 64 — LPDDR2-N: CKE Table**

Row Buffer Current State <sup>*3</sup>		Device Current State <sup>*4</sup>	CKE <sub>n-1</sub> <sup>*1</sup>	CKE <sub>n</sub> <sup>*1</sup>	CS_n <sup>*2</sup>	Command n <sup>*5</sup>	Operation n <sup>*5</sup>	Row Buffer Next State	Device Next State	Notes
All	Resetting	Resetting	H	L	X	ENTER POWER DOWN	Enter in Resetting Power Down	Resetting Power Down	Resetting Power Down	10
All	Idle	Idle	H	L	X	ENTER POWER DOWN	Enter in Idle Power Down	Idle Power Down	Idle Power Down	10
RB <sub>j</sub>	Active	Not Power Down	H	L	X	ENTER POWER DOWN	Enter in Active Power Down	Active Power Down	Active Power Down	10,11
RB <sub>k</sub>	Idle							Idle Power Down		
All	Resetting Power Down	Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	Resetting Power Down	9
All	Idle Power Down	Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	Idle Power Down	9
RB <sub>j</sub>	Active Power Down	Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	Active Power Down	9,11
RB <sub>k</sub>	Idle Power Down							Idle Power Down		
All	Resetting Power Down	Resetting Power Down	L	H	H	EXIT POWER DOWN	Exit Resetting Power Down	Resetting	Resetting	7,8
All	Idle Power Down	Idle Power Down	L	H	H	EXIT POWER DOWN	Exit Idle Power Down	Idle	Idle	7,8
RB <sub>j</sub>	Active Power Down	Active Power Down	L	H	H	EXIT POWER DOWN	Exit Active Power Down	Active	Not Power Down	7,8,11
RB <sub>k</sub>	Idle Power Down							Idle		

NOTE 1 “CKE<sub>n</sub>” is the logic state of CKE at clock rising edge n; “CKE<sub>n-1</sub>” was the state of CKE at the previous clock rising edge.

NOTE 2 “CS\_n” is the logic state of CS\_n at clock rising edge n;

NOTE 3 “Row Buffer Current State” is the state of a particular Row Buffer immediately prior to clock cycle n.

NOTE 4 “Device Current State” is the state of LPDDR2-NVM immediately prior to clock cycle n.

NOTE 5 “Command n” is the command registered at clock cycle n, and “Operation n” is the result of “Command n”.

NOTE 6 All states and sequences not shown are illegal or reserved, unless explicitly described elsewhere in this standard.

NOTE 7 Power Down exit time (t<sub>XP</sub>) should elapse before a command other than NOP is issued.

NOTE 8 The clock must toggle at least twice during the t<sub>XP</sub> period.

NOTE 9 Clock frequency may be reduced, and/or the clock may be stopped, during ‘Idle Power Down’, ‘Resetting Power Down’, or ‘Active Power Down’ states.

NOTE 10 Power Down may not be entered while Read, Write, Mode Register Read, Mode Register Write, or Preactive operations are in progress. A Power Down command shall be followed by a NOP command.

NOTE 11 RB<sub>j</sub> and RB<sub>k</sub> refer to different Row Buffer pairs, (j) and (k).

**5.20 LPDDR2-N: Truth Tables (cont'd)**

Table 65 shows the transition from the current state to the next state of a given Row Buffer due to command issued on the same Row Buffer.

Only allowed commands are shown, all other commands are illegal or reserved for the given Row Buffer state.

For the state definition refer to section LPDDR2-NVM state diagram.

**Table 65 — Current State Row Buffer n - Command to Row Buffer n**

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current State	
Idle	PREACTIVE	Load RAB	Preactivating	
	ACTIVATE	Select RAB & RDB, and activate RDB	Active	
	MRW	Load value to Mode Register	MR Writing	
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	6
Active	PREACTIVE	Load RAB	Preactivating	
	ACTIVATE	Select RAB & RDB, and activate RDB	Active	7
	READ	Select RDB & column, and start read burst	Reading	
	WRITE	Select RDB & column, and start write burst	Writing	
	MRW	Load value to Mode Register	MR Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	6
Reading	READ	Select RDB & column, and start new read burst	Reading	
	BST	Read burst terminate	Active	4
Writing	BST	Write burst terminate	Active	4
	WRITE	Select RDB & column, and start new write burst	Writing	
Power On	Reset	Begin Device Auto-Initialization	Resetting	6
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE 1 The table applies when both CKEn-1 and CKEn are HIGH, and after  $t_{XP}$  has been met if the previous state was Power Down.

NOTE 2 The following states must not be interrupted by a command issued to the same Row Buffer. NOP commands or allowable commands to other Row Buffer should be issued on any clock cycle occurring during these states.

Preactivating: starts with the registration of a Preactive command and ends when  $t_{RP}$  is met. The Row Buffer will return to the Idle state once  $t_{RP}$  is satisfied and any ongoing Read or Write operation is complete.

Row Activating: starts with registration of an Activate command and ends when  $t_{RCD}$  is met. Once  $t_{RCD}$  is met, the Row Buffer will be in the Row Active state.

NOTE 3 The following states must not be interrupted by any executable command; NOP commands must be applied to each clock cycle during these states.

Idle MR Reading: starts with the registration of a MRR command and ends when  $t_{MRR}$  has been met. Once  $t_{MRR}$  has been met, the Row Buffer will be in the Idle state.

Resetting MR Reading: starts with the registration of a MRR command and ends when  $t_{MRR}$  has been met. Once  $t_{MRR}$  has been met, the Row Buffer will be in the Resetting state.

Active MR Reading: starts with the registration of a MRR command and ends when  $t_{MRR}$  has been met. Once  $t_{MRR}$  has been met, the Row Buffer will be in the Active state.

MR Writing: starts with the registration of a MRW command and ends when  $t_{MRW}$  has been met. Once  $t_{MRW}$  has been met, the Row Buffer will be in the Idle state.

NOTE 4 BURST TERMINATE command affects the read/write burst started by the most recent READ/WRITE command.

NOTE 5 Reset command is achieved through MODE REG. WRITE command. Reset command sets all Row Address Buffers to 0x0000.

NOTE 6  $t_{RC}$  must be met between Activate command to Row Buffer n and subsequent Activate command to Row Buffer n.

## 5.20 LPDDR2-N: Truth Tables (cont'd)

Given the state of a Row Buffer (n), Table 66 shows allowed commands to another Row Buffer (m), and the corresponding next state. Only allowed commands are shown, all other commands are illegal or reserved for the given Row Buffer state, unless explicitly described elsewhere in this standard.

For the state definition refer to section LPDDR2-NVM state diagram.

**Table 66 — Current State Row Buffer n - Command to Row Buffer m**

Current State of Row Buffer n	Command for Row Buffer m	Operation	Next State for Row Buffer m	Notes
Any	NOP	Continue previous operation	Current State of Row Buffer m	
Idle	Any	Any command allowed to Row Buffer m	-	9
Row Activating, Active, or Preactivating	ACTIVATE	Select RABm & RDBm, and activate row in RDB m	Active	5
	READ	Select RDBm & column, and start read burst from RDBm	Reading	
	BST	Read or Write burst terminate an ongoing Read/Write from/to Row Buffer m	Active	3, 9
	WRITE	Select RDBm & column, and start write burst to RDBm	Writing	
	PREACTIVE	Load RABm	Preactivating	
	MRW	Load value to Mode Register	MR Writing	6, 7
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	6, 7, 8
	Reset	Begin Device Auto-Initialization	Resetting	4
Reading	READ	Select RDBm & column, and start read burst from RDBm	Reading	
	ACTIVATE	Select RABm & RDBm, and activate row in RDB m	Active	
	PREACTIVE	Load RABm	Preactivating	
Writing	WRITE	Select RDBm & column, and start write burst to RDBm	Writing	
	ACTIVATE	Select RABm & RDBm, and activate row in RDB m	Active	
	PREACTIVE	Load RABm	Preactivating	
Power On	Reset	Begin Device Auto-Initialization	Resetting	4
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE 1 The table applies when both CKEn-1 and CKEn are HIGH, and after  $t_{XP}$  has been met if the previous state was Power Down.

NOTE 2 The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:

Idle MR Reading: starts with the registration of a MRR command and ends when  $t_{MRR}$  has been met. Once  $t_{MRR}$  has been met, the Row Buffer will be in the Idle state.

Resetting MR Reading: starts with the registration of a MRR command and ends when  $t_{MRR}$  has been met. Once  $t_{MRR}$  has been met, the Row Buffer will be in the Resetting state.

Active MR Reading: starts with the registration of a MRR command and ends when  $t_{MRR}$  has been met. Once  $t_{MRR}$  has been met, the Row Buffer will be in the Active state.

MR Writing: starts with the registration of a MRW command and ends when  $t_{MRW}$  has been met. Once  $t_{MRW}$  has been met, all Row Buffers will be in the Idle state.

NOTE 3 BURST TERMINATE command affects the read/write burst started by the most recent READ/WRITE command.

NOTE 4 Reset command is achieved through MODE REGISTER WRITE command. Reset command sets all Row Address Buffers to 0x0000.

NOTE 5  $t_{RRD}$  must be met between Activate command to Row Buffer n and a subsequent Activate command to Row Buffer m.

NOTE 6 MRR is allowed during the Row Activating state and MRW is prohibited during the Row Activating state. (Row Activating starts with registration of an Activate command and ends when  $t_{RCD}$  is met.)

NOTE 7 MRR is allowed during the Preactivating state and MRW is prohibited during the Preactivating state. (Preactivating starts with registration of an Preactivate command and ends when  $t_{RP}$  is met.)

NOTE 8 The next state for Row Buffer m depends on the current state of Row Buffer m (Idle, Row Activating, or Active). Note that the state may be in transition when a MRR is issued. Therefore, if Row Buffer m is in the Row Activating state, the next state may be Active dependent upon  $t_{RCD}$ .

NOTE 9 BST is allowed only if a Read or Write burst is ongoing.

## 5.21 Data Mask Truth Table

Table 67 provides the data mask truth table.

**Table 67 — DM truth table**

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

NOTE 1 Used to mask write data, provided coincident with the corresponding data.

## 6 Absolute Maximum Ratings

### 6.1 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 68 — Absolute Maximum DC Ratings**

Parameter	Symbol	Min	Max	Units	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	2
VDD2 supply voltage relative to VSS	VDD2 (1.35V)	-0.4	1.8	V	2
	VDD2 (1.2V)	-0.4	1.6	V	2
VDDCA supply voltage relative to VSSCA	VDDCA	-0.4	1.6	V	2,4
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	2,3
VACC supply voltage relative to VSS	VACC (9V)	-0.4	11.5	V	6
	VACC (VAP)	-0.4	7	V	
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	T <sub>STG</sub>	-55	125	°C	5

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

NOTE 2 See “Power-Ramp” in 3.4 for relationships between power supplies.

NOTE 3  $V_{REFDQ} \leq 0.6 \times V_{DDQ}$ ; however,  $V_{REFDQ}$  may be  $\geq V_{DDQ}$  provided that  $V_{REFDQ} \leq 300\text{mV}$ .

NOTE 4  $V_{REFCA} \leq 0.6 \times V_{DDCA}$ ; however,  $V_{REFCA}$  may be  $\geq V_{DDCA}$  provided that  $V_{REFCA} \leq 300\text{mV}$ .

NOTE 5 Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 6 Refer to vendor datasheet for VACC absolute maximum value.

**7 AC & DC Operating Conditions**

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

**7.1 Recommended DC Operating Conditions****Table 69 — Recommended LPDDR2-S2 DC Operating Conditions**

Symbol	LPDDR2-S2A			LPDDR2-S2B			DRAM	Unit
	Min	Typ	Max	Min	Typ	Max		
VDD1	1.70	1.80	1.95	1.70	1.80	1.95	Core Power1	V
VDD2	N/A	N/A	N/A	1.14	1.20	1.3	Core Power2	V
VDDCA	1.14	1.20	1.3	1.14	1.20	1.3	Input Buffer Power	V
VDDQ	1.14	1.20	1.3	1.14	1.20	1.3	I/O Buffer Power	V

NOTE 1 When VDD2 is used, VDD1 uses significantly less current than VDD2

N/A(Not available)

**Table 70 — Recommended LPDDR2-S4 DC Operating Conditions**

Symbol	LPDDR2-S4A			LPDDR2-S4B			DRAM	Unit
	Min	Typ	Max	Min	Typ	Max		
VDD1	1.70	1.80	1.95	1.70	1.80	1.95	Core Power1	V
VDD2	1.28	1.35	1.42	1.14	1.20	1.3	Core Power2	V
VDDCA	1.14	1.20	1.3	1.14	1.20	1.3	Input Buffer Power	V
VDDQ	1.14	1.20	1.3	1.14	1.20	1.3	I/O Buffer Power	V

NOTE 1 VDD1 uses significantly less power than VDD2

**Table 71 — Recommended LPDDR2-N DC Operating Conditions**

Symbol	Voltage LPDDR2-N-A			LPDDR2-N-B			NVMem	Unit
	Min	Typ	Max	Min	Typ	Max		
VDD1	1.7	1.8	1.95	1.7	1.8	1.95	Core Power	V
VDD2	N/A	N/A	N/A	1.14	1.2	1.3	Core Power 2	V
VDDCA	1.14	1.2	1.3	1.14	1.2	1.3	Input Buffer Power	V
VDDQ	1.14	1.2	1.3	1.14	1.2	1.3	I/O Buffer Power	V
VACC <sup>(3)</sup>	-0.4	0.0	0.4	-0.4	0.0	0.4	Lockout Voltage	V
	1.7	1.8	1.95	1.7	1.8	1.95	Normal Operation	V
	8.5	9	9.5	8.5	9	9.5	Acceleration Power	V
	VAP-0.4V	VAP	VAP+0.4V	VAP-0.4V	VAP	VAP+0.4V		

NOTE 1 When VACC is in the lockout voltage range, program and erase functions are disabled and will not be executed. The lockout voltage range provides hardware program and erase protection for the LPDDR2-NVM array.

NOTE 2 The maximum time for the device to be in the Acceleration Power range for VACC is 80 hours.

NOTE 3 Refer to vendor datasheet for VACC acceleration power supply value and VAP value. VAP shall not be less than 3.3V.

## 7.2 Input Leakage Current

**Table 72 — Input Leakage Current**

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current For CA, CKE, CS_n, CK_t, CK_c Any input $0V \leq V_{IN} \leq V_{DDCA}$ (All other pins not under test = 0V)	$I_L$	-2	2	$\mu A$	2
$V_{REF}$ supply leakage current $V_{REFDQ} = V_{DDQ}/2$ or $V_{REFCA} = V_{DDCA}/2$ (All other pins not under test = 0V)	$I_{VREF}$	-1	1	$\mu A$	1

NOTE 1 The minimum limit requirement is for testing purposes. The leakage current on  $V_{REFCA}$  and  $V_{REFDQ}$  pins should be minimal.

NOTE 2 Although DM is for input only, the DM leakage shall match the DQ and DQS\_t/DQS\_c output leakage specification.

## 7.3 Operating Temperature Range

**Table 73 — Operating Temperature Range**

Parameter/Condition	Symbol	Min	Max	Unit
Standard	$T_{OPER}$	-25	85	$^{\circ}C$
Extended		85	105	$^{\circ}C$

NOTE 1 Operating Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 2 Some applications require operation of LPDDR2 in the maximum temperature conditions in the Extended Temperature Range between 85  $^{\circ}C$  and 105  $^{\circ}C$  case temperature. For LPDDR2 devices, some derating is necessary to operate in this range. See [MR4](#).

NOTE 3 Either the device case temperature rating or the temperature sensor (see [5.12.1](#)) may be used to set an appropriate refresh rate (SDRAM), determine the need for AC timing de-rating (SDRAM and NVM) and/or monitor the operating temperature (SDRAM and NVM). When using the temperature sensor, the actual device case temperature may be higher than the  $T_{OPER}$  rating that applies for the Standard or Extended Temperature Ranges. For example,  $T_{CASE}$  may be above 85  $^{\circ}C$  when the temperature sensor indicates a temperature of less than 85  $^{\circ}C$ .



## 8 AC and DC Input Measurement Levels

### 8.1 AC and DC Logic Input Levels for Single-Ended Signals

#### 8.1.1 AC and DC Input Levels for Single-Ended CA and CS\_n Signals

Table 74 — Single-Ended AC and DC Input Levels for CA and CS\_n Inputs

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IHCA}(AC)$	AC input logic high	$V_{ref} + 0.220$	Note 2	$V_{ref} + 0.300$	Note 2	V	1, 2
$V_{ILCA}(AC)$	AC input logic low	Note 2	$V_{ref} - 0.220$	Note 2	$V_{ref} - 0.300$	V	1, 2
$V_{IHCA}(DC)$	DC input logic high	$V_{ref} + 0.130$	VDDCA	$V_{ref} + 0.200$	VDDCA	V	1
$V_{ILCA}(DC)$	DC input logic low	VSSCA	$V_{ref} - 0.130$	VSSCA	$V_{ref} - 0.200$	V	1
$V_{RefCA}(DC)$	Reference Voltage for CA and CS_n inputs	$0.49 * VDDCA$	$0.51 * VDDCA$	$0.49 * VDDCA$	$0.51 * VDDCA$	V	3, 4

NOTE 1 For CA and CS\_n input only pins.  $V_{ref} = V_{RefCA}(DC)$ .

NOTE 2 See 9.5

NOTE 3 The ac peak noise on  $V_{RefCA}$  may not allow  $V_{RefCA}$  to deviate from  $V_{RefCA}(DC)$  by more than +/-1% VDDCA (for reference: approx. +/- 12 mV).

NOTE 4 For reference: approx. VDDCA/2 +/- 12 mV.

#### 8.1.2 AC and DC Input Levels for CKE

Table 75 — Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IHCKE}$	CKE Input High Level	$0.8 * VDDCA$	Note 1	V	1
$V_{ILCKE}$	CKE Input Low Level	Note 1	$0.2 * VDDCA$	V	1
Note 1 See 9.5					

#### 8.1.3 AC and DC Input Levels for Single-Ended Data Signals

Table 76 — Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IHDQ}(AC)$	AC input logic high	$V_{ref} + 0.220$	Note 2	$V_{ref} + 0.300$	Note 2	V	1, 2, 5
$V_{ILDQ}(AC)$	AC input logic low	Note 2	$V_{ref} - 0.220$	Note 2	$V_{ref} - 0.300$	V	1, 2, 5
$V_{IHDQ}(DC)$	DC input logic high	$V_{ref} + 0.130$	VDDQ	$V_{ref} + 0.200$	VDDQ	V	1
$V_{ILDQ}(DC)$	DC input logic low	VSSQ	$V_{ref} - 0.130$	VSSQ	$V_{ref} - 0.200$	V	1
$V_{RefDQ}(DC)$	Reference Voltage for DQ, DM inputs	$0.49 * VDDQ$	$0.51 * VDDQ$	$0.49 * VDDQ$	$0.51 * VDDQ$	V	3, 4

NOTE 1 For DQ input only pins.  $V_{ref} = V_{RefDQ}(DC)$ .

NOTE 2 See 9.5

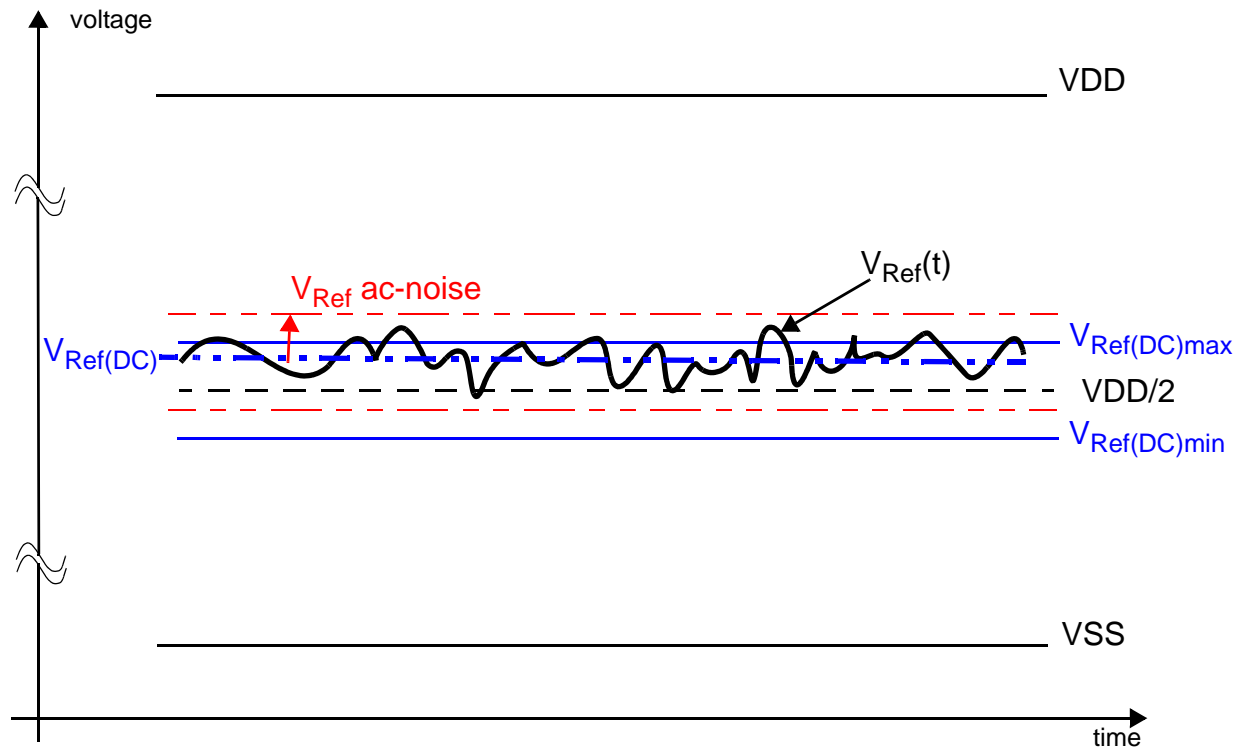
NOTE 3 The ac peak noise on  $V_{RefDQ}$  may not allow  $V_{RefDQ}$  to deviate from  $V_{RefDQ}(DC)$  by more than +/-1% VDDQ (for reference: approx. +/- 12 mV).

NOTE 4 For reference: approx. VDDQ/2 +/- 12 mV.

## 8.2 Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages  $V_{\text{RefCA}}$  and  $V_{\text{RefDQ}}$  are illustrated in Figure 106. It shows a valid reference voltage  $V_{\text{Ref}}(t)$  as a function of time. ( $V_{\text{Ref}}$  stands for  $V_{\text{RefCA}}$  and  $V_{\text{RefDQ}}$  likewise). VDD stands for VDDCA for  $V_{\text{RefCA}}$  and VDDQ for  $V_{\text{RefDQ}}$ .  $V_{\text{Ref}}(\text{DC})$  is the linear average of  $V_{\text{Ref}}(t)$  over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VDDQ or VDDCA also over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 74. Furthermore  $V_{\text{Ref}}(t)$  may temporarily deviate from  $V_{\text{Ref}}(\text{DC})$  by no more than  $\pm 1\%$  VDD.  $V_{\text{ref}}(t)$  cannot track noise on VDDQ or VDDCA if this would send  $V_{\text{ref}}$  outside these specifications.

:



**Figure 106 — Illustration of  $V_{\text{Ref}}(\text{DC})$  tolerance and  $V_{\text{Ref}}$  ac-noise limits**

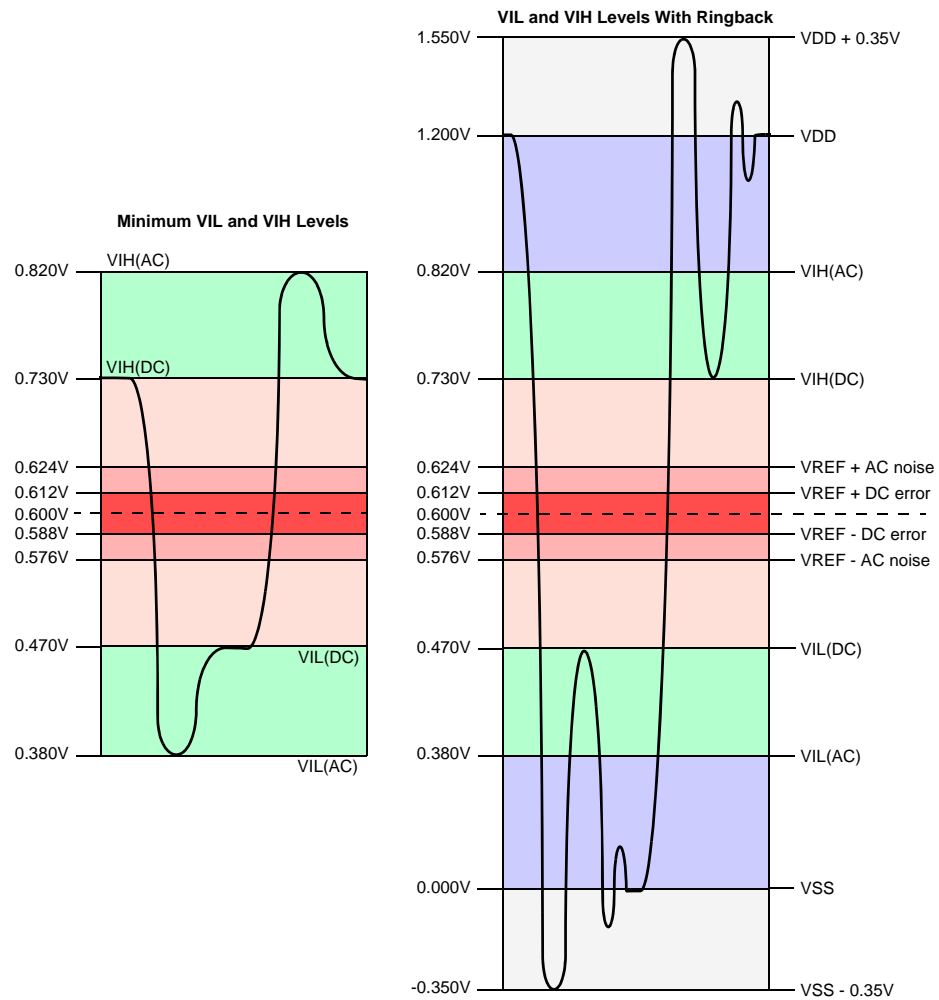
The voltage levels for setup and hold time measurements  $V_{\text{IH(AC)}}$ ,  $V_{\text{IH(DC)}}$ ,  $V_{\text{IL(AC)}}$  and  $V_{\text{IL(DC)}}$  are dependent on  $V_{\text{Ref}}$ .

“ $V_{\text{Ref}}$ ” shall be understood as  $V_{\text{Ref}}(\text{DC})$ , as defined in Figure 106.

This clarifies that dc-variations of  $V_{\text{Ref}}$  affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. Devices will function correctly with appropriate timing deratings with  $V_{\text{REF}}$  outside these specified levels so long as  $V_{\text{REF}}$  is maintained between  $0.44 \times V_{\text{DDQ}}$  (or  $V_{\text{DDCA}}$ ) and  $0.56 \times V_{\text{DDQ}}$  (or  $V_{\text{DDCA}}$ ) and so long as the controller achieves the required single-ended AC and DC input levels from instantaneous  $V_{\text{REF}}$  (see Table 74 and Table 76.) Therefore, system timing and voltage budgets need to account for  $V_{\text{REF}}$  deviations outside of this range.

This also clarifies that the LPDDR2 setup/hold specification and derating values need to include time and voltage associated with  $V_{\text{Ref}}$  ac-noise. Timing and voltage effects due to ac-noise on  $V_{\text{Ref}}$  up to the specified limit ( $\pm 1\%$  of VDD) are included in LPDDR2 timings and their associated deratings.

### 8.3 Input Signal

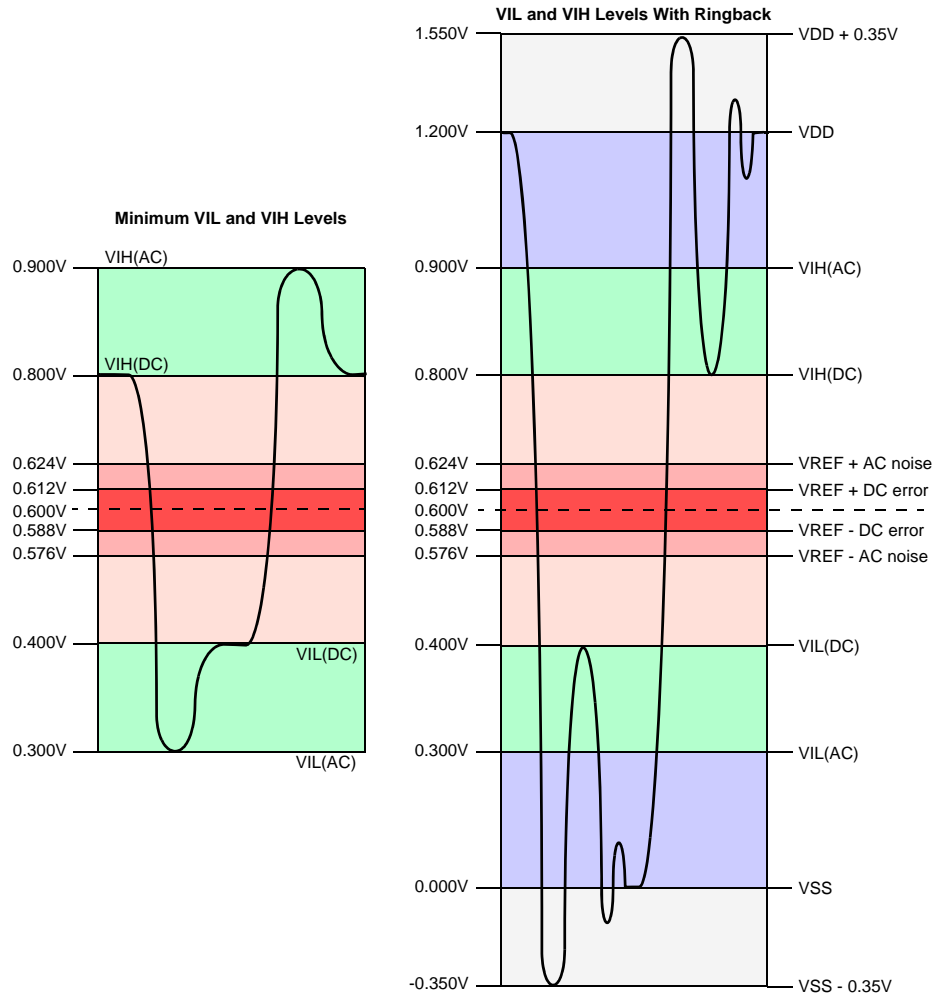


**Figure 107 — LPDDR2-466 to LPDDR2-1066 Input Signal**

NOTE 1 Numbers reflect nominal values.

NOTE 2 For CA0-9, CK\_t, CK\_c, and CS\_n, VDD stands for VDDCA. For DQ, DM/DNV, DQS\_t, and DQS\_c, VDD stands for VDDQ.

NOTE 3 For CA0-9, CK\_t, CK\_c, and CS\_n, VSS stands for VSSCA. For DQ, DM/DNV, DQS\_t, and DQS\_c, VSS stands for VSSQ.



**Figure 108 — LPDDR2-200 to LPDDR2-400 Input Signal**

NOTE 1 Numbers reflect nominal values

NOTE 2 For CA0-9, CK<sub>t</sub>, CK<sub>c</sub>, and CS<sub>n</sub>, VDD stands for VDDCA. For DQ, DM/DNV, DQS<sub>t</sub>, and DQS<sub>c</sub>, VDD stands for VDDQ.

NOTE 3 For CA0-9, CK<sub>t</sub>, CK<sub>c</sub>, and CS<sub>n</sub>, VSS stands for VSSCA. For DQ, DM/DNV, DQS<sub>t</sub>, and DQS<sub>c</sub>, VSS stands for VSSQ.

## 8.4 AC and DC Logic Input Levels for Differential Signals

### 8.4.1 Differential signal definition

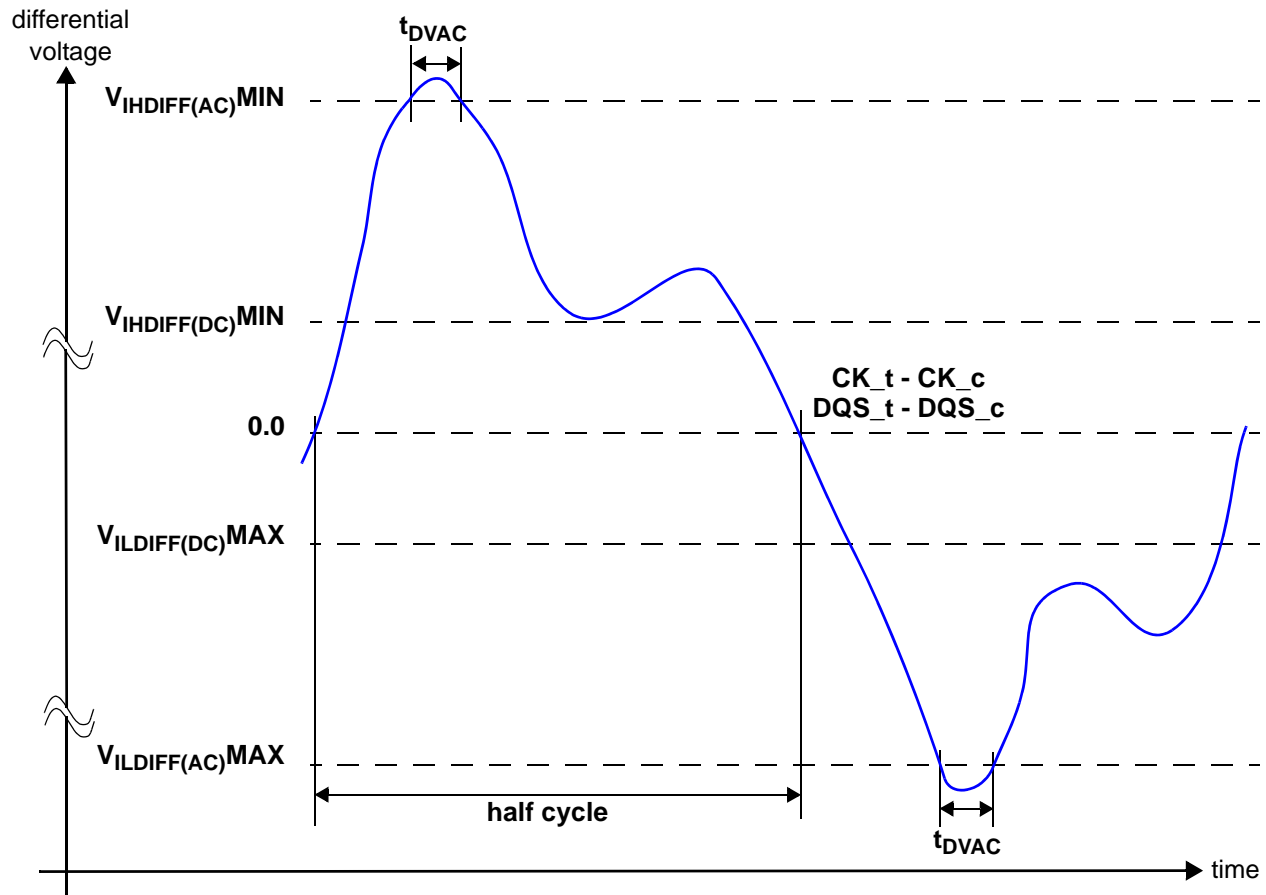


Figure 109 — Definition of differential ac-swing and “time above ac-level”  $t_{DVAC}$

### 8.4.2 Differential swing requirements for clock (CK<sub>t</sub> - CK<sub>c</sub>) and strobe (DQS<sub>t</sub> - DQS<sub>c</sub>)

Table 77 — Differential AC and DC Input Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IHdiff(dc)}$	Differential input high	$2 \times (V_{IH}(dc) - V_{ref})$	note 3	$2 \times (V_{IH}(dc) - V_{ref})$	note 3	V	1
$V_{ILdiff(dc)}$	Differential input low	Note 3	$2 \times (V_{IL}(dc) - V_{ref})$	Note 3	$2 \times (V_{IL}(dc) - V_{ref})$	V	1
$V_{IHdiff(ac)}$	Differential input high ac	$2 \times (V_{IH}(ac) - V_{ref})$	Note 3	$2 \times (V_{IH}(ac) - V_{ref})$	Note 3	V	2
$V_{ILdiff(ac)}$	Differential input low ac	note 3	$2 \times (V_{IL}(ac) - V_{ref})$	note 3	$2 \times (V_{IL}(ac) - V_{ref})$	V	2

NOTE 1 Used to define a differential signal slew-rate. For CK<sub>t</sub> - CK<sub>c</sub> use  $V_{IH}/V_{IL}(dc)$  of CA and VREFCA; for DQS<sub>t</sub> - DQS<sub>c</sub>, use  $V_{IH}/V_{IL}(dc)$  of DQs and VREFDQ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.

NOTE 2 For CK<sub>t</sub> - CK<sub>c</sub> use  $V_{IH}/V_{IL}(ac)$  of CA and VREFCA; for DQS<sub>t</sub> - DQS<sub>c</sub>, use  $V_{IH}/V_{IL}(ac)$  of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

NOTE 3 These values are not defined, however the single-ended signals CK<sub>t</sub>, CK<sub>c</sub>, DQS<sub>t</sub>, and DQS<sub>c</sub> need to be within the respective limits ( $V_{IH}(dc)$  max,  $V_{IL}(dc)$  min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to 9.5.

NOTE 4 For CK<sub>t</sub> and CK<sub>c</sub>,  $V_{ref} = V_{refCA}(DC)$ . For DQS<sub>t</sub> and DQS<sub>c</sub>,  $V_{ref} = V_{refDQ}(DC)$ .

**8.4.2 Differential swing requirements for clock (CK<sub>t</sub> - CK<sub>c</sub>) and strobe (DQS<sub>t</sub> - DQS<sub>c</sub>) (cont'd)**

**Table 78 — Allowed time before ringback (tDVAC) for CK<sub>t</sub> - CK<sub>c</sub> and DQS<sub>t</sub> - DQS<sub>c</sub>**

Slew Rate [V/ns]	tDVAC [ps] @  VIH/Ldiff(ac)  = 440mV	tDVAC [ps] @  VIH/Ldiff(ac)  = 600mV
	min	min
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

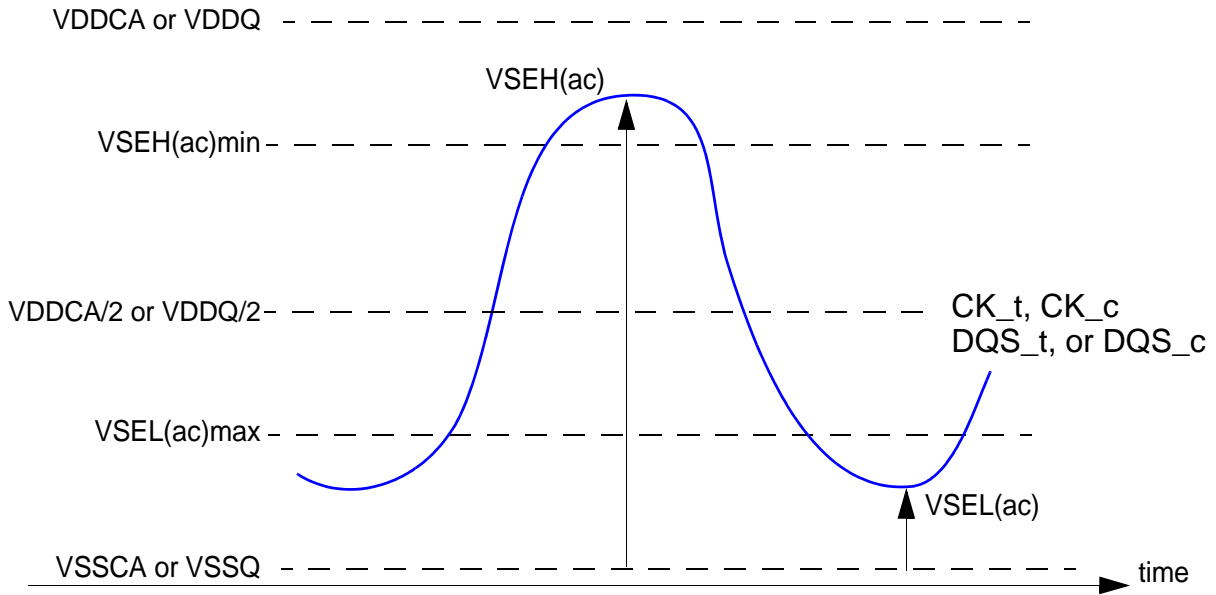
### 8.4.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK\_t, DQS\_t, CK\_c, or DQS\_c) has also to comply with certain requirements for single-ended signals.

CK\_t and CK\_c shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle.

DQS\_t, DQS\_c shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle preceeding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.



**Figure 110 — Single-ended requirement for differential signals.**

Note that while CA and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS\_t, DQS\_c and VDDCA/2 for CK\_t, CK\_c; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL(ac)max, VSEH(ac)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

The signal ended requirements for CK\_t, CK\_c, DQS\_t, and DQS\_c are found in [Table 74](#) and [Table 76](#), respectively.

**Table 79 — Single-ended levels for CK\_t, DQS\_t, CK\_c, DQS\_c**

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
VSEH(AC)	Single-ended high-level for strobes	$(VDDQ / 2) + 0.220$	note 3	$(VDDQ / 2) + 0.300$	note 3	V	1, 2
	Single-ended high-level for CK_t, CK_c	$(VDDCA / 2) + 0.220$	note 3	$(VDDCA / 2) + 0.300$	note 3	V	1, 2
VSEL(AC)	Single-ended low-level for strobes	note 3	$(VDDQ / 2) - 0.220$	note 3	$(VDDQ / 2) - 0.300$	V	1, 2
	Single-ended low-level for CK_t, CK_c	note 3	$(VDDCA / 2) - 0.220$	note 3	$(VDDCA / 2) - 0.300$	V	1, 2

NOTE 1 For CK\_t, CK\_c use VSEH/VSEL(ac) of CA; for strobes (DQS0\_t, DQS0\_c, DQS1\_t, DQS1\_c, DQS2\_t, DQS2\_c, DQS3\_t, DQS3\_c) use VIH/VIL(ac) of DQs.

NOTE 2 VIH(ac)/VIL(ac) for DQs is based on VREFDQ; VSEH(ac)/VSEL(ac) for CA is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here

NOTE 3 These values are not defined, however the single-ended signals CK\_t, CK\_c, DQS0\_t, DQS0\_c, DQS1\_t, DQS1\_c, DQS2\_t, DQS2\_c, DQS3\_t, DQS3\_c need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 175

## 8.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK\_t, CK\_c and DQS\_t, DQS\_c) must meet the requirements in Table 79. The differential input cross point voltage  $V_{IX}$  is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

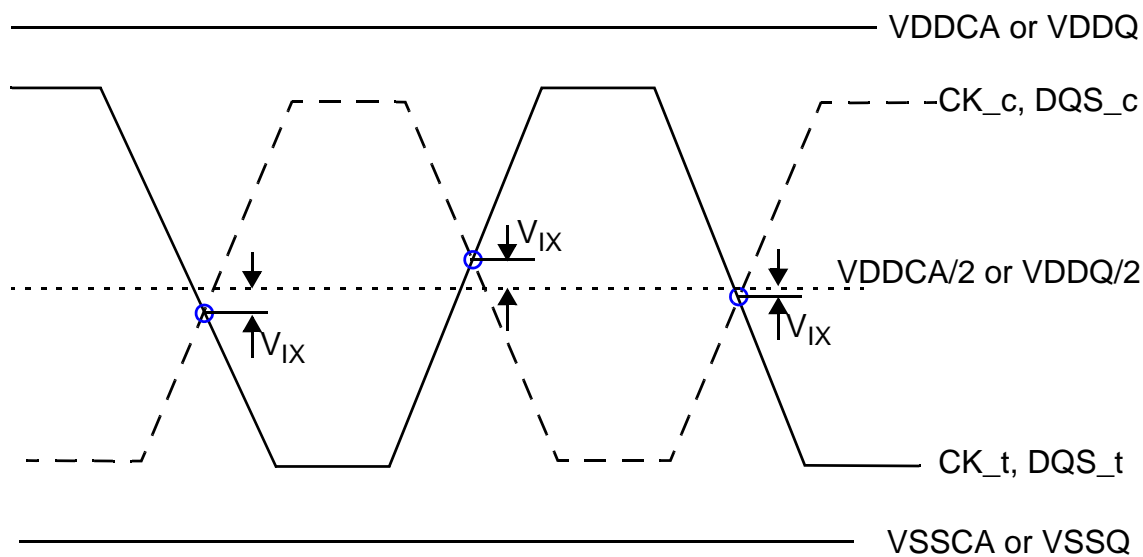


Figure 111 — Vix Definition

Table 80 — Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200		Unit	Notes
		Min	Max		
$V_{IXCA}$	Differential Input Cross Point Voltage relative to VDDCA/2 for CK_t, CK_c	- 120	120	mV	1,2
$V_{IXDQ}$	Differential Input Cross Point Voltage relative to VDDQ/2 for DQS_t, DQS_c	- 120	120	mV	1,2

NOTE 1 The typical value of  $V_{IX}(AC)$  is expected to be about  $0.5 \times VDD$  of the transmitting device, and  $V_{IX}(AC)$  is expected to track variations in VDD.  $V_{IX}(AC)$  indicates the voltage at which differential input signals must cross.

NOTE 2 For CK\_t and CK\_c,  $V_{ref} = V_{refCA}(DC)$ . For DQS\_t and DQS\_c,  $V_{ref} = V_{refDQ}(DC)$ .



## 8.6 Slew Rate Definitions for Single-Ended Input Signals

See 12.5 for single-ended slew rate definitions for address and command signals.

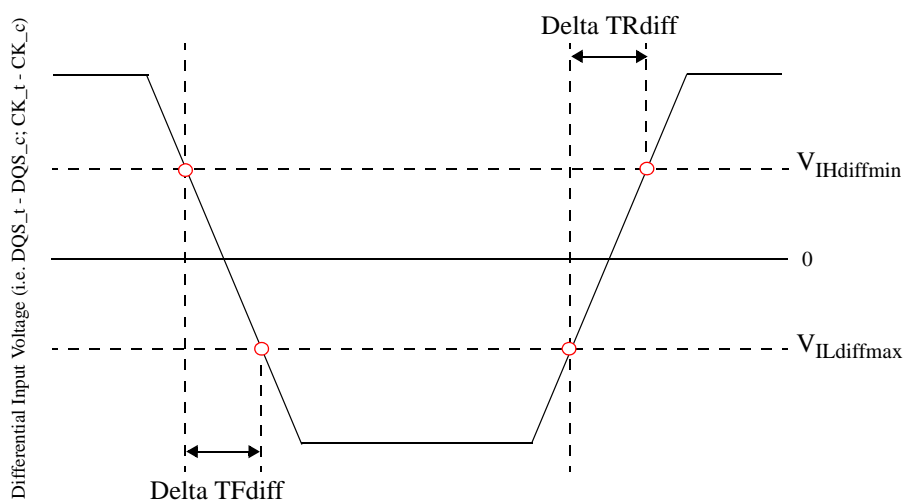
See 12.6 for single-ended slew rate definitions for data signals.

## 8.7 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK\_t, CK\_c and DQS\_t, DQS\_c) are defined and measured as shown in Table 81 and Figure 112.

**Table 81 — Differential Input Slew Rate Definition**

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK_t - CK_c and DQS_t - DQS_c).	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TR_{diff}$
Differential input slew rate for falling edge (CK_t - CK_c and DQS_t - DQS_c).	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TF_{diff}$
NOTE 1 The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds.			



**Figure 112 — Differential Input Slew Rate Definition for DQS\_t, DQS\_c and CK\_t, CK\_c**

## 9 AC and DC Output Measurement Levels

### 9.1 Single Ended AC and DC Output Levels

Table 82 shows the output levels used for measurements of single ended signals.

**Table 82 — Single-ended AC and DC Output Levels**

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	$0.9 \times V_{DDQ}$	V	1
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	$0.1 \times V_{DDQ}$	V	2
$V_{OH(AC)}$	AC output high measurement level (for output slew rate )	$V_{REFDQ} + 0.12$	V	
$V_{OL(AC)}$	AC output low measurement level (for output slew rate )	$V_{REFDQ} - 0.12$	V	
$I_{OZ}$	Output Leakage current (DQ, DM, DQS_t, DQS_c) (DQ, DQS_t, DQS_c are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$ )	Min	-5	uA
		Max	5	uA
$MM_{PUPD}$	Delta RON between pull-up and pull-down for DQ/DM	Min	-15	%
		Max	15	%

NOTE 1  $I_{OH} = -0.1mA$ .

NOTE 2  $I_{OL} = 0.1mA$ .

### 9.2 Differential AC and DC Output Levels

Table 83 shows the output levels used for measurements of differential signals (DQS\_t, DQS\_c).

**Table 83 — Differential AC and DC Output Levels**

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	$+ 0.20 \times V_{DDQ}$	V	
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	$- 0.20 \times V_{DDQ}$	V	

NOTE 1  $I_{OH} = -0.1mA$ .

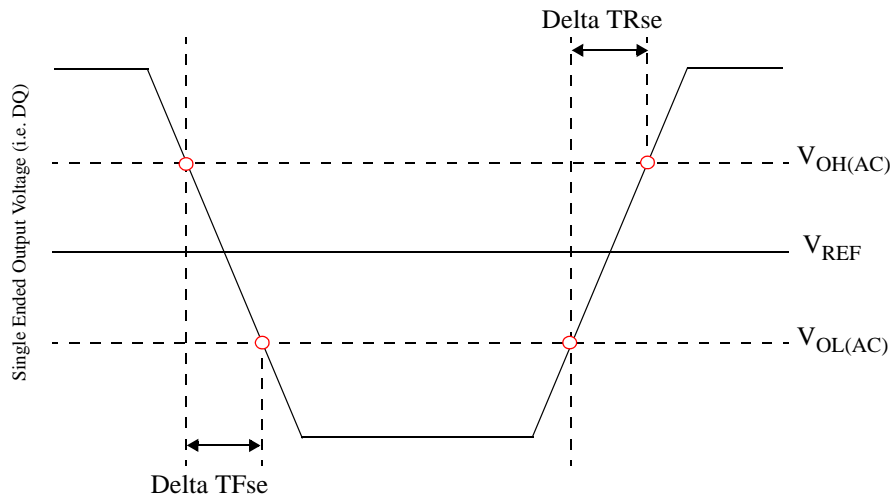
NOTE 2  $I_{OL} = 0.1mA$

### 9.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between  $V_{OL(AC)}$  and  $V_{OH(AC)}$  for single ended signals as shown in Table 84 and Figure 113.

**Table 84 — Single-ended Output Slew Rate Definition**

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TR_{se}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TF_{se}$
Note: Output slew rate is verified by design and characterization, and may not be subject to production test.			



**Figure 113 — Single Ended Output Slew Rate Definition**

**Table 85 — Output Slew Rate (single-ended)**

Parameter	Symbol	LPDDR2-1066 to LPDDR2-200		Units
		Min	Max	
Single-ended Output Slew Rate ( $R_{ON} = 40\Omega \pm 30\%$ )	SRQse	1.5	3.5	V/ns
Single-ended Output Slew Rate ( $R_{ON} = 60\Omega \pm 30\%$ )	SRQse	1.0	2.5	V/ns
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4	
Description: SR: Slew Rate <b>Q: Query Output (like in DQ, which stands for Data-in, Query-Output)</b> <b>se: Single-ended Signals</b> NOTE 1 Measured with output reference load. NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation. NOTE 3 The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ . NOTE 4 Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.				

9.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 86 and Figure 114.

Table 86 — Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	V <sub>OLdiff(AC)</sub>	V <sub>OHdiff(AC)</sub>	[V <sub>OHdiff(AC)</sub> - V <sub>OLdiff(AC)</sub> ] / DeltaTRdiff
Differential output slew rate for falling edge	V <sub>OHdiff(AC)</sub>	V <sub>OLdiff(AC)</sub>	[V <sub>OHdiff(AC)</sub> - V <sub>OLdiff(AC)</sub> ] / DeltaTFdiff
NOTE 1 Output slew rate is verified by design and characterization, and may not be subject to production test.			

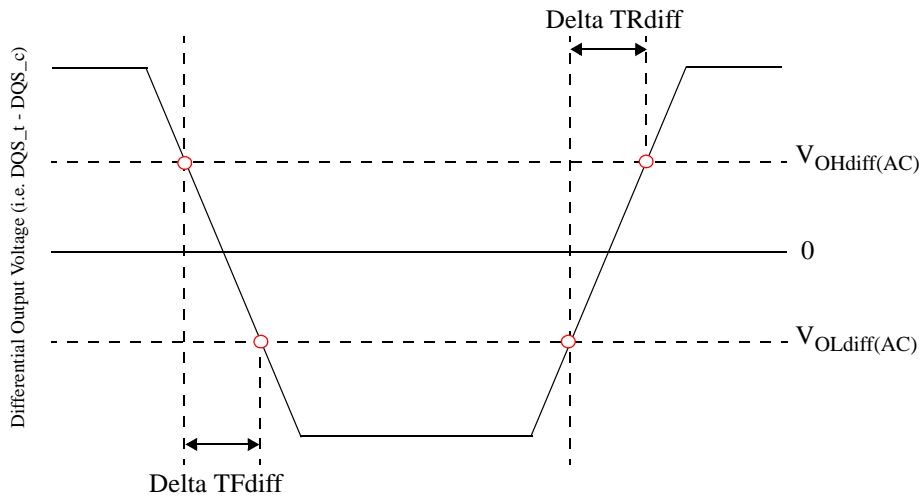


Figure 114 — Differential Output Slew Rate Definition

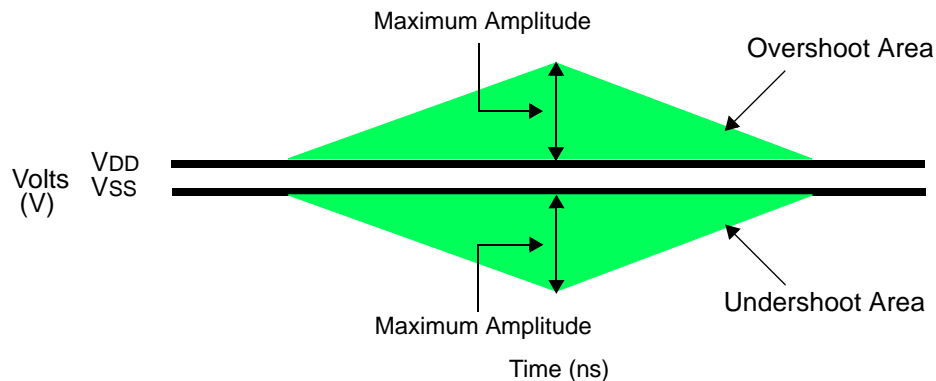
Table 87 — Differential Output Slew Rate

Parameter	Symbol	LPDDR2-1066 to LPDDR2-200		Units
		Min	Max	
Differential Output Slew Rate (RON = 40Ω +/- 30%)	SRQdiff	3.0	7.0	V/ns
Differential Output Slew Rate (RON = 60Ω +/- 30%)	SRQdiff	2.0	5.0	V/ns
Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) diff: Differential Signals NOTE 1 Measured with output reference load. NOTE 2 The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC). NOTE 3 Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.				

## 9.5 Overshoot and Undershoot Specifications

**Table 88 — AC Overshoot/Undershoot Specification**

Parameter		1066	933	800	667	533	466	400	333	266	200	Units
Maximum peak amplitude allowed for overshoot area. (See Figure 115)	Max	0.35										V
Maximum peak amplitude allowed for undershoot area. (See Figure 115)	Max	0.35										V
Maximum area above VDD. (See Figure 115)	Max	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns
Maximum area below VSS. (See Figure 115)	Max	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns
(CA0-9, CS_n, CKE, CK_t, CK_c, DQ, DQS_t, DQS_c, DM/DNV)												
NOTE 1 For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDDCA. For DQ, DM/DNV, DQS_t, and DQS_c, VDD stands for VDDQ.												
NOTE 2 For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSSCA. For DQ, DM/DNV, DQS_t, and DQS_c, VSS stands for VSSQ.												
NOTE 3 Maximum peak amplitude values are referenced from actual VDD and VSS values.												
NOTE 4 Maximum area values are referenced from maximum operating VDD and VSS values.												



**Figure 115 — Overshoot and Undershoot Definition**

NOTE 1 For CA0-9, CK\_t, CK\_c, CS\_n, and CKE, VDD stands for VDDCA. For DQ, DM/DNV, DQS\_t, and DQS\_c, VDD stands for VDDQ.

NOTE 2 For CA0-9, CK\_t, CK\_c, CS\_n, and CKE, VSS stands for VSSCA. For DQ, DM/DNV, DQS\_t, and DQS\_c, VSS stands for VSSQ.

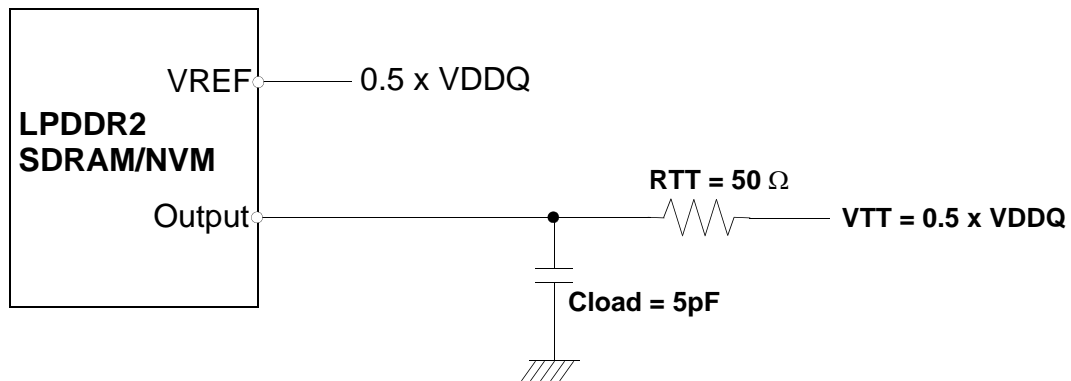
NOTE 3 Maximum peak amplitude values are referenced from actual VDD and VSS values.

NOTE 4 Maximum area values are referenced from maximum operating VDD and VSS values.

## 9.6 Output buffer characteristics

### 9.6.1 HSUL\_12 Driver Output Timing Reference Load

These ‘Timing Reference Loads’ are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



**Figure 116 — HSUL\_12 Driver Output Reference Load for Timing and Slew Rate**

NOTE 1: All output timing parameter values (like  $t_{DQSCK}$ ,  $t_{DQSQ}$ ,  $t_{QHS}$ ,  $t_{HZ}$ ,  $t_{RPRE}$  etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

## 9.7 $RON_{PU}$ and $RON_{PD}$ Resistor Definition

$$RON_{PU} = \frac{(VDDQ - V_{out})}{ABS(I_{out})}$$

NOTE 1: This is under the condition that  $RON_{PD}$  is turned off

$$RON_{PD} = \frac{V_{out}}{ABS(I_{out})}$$

NOTE 1: This is under the condition that  $RON_{PU}$  is turned off

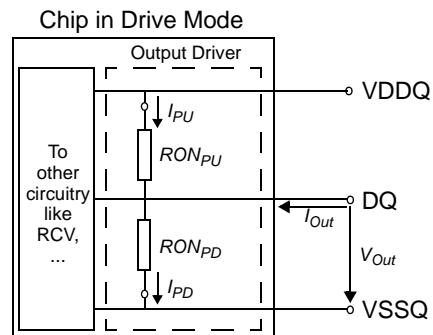


Figure 117 — Output Driver: Definition of Voltages and Currents

### 9.7.1 $RON_{PU}$ and $RON_{PD}$ Characteristics with ZQ Calibration

Output driver impedance  $RON$  is defined by the value of the external reference resistor  $RZQ$ . Nominal  $RZQ$  is  $240\Omega$ .

**Table 89 — Output Driver DC Electrical Characteristics with ZQ Calibration**

$RON_{NOM}$	Resistor	Vout	Min	Nom	Max	Unit	Notes
$34.3\Omega$	RON34PD	$0.5 \times VDDQ$	0.85	1.00	1.15	RZQ/7	1,2,3,4
	RON34PU	$0.5 \times VDDQ$	0.85	1.00	1.15	RZQ/7	1,2,3,4
$40.0\Omega$	RON40PD	$0.5 \times VDDQ$	0.85	1.00	1.15	RZQ/6	1,2,3,4
	RON40PU	$0.5 \times VDDQ$	0.85	1.00	1.15	RZQ/6	1,2,3,4
$48.0\Omega$	RON48PD	$0.5 \times VDDQ$	0.85	1.00	1.15	RZQ/5	1,2,3,4
	RON48PU	$0.5 \times VDDQ$	0.85	1.00	1.15	RZQ/5	1,2,3,4
$60.0\Omega$	RON60PD	$0.5 \times VDDQ$	0.85	1.00	1.15	RZQ/4	1,2,3,4
	RON60PU	$0.5 \times VDDQ$	0.85	1.00	1.15	RZQ/4	1,2,3,4
$80.0\Omega$	RON80PD	$0.5 \times VDDQ$	0.85	1.00	1.15	RZQ/3	1,2,3,4
	RON80PU	$0.5 \times VDDQ$	0.85	1.00	1.15	RZQ/3	1,2,3,4
$120.0\Omega$ (optional)	RON120PD	$0.5 \times VDDQ$	0.85	1.00	1.15	RZQ/2	1,2,3,4
	RON120PU	$0.5 \times VDDQ$	0.85	1.00	1.15	RZQ/2	1,2,3,4
Mismatch between pull-up and pull-down	$MM_{PUPD}$		-15.00		+15.00	%	1,2,3,4,5

NOTE 1 Across entire operating temperature range, after calibration.

NOTE 2  $RZQ = 240\Omega$

NOTE 3 The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

NOTE 4 Pull-down and pull-up output driver impedances are recommended to be calibrated at  $0.5 \times VDDQ$ .

NOTE 5 Measurement definition for mismatch between pull-up and pull-down,  $MM_{PUPD}$ : Measure  $RON_{PU}$  and  $RON_{PD}$ , both at  $0.5 \times VDDQ$ :

$$MM_{PUPD} = \frac{RON_{PU} - RON_{PD}}{RON_{NOM}} \times 100$$

For example, with  $MM_{PUPD}(\max) = 15\%$  and  $RON_{PD} = 0.85$ ,  $RON_{PU}$  must be less than 1.0.



### 9.7.2 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

**Table 90 — Output Driver Sensitivity Definition**

Resistor	Vout	Min	Max	Unit	Notes
RONPD	0.5 × VDDQ	$85 - (dRONdT \times  \Delta T ) - (dRONdV \times  \Delta V )$	$115 + (dRONdT \times  \Delta T ) + (dRONdV \times  \Delta V )$	%	1,2
RONPU					

NOTE 1  $\Delta T = T - T(@ \text{ calibration})$ ,  $\Delta V = V - V(@ \text{ calibration})$

NOTE 2 dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

**Table 91 — Output Driver Temperature and Voltage Sensitivity**

Symbol	Parameter	Min	Max	Unit	Notes
dRONdT	RON Temperature Sensitivity	0.00	0.75	% / C	
dRONdV	RON Voltage Sensitivity	0.00	0.20	% / mV	

### 9.7.3 $RON_{PU}$ and $RON_{PD}$ Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

**Table 92 — Output Driver DC Electrical Characteristics without ZQ Calibration**

$RON_{NOM}$	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3 $\Omega$	RON34PD	0.5 x VDDQ	24	34.3	44.6	$\Omega$	1
	RON34PU	0.5 x VDDQ	24	34.3	44.6	$\Omega$	1
40.0 $\Omega$	RON40PD	0.5 x VDDQ	28	40	52	$\Omega$	1
	RON40PU	0.5 x VDDQ	28	40	52	$\Omega$	1
48.0 $\Omega$	RON48PD	0.5 x VDDQ	33.6	48	62.4	$\Omega$	1
	RON48PU	0.5 x VDDQ	33.6	48	62.4	$\Omega$	1
60.0 $\Omega$	RON60PD	0.5 x VDDQ	42	60	78	$\Omega$	1
	RON60PU	0.5 x VDDQ	42	60	78	$\Omega$	1
80.0 $\Omega$	RON80PD	0.5 x VDDQ	56	80	104	$\Omega$	1
	RON80PU	0.5 x VDDQ	56	80	104	$\Omega$	1
120.0 $\Omega$ (optional)	RON120PD	0.5 x VDDQ	84	120	156	$\Omega$	1
	RON120PU	0.5 x VDDQ	84	120	156	$\Omega$	1

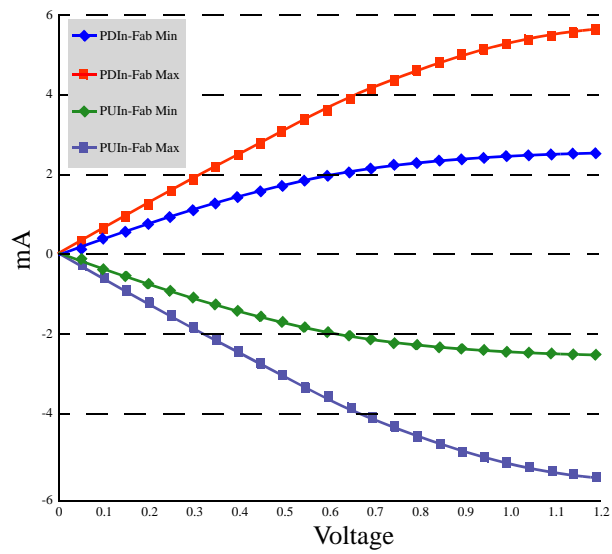
NOTE 1 Across entire operating temperature range, without calibration.

9.7.4 RZQ I-V Curve

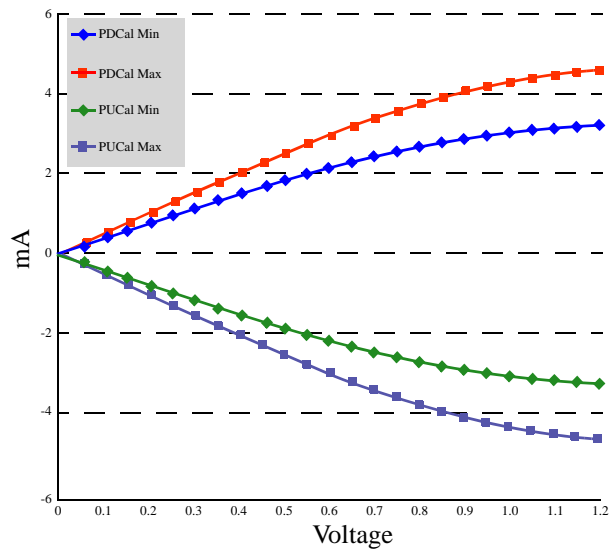
Table 93 — RZQ I-V Curve

Voltage[V]	RON = 240Ω (RZQ)							
	Pull-Down				Pull-Up			
	Current [mA] / RON [Ohms]				Current [mA] / RON [Ohms]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	-0.19	-0.32	-0.21	-0.26
0.10	0.38	0.64	0.40	0.53	-0.38	-0.64	-0.40	-0.53
0.15	0.56	0.94	0.60	0.78	-0.56	-0.94	-0.60	-0.78
0.20	0.74	1.26	0.79	1.04	-0.74	-1.26	-0.79	-1.04
0.25	0.92	1.57	0.98	1.29	-0.92	-1.57	-0.98	-1.29
0.30	1.08	1.86	1.17	1.53	-1.08	-1.86	-1.17	-1.53
0.35	1.25	2.17	1.35	1.79	-1.25	-2.17	-1.35	-1.79
0.40	1.40	2.46	1.52	2.03	-1.40	-2.46	-1.52	-2.03
0.45	1.54	2.74	1.69	2.26	-1.54	-2.74	-1.69	-2.26
0.50	1.68	3.02	1.86	2.49	-1.68	-3.02	-1.86	-2.49
0.55	1.81	3.30	2.02	2.72	-1.81	-3.30	-2.02	-2.72
0.60	1.92	3.57	2.17	2.94	-1.92	-3.57	-2.17	-2.94
0.65	2.02	3.83	2.32	3.15	-2.02	-3.83	-2.32	-3.15
0.70	2.11	4.08	2.46	3.36	-2.11	-4.08	-2.46	-3.36
0.75	2.19	4.31	2.58	3.55	-2.19	-4.31	-2.58	-3.55
0.80	2.25	4.54	2.70	3.74	-2.25	-4.54	-2.70	-3.74
0.85	2.30	4.74	2.81	3.91	-2.30	-4.74	-2.81	-3.91
0.90	2.34	4.92	2.89	4.05	-2.34	-4.92	-2.89	-4.05
0.95	2.37	5.08	2.97	4.23	-2.37	-5.08	-2.97	-4.23
1.00	2.41	5.20	3.04	4.33	-2.41	-5.20	-3.04	-4.33
1.05	2.43	5.31	3.09	4.44	-2.43	-5.31	-3.09	-4.44
1.10	2.46	5.41	3.14	4.52	-2.46	-5.41	-3.14	-4.52
1.15	2.48	5.48	3.19	4.59	-2.48	-5.48	-3.19	-4.59
1.20	2.50	5.55	3.23	4.65	-2.50	-5.55	-3.23	-4.65

#### 9.7.4 RZQ I-V Curve (cont'd)



**Figure 118 — RON 240 Ohms  
IV Curve after ZQReset**



**Figure 119 — RON = 240 Ohms  
IV Curve after calibration**

## 10 Input/Output Capacitance

### 10.1 Input/Output Capacitance

Table 94 — Input/output capacitance

Parameter	Symbol		LPDDR2 1066-466	LPDDR2 400-200	Units	Notes
Input capacitance, CK_t and CK_c	CCK	Min	1.0		pF	1,2
		Max	2.0		pF	1,2
Input capacitance delta, CK_t and CK_c	CDCK	Min	0		pF	1,2,3
		Max	0.20	0.25	pF	1,2,3
Input capacitance, all other input-only pins	CI	Min	1.0		pF	1,2,4
		Max	2.0		pF	1,2,4
Input capacitance delta, all other input-only pins	CDI	Min	-0.40	-0.50	pF	1,2,5
		Max	0.40	0.50	pF	1,2,5
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	Min	1.25		pF	1,2,6,7
		Max	2.5		pF	1,2,6,7
Input/output capacitance delta, DQS_t, DQS_c	CDDQS	Min	0		pF	1,2,7,8
		Max	0.25	0.30	pF	1,2,7,8
Input/output capacitance delta, DQ, DM	CDIO	Min	-0.5	-0.6	pF	1,2,7,9
		Max	0.5	0.6	pF	1,2,7,9
Input/output capacitance ZQ Pin	CZQ	Min	0		pF	1,2
		Max	2.5		pF	1,2
Package Input capacitance, CK_t and CK_c	CPKGCK	Min			pF	2,10
		Max			pF	2,10
Package Input capacitance delta, CK_t and CK_c	CDPKGCK	Min			pF	2,10,11
		Max			pF	2,10,11
Package Input capacitance, all other input-only pins	CPKGI	Min			pF	2,10,12
		Max			pF	2,10,12
Package Input capacitance delta, all other input-only pins	CDPKGI	Min			pF	2,10,13
		Max			pF	2,10,13
Package Input/output capacitance, DQ, DM, DQS_t, DQS_c	CPKGIO	Min			pF	2,10,5
		Max			pF	2,10,5
Package Input/output capacitance delta, DQS_t, DQS_c	CDPKGDS	Min			pF	2,10,14
		Max			pF	2,10,14
Package Input/output capacitance delta, DQ, DM	CDPKGIO	Min			pF	2,10,15
		Max			pF	2,10,15
Package Input/output capacitance, ZQ Pin	CDPKZQ	Min			pF	2,10
		Max			pF	2,10,16

(TOPER; V<sub>DDQ</sub> = 1.14-1.3V; V<sub>DDCA</sub> = 1.14-1.3V; V<sub>DD1</sub> = 1.7-1.95V, LPDDR2-S4A V<sub>DD2</sub> = 1.28-1.42V, LPDDR2-S2B, LPDDR2-N-B V<sub>DD2</sub> = 1.14-1.3V)

## 10.1 Input/Output Capacitance (cont'd)

Notes to [Table 94](#)

NOTE 1 This parameter applies to die device only (does not include package capacitance).

NOTE 2 This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating.

NOTE 3 Absolute value of CCK<sub>t</sub> - CCK<sub>c</sub>.

NOTE 4 CI applies to CS<sub>n</sub>, CKE, CA0-CA9.

NOTE 5  $CDI = CI - 0.5 * (CCK_t + CCK_c)$

NOTE 6 DM loading matches DQ and DQS.

NOTE 7 MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ohm typical)

NOTE 8 Absolute value of CDQS<sub>t</sub> and CDQS<sub>c</sub>.

NOTE 9  $CDIO = CIO - 0.5 * (CDQS_t + CDQS_c)$  in byte-lane.

NOTE 10 This parameter applies to package only (does not include die capacitance). This value is vendor specific.

NOTE 11 Absolute value of CPKGCK<sub>t</sub> and CPKGCK<sub>c</sub>.

NOTE 12 CPKGI applies to CS<sub>n</sub>, CKE, CA9-CA0.

NOTE 13  $CDPKGI = CPKGI - 0.5 * (CPKGDQS_t + CPKGDQS_c)$ .

NOTE 14 Absolute value of CPKGDQS<sub>t</sub> and CPKGDQS<sub>c</sub>.

NOTE 15  $CDPKGIO = CDPKGI - 0.5 * (CPKGDQS_t + CPKGDQS_c)$  in byte lane.

NOTE 16 Maximum external load capacitance on ZQ pin, including packaging, board, pin, resistor, and other LPDDR2 devices: 5 pF.

## 11 IDD Specification Parameters and Test Conditions

### 11.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:

LOW:  $V_{IN} \leq V_{IL(DC)} \text{ MAX}$

HIGH:  $V_{IN} \geq V_{IH(DC)} \text{ MIN}$

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See [Table 95](#) and [Table 96](#).

**Table 95 — Definition of Switching for CA Input Signals**

Switching for CA								
	CK <sub>t</sub> (RISING) / CK <sub>c</sub> (FALLING)	CK <sub>t</sub> (FALLING) / CK <sub>c</sub> (RISING)	CK <sub>t</sub> (RISING) / CK <sub>c</sub> (FALLING)	CK <sub>t</sub> (FALLING) / CK <sub>c</sub> (RISING)	CK <sub>t</sub> (RISING) / CK <sub>c</sub> (FALLING)	CK <sub>t</sub> (FALLING) / CK <sub>c</sub> (RISING)	CK <sub>t</sub> (RISING) / CK <sub>c</sub> (FALLING)	CK <sub>t</sub> (FALLING) / CK <sub>c</sub> (RISING)
Cycle	N		N+1		N+2		N+3	
CS <sub>n</sub>	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

NOTE 1 CS<sub>n</sub> must always be driven HIGH.

NOTE 2 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.

NOTE 3 The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.

**11.1 IDD Measurement Conditions (cont'd)****Table 96 — Definition of Switching for IDD4R**

Clock	CKE	CS_n	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Read_Rising	HLH	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Read_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

NOTE 1 Data strobe (DQS) is changing between HIGH and LOW every clock cycle.

NOTE 2 The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4R.

**Table 97 — Definition of Switching for IDD4W**

Clock	CKE	CS_n	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Write_Rising	HLL	LHLHLHL	L
Falling	HIGH	LOW	N	Write_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Write_Rising	HLL	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Write_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

NOTE 1 Data strobe (DQS) is changing between HIGH and LOW every clock cycle.

NOTE 2 Data masking (DM) must always be driven LOW.

NOTE 3 The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.



## 11.2 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range.

**Table 98 — LPDDR2 IDD Specification Parameters and Operating Conditions**

Parameter/Condition	Symbol	Power Supply	Units	Notes
<b>Operating one bank active-precharge current (SDRAM):</b>	IDD0 <sub>1</sub>	VDD1	mA	4
<b>Operating one RB active current (NVM):</b>	IDD0 <sub>2</sub>	VDD2	mA	4
$t_{CK} = t_{CK(avg)min}$ ; CKE is HIGH; CS <sub>n</sub> is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD0 <sub>IN</sub>	VDDCA VDDQ	mA	4,5
<b>Idle power-down standby current:</b>	IDD2P <sub>1</sub>	VDD1	mA	4
$t_{CK} = t_{CK(avg)min}$ ; CKE is LOW; CS <sub>n</sub> is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD2P <sub>2</sub>	VDD2	mA	4
	IDD2P <sub>IN</sub>	VDDCA VDDQ	mA	4,5
<b>Idle power-down standby current with clock stop:</b>	IDD2PS <sub>1</sub>	VDD1	mA	4
CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CS <sub>n</sub> is HIGH; All banks/RBs idle; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD2PS <sub>2</sub>	VDD2	mA	4
	IDD2PS <sub>IN</sub>	VDDCA VDDQ	mA	4,5
<b>Idle non power-down standby current:</b>	IDD2N <sub>1</sub>	VDD1	mA	4
$t_{CK} = t_{CK(avg)min}$ ; CKE is HIGH; CS <sub>n</sub> is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD2N <sub>2</sub>	VDD2	mA	4
	IDD2N <sub>IN</sub>	VDDCA VDDQ	mA	4,5
<b>Idle non power-down standby current with clock stop:</b>	IDD2NS <sub>1</sub>	VDD1	mA	4
CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is HIGH; CS <sub>n</sub> is HIGH; All banks/RBs idle; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD2NS <sub>2</sub>	VDD2	mA	4
	IDD2NS <sub>IN</sub>	VDDCA VDDQ	mA	4,5
<b>Active power-down standby current:</b>	IDD3P <sub>1</sub>	VDD1	mA	4
$t_{CK} = t_{CK(avg)min}$ ; CKE is LOW; CS <sub>n</sub> is HIGH; One bank/RB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD3P <sub>2</sub>	VDD2	mA	4
	IDD3P <sub>IN</sub>	VDDCA VDDQ	mA	4,5
<b>Active power-down standby current with clock stop:</b>	IDD3PS <sub>1</sub>	VDD1	mA	4
CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CS <sub>n</sub> is HIGH; One bank/RB active; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD3PS <sub>2</sub>	VDD2	mA	4
	IDD3PS <sub>IN</sub>	VDDCA VDDQ	mA	4,5

Parameter/Condition	Symbol	Power Supply	Units	Notes
<b>Active non power-down standby current:</b> $t_{CK} = t_{CK(avg)min}$ ; CKE is HIGH; CS_n is HIGH; One bank/RB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD3N <sub>1</sub>	VDD1	mA	4
	IDD3N <sub>2</sub>	VDD2	mA	4
	IDD3N <sub>IN</sub>	VDDCA VDDQ	mA	4,5
<b>Active non power-down standby current with clock stop:</b> CK_t=LOW, CK_c=HIGH; CKE is HIGH; CS_n is HIGH; One bank/RB active; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD3NS <sub>1</sub>	VDD1	mA	4
	IDD3NS <sub>2</sub>	VDD2	mA	4
	IDD3NS <sub>IN</sub>	VDDCA VDDQ	mA	4,5
<b>Operating burst read current:</b> $t_{CK} = t_{CK(avg)min}$ ; CS_n is HIGH between valid commands; One bank/RB active; BL = 4; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	IDD4R <sub>1</sub>	VDD1	mA	4
	IDD4R <sub>2</sub>	VDD2	mA	4
	IDD4R <sub>IN</sub>	VDDCA	mA	4
	IDD4R <sub>Q</sub>	VDDQ	mA	4,8
<b>Operating burst write current:</b> $t_{CK} = t_{CK(avg)min}$ ; CS_n is HIGH between valid commands; One bank/RB active; BL = 4; WL = WLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	IDD4W <sub>1</sub>	VDD1	mA	4
	IDD4W <sub>2</sub>	VDD2	mA	4
	IDD4W <sub>IN</sub>	VDDCA VDDQ	mA	4,5
<b>All Bank Refresh Burst current:</b> $t_{CK} = t_{CK(avg)min}$ ; CKE is HIGH between valid commands; $t_{RC} = t_{RFCabmin}$ ; Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	IDD5 <sub>1</sub>	VDD1	mA	1,4
	IDD5 <sub>2</sub>	VDD2	mA	1,4
	IDD5 <sub>IN</sub>	VDDCA VDDQ	mA	1,4,5
<b>All Bank Refresh Average current:</b> $t_{CK} = t_{CK(avg)min}$ ; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$ ; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	IDD5AB <sub>1</sub>	VDD1	mA	1,4
	IDD5AB <sub>2</sub>	VDD2	mA	1,4
	IDD5AB <sub>IN</sub>	VDDCA VDDQ	mA	1,4,5
<b>Per Bank Refresh Average current:</b> $t_{CK} = t_{CK(avg)min}$ ; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}/8$ ; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	IDD5PB <sub>1</sub>	VDD1	mA	1,2,4
	IDD5PB <sub>2</sub>	VDD2	mA	1,2,4
	IDD5PB <sub>IN</sub>	VDDCA VDDQ	mA	1,2,4,5
<b>Self refresh current (Standard Temperature Range):</b> CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; Maximum 1x Self-Refresh Rate;	IDD6 <sub>1</sub>	VDD1	mA	1,3,4,11,12
	IDD6 <sub>2</sub>	VDD2	mA	1,3,4,11,12
	IDD6 <sub>IN</sub>	VDDCA VDDQ	mA	1,3,4,5,11, 12

Parameter/Condition	Symbol	Power Supply	Units	Notes
<b>Self refresh current (Extended Temperature Range):</b> CK <sub>t</sub> =LOW, CK <sub>c</sub> =HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;	IDD6ET <sub>1</sub>	VDD1	mA	1,3,11,13
	IDD6ET <sub>2</sub>	VDD2	mA	1,3,11,13
	IDD6ET <sub>IN</sub>	VDDCA VDDQ	mA	1,3,5,11,13
<b>Deep Power-Down current:</b> CK <sub>t</sub> =LOW, CK <sub>c</sub> =HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;	IDD8 <sub>1</sub>	VDD1	uA	1,4
	IDD8 <sub>2</sub>	VDD2	uA	1,4
	IDD8 <sub>IN</sub>	VDDCA VDDQ	uA	1,4,5
<b>LPDDR2-N Program current:</b> CK <sub>t</sub> =LOW, CK <sub>c</sub> =HIGH; CKE is LOW; RBs active or idle; CS <sub>n</sub> is HIGH; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	IDDN <sub>P1</sub>	VDD1	mA	4,7
	IDDN <sub>P2</sub>	VDD2	mA	4,7
<b>LPDDR2-N Erase current:</b> CK <sub>t</sub> =LOW, CK <sub>c</sub> =HIGH; CKE is LOW; RBs active or idle; CS <sub>n</sub> is HIGH; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	IDDN <sub>E1</sub>	VDD1	mA	4,6,7
	IDDN <sub>E2</sub>	VDD2	mA	4,6,7

NOTE 1 Refresh currents and Deep Power Down currents are not relevant for NVM devices.

NOTE 2 Per Bank Refresh only applicable for LPDDR2-S4 devices of 1Gb or higher densities and LPDDR2-S2 devices of 4Gb and higher densities.

NOTE 3 This is the general definition that applies to full array Self Refresh. Refer to [Table 99](#) for details of Partial Array Self Refresh IDD6 specification.

NOTE 4 IDD values published are the maximum of the distribution of the arithmetic mean.

NOTE 5 Measured currents are the summation of VDDQ and VDDCA.

NOTE 6 Some LPDDR2-N devices do not support the erase function.

NOTE 7 To calculate total current consumption, the currents of all active operations must be considered.

NOTE 8 Guaranteed by design with output load of 5pF and RON = 400ohm.

NOTE 9 Currents related to VDD2 do not apply to LPDDR2-N-A and LPDDR2-S2A devices.

NOTE 10 IDD current specifications are tested after the device is properly initialized.

NOTE 11 In addition, supplier data sheets may include additional Self Refresh IDD values for temperature subranges within the Standard or Extended Temperature Ranges.

NOTE 12 1x Self-Refresh Rate is the rate at which the LPDDR2-SX device is refreshed internally during Self-Refresh before going into the Extended Temperature range.

NOTE 13 IDD6ET is a typical value, is sampled only and is not tested.

**Table 99 — IDD6 Partial Array Self-Refresh Current**

Parameter		LPDDR2-S2		LPDDR2-S4		Unit
		64Mb-2Gb	4Gb-8Gb	64Mb-512Mb	1Gb-8Gb	
IDD6 Partial Array Self-Refresh Current	Full Array	-	-	-	-	uA
	1/2 Array	-	-	-	-	uA
	1/4 Array	-	-	-	-	uA
	1/8 Array	NA	-	NA	-	uA

NOTE 1 LPDDR2-S2 SDRAM uses the same PASR scheme & IDD6 current value categorization as LPDDR (JESD209).

NOTE 2 LPDDR2-S4 SDRAM uses the same IDD6 current value categorization as LPDDR2-S2 SDRAM. Some LPDDR2-S4 SDRAM densities support both bank-masking & segment-masking. The IDD6 currents are measured using bank-masking only.

NOTE 3 IDD values published are the maximum of the distribution of the arithmetic mean.

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## 12 Electrical Characteristics and AC Timing

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### 12.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR2 device.

#### 12.1.1 Definition for $t_{CK}(avg)$ and $nCK$

$t_{CK}(avg)$  is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$t_{CK}(avg) = \left( \sum_{j=1}^N t_{CK_j} \right) / N$$

*where*  $N = 200$

Unit ' $t_{CK}(avg)$ ' represents the actual clock average  $t_{CK}(avg)$  of the input clock under operation. Unit ' $nCK$ ' represents one clock cycle of the input clock, counting the actual clock edges.  
 $t_{CK}(avg)$  may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

#### 12.1.2 Definition for $t_{CK}(abs)$

$t_{CK}(abs)$  is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.  
 $t_{CK}(abs)$  is not subject to production test.

#### 12.1.3 Definition for $t_{CH}(avg)$ and $t_{CL}(avg)$

$t_{CH}(avg)$  is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$t_{CH}(avg) = \left( \sum_{j=1}^N t_{CH_j} \right) / (N \times t_{CK}(avg))$$

*where*  $N = 200$

$t_{CL}(avg)$  is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$t_{CL}(avg) = \left( \sum_{j=1}^N t_{CL_j} \right) / (N \times t_{CK}(avg))$$

*where*  $N = 200$

#### 12.1.4 Definition for $t_{JIT}(per)$

$t_{JIT}(per)$  is the single period jitter defined as the largest deviation of any signal  $t_{CK}$  from  $t_{CK}(avg)$ .

$t_{JIT}(per) = \text{Min/max of } \{t_{CK_i} - t_{CK}(avg) \text{ where } i = 1 \text{ to } 200\}$ .

$t_{JIT}(per)_{act}$  is the actual clock jitter for a given system.

$t_{JIT}(per)_{allowed}$  is the specified allowed clock period jitter.

$t_{JIT}(per)$  is not subject to production test.

### 12.1.5 Definition for $t_{JIT(cc)}$

$t_{JIT(cc)}$  is defined as the absolute difference in clock period between two consecutive clock cycles.

$t_{JIT(cc)} = \text{Max of } |\{tCK_{i+1} - tCK_i\}|$ .

$t_{JIT(cc)}$  defines the cycle to cycle jitter.

$t_{JIT(cc)}$  is not subject to production test.

### 12.1.6 Definition for $t_{ERR(nper)}$

$t_{ERR(nper)}$  is defined as the cumulative error across n multiple consecutive cycles from  $tCK(avg)$ .

$t_{ERR(nper),act}$  is the actual clock jitter over n cycles for a given system.

$t_{ERR(nper),allowed}$  is the specified allowed clock period jitter over n cycles.

$t_{ERR(nper)}$  is not subject to production test.

$$tERR(nper) = \left( \sum_{j=i}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

$t_{ERR(nper),min}$  can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68LN(n)) \times tJIT(per), min$$

$t_{ERR(nper),max}$  can be calculated by the formula shown below:

$$tERR(nper), max = (1 + 0.68LN(n)) \times tJIT(per), max$$

Using these equations,  $t_{ERR(nper)}$  tables can be generated for each  $t_{JIT(per),act}$  value.

**12.1.7 Definition for duty cycle jitter  $t_{JIT}(\text{duty})$** 

$t_{JIT}(\text{duty})$  is defined with absolute and average specification of  $t_{CH}$  /  $t_{CL}$ .

$$t_{JIT}(\text{duty}), \text{min} = \text{MIN}((t_{CH}(\text{abs}), \text{min} - t_{CH}(\text{avg}), \text{min}), (t_{CL}(\text{abs}), \text{min} - t_{CL}(\text{avg}), \text{min})) \times t_{CK}(\text{avg})$$

$$t_{JIT}(\text{duty}), \text{max} = \text{MAX}((t_{CH}(\text{abs}), \text{max} - t_{CH}(\text{avg}), \text{max}), (t_{CL}(\text{abs}), \text{max} - t_{CL}(\text{avg}), \text{max})) \times t_{CK}(\text{avg})$$

**12.1.8 Definition for  $t_{CK}(\text{abs})$ ,  $t_{CH}(\text{abs})$  and  $t_{CL}(\text{abs})$** 

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

**Table 100 — Definition for  $t_{CK}(\text{abs})$ ,  $t_{CH}(\text{abs})$ , and  $t_{CL}(\text{abs})$** 

Parameter	Symbol	Min	Unit
Absolute Clock Period	$t_{CK}(\text{abs})$	$t_{CK}(\text{avg}), \text{min} + t_{JIT}(\text{per}), \text{min}$	ps
Absolute Clock HIGH Pulse Width	$t_{CH}(\text{abs})$	$t_{CH}(\text{avg}), \text{min} + t_{JIT}(\text{duty}), \text{min} / t_{CK}(\text{avg}), \text{min}$	$t_{CK}(\text{avg})$
Absolute Clock LOW Pulse Width	$t_{CL}(\text{abs})$	$t_{CL}(\text{avg}), \text{min} + t_{JIT}(\text{duty}), \text{min} / t_{CK}(\text{avg}), \text{min}$	$t_{CK}(\text{avg})$

NOTE 1  $t_{CK}(\text{avg}), \text{min}$  is expressed in ps for this table.

NOTE 2  $t_{JIT}(\text{duty}), \text{min}$  is a negative value.

## 12.2 Period Clock Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in Table 103 and how to determine cycle time de-rating and clock cycle de-rating.

### 12.2.1 Clock period jitter effects on core timing parameters (tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW )

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR2 device is characterized and verified to support  $tnPARAM = RU\{tPARAM / tCK(avg)\}$ .

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

#### 12.2.1.1 Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter (tCORE).

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

#### 12.2.1.2 Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter (tCORE).

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

### 12.2.2 Clock jitter effects on Command/Address timing parameters (tIS, tIH, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb)

These parameters are measured from a command/address signal (CKE, CS, CA0 - CA9) transition edge to its respective clock signal (CK\_t/CK\_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per)), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

### 12.2.3 Clock jitter effects on Read timing parameters

#### 12.2.3.1 tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left( \frac{tJIT(per), act, max - tJIT(per), allowed, max}{tCK(avg)} \right)$$

For example,

if the measured jitter into a LPDDR2-800 device has tCK(avg) = 2500 ps, tJIT(per),act,min = -172 ps and tJIT(per),act,max = + 193 ps, then

tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 0.9 - (193 - 100)/2500 = .8628 tCK(avg)

#### 12.2.3.2 tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0–31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per)).

#### 12.2.3.3 tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min.

tQSH(abs)min = tCH(abs)min – 0.05

tQSL(abs)min = tCL(abs)min – 0.05

These parameters determine absolute Data-Valid window at the LPDDR2 device pin.

Absolute min data-valid window @ LPDDR2 device pin =

min { ( tQSH(abs)min \* tCK(avg)min – tDQSQmax – tQHSmax ) , ( tQSL(abs)min \* tCK(avg)min – tDQSQmax – tQHSmax ) }

This minimum data-valid window shall be met at the target frequency regardless of clock jitter.

#### 12.2.3.4 tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.

tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min



## 12.2.4 Clock jitter effects on Write timing parameters

### 12.2.4.1 tDS, tDH

These parameters are measured from a data signal (DM<sub>n</sub>, DQ<sub>m</sub>: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn<sub>t</sub>, DQSn<sub>c</sub> : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

### 12.2.4.2 tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx<sub>t</sub>, DQSx<sub>c</sub>) crossing to its respective clock signal (CK<sub>t</sub>/CK<sub>c</sub>) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

### 12.2.4.3 tDQSS

This parameter is measured from a data strobe signal (DQSx<sub>t</sub>, DQSx<sub>c</sub>) crossing to the subsequent clock signal (CK<sub>t</sub>/CK<sub>c</sub>) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act, min - tJIT(per), allowed, min}{tCK(avg)}$$

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act, max - tJIT(per), allowed, max}{tCK(avg)}$$

For example,

if the measured jitter into a LPDDR2-800 device has tCK(avg)= 2500 ps, tJIT(per),act,min= -172 ps and tJIT(per),act,max= + 193 ps, then

$$tDQSS,(min,derated) = 0.75 - (tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-172 + 100)/2500 = .7788 tCK(avg)$$

and

$$tDQSS,(max,derated) = 1.25 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (193 - 100)/2500 = 1.2128 tCK(avg)$$

## 12.3 LPDDR2-SX Refresh Requirements by Device Density

Table 101 — LPDDR2-S2 Refresh Requirement Parameters (per density)

Parameter		Symbol	64 Mb	128 Mb	256 Mb	512 Mb	1 Gb	2 Gb	4 Gb	6 Gb	8 Gb	Unit
Number of Banks			4						8			
Refresh Window $T_{case} \leq 85^{\circ}\text{C}$		$t_{\text{REFW}}$	32									ms
Refresh Window $85^{\circ}\text{C} < T_{case} \leq 105^{\circ}\text{C}$		$t_{\text{REFW}}$	8									ms
Required number of REFRESH commands (min)		R	2,048	2,048	4,096	4,096	4096	8,192	8,192	8,192	8,192	
average time between REFRESH commands (for reference only) $T_{case} \leq 85^{\circ}\text{C}$	REFab	$t_{\text{REFI}}$	15.6	15.6	7.8	7.8	7.8	3.9	3.9	3.9	3.9	us
	REFpb	$t_{\text{REFIpb}}$	(REFpb not allowed below 4Gb)						0.4875	0.4875	0.4875	us
Refresh Cycle time		$t_{\text{RFCab}}$	90	90	90	90	130	130	130	210	210	ns
Per Bank Refresh Cycle time		$t_{\text{RFCpb}}$	NA						60	90	90	ns
Burst Refresh Window = $4 \times 8 \times t_{\text{RFCab}}$		$t_{\text{REFBW}}$	2.88	2.88	2.88	2.88	4.16	4.16	4.16	6.72	6.72	us

NOTE 1: Please refer to the addressing [Table 3](#).

Table 102 — LPDDR2-S4 Refresh Requirement Parameters (per density)

Parameter		Symbol	64 Mb	128 Mb	256 Mb	512 Mb	1 Gb	2 Gb	4 Gb	6 Gb	8 Gb	Unit
Number of Banks			4				8					
Refresh Window $T_{case} \leq 85^{\circ}\text{C}$		$t_{REFW}$	32									ms
Refresh Window $85^{\circ}\text{C} < T_{case} \leq 105^{\circ}\text{C}$		$t_{REFW}$	8									ms
Required number of REFRESH commands (min)		R	2,048	2,048	4,096	4,096	4,096	8,192	8,192	8,192	8,192	
average time between REFRESH commands (for reference only) $T_{case} \leq 85^{\circ}\text{C}$	REFab	$t_{REFI}$	15.6	15.6	7.8	7.8	7.8	3.9	3.9	3.9	3.9	us
	REFpb	$t_{REFIpb}$	(REFpb not allowed below 1 Gb.)				0.975	0.4875	0.4875	0.4875	0.4875	us
Refresh Cycle time		$t_{RFCab}$	90	90	90	90	130	130	130	210	210	ns
Per Bank Refresh Cycle time		$t_{RFCpb}$	NA				60	60	60	90	90	ns
Burst Refresh Window = $4 \times 8 \times t_{RFCab}$		$t_{REFBW}$	2.88	2.88	2.88	2.88	4.16	4.16	4.16	6.72	6.72	us

NOTE 1: Please refer to the addressing [Table 3](#).

## 12.4 AC Timings

Table 103 — LPDDR2 AC Timing Table<sup>\*9</sup>

Parameter	Symbol	min max	min t <sub>CK</sub>	LPDDR2										Unit
				1066	933	800	667	533	466 <sup>*5</sup>	400	333	266 <sup>*5</sup>	200 <sup>*5</sup>	
Max. Frequency <sup>*4</sup>		~		533	466	400	333	266	233	200	166	133	100	MHz
Clock Timing														
Average Clock Period	t <sub>CK</sub> (avg)	min		1.875	2.15	2.5	3	3.75	4.3	5	6	7.5	10	ns
		max		100										
Average high pulse width	t <sub>CH</sub> (avg)	min		0.45										t <sub>CK</sub> (avg)
		max		0.55										
Average low pulse width	t <sub>CL</sub> (avg)	min		0.45										t <sub>CK</sub> (avg)
		max		0.55										
Absolute Clock Period	t <sub>CK</sub> (abs)	min		t <sub>CK</sub> (avg)min + t <sub>JIT</sub> (per),min										ps
Absolute clock HIGH pulse width (with allowed jitter)	t <sub>CH</sub> (abs), allowed	min		0.43										t <sub>CK</sub> (avg)
		max		0.57										t <sub>CK</sub> (avg)
Absolute clock LOW pulse width (with allowed jitter)	t <sub>CL</sub> (abs), allowed	min		0.43										t <sub>CK</sub> (avg)
		max		0.57										t <sub>CK</sub> (avg)
Clock Period Jitter (with allowed jitter)	t <sub>JIT</sub> (per), allowed	min		-90	-95	-100	-110	-120	-130	-140	-150	-180	-250	ps
		max		90	95	100	110	120	130	140	150	180	250	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	t <sub>JIT</sub> (cc), allowed	max		180	190	200	220	240	260	280	300	360	500	ps
Duty cycle Jitter (with allowed jitter)	t <sub>JIT</sub> (duty), allowed	min		min((t <sub>CH</sub> (abs),min - t <sub>CH</sub> (avg),min), (t <sub>CL</sub> (abs),min - t <sub>CL</sub> (avg),min)) * t <sub>CK</sub> (avg)										ps
		max		max((t <sub>CH</sub> (abs),max - t <sub>CH</sub> (avg),max), (t <sub>CL</sub> (abs),max - t <sub>CL</sub> (avg),max)) * t <sub>CK</sub> (avg)										ps
Cumulative error across 2 cycles	t <sub>ERR</sub> (2per), allowed	min		-132	-140	-147	-162	-177	-191	-206	-221	-265	-368	ps
		max		132	140	147	162	177	191	206	221	265	368	
Cumulative error across 3 cycles	t <sub>ERR</sub> (3per), allowed	min		-157	-166	-175	-192	-210	-227	-245	-262	-314	-437	ps
		max		157	166	175	192	210	227	245	262	314	437	
Cumulative error across 4 cycles	t <sub>ERR</sub> (4per), allowed	min		-175	-185	-194	-214	-233	-253	-272	-291	-350	-486	ps
		max		175	185	194	214	233	253	272	291	350	486	
Cumulative error across 5 cycles	t <sub>ERR</sub> (5per), allowed	min		-188	-199	-209	-230	-251	-272	-293	-314	-377	-524	ps
		max		188	199	209	230	251	272	293	314	377	524	
Cumulative error across 6 cycles	t <sub>ERR</sub> (6per), allowed	min		-200	-211	-222	-244	-266	-288	-311	-333	-399	-555	ps
		max		200	211	222	244	266	288	311	333	399	555	
Cumulative error across 7 cycles	t <sub>ERR</sub> (7per), allowed	min		-209	-221	-232	-256	-279	-302	-325	-348	-418	-581	ps
		max		209	221	232	256	279	302	325	348	418	581	
Cumulative error across 8 cycles	t <sub>ERR</sub> (8per), allowed	min		-217	-229	-241	-266	-290	-314	-338	-362	-435	-604	ps
		max		217	229	241	266	290	314	338	362	435	604	
Cumulative error across 9 cycles	t <sub>ERR</sub> (9per), allowed	min		-224	-237	-249	-274	-299	-324	-349	-374	-449	-624	ps
		max		224	237	249	274	299	324	349	374	449	624	
Cumulative error across 10 cycles	t <sub>ERR</sub> (10per), allowed	min		-231	-244	-257	-282	-308	-334	-359	-385	-462	-641	ps
		max		231	244	257	282	308	334	359	385	462	641	



**Table 103 — LPDDR2 AC Timing Table<sup>\*9</sup>**

Parameter	Symbol	min max	min t <sub>CK</sub>	LPDDR2										Unit
				1066	933	800	667	533	466 <sup>*5</sup>	400	333	266 <sup>*5</sup>	200 <sup>*5</sup>	
ZQ Calibration Parameters														
Initialization Calibration Time	t <sub>ZQINIT</sub>	min		1										us
Long Calibration Time	t <sub>ZQCL</sub>	min	6	360										ns
Short Calibration Time	t <sub>ZQCS</sub>	min	6	90										ns
Calibration Reset Time	t <sub>ZQRESET</sub>	min	3	50										ns
Read Parameters <sup>*14</sup>														
DQS output access time from CK_t/CK_c	t <sub>DQSCK</sub>	min		2500										ps
		max		5500										
DQSCK Delta Short <sup>*18</sup>	t <sub>DQSCKDS</sub>	max		330	380	450	540	670	770	900	1080	1350	1800	ps
DQSCK Delta Medium <sup>*19</sup>	t <sub>DQSCKDM</sub>	max		680	780	900	1050	1350	1550	1800	1900	2000	2100	ps
DQSCK Delta Long <sup>*20</sup>	t <sub>DQSCKDL</sub>	max		920	1050	1200	1400	1800	2100	2400	-	-	-	ps
DQS - DQ skew	t <sub>DQSQ</sub>	max		200	220	240	280	340	370	400	500	600	700	ps
Data hold skew factor	t <sub>QHS</sub>	max		230	260	280	340	400	450	480	600	750	1000	ps
DQS Output High Pulse Width	t <sub>QSH</sub>	min		t <sub>CH</sub> (abs) - 0.05										t <sub>CK</sub> (avg)
DQS Output Low Pulse Width	t <sub>QSL</sub>	min		t <sub>CL</sub> (abs) - 0.05										t <sub>CK</sub> (avg)
Data Half Period	t <sub>QHP</sub>	min		min(t <sub>QSH</sub> , t <sub>QSL</sub> )										t <sub>CK</sub> (avg)
DQ / DQS output hold time from DQS	t <sub>QH</sub>	min		t <sub>QHP</sub> - t <sub>QHS</sub>										ps
Read preamble <sup>*15,*16</sup>	t <sub>RPRE</sub>	min		0.9										t <sub>CK</sub> (avg)
Read postamble <sup>*15,*17</sup>	t <sub>RPST</sub>	min		t <sub>CL</sub> (abs) - 0.05										t <sub>CK</sub> (avg)
DQS low-Z from clock <sup>*15</sup>	t <sub>LZ</sub> (DQS)	min		t <sub>DQSCK</sub> (MIN) - 300										ps
DQ low-Z from clock <sup>*15</sup>	t <sub>LZ</sub> (DQ)	min		t <sub>DQSCK</sub> (MIN) - (1.4 * t <sub>QHS</sub> (MAX))										ps
DQS high-Z from clock <sup>*15</sup>	t <sub>HZ</sub> (DQS)	max		t <sub>DQSCK</sub> (MAX) - 100										ps
DQ high-Z from clock <sup>*15</sup>	t <sub>HZ</sub> (DQ)	max		t <sub>DQSCK</sub> (MAX) + (1.4 * t <sub>DQSQ</sub> (MAX))										ps

### Table 103 — LPDDR2 AC Timing Table<sup>\*9</sup>

Parameter	Symbol	min max	min t <sub>CK</sub>	LPDDR2										Unit
				1066	933	800	667	533	466 <sup>*5</sup>	400	333	266 <sup>*5</sup>	200 <sup>*5</sup>	
Write Parameters <sup>*14</sup>														
DQ and DM input hold time (Vref based)	t <sub>DH</sub>	min		210	235	270	350	430	450	480	600	750	1000	ps
DQ and DM input setup time (Vref based)	t <sub>DS</sub>	min		210	235	270	350	430	450	480	600	750	1000	ps
DQ and DM input pulse width	t <sub>DIPW</sub>	min		0.35										t <sub>CK</sub> (avg)
Write command to 1st DQS latching transition	t <sub>DQSS</sub>	min		0.75										t <sub>CK</sub> (avg)
		max		1.25										
DQS input high-level width	t <sub>DQSH</sub>	min		0.4										t <sub>CK</sub> (avg)
DQS input low-level width	t <sub>DQSL</sub>	min		0.4										t <sub>CK</sub> (avg)
DQS falling edge to CK setup time	t <sub>DSS</sub>	min		0.2										t <sub>CK</sub> (avg)
DQS falling edge hold time from CK	t <sub>DSH</sub>	min		0.2										t <sub>CK</sub> (avg)
Write postamble	t <sub>WPST</sub>	min		0.4										t <sub>CK</sub> (avg)
Write preamble	t <sub>WPRE</sub>	min		0.35										t <sub>CK</sub> (avg)

**Table 103 — LPDDR2 AC Timing Table<sup>\*9</sup>**

Parameter	Symbol	min max	min t <sub>CK</sub>	LPDDR2										Unit
				1066	933	800	667	533	466 <sup>*5</sup>	400	333	266 <sup>*5</sup>	200 <sup>*5</sup>	
CKE Input Parameters														
CKE min. pulse width (high and low pulse width)	t <sub>CKE</sub>	min	3	3										t <sub>CK</sub> (avg)
CKE input setup time	t <sub>ISCKE</sub> *2	min		0.25										t <sub>CK</sub> (avg)
CKE input hold time	t <sub>IHCKE</sub> *3	min		0.25										t <sub>CK</sub> (avg)
Command Address Input Parameters <sup>*14</sup>														
Address and control input setup time (Vref based)	t <sub>IS</sub> <sup>*1</sup>	min		220	250	290	370	460	520	600	740	900	1150	ps
Address and control input hold time (Vref based)	t <sub>IH</sub> <sup>*1</sup>	min		220	250	290	370	460	520	600	740	900	1150	ps
Address and control input pulse width	t <sub>IPW</sub>	min		0.40										t <sub>CK</sub> (avg)
Boot Parameters (10 MHz - 55 MHz) <sup>*8,10,11</sup>														
Clock Cycle Time	t <sub>CKb</sub>	max	-	100										ns
		min		18										
CKE Input Setup Time	t <sub>ISCKEb</sub>	min	-	2.5										ns
CKE Input Hold Time	t <sub>IHCKEb</sub>	min	-	2.5										ns
Address & Control Input Setup Time	t <sub>ISb</sub>	min	-	1150										ps
Address & Control Input Hold Time	t <sub>IHb</sub>	min	-	1150										ps
DQS Output Data Access Time from CK_t/CK_c	t <sub>DQSCKb</sub>	min	-	2.0										ns
		max		10.0										
Data Strobe Edge to Ouput Data Edge t <sub>DQSQb</sub> - 1.2	t <sub>DQSQb</sub>	max	-	1.2										ns
Data Hold Skew Factor	t <sub>QHSb</sub>	max	-	1.2										ns
Mode Register Parameters														
MODE REGISTER Write command period	t <sub>MRW</sub>	min	5	5										t <sub>CK</sub> (avg)
Mode Register Read command period	t <sub>MRR</sub>	min	2	2										t <sub>CK</sub> (avg)

**Table 103 — LPDDR2 AC Timing Table<sup>\*9</sup>**

Parameter	Symbol	min max	min t <sub>CK</sub>	LPDDR2										Unit
				1066	933	800	667	533	466 <sup>*5</sup>	400	333	266 <sup>*5</sup>	200 <sup>*5</sup>	
LPDDR2 SDRAM Core Parameters <sup>*12</sup>														
Read Latency	RL	min	3	8	7	6	5	4		3	3			t <sub>CK</sub> (avg)
Write Latency	WL	min	1	4	4	3	2	2		1	1			t <sub>CK</sub> (avg)
ACTIVE to ACTIVE command period	t <sub>RC</sub>	min		t <sub>RAS</sub> + t <sub>RPab</sub> (with all-bank Precharge) t <sub>RAS</sub> + t <sub>RPpb</sub> (with per-bank Precharge)										ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	t <sub>CKESR</sub>	min	3	15						15				ns
Self refresh exit to next valid command delay	t <sub>XSR</sub>	min	2	t <sub>RFCab</sub> + 10										ns
Exit power down to next valid command delay	t <sub>XP</sub>	min	2	7.5						7.5				ns
LPDDR2-S4 CAS to CAS delay	t <sub>CCD</sub>	min	2	2						2				t <sub>CK</sub> (avg)
LPDDR2-S2 CAS to CAS delay	t <sub>CCD</sub>	min	1	1						1				t <sub>CK</sub> (avg)
Internal Read to Precharge command delay	t <sub>RTP</sub>	min	2	7.5						7.5				ns
RAS to CAS Delay	t <sub>RCD</sub>	Fast	3	15						15				ns
		Typ	3	18						18				ns
		Slow	3	24						24				ns
Row Precharge Time (single bank)	t <sub>RPpb</sub>	Fast	3	15						15				ns
		Typ	3	18						18				ns
		Slow	3	24						24				ns
Row Precharge Time (all banks)	t <sub>RPab</sub> 4-bank	Fast	3	15						15				ns
		Typ	3	18						18				ns
		Slow	3	24						24				ns
Row Precharge Time (all banks)	t <sub>RPab</sub> 8-bank	Fast	3	18						18				ns
		Typ	3	21						21				ns
		Slow	3	27						27				ns
Row Active Time	t <sub>RAS</sub>	min	3	42						42				ns
		max	-	70						70				us
Write Recovery Time	t <sub>WR</sub>	min	3	15						15				ns
Internal Write to Read Command Delay	t <sub>WTR</sub>	min	2	7.5						10				ns
Active bank A to Active bank B	t <sub>RRD</sub>	min	2	10						10				ns
Four Bank Activate Window	t <sub>FAW</sub>	min	8	50						50	60			ns
Minimum Deep Power Down Time	t <sub>DPD</sub>	min		500						500				us



**Table 103 — LPDDR2 AC Timing Table<sup>\*9</sup>**

Parameter	Symbol	min max	min t <sub>CK</sub>	LPDDR2										Unit
				1066	933	800	667	533	466 <sup>*5</sup>	400	333	266 <sup>*5</sup>	200 <sup>*5</sup>	
LPDDR2 NVM Core Parameters <sup>*12</sup>														
Read Latency	RL	min	3	8	7	6	5	4		3			t <sub>CK</sub> (avg)	
Write Latency	WL	min	1	4		3	2			1			t <sub>CK</sub> (avg)	
Activate to Read/Write command period (min)	t <sub>RCD</sub> MIN	min		15									ns	
		max		255									ns	
Activate to Read/Write command period	t <sub>RCD</sub> <sup>*6, *21</sup>	min	5	t <sub>RCD</sub> MIN									ns	
Activate to Activate command period (different Row Buffer)	t <sub>RRD</sub> <sup>*7, *21</sup>	min	5	t <sub>RCD</sub> MIN									ns	
Activate to Activate command period (same Row Buffer)	t <sub>RC</sub> <sup>*21</sup>	min	5	t <sub>RCD</sub> MIN									ns	
CAS to CAS delay	t <sub>CCD</sub>	min	2	2									t <sub>CK</sub> (avg)	
Write recovery time before Activate	t <sub>WRA</sub>	min	3	15									ns	
Internal write to read command delay	t <sub>WTR</sub>	min	2	7.5					10					ns
Preactive to Activate command period	t <sub>RP</sub>	min	3	3									t <sub>CK</sub> (avg)	
Activate to Preactive command period	t <sub>RAS</sub> <sup>*21</sup>	min	5	t <sub>RCD</sub> MIN									ns	
Exit power down to next valid command delay	t <sub>XP</sub>	min	2	10									ns	

**Table 103 — LPDDR2 AC Timing Table<sup>\*9</sup>**

Parameter	Symbol	min max	min t <sub>CK</sub>	LPDDR2										Unit
				1066	933	800	667	533	466 <sup>*5</sup>	400	333	266 <sup>*5</sup>	200 <sup>*5</sup>	
LPDDR2 Temperature De-Rating														
t <sub>DQSK</sub> De-Rating	t <sub>DQSK</sub> (Derated)	max		5620	6000									ps
Core Timings Temperature De-Rating for SDRAM	t <sub>RCD</sub> (Derated)	min		t <sub>RCD</sub> + 1.875									ns	
	t <sub>RC</sub> (Derated)	min		t <sub>RC</sub> + 1.875									ns	
	t <sub>RAS</sub> (Derated)	min		t <sub>RAS</sub> + 1.875									ns	
	t <sub>RP</sub> (Derated)	min		t <sub>RP</sub> + 1.875									ns	
	t <sub>RRD</sub> (Derated)	min		t <sub>RRD</sub> + 1.875									ns	
Core Timings Temperature De-Rating for NVM <sup>*22</sup>	t <sub>RCD</sub> (Derated)	min		t <sub>RCD</sub> + t <sub>NVMDERATING</sub>									ns	
	t <sub>RC</sub> (Derated)	min		t <sub>RC</sub> + t <sub>NVMDERATING</sub>									ns	
	t <sub>RAS</sub> (Derated)	min		t <sub>RAS</sub> + t <sub>NVMDERATING</sub>									ns	
	t <sub>RRD</sub> (Derated)	min		t <sub>RRD</sub> + t <sub>NVMDERATING</sub>									ns	

NOTE 1 Input set-up/hold time for signal(CA0 ~ 9, CS\_n)

NOTE 2 CKE input setup time is measured from CKE reaching high/low voltage level to CK\_t/CK\_c crossing.

NOTE 3 CKE input hold time is measured from CK\_t/CK\_c crossing to CKE reaching high/low voltage level .

NOTE 4 Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.

NOTE 5 The speed bins 466, 266, and 200 are for NVM only.

NOTE 6 For NVM, t<sub>RCDMIN</sub> defines the minimum tRCD value. Vendors may choose a minimum tRCD value within the range of t<sub>RCDMIN</sub>.

NOTE 7 For NVM, vendors may choose a value for tRRD that is less than or equal to the tRCD value.

NOTE 8 To guarantee device operation before the LPDDR2 device is configured a number of AC boot timing parameters are defined in the [Table 103](#) . Boot parameter symbols have the letter **b** appended, e.g., tCK during boot is t<sub>CKb</sub>.

NOTE 9 Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.

NOTE 10 The SDRAM/NVM will set some Mode register default values upon receiving a RESET (MRW) command as specified in [3.5](#).

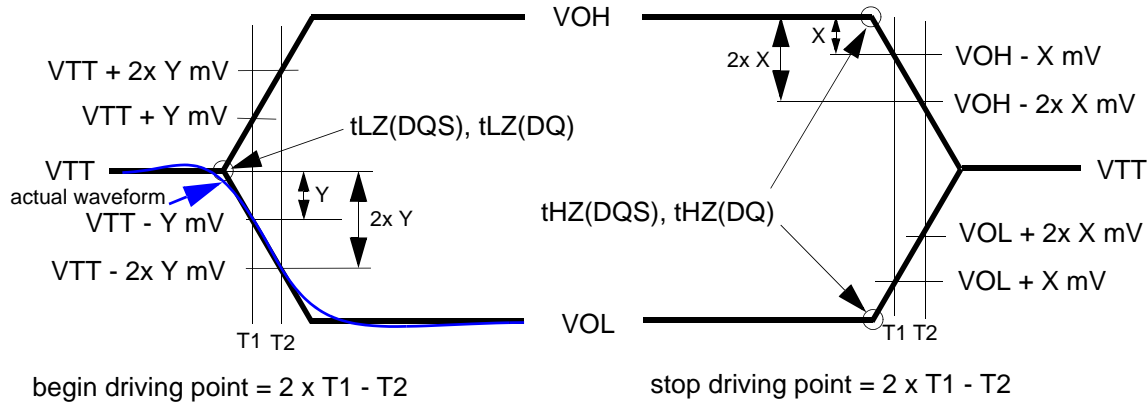
NOTE 11 The output skew parameters are measured with Ron default settings into the reference load.

NOTE 12 The min tCK column applies only when tCK is greater than 6ns for LPDDR2-SX devices and 10ns for LPDDR2-N devices. In this case, both min tCK values and analog timings (ns) shall be satisfied.

NOTE 13 All AC timings assume an input slew rate of 1V/ns.

NOTE 14 Read, Write, and Input Setup and Hold values are referenced to Vref.

## 12.4 AC Timings (cont'd)



**Figure 120 — HSUL\_12 Driver Output Reference Load for Timing and Slew Rate**

The parameters  $tLZ(DQS)$ ,  $tLZ(DQ)$ ,  $tHZ(DQS)$ , and  $tHZ(DQ)$  are defined as single-ended. The timing parameters  $tRPRE$  and  $tRPST$  are determined from the differential signal  $DQS\_t - DQS\_c$ .

**NOTE 15** For low-to-high and high-to-low transitions, the timing reference will be at the point when the signal crosses  $V_{TT}$ .  $tHZ$  and  $tLZ$  transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for  $tRPST$ ,  $tHZ(DQS)$  and  $tHZ(DQ)$ ), or begins driving (for  $tRPRE$ ,  $tLZ(DQS)$ ,  $tLZ(DQ)$ ). Figure 120 shows a method to calculate the point when device is no longer driving  $tHZ(DQS)$  and  $tHZ(DQ)$ , or begins driving  $tLZ(DQS)$ ,  $tLZ(DQ)$  by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

**NOTE 16** Measured from the start driving of  $DQS\_t - DQS\_c$  to the start driving the first rising strobe edge.

**NOTE 17** Measured from the from start driving the last falling strobe edge to the stop driving  $DQS\_t - DQS\_c$ .

**NOTE 18**  $tDQCKDS$  is the absolute value of the difference between any two  $tDQCK$  measurements (within a byte lane) within a contiguous sequence of bursts within a 160ns rolling window.  $tDQCKDS$  is not tested and is guaranteed by design. Temperature drift in the system is  $< 10C/s$ . Values do not include clock jitter.

**NOTE 19**  $tDQCKDM$  is the absolute value of the difference between any two  $tDQCK$  measurements (within a byte lane) within a 1.6us rolling window.  $tDQCKDM$  is not tested and is guaranteed by design. Temperature drift in the system is  $< 10C/s$ . Values do not include clock jitter.

**NOTE 20**  $tDQCKDL$  is the absolute value of the difference between any two  $tDQCK$  measurements (within a byte lane) within a 32ms rolling window.  $tDQCKDL$  is not tested and is guaranteed by design. Temperature drift in the system is  $< 10C/s$ . Values do not include clock jitter.

**NOTE 21** Min  $tCK$  of 5 clocks is valid when the Overlay Window is disabled. Refer to vendor datasheets for min  $tCK$  when the Overlay Window is enabled.

**NOTE 22** For LPDDR2-NVM De-rating, the de-rating value found in MR20 OP5:OP4 ( $t_{NVMDETERATING}$ ) shall be used to de-rate the following parameters:  $tRCD$ ,  $tRRD$ ,  $tRAS$ , and  $tRC$ .

## 12.5 CA and CS\_n Setup, Hold and Derating

For all input signals (CA and CS\_n) the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see [Table 104](#)) to the  $\Delta tIS$  and  $\Delta tIH$  derating value (see [Table 105](#) and [Table 106](#)) respectively. Example: tIS (total setup time) = tIS(base) +  $\Delta tIS$ .

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{REF(dc)}$  and the first crossing of  $V_{IH(ac)min}$ . Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{REF(dc)}$  and the first crossing of  $V_{IL(ac)max}$ . If the actual signal is always earlier than the nominal slew rate line between shaded ' $V_{REF(dc)}$  to ac region', use nominal slew rate for derating value (see [Figure 121](#)). If the actual signal is later than the nominal slew rate line anywhere between shaded ' $V_{REF(dc)}$  to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see [Figure 123](#)).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{IL(dc)max}$  and the first crossing of  $V_{REF(dc)}$ . Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{IH(dc)min}$  and the first crossing of  $V_{REF(dc)}$ . If the actual signal is always later than the nominal slew rate line between shaded ' $dc$  to  $V_{REF(dc)}$  region', use nominal slew rate for derating value (see [Figure 122](#)). If the actual signal is earlier than the nominal slew rate line anywhere between shaded ' $dc$  to  $V_{REF(dc)}$  region', the slew rate of a tangent line to the actual signal from the dc level to  $V_{REF(dc)}$  level is used for derating value (see [Figure 124](#)).

For a valid transition the input signal has to remain above/below  $V_{IH/IL(ac)}$  for some time  $t_{VAC}$  (see [Table 107](#)).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached  $V_{IH/IL(ac)}$  at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach  $V_{IH/IL(ac)}$ .

For slew rates in between the values listed in [Table 105](#), the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

**Table 104 — CA and CS\_n Setup and Hold Base-Values for 1V/ns**

unit [ps]	LPDDR2						reference
	1066	933	800	667	533	466	
tIS(base)	0	30	70	150	240	300	$V_{IH/L(ac)} = V_{REF(dc)} \pm 220mV$
tIH(base)	90	120	160	240	330	390	$V_{IH/L(dc)} = V_{REF(dc)} \pm 130mV$

unit [ps]	LPDDR2				reference
	400	333	266	200	
tIS(base)	300	440	600	850	$V_{IH/L(ac)} = V_{REF(dc)} \pm 300mV$
tIH(base)	400	540	700	950	$V_{IH/L(dc)} = V_{REF(dc)} \pm 200mV$

NOTE 1 ac/dc referenced for 1V/ns CA and CS\_n slew rate and 2V/ns differential CK\_t-CK\_c slew rate.

## 12.5 CA and CS\_n Setup, Hold and Derating (cont'd)

**Table 105 — Derating values LPDDR2 tIS/tIH - ac/dc based AC220**

ΔtIS, ΔtIH derating in [ps] AC/DC based AC220 Threshold -> VIH(ac)=VREF(dc)+220mV, VIL(ac)=VREF(dc)-220mV DC100 Threshold -> VIH(dc)=VREF(dc)+130mV, VIL(dc)=VREF(dc)-130mV																	
		CK_t,CK_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

NOTE 1 Cell contents shaded in red are defined as 'not supported'.

**Table 106 — Derating values LPDDR2 tIS/tIH - ac/dc based - AC300**

ΔtIS, ΔtIH derating in [ps] AC/DC based AC300 Threshold -> VIH(ac)=VREF(dc)+300mV, VIL(ac)=VREF(dc)-300mV DC200 Threshold -> VIH(dc)=VREF(dc)+200mV, VIL(dc)=VREF(dc)-200mV																	
		CK_t,CK_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

NOTE 1 Cell contents shaded in red are defined as 'not supported'.

**Table 107 — Required time  $t_{VAC}$  above  $V_{IH}(ac)$  {below  $V_{IL}(ac)$ } for valid transition**

Slew Rate [V/ns]	$t_{VAC}$ @ 300mV [ps]		$t_{VAC}$ @ 220mV [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
< 0.5	0	-	150	-

## 12.5 CA and CS\_n Setup, Hold and Derating (cont'd)

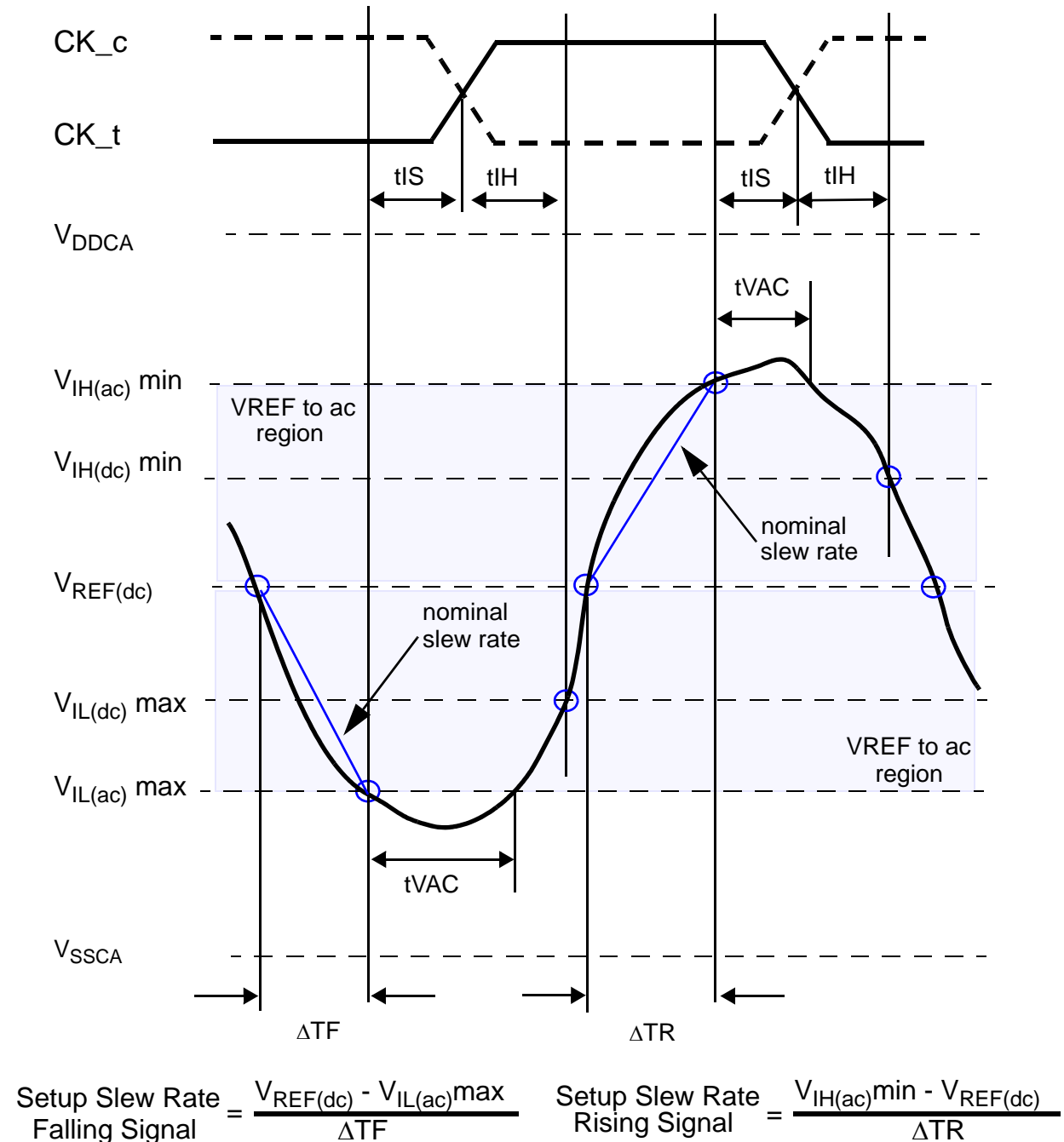


Figure 121 — Illustration of nominal slew rate and  $t_{VAC}$  for setup time  $t_{IS}$  for CA and CS\_n with respect to clock.

## 12.5 CA and CS\_n Setup, Hold and Derating (cont'd)

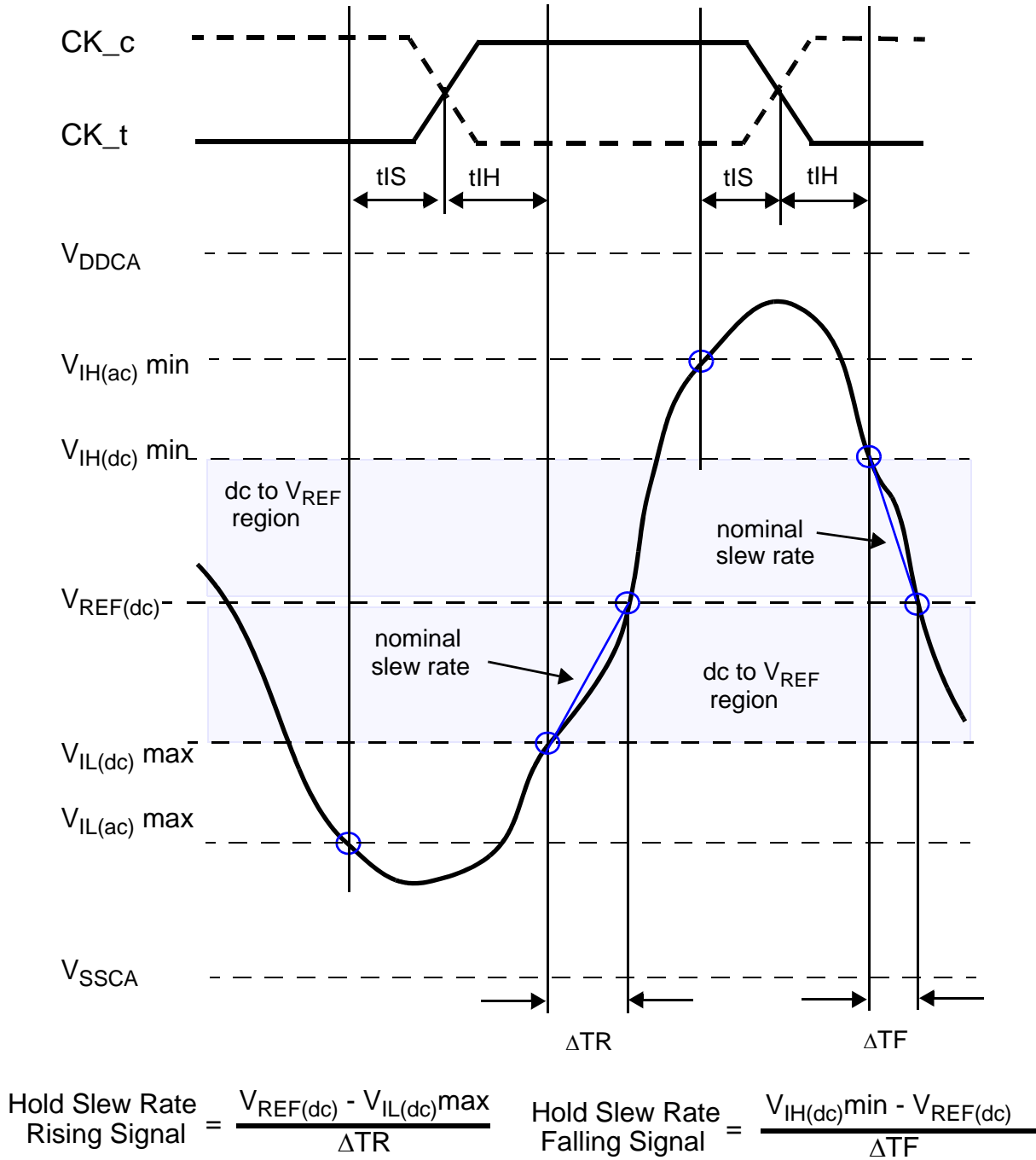


Figure 122 — Illustration of nominal slew rate for hold time  $t_{IH}$  for CA and CS\_n with respect to clock

## 12.5 CA and CS\_n Setup, Hold and Derating (cont'd)

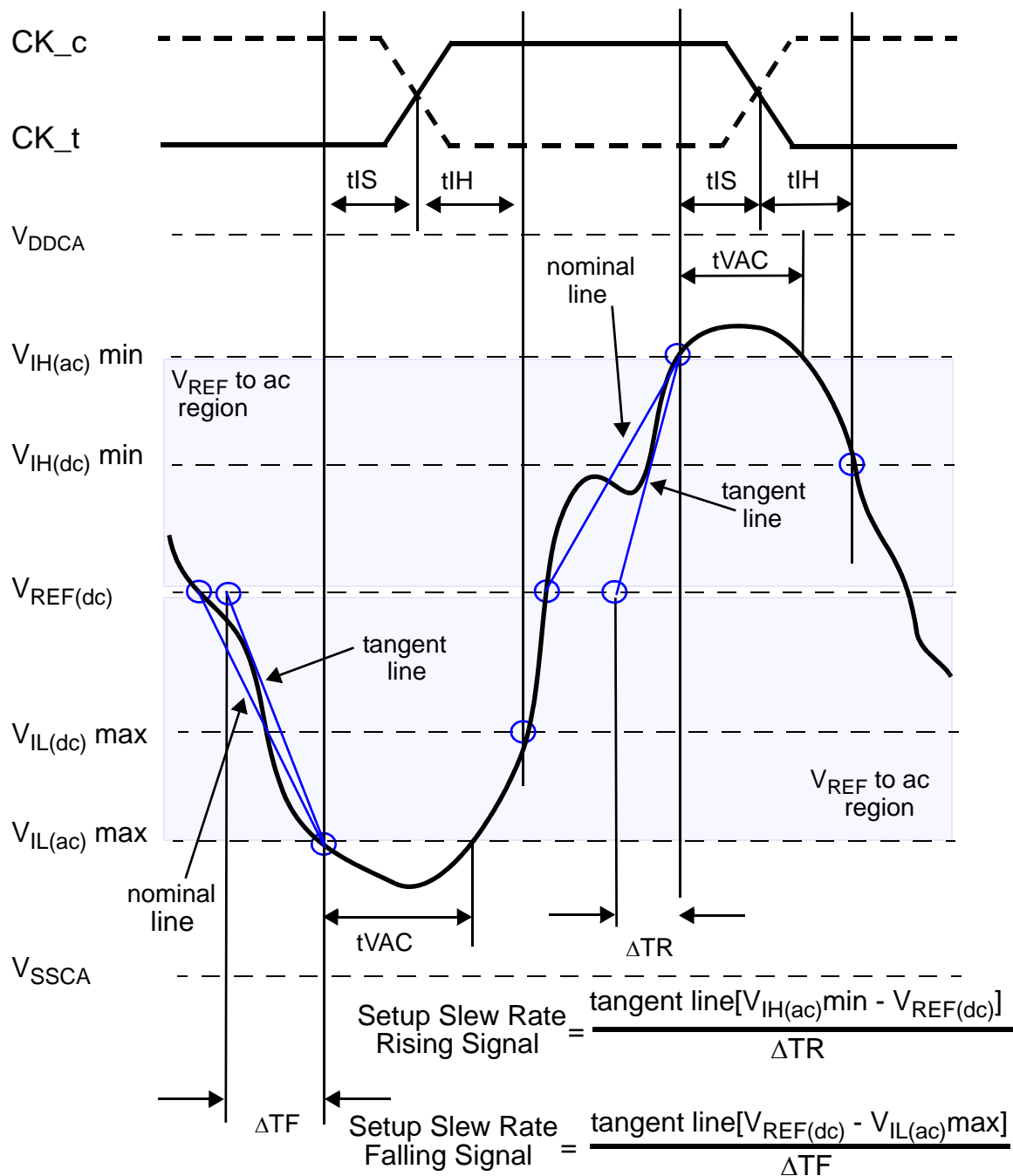


Figure 123 — Illustration of tangent line for setup time  $t_{IS}$   
for CA and CS\_n with respect to clock



## 12.5 CA and CS\_n Setup, Hold and Derating (cont'd)

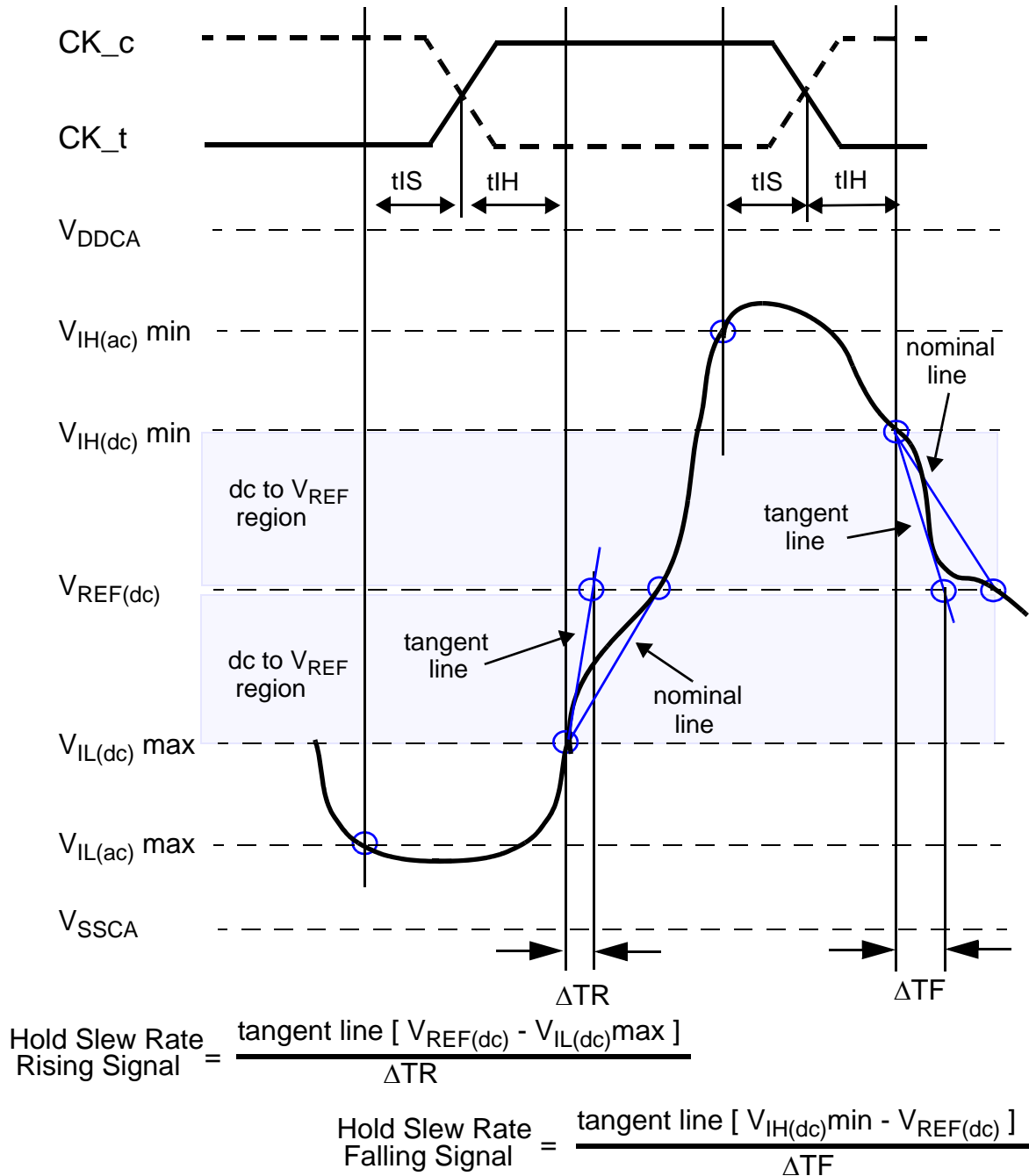


Figure 124 — Illustration of tangent line for for hold time  $t_{IH}$   
for CA and CS\_n with respect to clock

## 12.6 Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see [Table 108](#)) to the  $\Delta tDS$  and  $\Delta tDH$  (see [Table 109](#) and [Table 110](#)) derating value respectively. Example: tDS (total setup time) = tDS(base) +  $\Delta tDS$ .

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{REF(dc)}$  and the first crossing of  $V_{IH(ac)min}$ . Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{REF(dc)}$  and the first crossing of  $V_{IL(ac)max}$  (see [Figure 125](#)). If the actual signal is always earlier than the nominal slew rate line between shaded ' $V_{REF(dc)}$  to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded ' $V_{REF(dc)}$  to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see [Figure 127](#)).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{IL(dc)max}$  and the first crossing of  $V_{REF(dc)}$ . Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{IH(dc)min}$  and the first crossing of  $V_{REF(dc)}$  (see [Figure 126](#)). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to  $V_{REF(dc)}$  region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to  $V_{REF(dc)}$  region', the slew rate of a tangent line to the actual signal from the dc level to  $V_{REF(dc)}$  level is used for derating value (see [Figure 128](#)).

For a valid transition the input signal has to remain above/below  $V_{IH/IL(ac)}$  for some time  $t_{VAC}$  (see [Table 111](#)).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached  $V_{IH/IL(ac)}$  at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach  $V_{IH/IL(ac)}$ .

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

**Table 108 — Data Setup and Hold Base-Values**

[ps]	LPDDR2						reference
	1066	933	800	667	533	466	
tDS(base)	-10	15	50	130	210	230	$V_{IH/L(ac)} = V_{REF(dc)} \pm 220mV$
tDH(base)	80	105	140	220	300	320	$V_{IH/L(dc)} = V_{REF(dc)} \pm 130mV$

unit [ps]	LPDDR2				reference
	400	333	266	200	
tDS(base)	180	300	450	700	$V_{IH/L(ac)} = V_{REF(dc)} \pm 300mV$
tDH(base)	280	400	550	800	$V_{IH/L(dc)} = V_{REF(dc)} \pm 200mV$

NOTE 1 ac/dc referenced for 1V/ns DQ, DM slew rate and 2V/ns differential DQS\_t-DQS\_c slew rate.

## 12.6 Data Setup, Hold and Slew Rate Derating (cont'd)

**Table 109 — Derating values LPDDR2 tDS/tDH - ac/dc based AC220**

$\Delta t_{DS}$ , $\Delta t_{DH}$ derating in [ps] AC/DC based AC220 Threshold -> $V_{IH}(ac)=V_{REF}(dc)+220mV$ , $V_{IL}(ac)=V_{REF}(dc)-220mV$ DC130 Threshold -> $V_{IH}(dc)=V_{REF}(dc)+130mV$ , $V_{IL}(dc)=V_{REF}(dc)-130mV$																	
		DQS_t, DQS_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$
DQ,DM Slew rate V/ns	2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
	1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
	0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
	0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
	0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
	0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

NOTE 1 Cell contents shaded in red are defined as 'not supported'.

**Table 110 — Derating values LPDDR2 tDS/tDH - ac/dc based AC300**

$\Delta t_{DS}$ , $\Delta t_{DH}$ derating in [ps] AC/DC based AC300 Threshold -> $V_{IH}(ac)=V_{REF}(dc)+300mV$ , $V_{IL}(ac)=V_{REF}(dc)-300mV$ DC200 Threshold -> $V_{IH}(dc)=V_{REF}(dc)+200mV$ , $V_{IL}(dc)=V_{REF}(dc)-200mV$																	
		DQS_t, DQS_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$
DQ,DM Slew rate V/ns	2.0	150	100	150	100	150	100	-	-	-	-	-	-	-	-	-	-
	1.5	100	67	100	67	100	67	116	83	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-4	-8	-4	-8	12	8	28	24	44	40	-	-	-	-
	0.8	-	-	-	-	-12	-20	4	-4	20	12	36	28	52	48	-	-
	0.7	-	-	-	-	-	-	-3	-18	13	-2	29	14	45	34	61	66
	0.6	-	-	-	-	-	-	-	-	2	-21	18	-5	34	15	50	47
	0.5	-	-	-	-	-	-	-	-	-	-	-12	-32	4	-12	20	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-35	-40	-11	-8

NOTE 1 Cell contents shaded in red are defined as 'not supported'.

**Table 111 — Required time  $t_{VAC}$  above  $V_{IH}(ac)$  {below  $V_{IL}(ac)$ } for valid transition**

Slew Rate [V/ns]	$t_{VAC}$ @ 300mV [ps]		$t_{VAC}$ @ 220mV [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
< 0.5	0	-	150	-

## 12.6 Data Setup, Hold and Slew Rate Derating (cont'd)

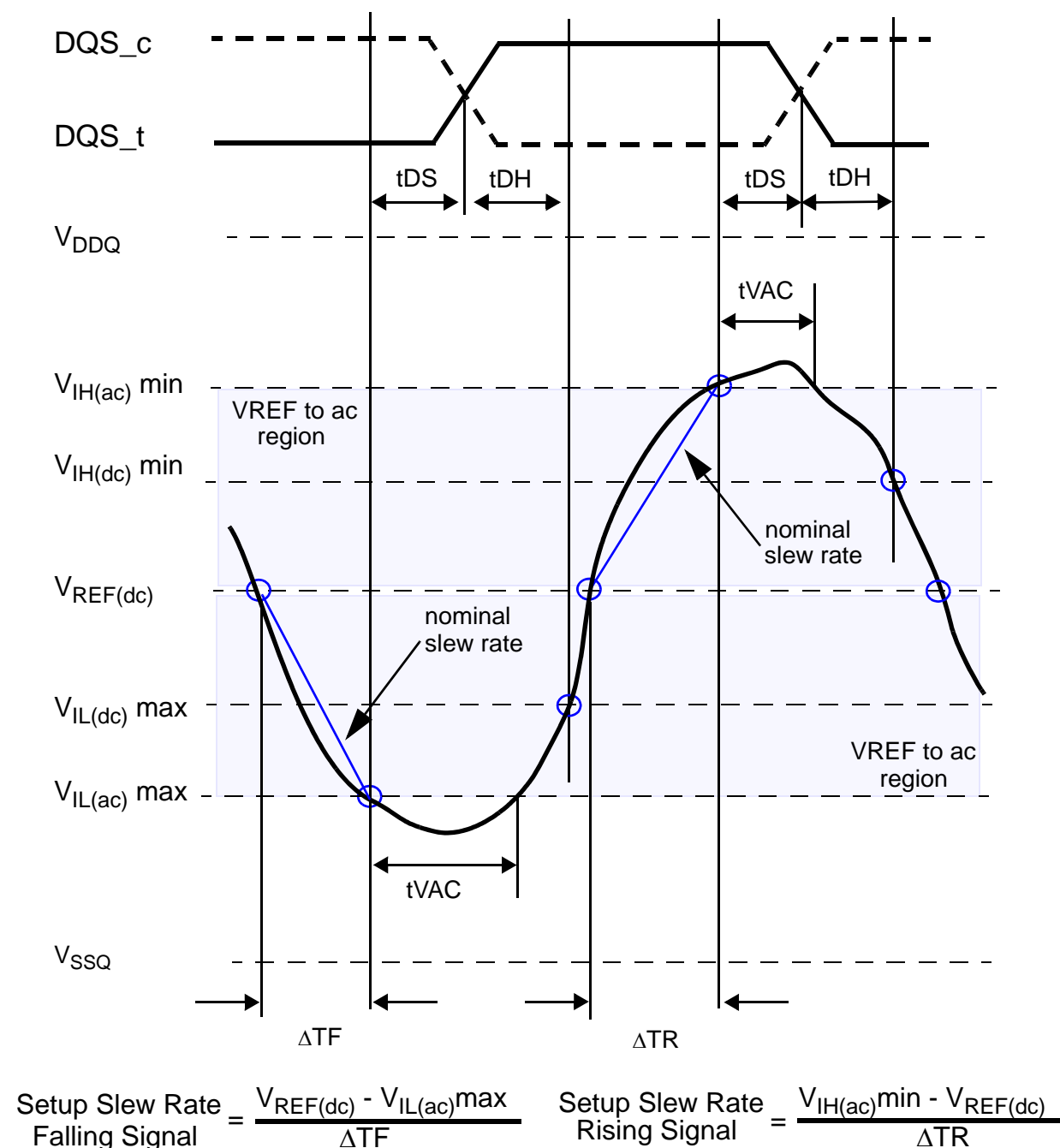


Figure 125 — Illustration of nominal slew rate and  $t_{VAC}$  for setup time  $t_{DS}$  for DQ with respect to strobe

## 12.6 Data Setup, Hold and Slew Rate Derating (cont'd)

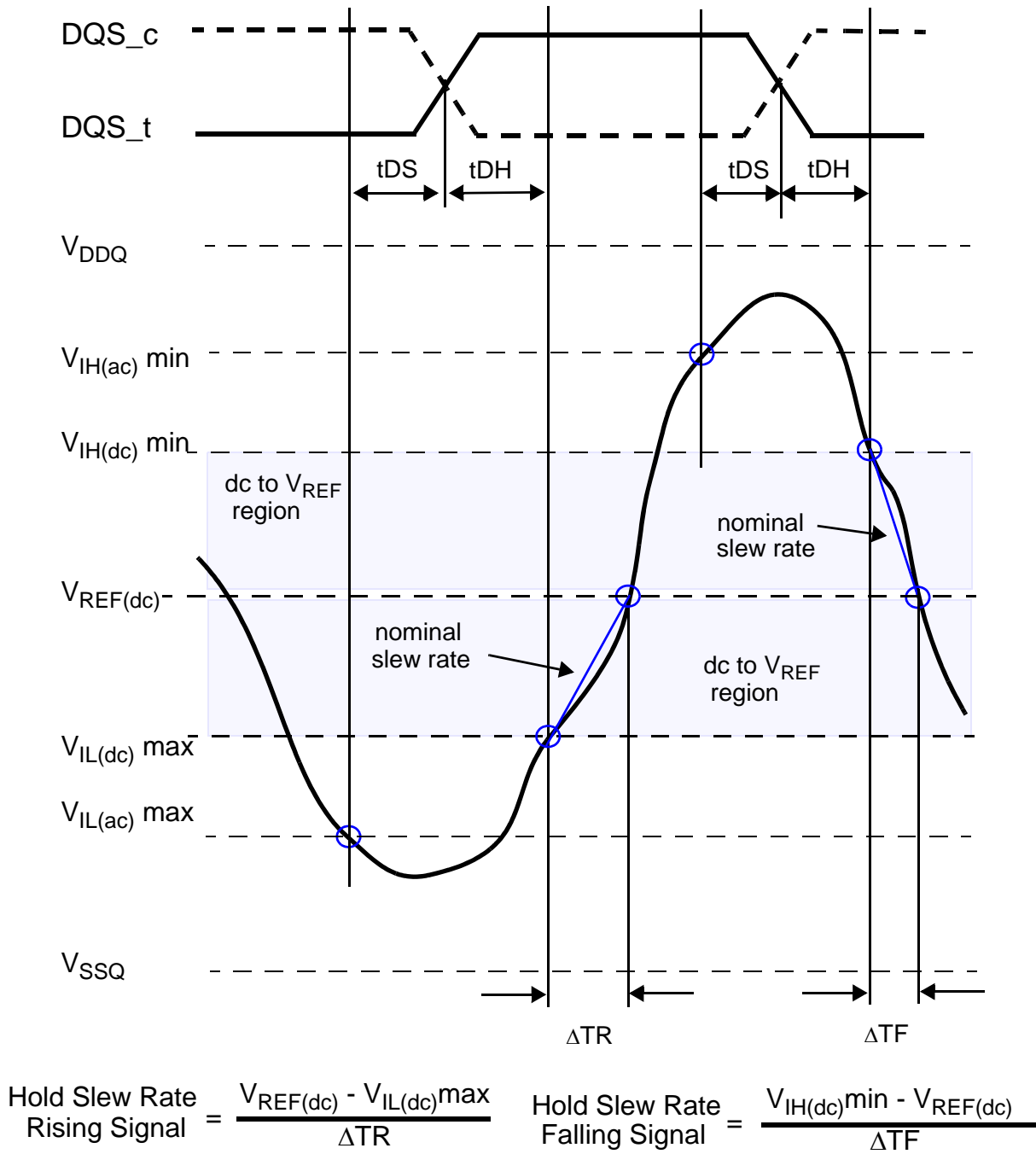


Figure 126 — Illustration of nominal slew rate for hold time  $t_{DH}$  for DQ with respect to strobe

## 12.6 Data Setup, Hold and Slew Rate Derating (cont'd)

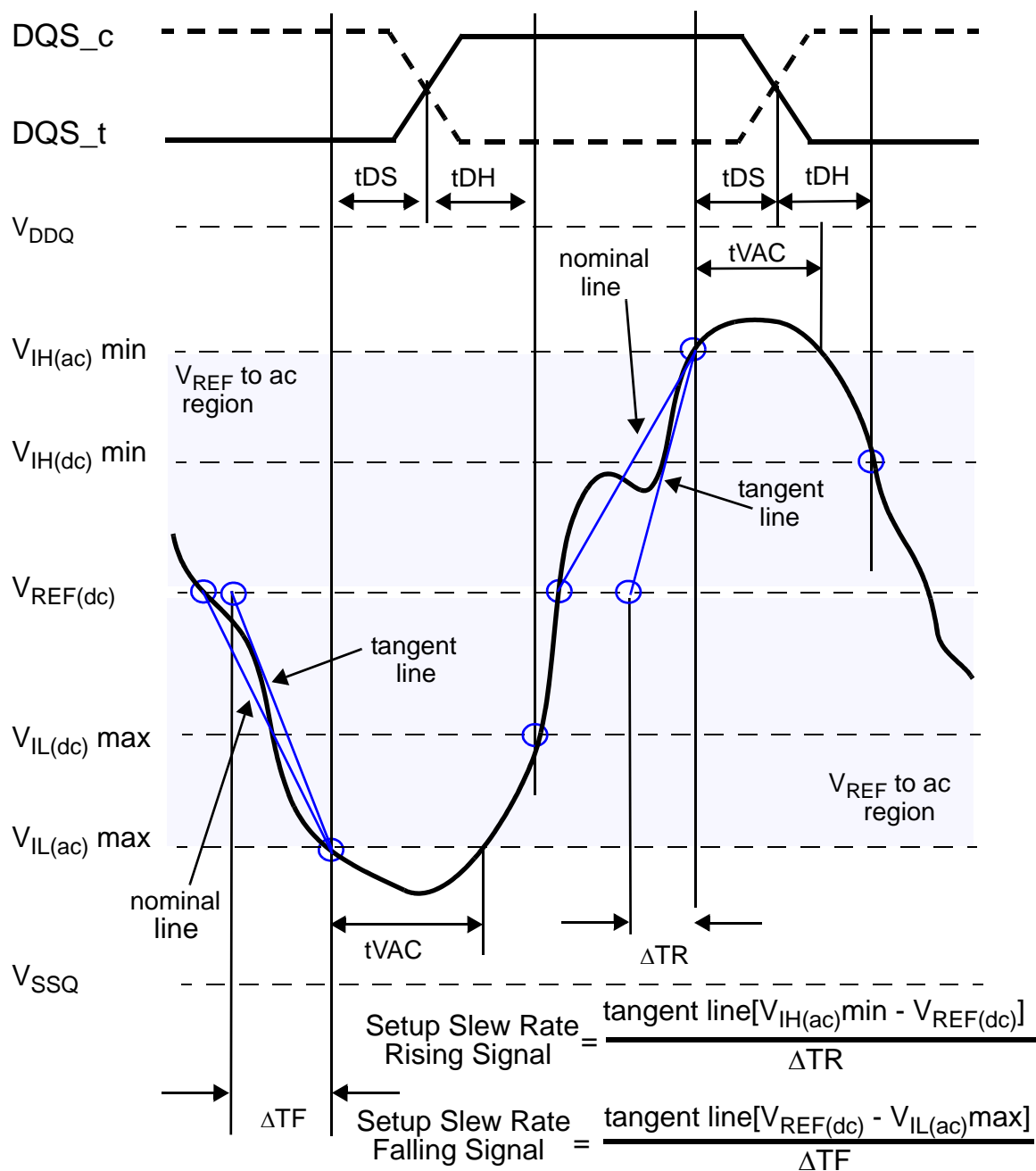


Figure 127 — Illustration of tangent line for setup time  $t_{DS}$  for DQ with respect to strobe

## 12.6 Data Setup, Hold and Slew Rate Derating (cont'd)

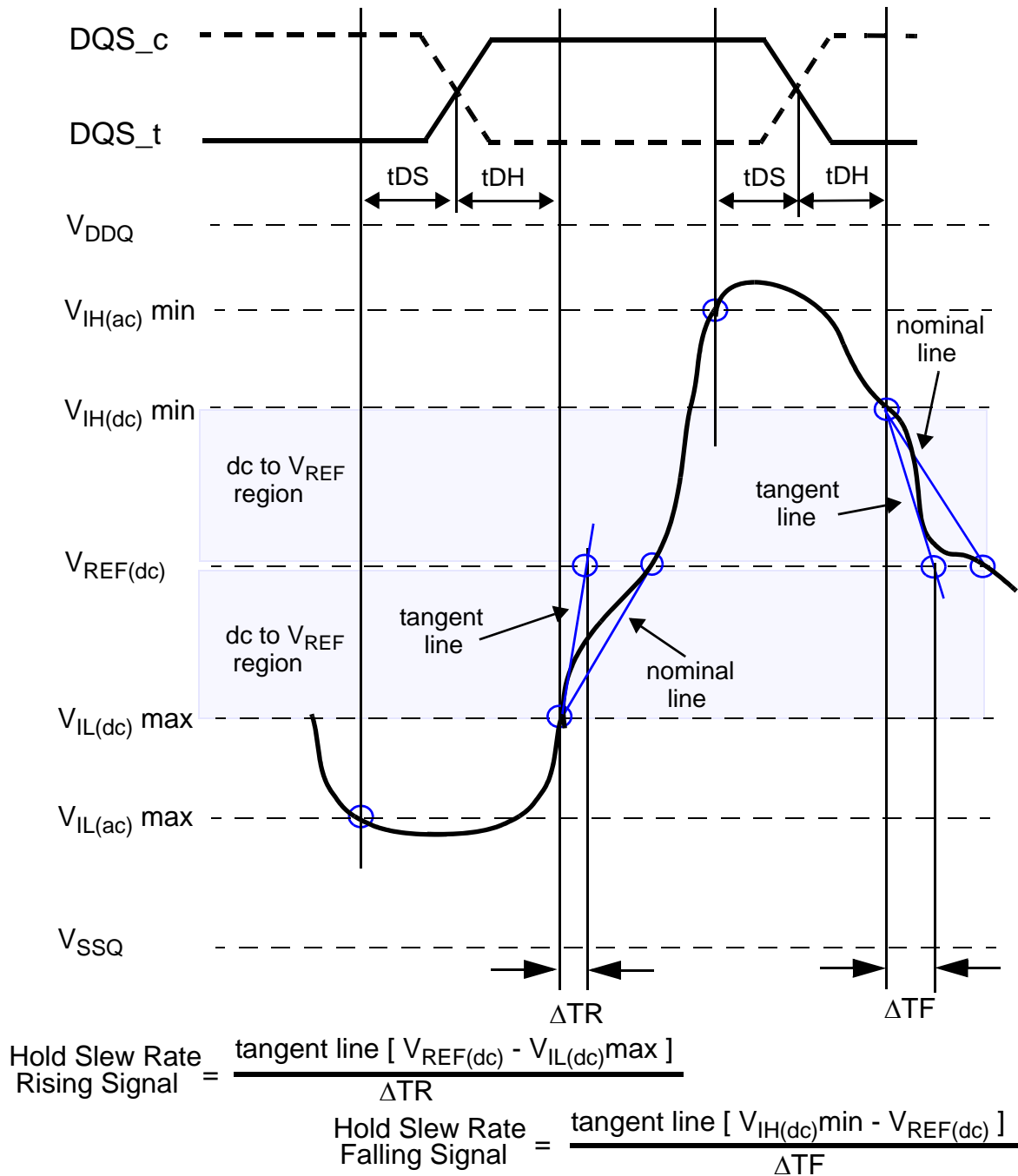


Figure 128 — Illustration of tangent line for for hold time  $t_{DH}$   
for DQ with respect to strobe

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## Annex A LPDDR2-NVM Software Application Notes

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### A.1 Scope

LPDDR2-NVM can be produced from a variety of memory array technologies.

The variety of technologies causes variation in software that manages the non-volatile arrays.

This application note shows a program method for a particular NV memory technology as an example of possible implementation.

### A.2 Programming operations based on Programming Region

#### A.2.1 Introduction

This section describes a particular program method that might be implemented in some LPDDR2-NVM devices. The scope of this section is only to provide an example, other technology or product may implement a different program method.

Users should refer to the vendor memory datasheet for complete information.

Some LPDDR2-NVM devices may implement innovative features specially developed to improve the storage flexibility and efficiency of memory arrays.

#### A.2.2 Programming Modes

Typically, the memory array of an NVM is divided into multiple blocks. Each block can be divided in uniform programming regions.

Each programming region in a block can be configured for one of two programming modes: Control Mode or Object Mode. The programming mode is automatically set based on the data pattern when a region is first programmed. The selection of either Control Mode or Object Mode is done according to the specific needs of the system with consideration given to two types of information:

- Control Mode: Flash File System (FFS) or Header information, including frequently changing code or data. Control Mode allows for multiple programs within a programming region between block erases.
- Object Mode: Large, infrequently changing code or data, such as objects or payloads. Object Mode allows only a single program operation within each programming region between block erases.

By implementing the appropriate programming mode, software can efficiently organize how information is stored in the flash memory array.

Control Mode programming regions and Object Mode programming regions can be intermingled within the same erase block. However, the programming mode of any region within a block can be changed only after erasing the entire block.

#### A.2.3 Programming Regions

The following table shows the amount of Programming Regions within each block for various block sizes and 512-Byte and 1-KByte Programming region size.

Refer to the device datasheet to discover the actual size of the Programming Region.

**Table 112 — Number of Programming Regions**

Block Size	Programming Region Size	
	512Byte	1KByte
64KByte	128	64
128KByte	256	128
256KByte	512	256

Erase operations have a Block granularity, whereas program operations have a Programming Region granularity.

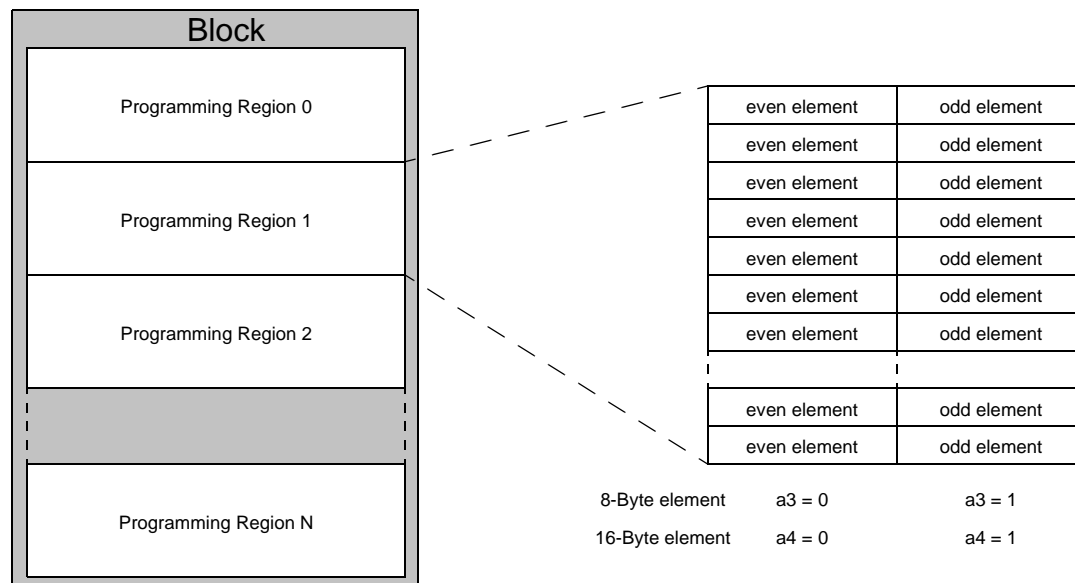
The user can configure each Programming Region to be programmed either in the Control mode or in the Object mode.

A given Block can contain Programming Regions configured in the Control mode and others configured in the Object mode.



### A.2.3 Programming Regions (cont'd)

Special care should be taken when selecting the programming mode for the Programming Regions because once the Programming Regions are configured their program mode cannot be changed until the entire Block is erased.



Each Programming Region is split into elements, and the element size can be either 8 Bytes or 16 Bytes. There are even elements and odd elements as defined in [Table 113](#), where a3 and a4 are byte address bits.

### Figure 129 — Programming Regions and elements

### Table 113 — Even and Odd elements

Element	8-Byte	16-Byte
Even Element	a3 = 0	a4 = 0
Odd Element	a3 = 1	a4 = 1

## A.2.4 Program Modes

There are two program modes, which allow the memory to store different types of data.

#### A.2.4.1 Control Mode

The Control mode is best suited to the storage of small, dynamic information. Typically such data is contained within one Programming Region and it will be frequently updated and/or new data will be added to it.

Programming Regions are configured in the Control mode by programming data only to the even elements. The odd elements must remain erased, that is they should not contain any zeros (see [Figure 129](#) ).

In a Programming Region of 1-KByte (512Byte) configured in the Control mode, only 512 Byte (256Byte) of data can be stored, in particular only even elements are writable while odd elements are reserved.

Some LPDDR2-NVM devices will allow to program each byte of the even elements only once. Some others will not have this restriction, therefore each byte might be programmed subsequently several times without erasing the Block.

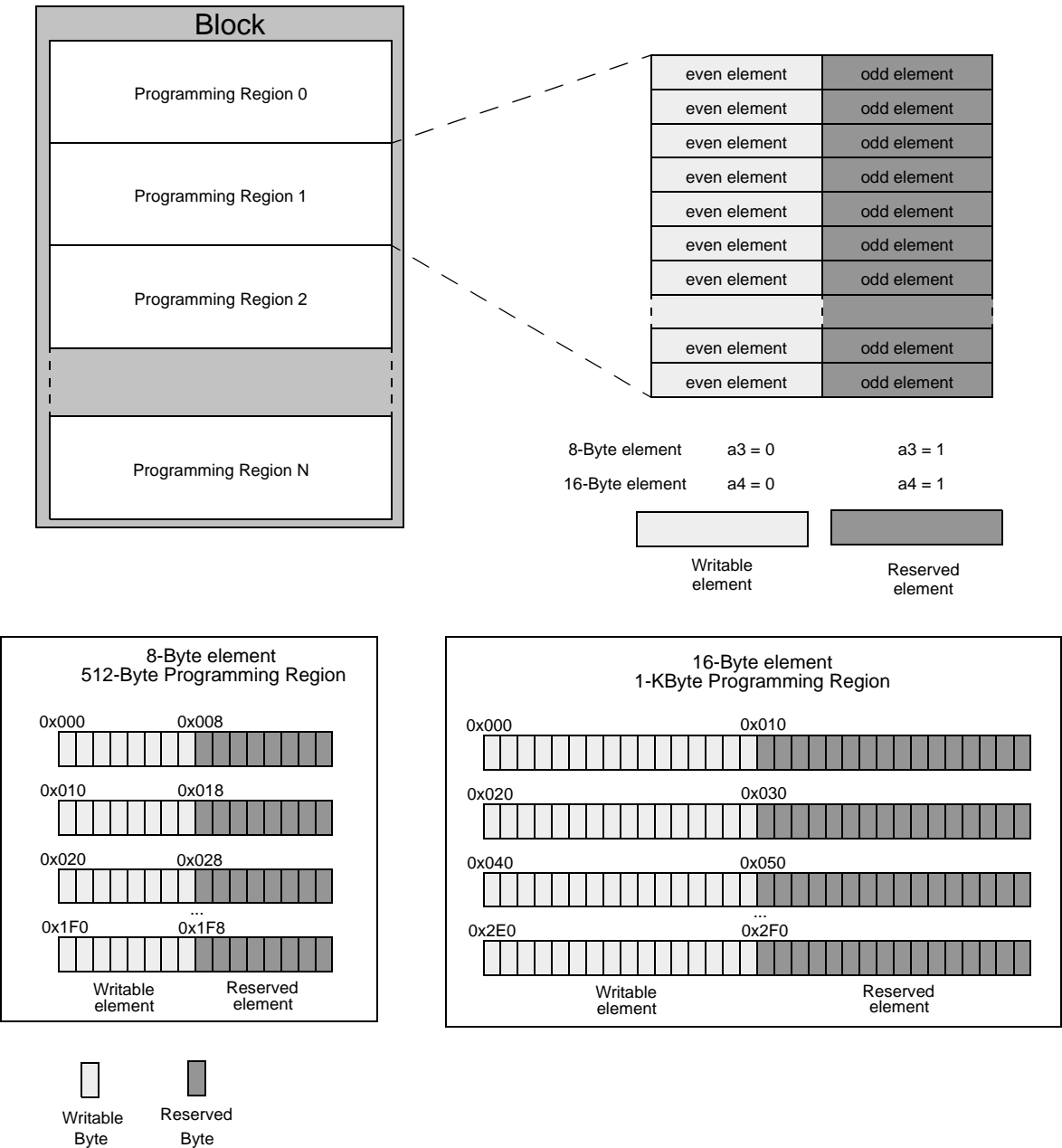
When the Programming Regions are configured in the Control mode, any program command can be used: the Single Word (if supported) or the Buffered Program command.

Once a Programming Region has been configured in the Control mode, if a zero is written to an odd element, the program operation is terminated without programming the array and an error is generated.

The Status Register bits MR22.OP4 (PSB) and MR23.OP1 (CMSB) are set to '1'. (Refer to Status Register description and to [Table 114](#) for details).

A.2.4.1 Control Mode (cont'd)

The program mode of a Programming Region configured in the Control mode can only be changed by first erasing the Block that contains the Programming Region.



NOTE 1 Only the even elements of a Programming Region configured Control Mode are writable.  
NOTE 2 Reserved elements return “0xFF” when read.

Figure 130 — Programming Regions Configured in Control Mode

### A.2.4.2 Object Mode

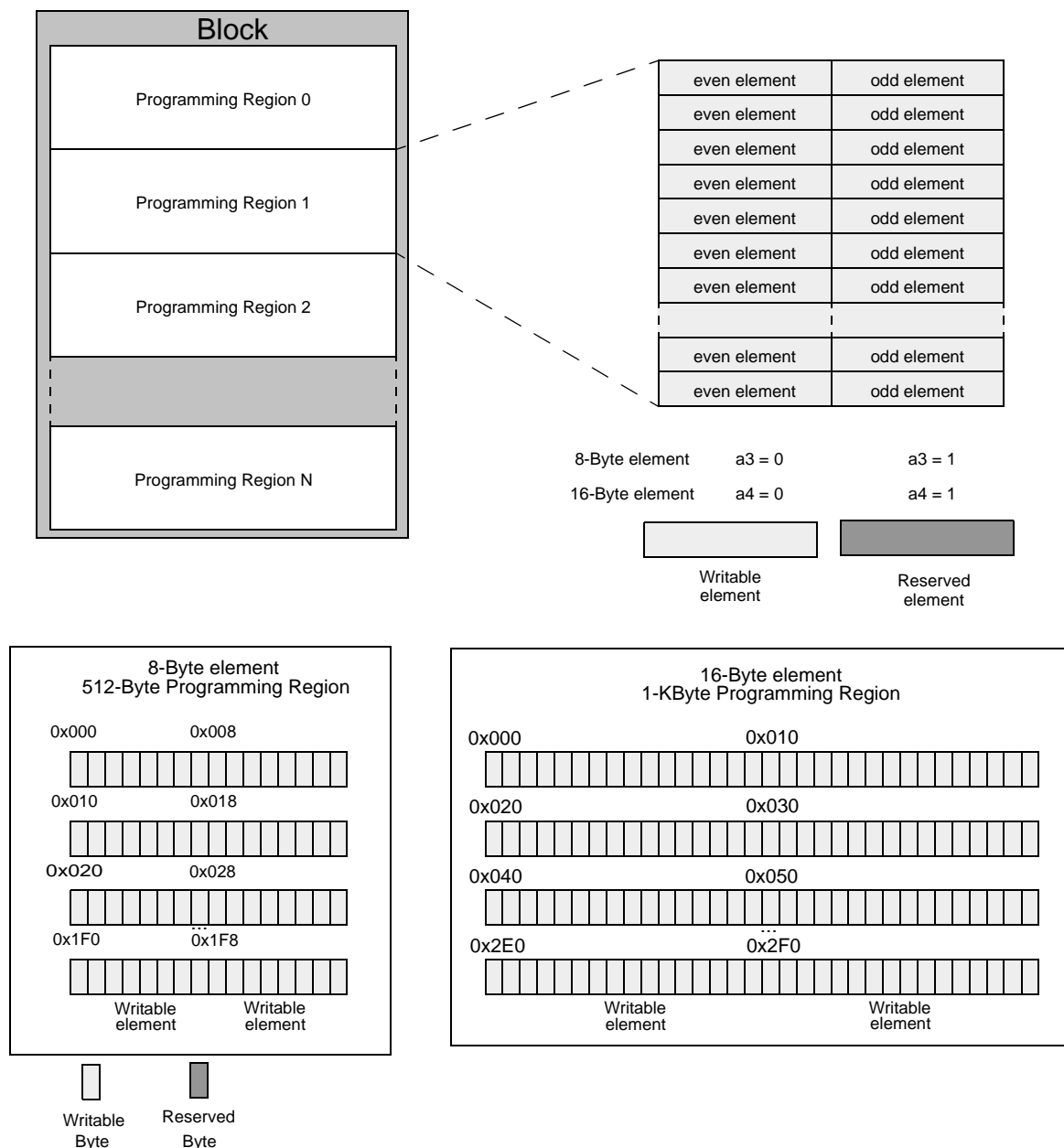
The Object mode is best suited to the storage of large, static information. In a Programming Region of 1-KByte (512-Byte) configured in the Object mode, 1-KByte (512-Byte) of data can be stored.

When a Programming Region is configured in the Object mode, it cannot be reprogrammed nor have new data added without first erasing the entire Block that contains the Programming Region.

Programming Regions are configured in the Object mode simply by programming at least one bit in one of the odd elements.

If the programmed data is smaller than 1-KByte (512Byte), the unused space remains in the erased state (all the bytes set to 0xFF), but can no longer be used to program data. See [Figure 129](#).

Only the Buffered Program command can be used to establish an Object mode region.



NOTE: All elements of a Programming Region configured Object Mode are writable.

**Figure 131 — Programming Regions Configured in Object Mode**

### A.2.4.3 Programming Region Configuration

Based on the current programming region status, the following table shows the next programming region status after a programming operations.

**Table 114 — Relationships Between Program Commands and Programming modes**

Programming Region Status	Next Programming Region Status			
	Element	Buffered Program		Single Word Program <sup>(3)</sup>
Erased	Even <sup>(1)</sup>	Control mode	Object mode	Control mode
	Odd <sup>(2)</sup>	Object mode		Not allowed <sup>(4)</sup>
Control Program mode	Even <sup>(1)</sup>	Control mode		Control mode
	Odd <sup>(2)</sup>	Not allowed <sup>(5)</sup>		Not allowed <sup>(4)</sup>
Object Program mode	Even <sup>(1)</sup>	Not allowed <sup>(6)</sup>	Not allowed <sup>(6)</sup>	Not allowed <sup>(6)</sup>
	Odd <sup>(2)</sup>	Not allowed <sup>(6)</sup>		Not allowed <sup>(4)</sup>

NOTE 1 At least one bit is programmed in an even element

NOTE 2 At least one bit is programmed in an odd element

NOTE 3 If supported

NOTE 4 Program aborted, Status Register error bits MR22.OP4 (PSB), MR23.OP0 (OMSB) and MR23.OP1 (CMSB) are set

NOTE 5 Program aborted, Status Register error bits MR22.OP4 (PSB) MR23.OP1 (CMSB) are set

NOTE 6 Program aborted, subsequent program not allowed, Status Register error bits MR22.OP4 (PSB) MR23.OP0 (OMSB) are set

Figure 132 shows an example of Programming Region configuration. The Programming Region size is 512Byte, the element size is 8Byte, and the Block sizes are 64KByte, 128KByte and 256KByte.

Independently of the Block size, the Programming Region configuration is periodic: the first 124 Programming Regions (62KByte) are configured in Object Mode Region, and the following 4 Programming Regions (2KByte) are configured in Control Mode.

### A.2.4.3 Programming Region Configuration (cont'd)

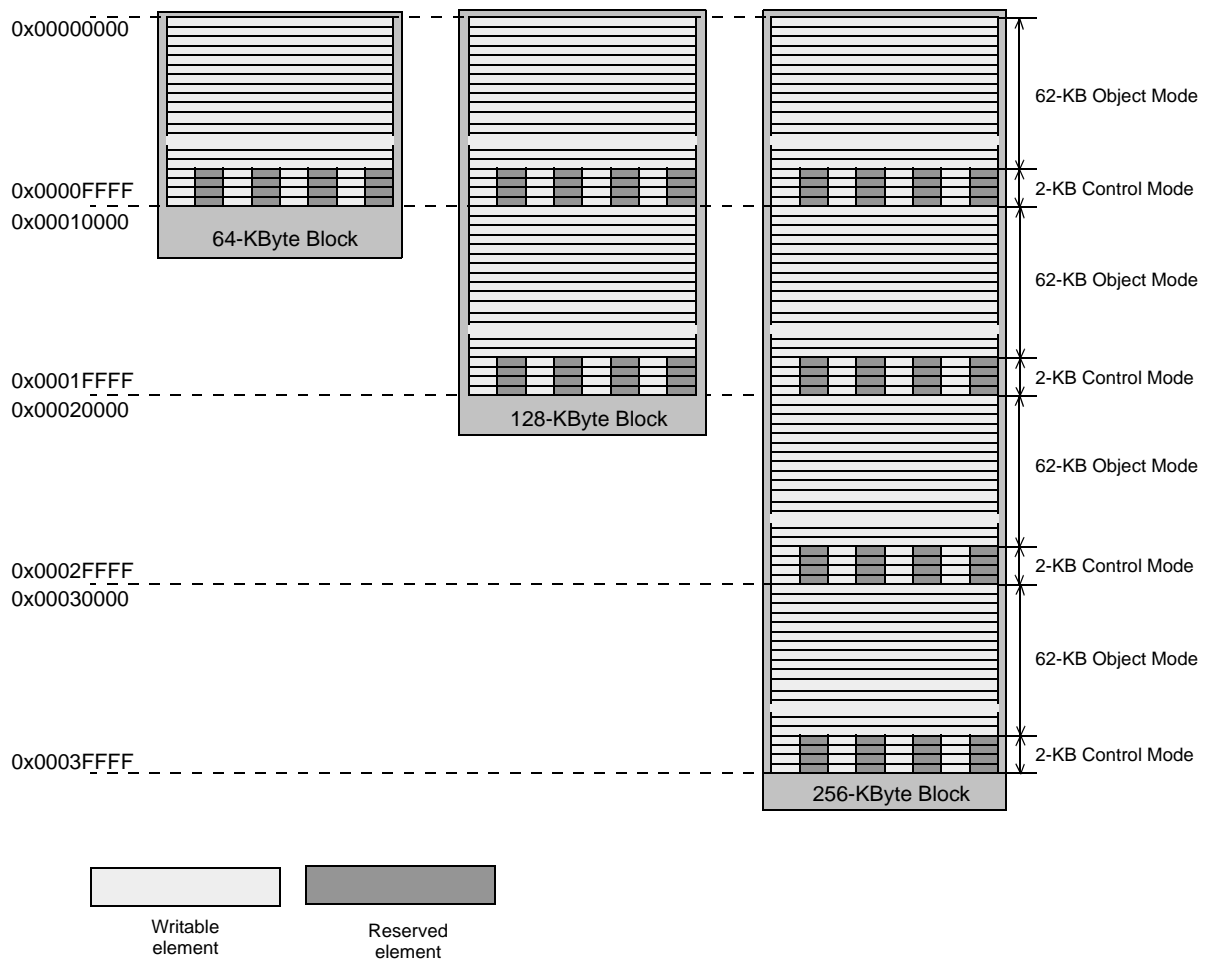


Figure 132 — Control Mode and Program Mode Example

## Annex B LPDDR2-NVM Boot Procedure

### B.1 Booting From an LPDDR2-NVM Device

Figure 133 illustrates an example LPDDR2 memory subsystem that includes both NVM and SDRAM memories. Chip Select (CS<sub>x</sub>) and Clock Enable (CKE<sub>x</sub>) are assigned on a per chip basis, the data bus and the remainder of the command bus are common to both devices. Because LPDDR2 devices (both DRAM and NVM) assign specific functions to the different byte lanes of the data bus and even to specific bits within the bytes, byte and bit swapping shall be avoided. The ZQ input requires connection to a precision 240 ohm resistor that is used to calibrate each device's output drive strength. The ZQ inputs can use a common 240 ohm resistor or have captive resistors, in this example we use a common resistor.

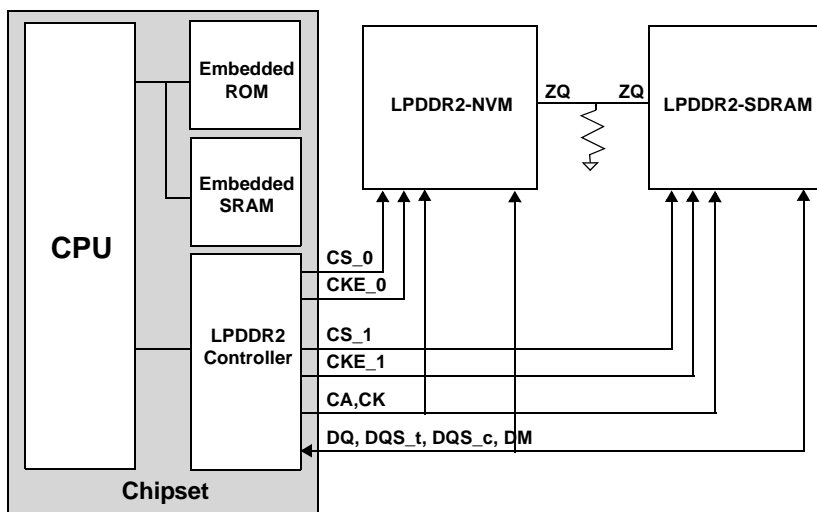


Figure 133 — LPDDR2 based system using both LPDDR2-SDRAM and LPDDR2-NVM

Chipsets implementing an LPDDR2 interface will need to perform a “pre-boot” process prior to accessing the LPDDR2-NVM device. The pre-boot process will perform the LPDDR2-NVM device initialization (as described in Section 3.5.1 - Power Ramp and Device Initialization in the LPDDR2-NVM spec) and configure both the LPDDR2 controller and the external LPDDR2-NVM device properly prior to starting code execution from external memory. The pre-boot process may be performed by executing a code residing in an embedded ROM or it might be implemented using hardware in the memory controller.

## **B.1 Booting From an LPDDR2-NVM Device (cont'd)**

The pre-boot process is composed by the following steps:

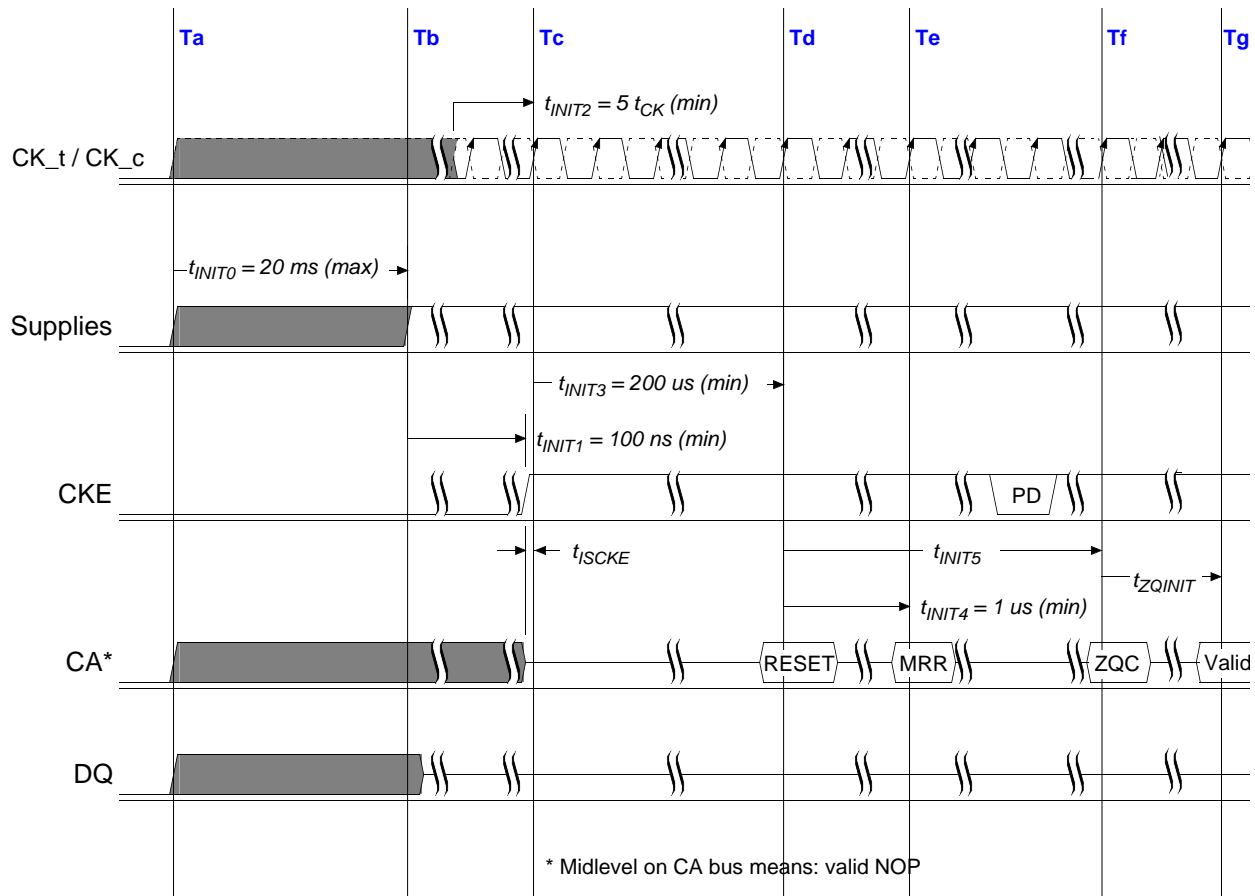
1. Memory Controller Preliminary Configuration
  - Configure the memory controller with initial latency settings compatible with the possible LPDDR2-NVM devices that may reside on the LPDDR2 bus
2. Initialization Sequence
  - Apply clock (frequency between 10MHz and 55MHz)
  - Drive CKE High
  - Issue the Reset command and wait until the DAI bit in MR0 transitions to 0. It is recommended that this delay (tINIT5) be accomplished by polling the DAI bit in MR0.
  - Issue a ZQ Initialization Command
3. Search for an LPDDR2-NVM memory
  - Starting from CS0, check the first LPDDR2-NVM device in the bus by reading MR0
4. Memory Controller and LPDDR2-NVM configuration
  - Read MR8 to retrieve the memory type, bus width, density and configure the memory controller accordingly
  - Read MR20 to retrieve Row Data Buffer Size and number of Row Data Buffers, then configure the memory controller accordingly
  - Optionally, set the proper Burst Length value in MR1 of the LPDDR2-NVM
  - Optionally, adjust tRCD memory controller setting according to MR21 and the actual tCKb value.
5. Start to read the boot code from the external LPDDR2-NVM device.

Once the pre-boot process has completed and code execution is passed to the external LPDDR2-NVM memory device the final portion of the memory bus configuration process occurs. During this stage the boot process will optimize timings and finally increase the clock rate to the target value.

6. Specify how frequently the output impedance should be calibrated
7. Set the appropriate output drive strength
8. Adjust the configuration settings in the controller and memories for higher clock rates
9. Bump up the bus operating frequency
10. Perform data training

### B.1.1 Power Ramp and Initialization

During power-on the LPDDR2 power supplies are expected to ramp up to the nominal operating voltages within 20ms. At this point CKE should be driven low and the CK\_t/CK\_c clock signals should begin to toggle. During this early part of the boot process the host chipset is expected to clock the LPDDR2 bus at a frequency between 10MHz and 55MHz. After 100ns and at least five clocks, CKE is driven high to begin internal initialization of the LPDDR2 device. The device is ready to receive the RESET command 200us after CKE is driven high. The device is ready to receive the RESET command 200us after CKE is driven high.



**Figure 134 — Power-Up and Initialization (see the LPDDR2-NVM spec for details)**

Once the RESET command has been issued the boot process must wait for 1us before continuing. After the 1us tINIT4 time has elapsed the boot process will poll the Device AutoInitialization (DAI) bit in the Device Information Register (MR0). The DAI bit will transition from high to low when the reset operation has completed.

The LPDDR2 devices after RESET assume the following default configuration:

BL=4;

BT= Sequential, Wrap;

RL=3, WL=1;

DS=40Ohm.

It is recommended that the memory controller default configuration should match with the LPDDR2 devices (at least RL, otherwise it would not be possible to read the Mode Registers).



### **B.1.2 ZQ Initialization**

Once reset has completed, the ZQ Initialization command (FFh) is written to the Calibration Mode Register (MR10). During ZQ initialization the on-die output impedance is compared with a 240 ohm precision resistor that is connected between ground and the device's ZQ input. Multiple LPDDR2 devices can share the precision resistor as long as only one of the devices performs calibration at any particular time. Upon completion of the ZQ Initialization the device's output impedance will be within 15% of the nominal value.

At the lower operating frequencies used during the boot process the default drive strength value of 40 ohms is adequate. Adjustment of the drive strength will occur later in the boot process when the clock rate is bumped up prior to normal operation.

### **B.1.3 Determine the LPDDR2 bus width, memory type, RDB size and density**

The boot process then reads the Basic Configuration 4 Mode Register (MR8) from the LPDDR2 device on CS0 to determine the data bus width, memory type and also the device density. When the memory is an NVM, MR20 is read to determine the RDB size. The controller is then configured to operate with the appropriate bus width (x8, x16 or x32). The density value read back from MR8 is used to configure the address space assigned to CS0. The data bus width and the RDB size is relevant system information and is used to ensure proper memory addressing and is mandatory to configure the memory controller accordingly. The embedded ROM can be programmed, or the HW could be used, to step through the remaining LPDDR2 chip selects and configure the host controller according to the information available in the respective mode registers.

### **B.1.4 Align controller and memory latency settings (RL, WL, tRCD)**

Prior to performing standard read and write operations the host controller and target memory must align their Read/Write latencies. The default values for LPDDR2-NVM devices is a three clock read latency and a one clock write latency. These default values are suitable for normal operation for the specified boot frequency (10MHz to 55MHz). If necessary, the memory controller latencies should be adjusted to match those of the LPDDR2-NVM device.

The remaining latency issue needing attention is aligning the host controller with the LPDDR2- NVM tRCD latencies. The value held in the read only tRCD Mode Register (MR21) specifies the minimum tRCD value for the LPDDR2-NVM device. The embedded boot code should configure the LPDDR2 controller latency values to accommodate the tRCD value indicated in [MR21](#).

### **B.1.5 Determining whether to boot from the LPDDR2 Bus**

After the initial latencies have been specified the boot process will determine whether a bootable non-volatile device resides on the LPDDR2 bus. If there is a bootable NVM device on the LPDDR2 bus it will likely reside on the first chip select (CS0). If the device is nonvolatile, program operation will be redirected to the LPDDR2-NVM device on CS0. If the device is volatile (SDRAM), the embedded ROM will continue to search for alternate boot memories.

### **B.1.6 Continued Boot Out Of the LPDDR2-NVM Device**

Once the boot process has passed to the LPDDR2-NVM device, system level characteristics are considered. For the most part this portion of the boot process is used to maximize data throughput by adjusting the output drive strength, clock rate and the data capture point during read operations.

### **B.1.7 Output Drive Strength**

Given various system level considerations, adjustment of the output drive strength away from the default 40 ohm setting may be required. This step is required to optimize driver output impedance to accommodate issues like bus loading (# of devices), PoP/MCP package type, trace length on the PCB and sourcing capabilities of the output driver power supplies.

The I/O Configuration Mode Register (MR3) is used to configure the LPDDR2-NVM output drive strength. Available configuration settings include 34.3, 40 (default), 48, 60 and 80 ohm values (120 ohm value is optional).

### B.1.8 Setting the Output Impedance Calibration Interval

During normal operation both operating voltage and temperature drift can cause the output drive strength to change away from the value selected during the boot process. These changes are dealt with by periodically calibrating the output impedance against the 240 ohm precision resistor connected to the ZQ input. Periodic calibration is performed to assure that the selected output impedance remains within the nominal +/-15% spec.

LPDDR2 controllers include a periodic timer that will indicate the length of time between calibration cycles. Once the timer interval has expired the controller will automatically issue a Short Calibration command that will move the output impedance by up to 1.5% toward the ideal setting. The calibration interval is calculated by considering the maximum voltage and temperature drift rates. Given a maximum temperature drift rate of 1.0°C/s and a maximum voltage drift rate of 15mV/s the Short Calibration operation should be performed at least every 400ms. The equation below is the strategy suggested by JEDEC to determine how frequently output impedance should be calibrated.

$$\begin{aligned} \text{ZQS\_Interval} &= (\text{ZQS\_Correction} / ((\text{T\_Sensitivity} * \text{T\_DriftRate}) + (\text{V\_Sensitivity} * \text{VDriftRate}))) \\ &= 1.5\% / (((0.75\%/^{\circ}\text{C}) * (1.0^{\circ}\text{C/s})) + ((0.2\%/m\text{V}) * (15m\text{V/s}))) \\ &= 400ms \end{aligned}$$

If a single 240 ohm ZQ resistor is common to all LPDDR2 devices the ZQS Calibration operation must be performed serially on a per device basis. If each LPDDR2 device has its own ZQ resistor the ZQS Calibration operation must still be performed on a per device basis. See the LPDDR2-NVM spec for further guidance on how to determine the required length of time between ZQS calibration.

### B.1.9 Increasing the Clock Rate

At this point in the boot process, preparation to increase the clock rate can begin. This process has three steps. The first step is to alter the memory controller settings to accommodate the latency characteristics of the memory devices on the LPDDR2 bus. The second step is to increase the clock frequency to the target rate. The third and final step is to perform data training to maximize read timing margin.

While the first step (adjusting latency settings) can be executed from code located in the LPDDR2-NVM device, the second (increasing clock rate) and third (data training) steps should not be performed using code executing from a device residing on the LPDDR2 bus. The code used to increase the clock rate and to perform data training should be executed out of embedded memory located in the chipset. The required code could reside in either the embedded ROM or it could be copied temporarily into the chipset's embedded SRAM for execution. Once these three steps have been performed, program operation will be redirected to the LPDDR2-NVM device with the LPDDR2 bus running at the target frequency.

Configuration of additional devices residing on the LPDDR2 bus can be performed either before or after the clock rate is increased. If additional devices are configured before the clock rate is increased, extensions to the code that manages the LPDDR2-NVM device can be developed. If additional LPDDR2 devices are to be brought on line after the clock rate is increased, the configuration code for the additional devices could be executed out of the LPDDR2-NVM device.

### B.1.10 Controller Latency Settings for Higher Clock Rates

The first step toward increasing the clock rate is adjusting the controller settings to account for the memory device's operational characteristics. The key characteristics include the time required between the Active and Read/Write commands (tRCD) and also the Read/Write Latencies (RL, WL).

The tRCD value can be read from the tRCD Mode Register ([MR21](#)). The number of clocks required to meet the tRCD spec given a target operating frequency is then calculated and loaded into the memory controller. This process is repeated for each device sharing the LPDDR2 bus.

Appropriate Read Latency and Write Latency values are then chosen given device characteristics and the target operating frequency. Once determined, the RL/WL values are loaded into the Device Feature 2 Mode Register ([MR2](#)). The memory controller is also configured to align with the appropriate RL/WL values for each of the devices on the LPDDR2 bus.

### B.1.11 Increasing the Clock Rate

After the latency values have been changed in both the LPDDR2 devices and in the controller the clock rate can be increased to the target operating frequency. Figure 135 describes the timings relevant to changing the clock frequency. In this example, the clock rate is changed while the device is in the Power-Down state. The clock may also be changed when CKE is HIGH. See the LPDDR2 specification for details.

The device must be stable at the new clock frequency for at least two clock cycles before exiting the Power-Down state (two clocks (min), CKE returns high). Once CKE returns high the LPDDR2-NVM device will require 10ns to exit Power-Down ( $t_{XP}$ ) before accepting the first valid command.

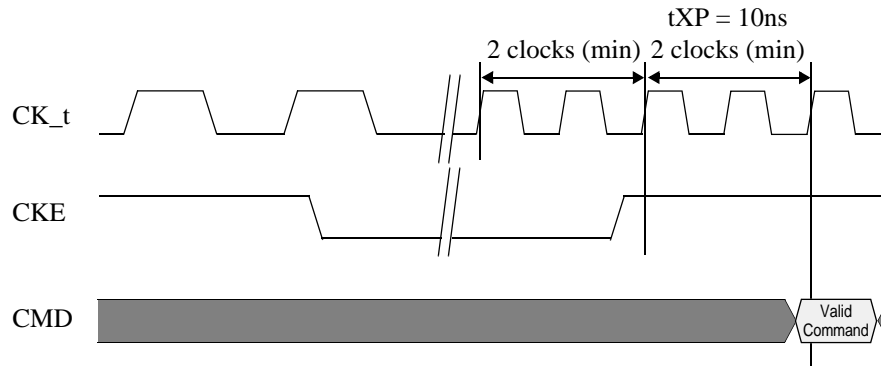


Figure 135 — Clock Rate Change Timings

### B.1.12 Data Training

The final step in the boot process is to optimize the controller's read timings. In particular, this step is used to skew the data capture point with respect to the DQS\_t, DQS\_c signal generated by the target memory device during a read operation. This offset will be different for each device residing on the memory bus, requiring that an offset be associated with each chip select.

In most implementations the host software will request that the controller perform data training. The controller will then find the optimal read capture point without intervention from the host. Once the controller has completed data training, code execution will be redirected back to the LPDDR2-NVM device at the new clock rate.

### B.1.13 Summary

This application note has described how a system can boot from an LPDDR2-NVM device that shares the LPDDR2 bus with an LPDDR2-SDRAM device. Only a few extensions to the chipset's embedded ROM, or dedicated HW, are required to facilitate booting from the LPDDR2 bus. Once code execution has passed from the embedded ROM, or dedicated HW, to the LPDDR2-NVM device the remaining boot code takes into account system level characteristics.

## Annex C LPDDR2-N: Replay Protected Memory Block (RPMB)

### C.1 Acronyms

**Table 115 — Definition of acronyms**

Term	Definition
RPMB	Replay Protected Memory Block
MAC	Message Authentication Code
NVM	Non Volatile Memory
OTP	One Time Programmable

### C.2 Introduction

The RPMB feature for LPDDR2-NVM described in this section is optional.

A signed access to one or more Replay Protected Memory Block is provided. This function provides means for the system to store data to the specific memory area in an authenticated and replay protected manner. This is provided by first programming authentication key information to the LPDDR2-NVM memory (shared secret), then configuring one or more RPMB resources.

As the system can not be authenticated yet in this phase, the authentication key programming has to take place in a secure environment like in an OEM production. Further on the authentication key is utilized to sign the read and write accesses made to the replay protected memory area with a Message Authentication Code (MAC). Usage write count register provides additional protection against replay of messages where messages could be recorded and played back later by an attacker.

### C.3 Map of Control Registers (offsets and definitions)

Table 116 describes the Overlay Window register map.

**Table 116 — Overlay Window: Control Register Offsets and Definitions (Part 1 of 2)**

Byte-Addressing		Type	Register Item	Default Value (hex)	Notes
Offset (hex)	# of bytes (decimal)				
0x001 – 0x000	2	R	Overlay Window Query String “P”	0x00 - 0x50	
0x003 – 0x002	2	R	Overlay Window Query String “F”	0x00 - 0x46	
0x005 – 0x004	2	R	Overlay Window Query String “O”	0x00 - 0x4F	
0x007 – 0x006	2	R	Overlay Window Query String “W”	0x00 - 0x57	
0x009 – 0x008	2	R	Overlay Window ID	0x00 - 0x20	
0x00B – 0x00A	2	R	Overlay Window Revision	Vendor-Specific	
0x00D – 0x00C	2	R	Overlay Window Size	Vendor-Specific	
0x00F – 0x00E	2		Reserved for JEDEC		
0x011 – 0x010	2	R	Program-Buffer Offset	Vendor-Specific	
0x013 – 0x012	2	R	Program-Buffer Size	Vendor-Specific	
0x01F – 0x014	12		Reserved for JEDEC		
0x021 – 0x020	2	R	JEDEC Manufacturer ID	Vendor-Specific	
0x023 – 0x022	2	R	JEDEC Device ID	Vendor-Specific	
0x03D – 0x024	26		Reserved for JEDEC		
0x03F - 0x03E	2	W	Reserved for JEDEC		

**Table 116 — Overlay Window: Control Register Offsets and Definitions (Part 2 of 2)**

Byte-Addressing		Type	Register Item	Default Value (hex)	Notes
Offset (hex)	# of bytes (decimal)				
0x07F – 0x040	64	Vendor-Specific	Reserved for Vendor Use	Vendor-Specific	
0x081 – 0x080	2	W	Command Code	0x00 - 0x00	
0x083 – 0x082	2		Reserved for JEDEC		
0x087 – 0x084	4	R/W	Command Data		
0x08B – 0x088	4	W	Command Address		
0x08F – 0x08C	4		Reserved for JEDEC		
0x093 – 0x090	4	W	Multi-Purpose Register		
0xBF - 0x094	44	-	Reserved for JEDEC		
0x0C1 - 0x0C0	2	W	Command Execute	0x00 - 0x00	
0x0C7 - 0x0C2	6	-	Reserved for JEDEC		
0x0C9 - 0x0C8	2	R/W	Suspend	0x00 - 0x00	
0x0CB - 0x0CA	2	R/W	Abort	0x00 - 0x00	
0x0CD - 0x0CC	2	R/W	Status Register	0x00 - 0x80	
0x0CF - 0x0CE	2	R	Command Result	0x00 - 0x00	2
0x0DF - 0x0D0	16		Reserved for Vendor Use		
0x0FF - 0x0E0	32	-	Reserved for Vendor Use		
0x10F – 0x100	16	R/W	Nonce		
0x113 – 0x110	4	R/W	Write Counter		1
0x115 – 0x114	2	R	Command Response	0x0000	2
0x11F – 0x116	10	-	Reserved for JEDEC		
0x133 – 0x120	20	R/W	MAC Register		2
0x13F – 0x134	12	-	Reserved for JEDEC use		
Vendor-Specific	Vendor-Specific	Vendor-Specific	Reserved for Vendor Use		
Vendor-Specific	Vendor-Specific	Vendor-Specific	Program-Buffer		

NOTE 1: After the successful completion of an authenticated Erase, Program or Overwrite operation the Write Counter value is automatically incremented by the device and OW Write Counter register is updated with the new value. The OW Write Counter register can be read only after the execution of an Authenticated Program, Overwrite, Erase, Write Counter Digest command when the device returns ready (DRB='1').

NOTE 2: The MAC, Command Response and Command Result registers can be read only when the device is ready.

### C.3.1 Command Result Register

The Command Result Register provides information about the status of the internal Write Counter (valid, expired) and successfulness of an authenticated operation.

The Command Result Register is valid when the device is ready (DRB = '1').

Note that the Command Result Register may be used by other embedded operations, therefore its content may change if one of these operations is executed.

**Table 117 — Command Result data structure**

Bit	Name	Description
OR[7]	WCS Write Counter Status	WCS indicates whether the internal Write Counter has reached the maximum value 0 = write counter is valid 1 = write counter is expired.
OR[6:0]	ROR RPMB Operation Result	ROR indicates the successfulness of the access made to the Replay Protected Memory Block

The table is listing the defined results and possible reasons for failures.

**Table 118 — Command Result**

Valid Write Counter	Expired Write Counter	Description
0x00	0x80 <sup>(1)</sup>	Operation OK
0x01	0x81	General failure
0x02	-	Authentication failure (MAC comparison not matching, MAC calculation failure)
0x03	-	Counter failure (counters not matching in comparison, counter incrementing failure)
0x04 <sup>(2)</sup>	0x84 <sup>(2)</sup>	Address failure (address out of range)
0x05	0x85	Write failure (data/counter/result write failure) Invalid RPMB Start Address, RPMB End Address values.
0x06	0x86	Read failure (data/counter/result read failure)
0x07 <sup>(3,2)</sup>	-	Authentication Key not enabled yet
0x08 <sup>(4,2)</sup>	-	No RPMB resource enabled yet
0x09 <sup>(2)</sup>	-	Authenticated command issued during program, overwrite or erase suspend
0x0A <sup>(2)</sup>	-	Non Authenticated command issued on an RPMB range <sup>(5)</sup>
0x0B <sup>(6,2)</sup>	-	Authenticated Key, RPMB ID, RPMB Start Address, RPMB End Address Register locked down

NOTE 1: This value can occur in two cases: either after a successful digest command executed with expired counter (0x0FFF FFFF), or after a successful authenticated write initiated with a counter value of 0x0FFF FFFE.

NOTE 2: The MAC Register content is not valid when one of these values occurs.

NOTE 3: This value is the only valid Result value until the Authentication Key has been enabled (after which it can never occur again)

NOTE 4: This value is the only valid Result value if the Authentication Key is enabled but no RPMB resource is enabled.

NOTE 5: If a non authenticated command is issued on an RPMB range the operation fails, the Status Register error bits 4 and 5 are set.

NOTE 6: This value can only occur when Write Security Register command is issued.

### C.3.2 Nonce Register

The host shall write 16-Byte Nonce value into this register for the execution of Memory Data Digest and Write Counter Digest commands. Nonce Register is readable for software debug.

The value of this register is undefined after power up or reset.

This register can be written or read only when the device is ready (DRB = '1').

**Table 119 — Nonce Register**

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x10F – 0x100	16	R/W	Nonce	

### C.3.3 OW Write Counter Register

The OW Write Counter Register is a 32-bit Register and shall be written with the expected counter value for the execution of several authenticated commands.

The value of this register is undefined after power up or reset.

The OW Write Counter Register can be read to retrieve the internal Write Counter value only after the execution of an Authenticated Erase/Program/Overwrite, Write Counter Digest, when the device returns ready (DRB='1').

The internal Write Counter is a non volatile register which stores the total amount of successful authenticated program, overwrite, erase operations executed by the device.

**Table 120 — Write Counter Register**

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x113 – 0x110	4	R/W	Write Counter	

See [C.4.1](#) for details about internal Write Counter.

### C.3.4 Command Response Register

The Command Response Register can be read only after the execution of an authenticated command and when the device returns ready (DRB='1').

**Table 121 — Command Response Register**

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x115 – 0x114	2	R	Command Response	0x0000

Table 122 defines the value stored in the Command Response Register after the completion of each authenticated command. This register can be read only when the device is ready (DRB = '1'), and it is updated even when the operation is aborted or fails.

**Table 122 — Response**

Command	Value
Write Security Register	0x00A3
Read Security Register	0x00AE
Write Counter Digest	0x00A4
Authenticated Single Word Program	0x00A1
Authenticated Single Word Overwrite	0x00A2
Authenticated Buffered Program	0x00A9
Authenticated Buffered Overwrite	0x00AA
Authenticated Block Erase	0x00A0
Memory Data Digest	0x00A6

### C.3.5 MAC Register

The MAC Register is a 20-Byte register and shall be written with the expected MAC value for the execution of several authenticated commands.

This OW register can be read to retrieve the MAC value after the execution of an authenticated command, when the device returns ready (DRB='1').

The MAC register is updated only if the Authentication Key is enabled.

Note that MAC Register content is not valid if there is an attempt to issue an authenticated command during suspend, or a non authenticated command on an RPMB range, or in case of address failure.

**Table 123 — MAC Register**

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x133 – 0x120	20	R/W	MAC Register	

The value of this register is undefined after power up or reset and it is updated with the execution of an authenticated command.



## C.4 Write Counter, Authentication Key and RPMB Resource

### C.4.1 Write Counter

The Write Counter is an internal 32-bit non volatile register used to count the total amount of successful authenticated program, overwrite, or erase operations executed by the device.

Its initial value after LPDDR2-NVM production is 0x0000 0000. The maximum counter value is 0x0FFF FFFF.

The Write Counter value will be incremented by one automatically by the LPDDR2-NVM Replay Protected Memory Block engine only if the authenticated program, overwrite, or erase operation is executed successfully (no error flag is set in the Status Register).

The value can not be reset. After the counter has reached its maximum value (0x0FFF FFFF), it will not be incremented anymore (overflow prevention), the bit [7] in Command Result Register will be permanently set and the operation being executed will fail.

### C.4.2 Authentication Key

Programmable authentication key register. This register can be programmed or overwritten until the Authentication Lock-Down bit in the Authentication Configuration Register has been set. This register can not be read. The key is used by the LPDDR2-NVM Replay Protected Memory Block engine to authenticate the accesses when MAC is calculated. The Authentication Key is 256-bit and it is written using the Write Security Register command (see [C.6.1](#)).

### C.4.3 Authentication Key Configuration Register

The Authentication Key Configuration Register includes the Authentication Enable bit and the Authentication Lock-Down bit and it is written using the Write Security Register command (see [C.6.1](#)).

**Table 124 — Authentication Key Configuration Register Definition**

Bit	Name	Description	Default
0	AE Authentication Enable bit	0 = Authenticated Operation disabled 1 = Authenticated Operation enabled	'0'
1	AL Lock-Down bit	0 = Authentication Key writable 1 = Authentication Key permanently locked	'0'
from 2 to 15	Reserved	-	'0'

The Authentication Enable bit (bit 0 of Authentication Key Configuration Register) shall be written to '1' to enable the Authentication Key.

If the Authentication Enable bit is not yet programmed to '1', the execution of an authenticated command is not allowed. If the host attempts to execute an authenticated command, the operation will fail and the message 0x07 (Authentication Enable bit not yet programmed) is returned in Result Command Register.

Authentication Lock-Down bit (bit 1 of Authentication Key Configuration Register) shall be written to '1' to permanently lock the Authentication Key and Authentication Enable bit. When the Authentication Lock-Down bit is written to '1' the Authentication Key and the Authentication Enable bit can not be modified.

The Authentication Lock-Down bit is OTP.

LPDDR2-NVM device is delivered with Authentication Enable bit and Authentication Lock-Down bit equal to '0' (default value).

Authentication Enable bit and Authentication Lock-Down shall be programmed after the Authentication Key.

#### C.4.4 RPMB ID, RPMB Start Address, RPMB End Address

LPDDR2-NVM device supports one or more RPMB resources, the number of supported RPMB resources is vendor specific. Each RPMB resource is identified by a 16-bit RPMB ID. If the device supports a single RPMB resource, the RPMB ID shall be equal to 0x00.

RPMB Start Address and RPMB End Address registers define the RPMB range identified by an RPMB ID.

**Table 125 — RPMB Resource**

# of bytes	Description
2	RPMB ID
4	RPMB Start Address
4	RPMB End Address

RPMB Start Address and RPMB End Address shall be less than the device density. RPMB Start Address and RPMB End Address can be set with 16KByte granularity. Therefore RPMB Start Address bits from 0 to 13 are implied to be '0' and shall be program to '0', and RPMB End Address bits from 0 to 13 are implied to be '1' and shall be programmed to '1'. The RPMB range is determined by RPMB Start Address[Max:14] and RPMB End Address[Max:14].

In particular, if the device technology requires the Erase command, the RPMB Start/End Address may be equal to the Block size.

RPMB Start Address and RPMB End Address values shall be written using a single Write Security Register command. The RPMB End Address value shall be greater than the RPMB Start Address. The device checks if this requirement is met during Write Security Register command execution.

#### C.4.5 RPMB Configuration Register

The RPMB Configuration Register includes the RPMB Enable bit and the RPMB Lock-Down bit.

RPMB Enable bit (bit 0 of RPMB Configuration Register) shall be written to '1' to enable the relevant RPMB resource. If RPMB Enable bit is '0', it is not necessary to use Authenticated Commands to change the RPMB content.

RPMB Start Address and RPMB End Address shall be programmed before the RPMB Enable bit.

RPMB Lock-Down bit (bit 1 of RPMB Configuration Register) shall be written to '1' to permanently lock the relevant RPMB Start Address, RPMB End Address and RPMB Enable bit. When the RPMB Lock-Down bit is written to '1' the relevant RPMB Start Address, RPMB End Address and RPMB Enable bit can not be modified.

The RPMB Lock-Down bit is OTP.

LPDDR2-NVM device is delivered with RPMB Lock-Down and RPMB Enable bit equal to '0' (default value) for each RPMB resource.

**Table 126 — RPMB Configuration Register Definition**

Bit	Name	Description	Default
0	RPMBE RPMB Enable bit	0 = RPMB resource disabled 1 = RPMB resource enabled	'0'
1	RPMBL Lock-Down bit	0 = RPMB resource writable 1 = RPMB resource permanently locked	'0'
from 2 to 15	Reserved	-	'0'

## C.5 Message Authentication Code Calculation

The message authentication code (MAC) is calculated using HMAC SHA-1 as defined in [HMAC-SHA]. The HMAC SHA-1 calculation takes as input a key and a message. The resulting signature (MAC) is 160 bits (20 Bytes). The key used for the MAC calculation is always the 256 bit Authentication Key stored in the LPDDR2-NVM.

The message used as input to the MAC calculation is the concatenation of some OW registers value, the write counter, buffer program content for embedded operation using the buffer program, memory content for memory data digest.

When issuing an Authenticated Erase Command, an Authenticated Single Word/Buffered Program command or an Authenticated Single Word/Buffered Overwrite command, the host shall calculate the signature as described in [Table 127](#), and store it in the Overlay Window MAC register.

After the completion of an Authenticated Erase Command, an Authenticated Single Word/Buffered Program command or an Authenticated Single Word/Buffered Overwrite command, the LPDDR2-NVM device updates the MAC register as described in [Table 128](#).

After the completion of a Memory Data Digest command or a Write Counter Digest command, the LPDDR2-NVM device provides the signature calculated as described in [Table 128](#) in the MAC register.

**Table 127 — MAC calculation bytes order for command authentication**

Field	Authenticated Erase Command	Authenticated Single Word Program <sup>(1)</sup>	Authenticated Single Word Overwrite <sup>(1)</sup>	Authenticated Buffered Program	Authenticated Buffered Overwrite <sup>(1)</sup>	Memory Data Digest	Write Counter Digest
First	CmdCode	CmdCode	CmdCode	CmdCode	CmdCode	-	-
Second	Counter <sup>(4)</sup>	Counter <sup>(4)</sup>	Counter <sup>(4)</sup>	Counter <sup>(4)</sup>	Counter <sup>(4)</sup>	-	-
Third	4 bytes = 0x00	Data	Data	MPReg	MPReg	-	-
Fourth	Address	Address	Address	Address	Address	-	-
Fifth	-	-	-	2 bytes = 0x00	2 bytes = 0x00	-	-
Sixth	-	-	-	PB[D-1:0] <sup>(3)</sup>	PB[D-1:0] <sup>(3)</sup>	-	-

**Table 128 — MAC calculation bytes order for Result, Data, Write Counter authentication**

Field	Authenticated Erase Command	Authenticated Single Word Program <sup>(1)</sup>	Authenticated Single Word Overwrite <sup>(1)</sup>	Authenticated Buffered Program	Authenticated Buffered Overwrite <sup>(1)</sup>	Memory Data Digest	Write Counter Digest
First	Response	Response	Response	Response	Response	Response	Response
Second	Counter <sup>(4,6)</sup>	Counter <sup>(4,6)</sup>	Counter <sup>(4,6)</sup>	Counter <sup>(4,6)</sup>	Counter <sup>(4,6)</sup>	4 bytes = 0x00	Counter <sup>(4,6)</sup>
Third	4 bytes = 0x00	4 bytes = 0x00	4 bytes = 0x00	4 bytes = 0x00	4 bytes = 0x00	MPReg	4 bytes = 0x00
Fourth	Address	Address	Address	Address	Address	Address	4 bytes = 0x00
Fifth	Result	Result	Result	Result	Result	Result	Result
Sixth	-	-	-	-	-	Nonce	Nonce
Seventh	-	-	-	-	-	N bytes <sup>(5)</sup> = Digested Data	-

### C.5 Message Authentication Code Calculation (cont'd)

The following notes apply to both [Table 127](#) and [Table 128](#).

NOTE 1: Authenticated Single Word command, Authenticated Single Word Overwrite command and Authenticated Buffered Overwrite command are optional and supported only by some NVM technologies

NOTE 2: Counter = Write Counter[3:0], CmdCode = Command Code[1:0], Data = Command Data[3:0], MPReg = Multi-Purpose Register[3:0], Address = Command Address[3:0], PB[D-1:0] = Program Buffer[D-1:0] where D is the top location of the program buffer, Nonce = Nonce[15:0], Result = Command Result[1:0], Response = Command Response[1:0].

NOTE 3: D is the Program Buffer size. If the amount of bytes being programmed is less than the Program Buffer size, not relevant Program buffer bytes shall be considered 0x00 during MAC calculation, the host shall fill the entire Program Buffer, "0x00" value shall be written to not relevant Program buffer bytes.

NOTE 4: Four most significant bits of the Write Counter are '0'.

NOTE 5: N is the amount of bytes on which the MAC is calculated during Memory Data Digest command.

NOTE 6: The incremented counter value shall be used if Authenticated Erase/Program/Overwrite is completed successfully.

Example: Assume that the write counter is 0x01234567 and the Program Buffer Size is 32 Bytes. The host wants to program the pattern 0xA0, 0xA1, 0xA2, 0xA3, 0xA4, 0xA5, 0xA6, 0xA7 at starting address 0x00000010. The host set the Overlay window register with the following values: Command Code = 0x00A9, Multi-Purpose Register = 0x00000008, Command Address = 0x00000010, and it loads the pattern into the Program buffer starting at the offset: Program-Buffer Offset + 0x0010 within the OW.

The HMAC SHA-1 shall be calculated over the following message:

Com. Code	Write Counter	Multi-Purpose Register	Command Address	2 bytes 0x00	
0x00, 0xA9, 0x01, 0x23, 0x45, 0x67, 0x00, 0x00, 0x00, 0x08, 0x00, 0x00, 0x00, 0x10, 0x00, 0x00,	Program Buffer[0] ...Program Buffer[15]				
0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,					
Program Buffer[16] ...Program Buffer[31]					
0xA0, 0xA1, 0xA2, 0xA3, 0xA4 0xA5, 0xA6 0xA7, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00					

Reference: [HMAC-SHA] H. Krawczyk, M. Bellare, R. Canetti. "HMAC: Keyed-Hashing for Message Authentication", RFC 2104, February 1997.

## C.6 LPDDR2-NVM RPMB commands

This section defines the set of commands for the execution of authenticated operations.

The commands for authenticated operations are: Write Security Register, Authenticated Single Word Program, Authenticated Single Word Overwrite, Authenticated Buffered Program, Authenticated Buffered Overwrite, Authenticated Block Erase, Write Counter Digest, Memory Data Digest, Command Result Digest.

Write Security Register command can be used to store the authentication key and configure the RPMB resource.

Write Counter value can be authenticated using the Write Counter Digest command.

Erase, program, or overwrite commands issued in an RPMB range are executed only if the command is successfully authenticated (MAC provided by the host matches the MAC calculated by the device), and if the write counter value provided by the host is equal to the write counter value stored in the device.

[Table 129](#) summarizes the command code values for the authenticated commands. The command code shall be written into the Command Code Register within the Overlay Window (see Overlay Window register map table) to select the desired operation to be executed.

**Table 129 — LPDDR2 RPMB Commands**

Command	Code
Write Security Register	0x00A3
Read Security Register	0x00AE
Write Counter Digest	0x00A4
Authenticated Single Word Program <sup>(2)</sup>	0x00A1
Authenticated Single Word Overwrite <sup>(3)</sup>	0x00A2
Authenticated Buffered Program	0x00A9
Authenticated Buffered Overwrite <sup>(3)</sup>	0x00AA
Authenticated Block Erase	0x00A0
Memory Data Digest	0x00A6

NOTE 1: The Command Code Register default value is 0x0000 (NOP). If the Command Execute Register is set to '0x0001' when Command Code Register is at the default value (0x0000), the device will become busy and then ready without executing any operation (NOP).

NOTE 2: Authenticated Single Word Program is optional.

NOTE 3: Authenticated Single Word Overwrite and Authenticated Buffered Overwrite are optional and are only supported by some NVM technologies and some LPDDR2-NVM devices.

An embedded controller handles all timings and verifies the correct execution of LPDDR2-NVM operations.

The commands can be initiated when the embedded controller is not busy (DRB = '1'). The Device Ready Bit (DRB) is read as part of the Status Register.

VACC shall not change during the period starting from at least 1us prior to the initiation of any embedded operation until that embedded operation is complete.

During the execution of an embedded operation, the device can be placed in Power Down mode by driving CKE low, see Power Down section for detailed description on how to enter and exit Power Down.

### C.6.1 Write Security Register Command

Write Security Register command allows to program the Authentication Key, the Authentication Key Configuration, and to define the RPMB resources. As the system can not be authenticated yet in this phase the authentication key programming have to take place in a secure environment like in an OEM production.

There are two types of data that can be configured: Authentication Key resource and RPMB resources. Type is provided using the Command Data [15:0].

Each RPMB resource is identified by an ID. RPMB ID is provided using Command Data [31:16]. The number of available RPMB resources is vendor specific.

Table 130 shows the value to be loaded into the Command Data Register according to the type of data to be written.

The desired data to be written into the Security Registers shall be stored in the Program Buffer.

The offset of the first Security Register to be written shall be stored in Command Address Register as defined on Table 131. The Multi-Purpose Register shall contain the number of bytes to be programmed.

The program operation is performed by the embedded controller.

This command can not be issued during suspend.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:

- Write the offset of the first Security Register to the Command Address register,
- Write Register Type and ID to the Command Data Register,
- Write the Data Count value (number of bytes to be programmed) to the Multi-Purpose Register,
- Write data into the Program Buffer.
- Write 0x00A3 to the Command Code Register,
- Write 0x0001 to the Command Execute Register.

**Table 130 — Data Type Definition**

Command Data Register	Field	Data Type	
		Authentication Key	RPMB
Command Data [31:16]	ID	0x0000 (default)	RPMB ID
Command Data [15:0]	Type	0x0000	0x0001

**Table 131 — Security Register Mapping for Write Security Reg. Command**

Data Type	Command Addr. Reg. Value	Program Buffer Range	# of bytes	Program Buffer Value
Authentication Key / Configuration	0x0000	Progr.Buffer[0x01F:0x000]	32	Authent.Key[0x1F:0x00]
	0x0020	Progr.Buffer[0x021:0x020]	2	Authent. Key Config. [1:0]
RPMB	0x0000	Progr.Buffer[0x003:0x000]	4	RPMB Start Address [3:0]
	0x0004	Progr.Buffer[0x007:0x004]	4	RPMB End Address [3:0]
	0x0008	Progr.Buffer[0x009:0x008]	2	RPMB Configuration [1:0]

The Status Register DRB bit, indicates the progress of the Program operation. It should be read to check whether the operation has completed or not.

After completion of the Program operation (DRB= 1), one of the Status Register error bits (5, 4, 3 and 1) going High means that an error was detected: either a failure occurred during programming, VACC is outside the allowed voltage range. See Section Device Status Register for detailed information.

Providing not allowed values for Command Data Register, Command Address Register, and Multi-Purpose Register can result in undefined operation.

The program operation can not be suspended or aborted.

### C.6.1 Write Security Register Command (cont'd)

Authenticated Operations are enabled when Authentication Enable bit in the Authentication Key Configuration Register is '1'.

The Authentication Key can be programmed only when Authentication Lock-Down bit is '0'. If there is an attempt to program the Authentication Key or Authentication Key Configuration when the Authentication Lock-Down bit is '1', the operation will fail and the Command Result Register is set 0x0B.

RPMB Start Address and RPMB End Address values shall be written with a single Write Security Register command.

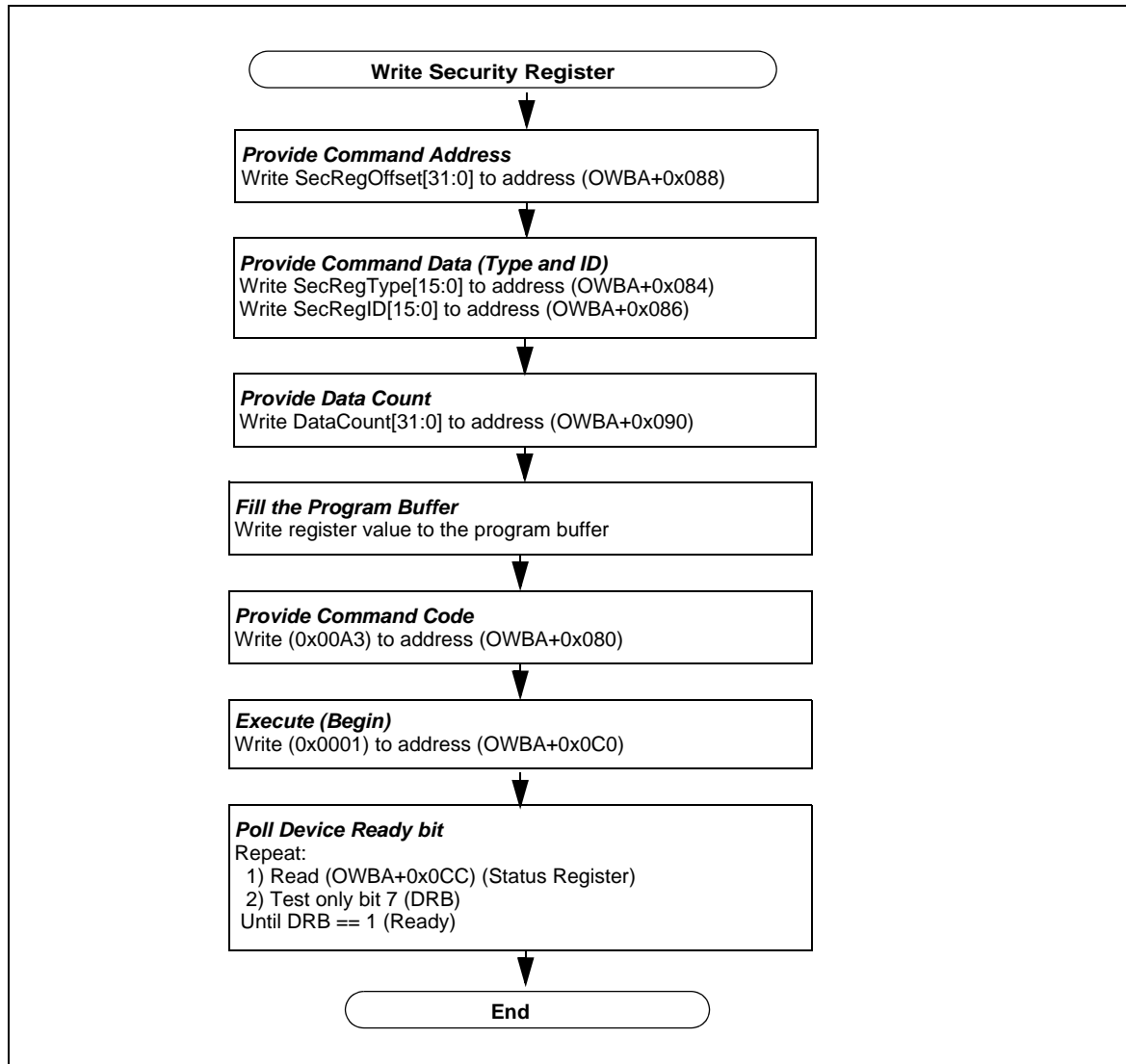
RPMB Start Address and RPMB End Address can be programmed only when the relevant RPMB Lock-Down bit is '0'. If there is an attempt to program these registers when the RPMB Lock-Down bit is '1', the operation will fail and the Command Result Register is set 0x0B. Since RPMB Lock-Down bits are OTP, the RPMB resource will no longer be available after the relevant Lock-Down bit has been set.

C.4.4 defines the constraints for RPMB Start Address value and RPMB End Address value.

The RPMB End Address value shall not be lower than the RPMB Start Address value. The device check if this requirement is met before programming them. If RPMB End Address value is lower than the RPMB Start Address value, the programming will fail and the Command Result Register is set 0x05.

**Table 132 — Write Security Register Error Conditions**

7	6	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Write Security Data operation failure.
1	0	0	1	0	0	1	0	Write Security Data operation abort. a) Attempt to program Authentication Key or Authentication Key Configuration with Authentication Lock-Down bit equal to '1' b) Attempt to program RPMB Enable/Start/End address with RPMB Lock-Down bit equal to '1'
1	0	1	1	0	0	0	0	Write Security Data operation abort. a) Program address outside the allowed address space b) Invalid RPMB ID c) Attempt to program invalid RPMB Start/End address content.
1	0	0	1	1	0	0	0	Write Security Data operation abort. VACC not at appropriate level for Program operation.
1	1	1	1	0	0	0	0	Write Security Data operation abort. Attempting to execute the command during Erase Suspend.
1	0	1	1	0	1	0	0	Write Security Data operation abort. Attempting to execute the command during Program Suspend.
1	1	1	1	0	1	0	0	Write Security Data operation abort. Attempting to execute the command during Erase and Program Suspend.

**C.6.1 Write Security Register Command (cont'd)**

NOTE 1: The Overlay Window must be open to issue Write Security Register command.

NOTE 2: OWBA is the byte address of the Overlay Window Base Address.

NOTE 3: The device must be Ready (DRB==1') before starting the command sequence.

NOTE 4: DataCount[31:0] is amount of byte being programmed.

NOTE 5: SecRegOffset[31:0] is the target byte offset of the programming operation, SecRegType is the type of data and SecRegID is the ID of the data to be written (see [Table 130](#) and [Table 131](#)).

**Figure 136 — Write Security Register Flowchart**



### C.6.2 Read Security Register Command

RPMB Registers and Authentication Key Configuration Register can be read with the Read Security Register command (code 0x00AE). The Read Security Register command copies the content of the desired register into the Command Result. Multiple Read Security Register commands can be used to retrieve the value of registers wider than Command Result.

There are two types of data that can be read: Authentication Key resource and RPMB resources. Type is provided using the Command Data [15:0].

Each RPMB resource is identified by an ID. The ID of the resource to be read is provided using Command Data [31:16].

Table 130 shows the values to be loaded into the Command Data Register according to the type of data to be read.

Table 133 shows the offset value that shall be loaded into the Command Address Register to select the desired portion of the Security Register. Please note that if an attempt is made to read the Authentication Key Register, the device will return undefined data.

Read Security Register operation is performed by the embedded controller.

This command can not be issued during suspend.

This command cannot be aborted or suspended.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:

Write the desired register offset to the Command Address Register,  
Write Register Type and ID to the Command Data Register,  
Write 0x00AE to the Command Code Register,  
Write 0x0001 to the Command Execute Register,  
Read the Security Register data from the Command Result Register, if there are no errors in the Status Register.

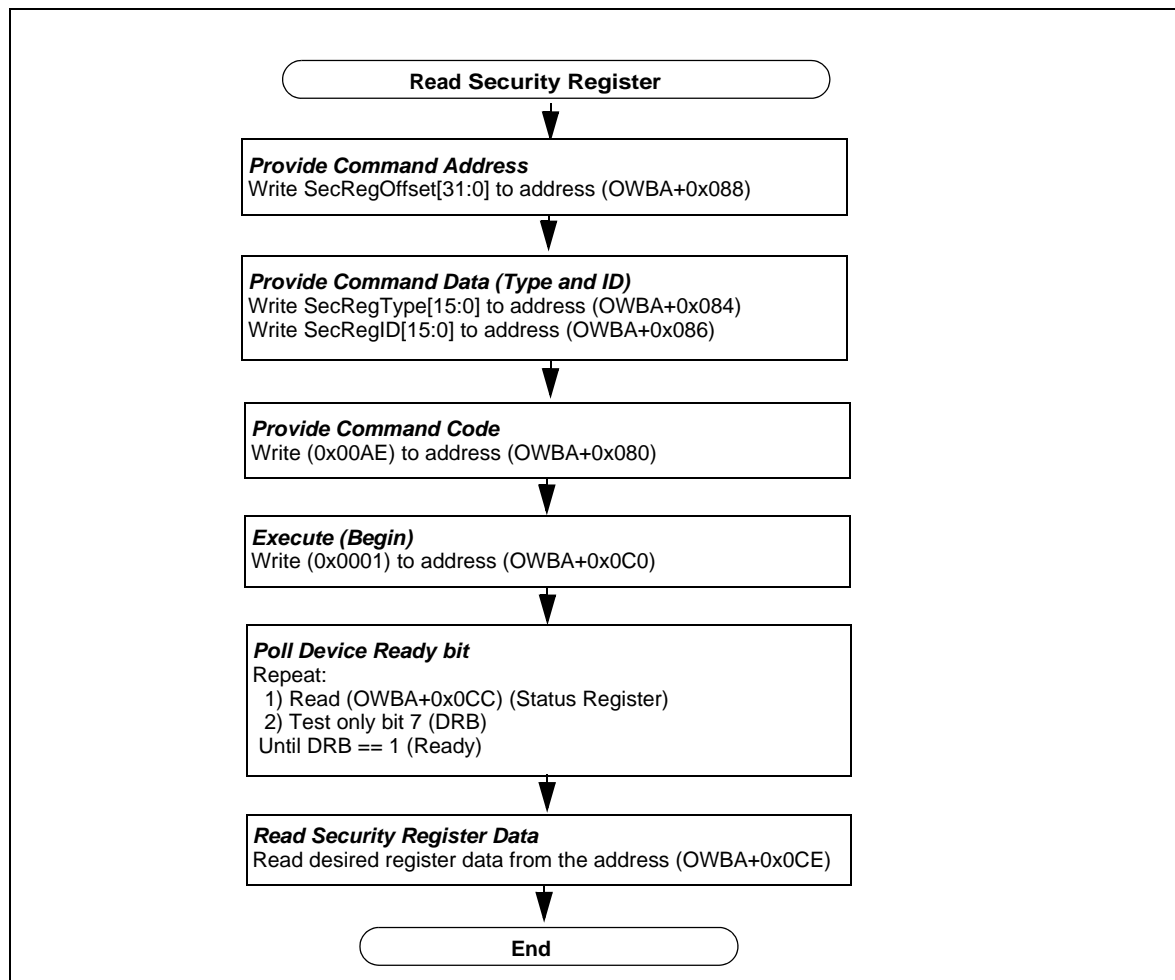
Status Register SR4 (PSB) and SR5 (ESB) bits are set to '1' to indicate that the Read Security Register operation has failed.

**Table 133 — Security Register Mapping for Read Security Reg. Command**

Data Type	Command Addr. Reg. Value	Security Register Mapping
Authentication Key Configuration	0x0020	Authent. Key Config. [1:0]
RPMB	0x0000	RPMB Start Address [1:0]
	0x0002	RPMB Start Address [3:2]
	0x0004	RPMB End Address [1:0]
	0x0006	RPMB End Address [3:2]
	0x0008	RPMB Configuration [1:0]

**Table 134 — Read Security Register Error Conditions**

7	6	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	1	1	0	1	0	0	Read Security Register operation failure. Attempting to execute the command during Program Suspend
1	1	1	1	0	0	0	0	Read Security Register operation failure. Attempting to execute the command during Erase Suspend
1	1	1	1	0	1	0	0	Read Security Register operation failure. Attempting to execute the command during Erase Suspend and Program Suspend

**C.6.2 Read Security Register Command (cont'd)**

NOTE 1: The Overlay Window must be open to issue Read Security Register command.

NOTE 2: OWBA is the byte address of the Overlay Window Base Address.

NOTE 3: The device must be Ready (DRB==’1’) before starting the command sequence.

NOTE 4: SecRegOffset[31:0] is the target byte offset of the Security Register, SecRegType is the type of data and SecRegID is the ID of the data to be read (see [Table 130](#) and [Table 133](#)).

**Figure 137 — Read Security Register Flowchart**

### C.6.3 Write Counter Digest Command

Write Counter Digest command provides the digestment of write counter value (the MAC).

The host shall provide a 16-Byte Nonce, which will be used in the MAC calculation.

Note that the OW Write Counter register is updated during the execution of the authenticated program, overwrite, erase command or Write Counter Digest command; and it shall be read only when the device is ready.

The Write Counter Digest command can not be issued during suspend.

The Write Counter Digest operation is performed by the embedded controller.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:

Write 0x00A4 to the Command Code Register,  
Write the nonce into the Nonce Register,  
Write 0x0001 to the Command Execute Register.

The Status Register DRB bit, indicates the progress of the Write Counter Digest operation. It should be read to check whether the operation has completed or not.

After completion of the Write Counter Digest operation (DRB= 1), the device updates the following Overlay Window registers: the Write Counter, the Command Result, the Command Response and the MAC.

See C.5 for details about MAC calculation.

The Nonce value received in the request is available in the Nonce Register.

The Write Counter Digest operation can not be suspended but it can be aborted.

The successfulness of the Write Counter Digest can be checked reading the Command Result Register (when DRB = '1').

If Write Counter Digest command is issued during suspend then returned result is 0x09 (Command issued during suspend), the Status Register error bits 4 and 5 are set, and MAC Register content is no longer valid.

If reading of the counter value fails then returned result is 0x06 (Read failure).

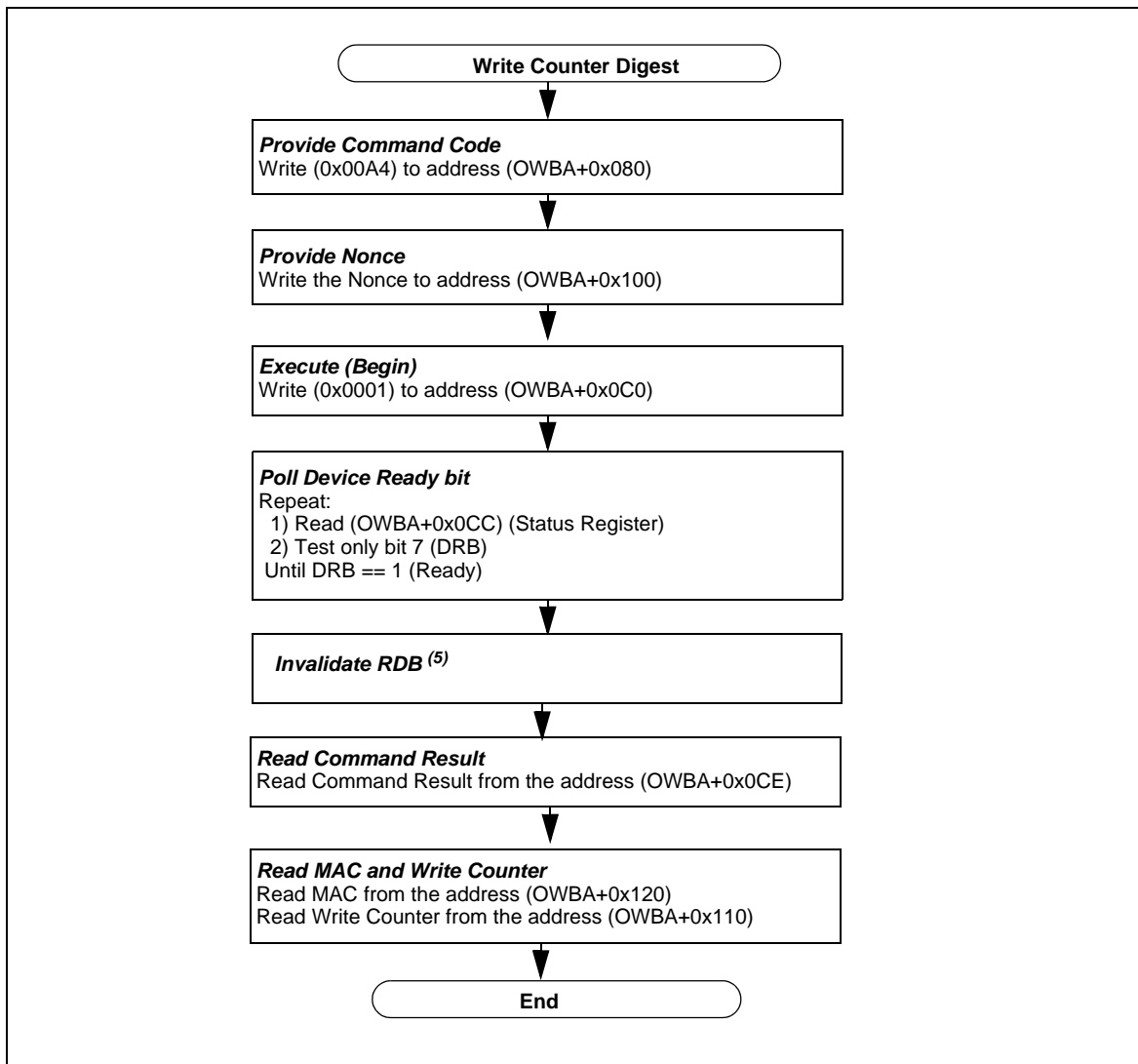
If the Write Counter Digest command is aborted or if some other error occurs then result is 0x01 (General failure).

If Counter has expired also bit 7 is set to 1 in returned result (Result values 0x80, 0x86 and 0x81).

Note that the MAC Register content is no longer valid if the Write Counter Digest command has been aborted.

**Table 135 — Write Counter Digest Error Conditions**

7	6	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	1	1	0	1	0	0	Write Counter Digest operation failure. Attempting to execute the command during Program Suspend
1	1	1	1	0	0	0	0	Write Counter Digest operation failure. Attempting to execute the command during Erase Suspend
1	1	1	1	0	1	0	0	Write Counter Digest operation failure. Attempting to execute the command during Erase Suspend and Program Suspend

**C.6.3 Write Counter Digest Command (cont'd)**

NOTE 1: The Overlay Window must be open to issue Write Counter Digest command

NOTE 2: OWBA is the byte address of the Overlay Window Base Address

NOTE 3: The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4: Command Result shall be read when the device is ready (DRB=='1').

NOTE 5: RDB invalidation may be required to avoid risk of incoherency between memory array content and RDB content. For more details refer to [4.7.12](#).

**Figure 138 — Write Counter Digest Flowchart**

#### C.6.4 Memory Data Digest Command

The Memory Data Digest command provides the digestment of data stored in an RPMB range of the memory (the MAC).

The host shall provide: 16-Byte Nonce, the start address of the data region in the Command Address Register, and the amount of bytes of the data region in the Multi-Purpose Register.

Start address shall be 32-Byte aligned and the amount of bytes of the data region shall be a multiple of 32 Bytes and equal or lower than 1 KByte. Providing not allowed values can result in undefined operation.

The device will read the data region and use it for the MAC calculation.

Data from the RPMB range can be read issuing PREACTIVE, ACTIVATE and READ commands, and it is not mandatory to execute the Memory Data Digest command to read RPMB range.

The Memory Data Digest command is performed by the embedded controller.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:

- Write 0x00A6 to the Command Code Register,
- Write the nonce into the Nonce Register,
- Write the desired address into the Command Address register,
- Write the desired amount of bytes into the Multi-Purpose register,
- Write 0x0001 to the Command Execute Register.

The Status Register DRB bit, indicates the progress of the authentication operation. It should be read to check whether the operation has completed or not.

After completion of the Memory Data Digest operation (DRB = '1'), the device updates the following Overlay Window registers: the Command Result, the Command Response, and the MAC.

See C.5 for details about MAC calculation.

The Nonce value received in the request is available in the Nonce Register.

The Memory Data Digest operation can be suspended and it can be aborted.

PSSB (SR.2) bit of the Status Register is set to '1' during Memory Data Digest suspended.

The successfulness of the Memory Data Digest can be checked reading the Command Result Register (when DRB = '1').

If Memory Data Digest command is issued during suspend then returned result is 0x09 (Command issued during suspend), the Status Register error bits 4 and 5 are set, and MAC Register content is no longer valid.

If the address is outside RPMB range then Command Result Register is set to 0x04 (Address failure), no Status Register error bits are set, and MAC Register content is no longer valid. If the MAC calculation fails Command Result Register is set to 0x02 (Authentication failure), otherwise it is set to 0x00 (Operation OK). If Memory Data Digest is aborted or if some other error occurs during the read procedure then returned result is 0x01 (General failure).

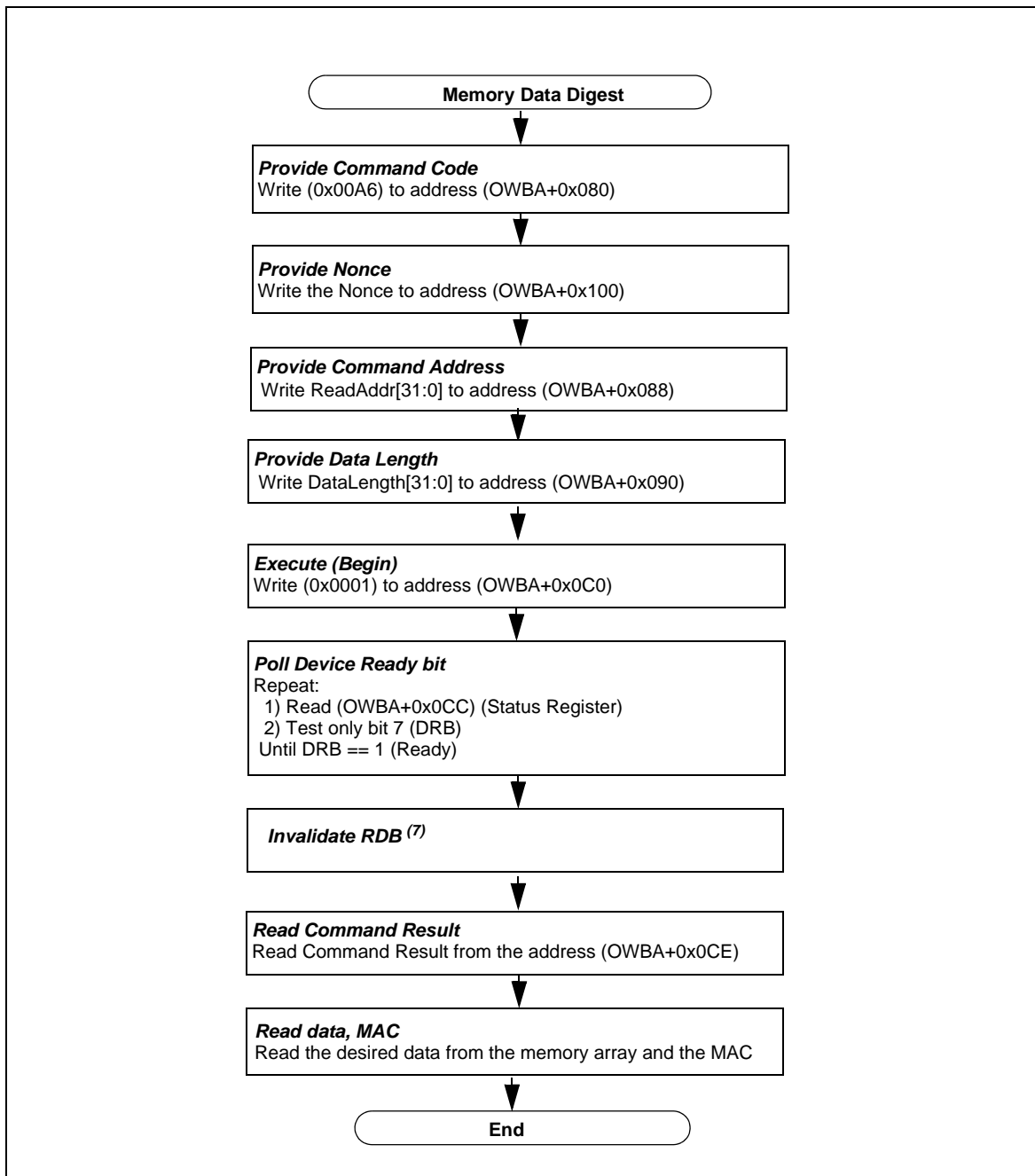
If the Counter has expired, bit 7 is also set to 1 in returned result (Result values 0x80, 0x84 and 0x82).

Note that the MAC Register content is no longer valid if the Memory Data Digest command has been aborted.

**Table 136 — Memory Data Digest Error Conditions**

7	6	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	1	1	0	1	0	0	Memory Data Digest operation failure. Attempting to execute the command during Program Suspend
1	1	1	1	0	0	0	0	Memory Data Digest operation failure. Attempting to execute the command during Erase Suspend
1	1	1	1	0	1	0	0	Memory Data Digest operation failure. Attempting to execute the command during Erase Suspend and Program Suspend

#### C.6.4 Memory Data Digest Command (cont'd)



NOTE 1: The Overlay Window must be open to issue Memory Data Digest command

NOTE 2: OWBA is the byte address of the Overlay Window Base Address

NOTE 3: The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4: Command Result can be read when the device is ready (DRB=='1').

NOTE 5 ReadAddr[31:0] is the target byte address of the data region to be digested, and it shall be 32-Byte aligned.

NOTE 6: DataLength[31:0] is amount of bytes the data region to be digested, and it shall be a multiple of 32.

NOTE 7: RDB invalidation may be required to avoid risk of incoherency between memory array content and RDB content. For more details refer to [4.7.12](#).

**Figure 139 — Memory Data Digest Flowchart**

### C.6.5 Authenticated Block Erase Command

The Authenticated Block Erase command is used to erase a Block included in an RPMB range. It sets all the bits within the selected Block to '1'. All previous data in the Block is lost. If the Block is locked, the erase operation will abort, the data in the Block will not be changed and the Device Status Register will output the error.

The erase operation is performed by the embedded controller.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:

Write 0x00A0 to the Command Code Register,

Write any address within the desired block to the Command Address Registers,

Write the expected write counter value into OW Write Counter Register

Write the MAC to MAC register

Write 0x0001 to the Command Execute Register

The Authenticated Block Erase command can be suspended but it can not be aborted.

Note that some NVM technologies do not need Erase command, therefore some NVM devices will not support it.

The Status Register DRB bit indicates the progress of the Authenticated Block Erase operation. It should be read to check whether the operation has completed or not.

The successfulness of the Authenticated Block Erase command should be checked by reading the Status Register and the Command Result Register (when DRB = '1').

If the Authenticated Block Erase command is issued during suspend, the operation fails, the Status Register error bits 4 and 5 are set, the Command Result register is set to 0x09 (Command issued during suspend), and MAC Register content is no longer valid.

If the Block being erased is locked an error will be set in the Status Register and the operation will abort without affecting the data in the memory array.

If the address is outside RPMB range then Command Result Register is set to 0x04 (Address failure), no Status Register error bits are set, and MAC Register content is no longer valid.

Then the device checks whether the write counter has expired. If the write counter is expired the LPDDR2-NVM device sets the Command Result Register to 0x85 (write failure, write counter expired), and no Status Register error bit is set.

If the write counter is not expired, the LPDDR2-NVM starts MAC calculation as described in [Table 127](#). Note that the OW Write Counter Register and not the internal Write Counter Register shall be used for this calculation.

LPDDR2-NVM device compares the calculated MAC with the MAC value received in the MAC Register.

If the two MAC's are different the Command Result Register is set to 0x02 (authentication failure). The Authenticated Block Erase command is not executed.

If the MAC in the request and the calculated MAC are equal then the LPDDR2-NVM device compares the write counter in the request, present in the OW Write Counter Register, with the write counter stored in the device. If the two counters are different then the device sets the Command Result Register to 0x03 (counter failure). The embedded operation is not executed.

If the MAC and write counter comparisons are successful the command request is considered to be authenticated, and the erase operation is executed.

If the embedded command is successfully completed the write counter is incremented by 1.

If the erase command fails, the Status Register error bit 5 is set and the returned Command Result Register is 0x05 (write failure).

If some other error occurs during the embedded command procedure then returned result is 0x01 (General failure).

After completion of the Authenticated Block Erase operation (DRB= 1), the device updates the following Overlay Window registers: the Command Result, the Write Counter, the Command Response and the MAC.

During the busy state, the device updates automatically the OW MAC Register as described in [Table 128](#).

The reset command interrupts an ongoing erase operation. As data integrity cannot be guaranteed when the erase operation is aborted, the memory array content must be considered invalid.

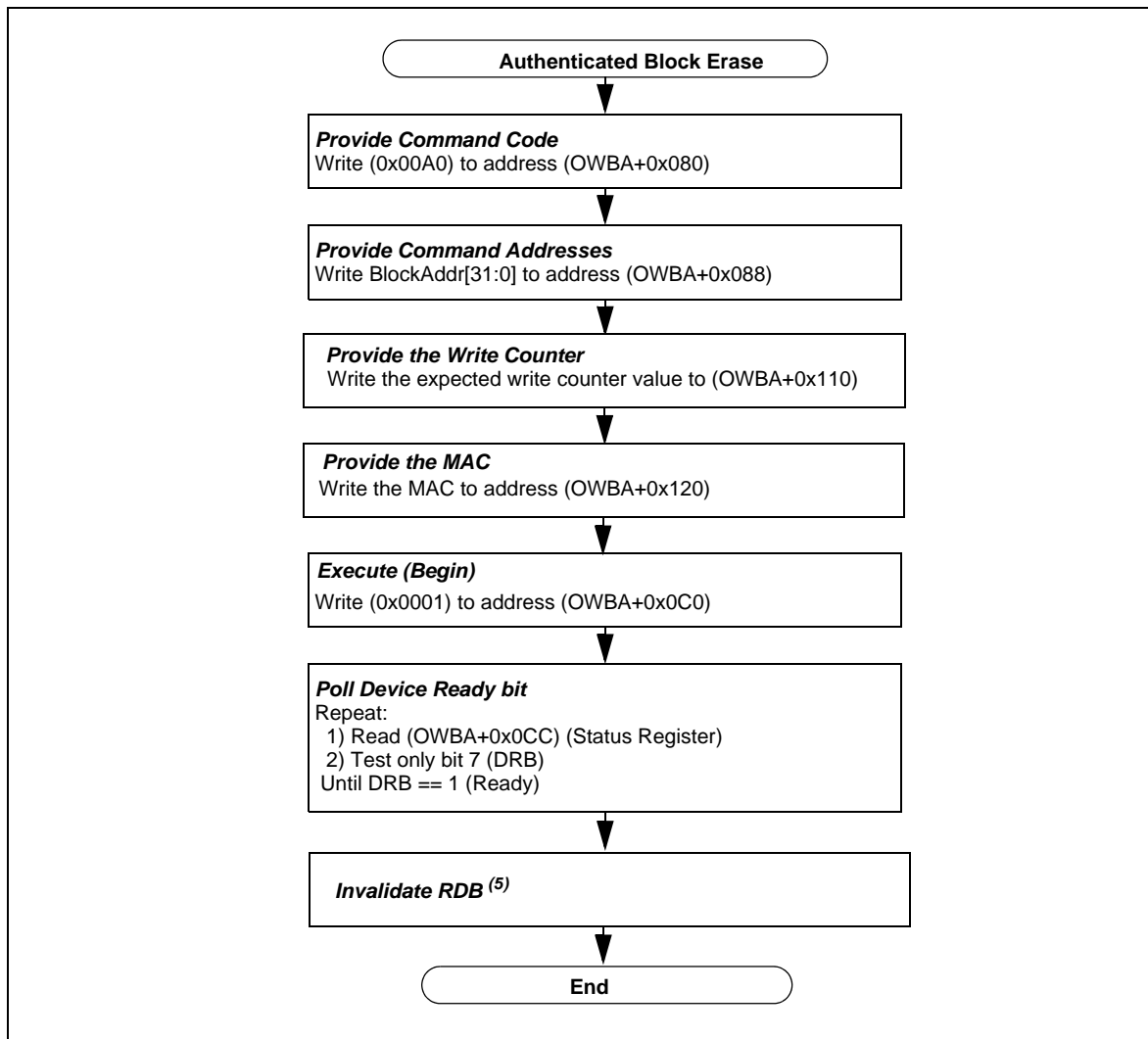
### C.6.5 Authenticated Block Erase Command (cont'd)

**Table 137 — Authenticated Block Erase Error Conditions**

7	6	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	1	0	0	0	0	0	Erase operation failure
1	0	1	0	0	0	1	0	Erase operation abort. An erase operation was attempted on a locked block.
1	0	1	0	1	0	0	0	Erase operation abort. VACC not at appropriate level for Erase operation.
1	0	1	1	0	0	0	0	Erase operation abort. Block address outside the LPDDR2-NVM address space.
1	1	1	1	0	0	0	0	Erase operation abort. Attempting to erase a block during Erase Suspend.
1	0	1	1	0	1	0	0	Erase operation abort. Attempting to erase a block during Program Suspend.
1	1	1	1	0	1	0	0	Erase operation abort. Attempting to erase a block during Erase Suspend and Program Suspend.

Figure 140 shows the Authenticated Block Erase Flowchart.





NOTE 1 The Overlay Window must be open to issue Authenticated Block Erase command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 BlockAddr[31:0] is any byte address within the block being erased

NOTE 5 RDB invalidation may be required to avoid risk of incoherency between memory array content and RDB content. For more details refer to [4.7.12](#).

**Figure 140 — Authenticated Block Erase Flowchart**

### C.6.6 Authenticated Single Word Program Command

The Authenticated Single Word Program command is used to program a single word (2-byte data) into an RPMB range.

This command is optional.

The program operation is performed by the embedded controller.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:

- Write 0x00A1 to the Command Code Register,
- Write desired location address to the Command Address Register,
- Write desired program data to the Command Data Register (Command Data[15:0] only),
- Write the expected write counter value into OW Write Counter Register
- Write the MAC to MAC register
- Write 0x0001 to the Command Execute Register.

Programming can be performed in one block at a time.

The Status Register DRB bit indicates the progress of the Program operation. It should be read to check whether the operation has completed or not.

After completion of the Program operation (DRB= 1), one of the Status Register error bits (4,3 and 1) going High means that an error was detected: either a failure occurred during programming, VACC is outside the allowed voltage range or an attempt to program a locked Block was made. See Section Device Status Register for detailed information.

The authenticated program operation can be suspended but it can not be aborted.

The successfulness of the Authenticated Single Word Program command should be checked by reading the Status Register and the Command Result Register (when DRB = '1').

If the Authenticated Single Word Program command is issued during suspend, the operation fails, the Status Register error bits 4 and 5 are set, the Command Result register is set to 0x09 (Command issued during suspend), and MAC Register content is no longer valid.

If the address is outside RPMB range then Command Result Register is set to 0x04 (Address failure), no Status Register error bits are set, and MAC Register content is no longer valid.

The device checks whether the write counter has expired. If the write counter is expired the LPDDR2-NVM device sets the Command Result Register to 0x85 (write failure, write counter expired), and no Status Register error bit is set.

If the write counter is not expired, the LPDDR2-NVM starts MAC calculation as described in [Table 127](#). Note that the OW Write Counter Register and not the internal Write Counter Register shall be used for this calculation.

LPDDR2-NVM device compares the calculated MAC with the MAC value received in the MAC Register.

If the two MAC's are different the Command Result Register is set to 0x02 (authentication failure). The Authenticated Single Word Program command is not executed.

If the MAC in the request and the calculated MAC are equal then the LPDDR2-NVM device compares the write counter in the request, present in the OW Write Counter Register, with the write counter stored in the device. If the two counters are different then the device sets the Command Result Register to 0x03 (counter failure). The embedded operation is not executed.

If the MAC and write counter comparisons are successful the command request is considered to be authenticated, and the program operation is executed.

If the embedded command is successfully completed the write counter is incremented by 1.

If the program command fails, the Status Register error bit 4 is set and the returned Command Result Register is 0x05 (write failure).

If some other error occurs during the embedded command procedure then returned result is 0x01 (General failure).

After completion of the Authenticated Single Word Program operation (DRB= 1), the device updates the following Overlay Window registers: the Command Result, the Write Counter, the Command Response and the MAC.

During the busy state, the device updates automatically the OW MAC Register as described in [Table 128](#).

The reset command interrupts an ongoing program operation. As data integrity cannot be guaranteed when the program operation is aborted, the memory array content must be considered invalid.

### C.6.6 Authenticated Single Word Program Command

Some NVM technologies support the Authenticated Single Word Program command only under particular conditions.

For example, for LPDDR2-NVM device that has the notion of program region, Authenticated Single Word Program Command is supported only by program regions configured in the Control Program mode, and with Command Address value belonging to a particular portion of the program region.

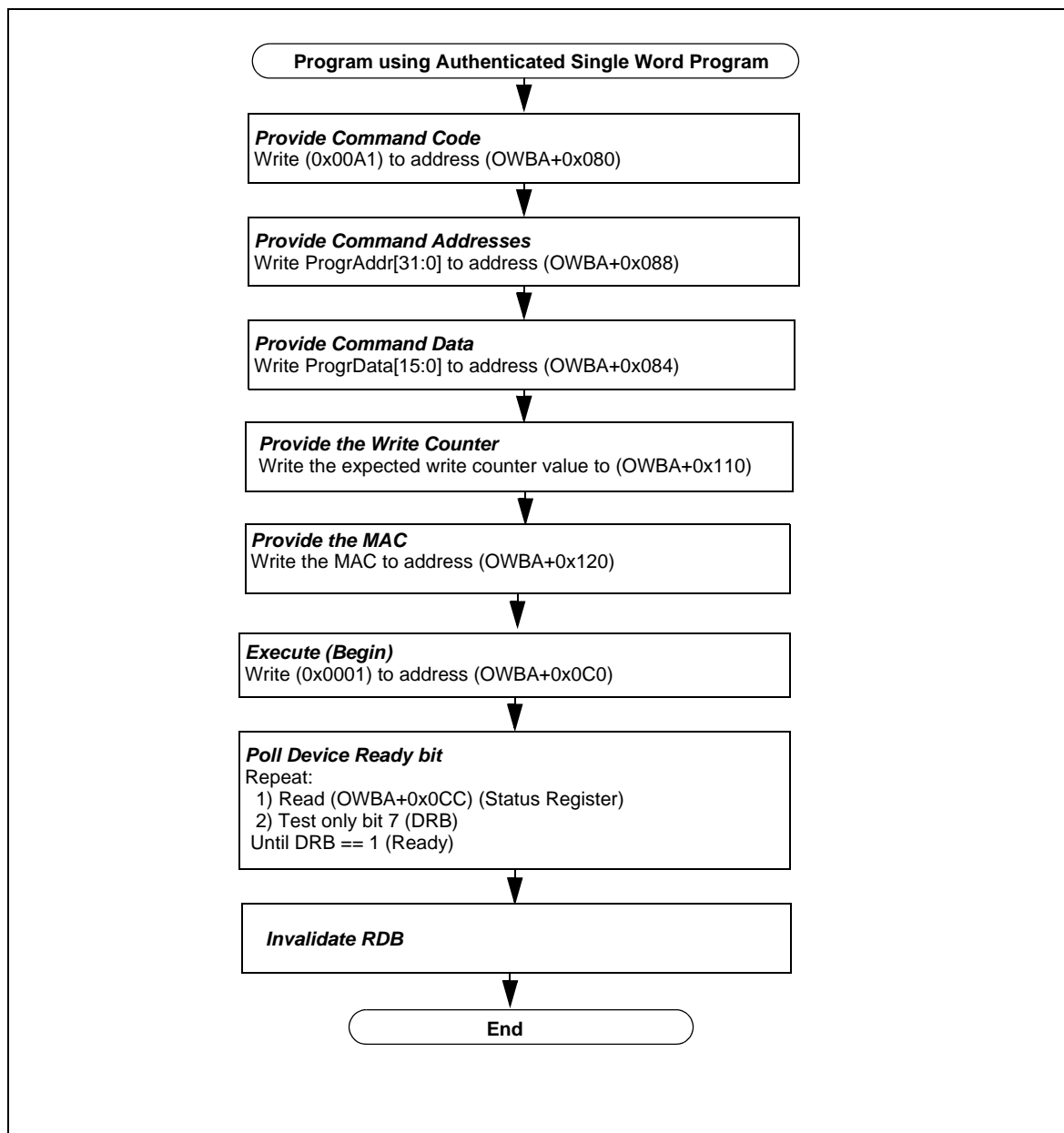
If an Authenticated Single Word Program command is issued to a Program Region configured in the Object Program mode, the Program operation is aborted and PSB and OMSB Status Register bits are set.

For details about program region and program method see the application note.

**Table 138 — Authenticated Single Word Program Error Conditions**

7	6 <sup>(1)</sup>	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Authenticated Single Word Program operation failure.
1	0	0	1	0	0	1	0	Authenticated Single Word Program operation abort. A program operation was attempted on a locked block.
1	0	0	1	1	0	0	0	Authenticated Single Word Program operation abort. VACC not at appropriate level for Program operation.
1	0	1	1	0	0	0	0	Authenticated Single Word Program operation abort. Program address outside the LPDDR2-NVM address space
1	0	1	1	0	1	0	0	Authenticated Single Word Program operation abort. Attempting to program during Suspend.

NOTE 1: ESSB Status Register bit is '1' in case of command issued during Erase Suspend.



NOTE 1 The Overlay Window must be open to issue Authenticated Single Word Program command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 ProgrAddr[31:0] is the target byte address of the programming operation, and ProgrAddr[0] shall be '0'.

NOTE 5 ProgrData[15:0] is the desired 2-byte data to be programmed.

NOTE 6 RDB invalidation may be required to avoid risk of incoherency between memory array content and RDB content. For more details refer to [4.7.12](#).

**Figure 141 — Authenticated Single Word Program Flowchart**

### C.6.7 Authenticated Single Word Overwrite Command

Authenticated Single Word Overwrite is supported only by some NVM technologies and some LPDDR2-NVM devices.

The Authenticated Single Word Overwrite command is used to write a single word (2-byte data) into an RPMB range.

The overwrite command allows to change the status of each bit from '1' to '0' or from '0' to '1'.

With the overwrite command the data is written to the memory array allowing to change each bit to '0' or to '1'. With the program command only the data bits equal to '0' are written to the memory array, while the data bits equal to '1' are not.

The overwrite operation is performed by the embedded controller.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:

- Write 0x00A2 to the Command Code Register,
- Write desired location address to the Command Address Register,
- Write desired program data to the Command Data Register (Command Data[15:0] only),
- Write the expected write counter value into OW Write Counter Register
- Write the MAC to MAC register
- Write 0x0001 to the Command Execute Register.

Overwriting can be performed in one block at a time.

The Status Register DRB bit, indicates the progress of the Overwrite operation. It should be read to check whether the operation has completed or not.

After completion of the overwrite operation (DRB= 1), one of the Status Register error bits (4, 3 and 1) going High means that an error was detected: either a failure occurred during overwriting, VACC is outside the allowed voltage range or an attempt to overwrite a locked Block was made. See 4.1.1.8 for detailed information.

The overwrite operation can be suspended but it can not be aborted.

The successfulness of the Authenticated Single Word Overwrite command should be checked by reading the Status Register and the Command Result Register (when DRB = '1').

If the Authenticated Single Word Overwrite command is issued during suspend, the operation fails, the Status Register error bits 4 and 5 are set, the Command Result register is set to 0x09 (Command issued during suspend), and MAC Register content is no longer valid.

If the address is outside RPMB range then Command Result Register is set to 0x04 (Address failure), no Status Register error bits are set, and MAC Register content is no longer valid.

The device checks whether the write counter has expired. If the write counter is expired the LPDDR2-NVM device sets the Command Result Register to 0x85 (write failure, write counter expired), and no Status Register error bit is set.

If the write counter is not expired, the LPDDR2-NVM performs MAC calculation as described in Table 127. Note that the OW Write Counter Register and not the internal Write Counter Register shall be used for this calculation.

LPDDR2-NVM device compares the calculated MAC with the MAC value received in the MAC Register.

If the two MAC's are different the Command Result Register is set to 0x02 (authentication failure). The Authenticated Single Word Overwrite command is not executed.

If the MAC in the request and the calculated MAC are equal then the LPDDR2-NVM device compares the write counter in the request, present in the OW Write Counter Register, with the write counter stored in the device. If the two counters are different then the device sets the Command Result Register to 0x03 (counter failure). The embedded operation is not executed.

If the MAC and write counter comparisons are successful the command request is considered to be authenticated, and the overwrite operation is executed.

If the embedded command is successfully completed the write counter is incremented by 1.

**C.6.7 Authenticated Single Word Overwrite Command (cont'd)**

If the overwrite command fails, the Status Register error bit 4 is set and the returned Command Result Register is 0x05 (write failure).

If some other error occurs during the embedded command procedure then returned result is 0x01 (General failure).

After completion of the Authenticated Single Word Overwrite operation (DRB= 1), the device updates the following Overlay Window registers: the Command Result, the Write Counter, the Command Response and the MAC.

During the busy state, the device updates automatically the OW MAC Register as described in [Table 128](#).

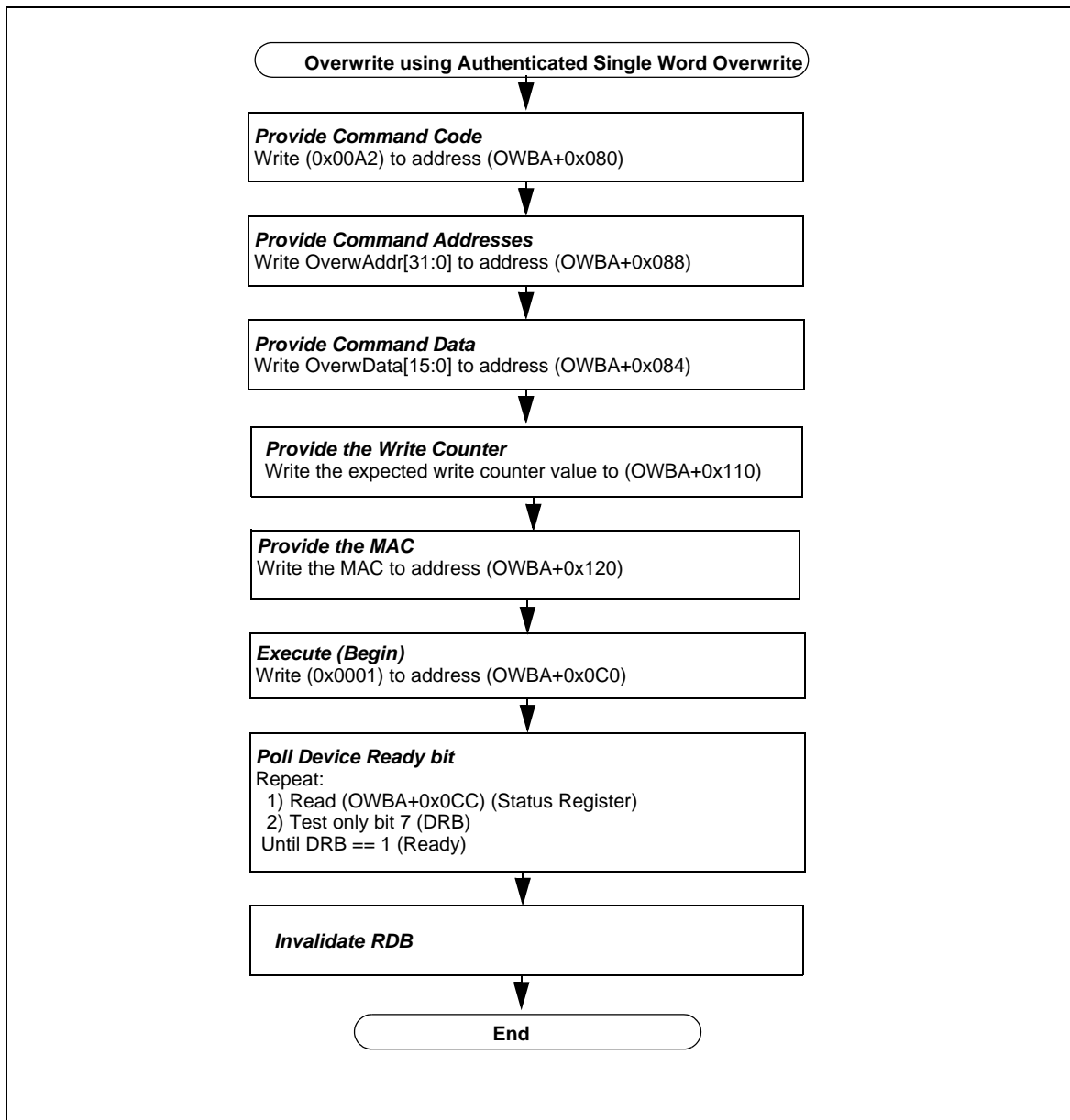
The reset command interrupts an ongoing program operation. As data integrity cannot be guaranteed when the overwrite operation is aborted, the memory array content must be considered invalid.

**Table 139 — Authenticated Single Word Overwrite Error Conditions**

7	6 <sup>(1)</sup>	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Single Word Overwrite operation failure.
1	0	0	1	0	0	1	0	Single Word Overwrite operation abort. An overwrite operation was attempted on a locked block.
1	0	0	1	1	0	0	0	Single Word Overwrite operation abort. Program voltage violation.
1	0	1	1	0	0	0	0	Single Word Overwrite operation abort. Overwrite address outside the LPDDR2-NVM address space
1	0	1	1	0	1	0	0	Single Word Overwrite operation abort. Attempting to program during Overwrite suspend or Program Suspend.

NOTE 1: ESSB Status Register bit is '1' in case of command issued during Erase Suspend.

### C.6.7 Authenticated Single Word Overwrite Command (cont'd)



NOTE 1 The Overlay Window must be open to issue the Authenticated Single Word Overwrite command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 OverwAddr[31:0] is the target byte address of the overwriting operation, and OverwAddr[0] shall be '0'.

NOTE 5 OverwData[15:0] is the desired 2-byte data to be overwritten.

NOTE 6 RDB invalidation may be required to avoid risk of incoherency between memory array content and RDB content. For more details refer to [4.7.12](#).

**Figure 142 — Authenticated Single Word Overwrite Flowchart**

### C.6.8 Authenticated Buffered Program Command

The Authenticated Buffered Program Command makes use of the device's Program Buffer to speed up programming. The Authenticated Buffered Program command dramatically reduces in-system programming time compared to other non-buffered program commands.

If N is the size of the Program Buffer within the Overlay Window, up to N-Bytes can be loaded into the Program Buffer and programmed into the specified N-Byte aligned location in the main array. The region is determined by bit [31: K] of the Command Address Register value, where  $N=2^k$ .

The first word data of the Program Buffer to be programmed depends on bit [K-1:0] of Command Address value.

The programming operation proceeds for a contiguous number of bytes equal to the Data Count value. The Data Count value is in units of bytes and written in the Multi-Purpose Registers.

Note that the host shall fill the entire Program Buffer even if the amount of bytes being programmed is less than the Program Buffer size; "0x00" value shall be written to not relevant Program buffer bytes.

If the Command Address [K-1:0] value plus the Data Count Register value exceeds the program buffer boundary (N-byte), the programming operation ends without programming the memory array and the Status Register will show an error (0xB0).

The programming operation doesn't wrap within the program buffer and doesn't cross into the next programming region.

The Overlay Window must be open and the device must be ready (DRB= 1) before starting the command sequence.

The Command Sequence is:

- Write the starting address to the Command Address register,
- Write the Data Count value (number of bytes to be programmed) to the Multi-Purpose Register,
- Write the expected write counter value into OW Write Counter Register
- Write the MAC to MAC register
- Write data into the Program Buffer. The Program Buffer fits within the N-byte aligned array space,
- Write 0x00A9 to the Command Code Register,
- Write 0x0001 to the Command Execute Register.

The Authenticated Buffered Program command can be suspended but it can not be aborted.

The Status Register DRB bit, indicates the progress of the Authenticated Buffered Program operation. It should be read to check whether the operation has completed or not.

The successfulness of the Authenticated Buffered Program command should be check by reading the Status Register and the Command Result Register (when DRB = '1').

If Authentication Buffered Program command is issued during suspend, the operation fails, the Status Register error bits 4 and 5 are set, and the Command Result register is set to 0x09 (Command issued during suspend), and MAC Register content is no longer valid.

If the address is outside RPMB range then Command Result Register is set to 0x04 (Address failure) and no Status Register error bits are set, and MAC Register content is no longer valid.

If the Block being programmed is locked an error will be set in the Status Register and the operation will abort without affecting the data in the memory array.

Then the device checks whether the write counter has expired. If the write counter is expired the LPDDR2-NVM device sets the Command Result Register to 0x85 (write failure, write counter expired), and no Status Register error bit is set.

If the write counter was not expired, the LPDDR2-NVM starts the MAC calculation as described in [Table 127](#). Note that the OW Write Counter Register and not the internal Write Counter Register shall be used for this calculation.

LPDDR2-NVM device compares the calculated MAC with the MAC value received in the MAC Register.

If the two MAC's are different the Command Result Register is set to 0x02 (authentication failure). The Buffered Program command is not executed.

If the MAC in the request and the calculated MAC are equal then the LPDDR2-NVM device compares the write counter in the request, present in the OW Write Counter Register, with the write counter stored in the device. If the two counters are different then device sets the Command Result Register to 0x03 (counter failure). The embedded operation is not executed.



### C.6.8 Authenticated Buffered Program Command (cont'd)

If the MAC and write counter comparisons are successful the command request is considered to be authenticated, and the program operation is executed.

If the embedded command is successfully completed the write counter is incremented by 1.

If the buffered program command fails, the Status Register error bit 4 is set and the returned Command Result Register is 0x05 (write failure).

If some other error occurs during the embedded command procedure then returned result is 0x01 (General failure).

After completion of the Authenticated Buffered Program operation (DRB= 1), the device updates the following Overlay Window registers: the Command Result, the Write Counter, the Command Response and the MAC.

During the busy state, the device updates automatically the MAC OW Register as described in [Table 128](#).

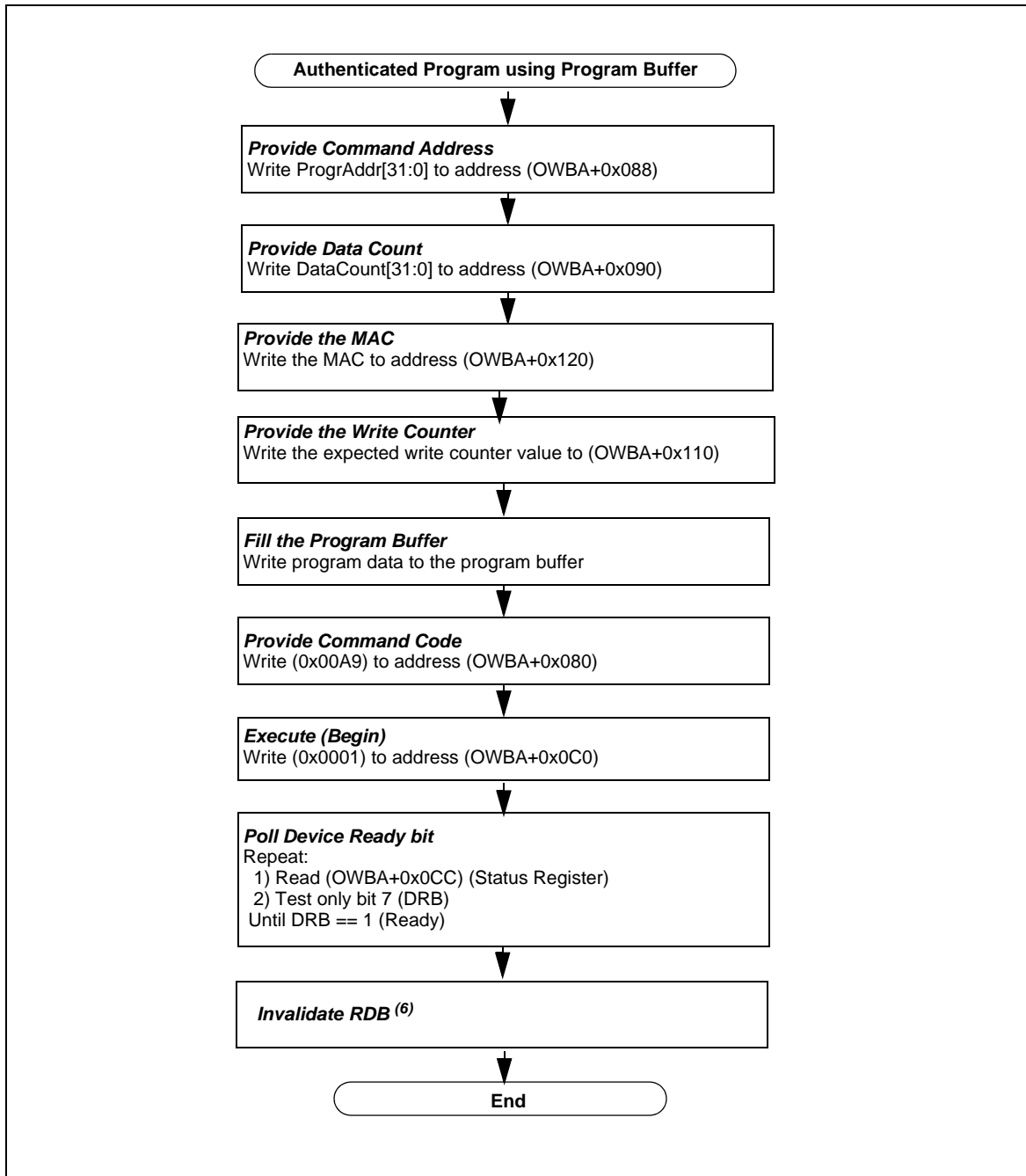
The reset command interrupts an ongoing program operation. As data integrity cannot be guaranteed when the program operation is aborted, the memory array content must be considered invalid.

**Table 140 — Buffered Program Error Conditions**

7	6 <sup>(1)</sup>	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Buffered Program operation failure.
1	0	0	1	0	0	1	0	Buffered Program operation abort. An program operation was attempted on a locked block.
1	0	0	1	1	0	0	0	Buffered Program operation abort. Invalid VACC voltage.
1	0	1	1	0	0	0	0	Buffered Program operation abort. Program address outside the LPDDR2-NVM address space
1	0	1	1	0	1	0	0	Buffered Program operation abort. Attempting to program during Program Suspend.
1	0	1	1	0	0	0	0	Buffered Program operation abort. Command Address [K-1:0] value plus the Data Count Register value exceeds the program buffer boundary (it is greater than N byte).

NOTE 1: ESSB Status Register bit is '1' in case of command issued during Erase Suspend.

[Figure](#) shows the Authenticated Buffered Program Flowchart.

**C.6.8 Authenticated Buffered Program Command (cont'd)**

NOTE 1: The Overlay Window must be open to issue Buffered Program command.

NOTE 2: OWBA is the byte address of the Overlay Window Base Address

NOTE 3: The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4: DataCount[31:0] is amount of byte being programmed

NOTE 5: ProgrAddr[31:0] is the target byte address of the programming operation.

NOTE 6: RDB invalidation may be required to avoid risk of incoherency between memory array content and RDB content. For more details refer to [4.7.12](#).

**Figure 143 — Authenticated Buffered Program Flowchart**

**C.6.9 Authenticated Buffered Overwrite Command**

This is a command supported only by some NVM technologies and LPDDR2-NVM devices.

The Authenticated Buffered Overwrite Command makes use of the device's Program Buffer to speed up overwriting data to the memory array. The Authenticated Buffered Overwrite command reduces in-system overwriting time compared to other non-buffered overwrite commands.

The overwrite command allows to change the status of each bit from '1' to '0' or from '0' to '1'.

With the overwrite command the data is written to the memory array allowing to change each bit to '0' or to '1'. With the program command only the data bits equal to '0' are written to the memory array, while the data bits equal to '1' are not.

If N is the size of the Program Buffer within the Overlay Window, up to N-Bytes can be loaded into the Program Buffer and overwritten into the specified N-Byte aligned location in the main array. The region is determined by bit [31: K] of the Command Address Register value, where  $N=2^k$ .

The first word data of the Program Buffer to be overwritten depends on bit [K-1:0] of Command Address value. The overwriting operation proceeds for a contiguous number of bytes equal to the Data Count value. The Data Count value is in units of bytes and written in the Multi-Purpose Registers.

Note that the host shall fill the entire Program Buffer even if the amount of bytes being programmed is less than the Program Buffer size; "0x00" value shall be written to not relevant Program buffer bytes.

If the Command Address [K-1:0] value plus the Data Count Register value exceeds the program buffer boundary (N-byte), the overwriting operation ends without overwriting the memory array and the Status Register will show an error (0xB0).

The overwriting operation doesn't wrap within the program buffer and doesn't cross into the next programming region.

The Overlay Window must be open and the device must be ready (DRB= 1) before starting the command sequence.

The Command Sequence is:

- Write the starting address to the Command Address Registers,
- Write the Data Count value (number of bytes to be overwritten) to the Multi-Purpose Registers,
- Write the expected write counter value into OW Write Counter Register
- Write the MAC to MAC register
- Write data into the Program Buffer. The Program Buffer fits within the N-byte aligned array space,
- Write 0x00AA to the Command Code Register,
- Write 0x0001 to the Command Execute Register.

If the Block being overwritten is locked an error will be set in the Status Register and the operation will abort without affecting the data in the memory array.

The Authenticated Buffered Overwrite command can be suspended but it can not be aborted.

The Status Register DRB bit, indicates the progress of the Authenticated Overwrite operation. It should be read to check whether the operation has completed or not.

The successfulness of the Authenticated Buffered Overwrite command should be checked by reading the Status Register and the Command Result Register (when DRB = '1').

If the Authenticated Buffered Overwrite command is issued during suspend, the operation fails, the Status Register error bits 4 and 5 are set, the Command Result register is set to 0x09 (Command issued during suspend), and MAC Register content is no longer valid.

If the address is outside RPMB range then Command Result Register is set to 0x04 (Address failure), no Status Register error bits are set, and MAC Register content is no longer valid.

If the Block being programmed is locked an error will be set in the Status Register and the operation will abort without affecting the data in the memory array.

Then the device checks whether the write counter has expired. If the write counter is expired the LPDDR2-NVM device sets the Command Result Register to 0x85 (write failure, write counter expired), and no Status Register error bit is set.

If the write counter is not expired, the LPDDR2-NVM starts MAC calculation as described in [Table 127](#). Note that the OW Write Counter Register and not the internal Write Counter Register shall be used for this calculation.

LPDDR2-NVM device compares the calculated MAC with the MAC value received in the MAC Register.

### **C.6.9 Authenticated Buffered Overwrite Command (cont'd)**

If the two MAC's are different the Command Result Register is set to 0x02 (authentication failure). The Authenticated Buffered Overwrite command is not executed.

If the MAC in the request and the calculated MAC are equal then the LPDDR2-NVM device compares the write counter in the request, present in the OW Write Counter Register, with the write counter stored in the device. If the two counters are different then the device sets the Command Result Register to 0x03 (counter failure). The embedded operation is not executed.

If the MAC and write counter comparisons are successful the command request is considered to be authenticated, and the overwrite operation is executed.

If the embedded command is successfully completed the write counter is incremented by 1.

If the buffered overwrite command fails, the Status Register error bit 4 is set and the returned Command Result Register is 0x05 (write failure).

If some other error occurs during the embedded command procedure then returned result is 0x01 (General failure).

After completion of the Authenticated Buffered Overwrite operation (DRB= 1), the device updates the following Overlay Window registers: the Command Result, the Write Counter, the Command Response and the MAC.

During the busy state, the device updates automatically the OW MAC Register as described in [Table 128](#).

The reset command interrupts an ongoing overwrite operation. As data integrity cannot be guaranteed when the program operation is aborted, the memory array content must be considered invalid.

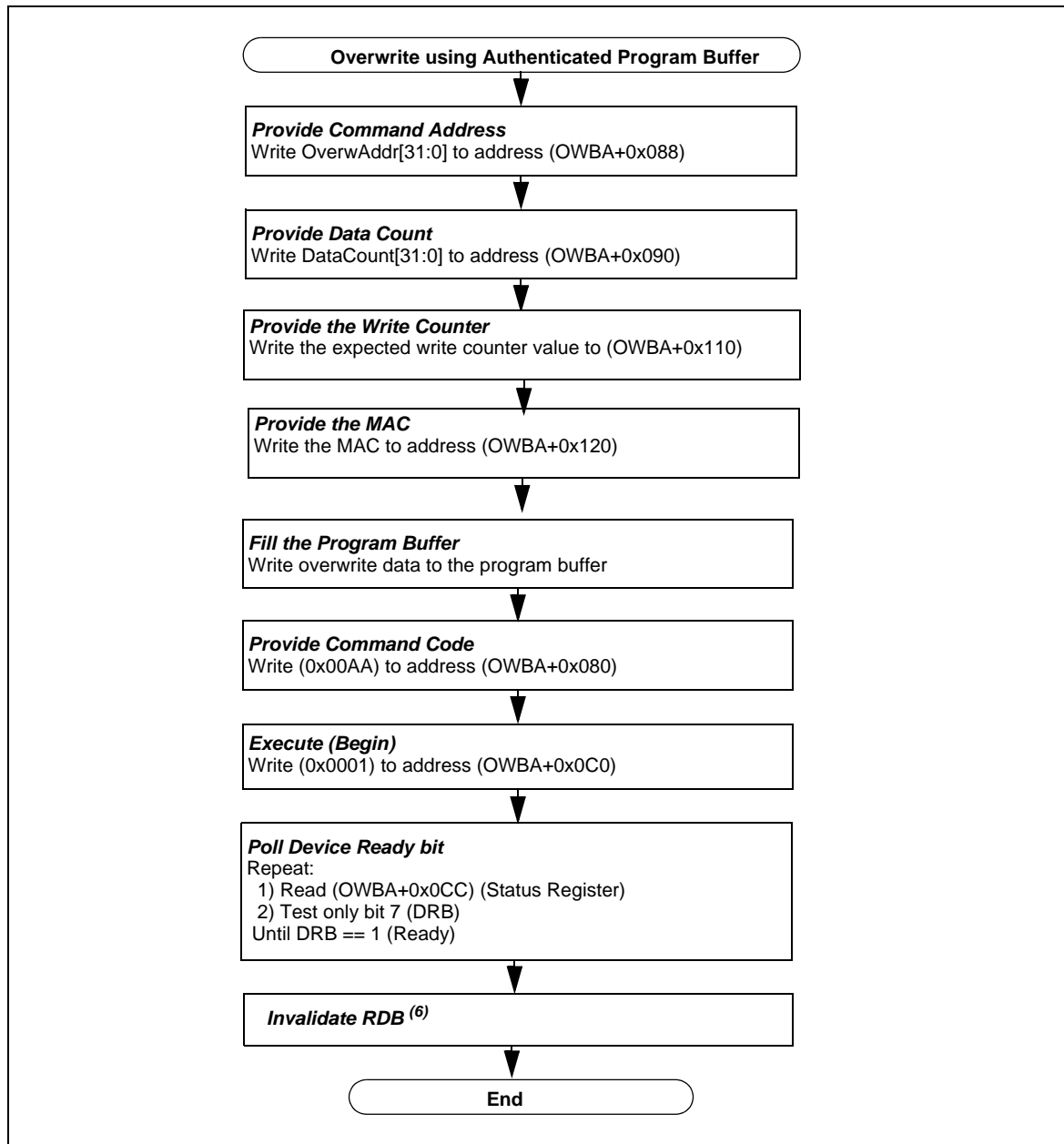
**Table 141 — Authenticated Buffered Overwrite Error Conditions**

7	6 <sup>(1)</sup>	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Buffered Overwrite operation failure.
1	0	0	1	0	0	1	0	Buffered Overwrite operation abort. An overwrite operation was attempted on a locked block.
1	0	0	1	1	0	0	0	Buffered Overwrite operation abort. Invalid VACC voltage.
1	0	1	1	0	0	0	0	Buffered Overwrite operation abort. Overwrite address outside the LPDDR2-NVM address space
1	0	1	1	0	1	0	0	Buffered Overwrite operation abort. Attempting to overwrite during Overwrite Suspend or Program Suspend.
1	0	1	1	0	0	0	0	Buffered Overwrite operation abort. Command Address [K-1:0] value plus the Data Count Register value exceeds the program buffer boundary (it is greater than N byte).

NOTE 1: ESSB Status Register bit is '1' in case of command issued during Erase Suspend.

### C.6.9 Authenticated Buffered Overwrite Command (cont'd)

Figure 144 shows the Authenticated Buffered Overwrite Flowchart.



NOTE 1 The Overlay Window must be open to issue Authenticated Buffered Overwrite command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 DataCount[31:0] is amount of byte being overwritten

NOTE 5 OverwAddr[31:0] is the target byte address of the overwriting operation.

NOTE 6 RDB invalidation may be required to avoid risk of incoherency between memory array content and RDB content. For more details refer to 4.7.12.

**Figure 144 — Authenticated Buffered Overwrite Flowchart**

## C.7 Dual operations with Authenticated Command

*Please note: this section is meant to replace section 4.8 in the LPDDR2 JEDEC standard.*

In some LPDDR2-NVM devices, the memory array may be divided into two or more partitions (multiple partition architecture). Refer to vendor datasheets to determine support for multiple partition architecture.

LPDDR2-NVM devices that support multiple partition architecture provide greater flexibility for software developers to split the code and data spaces within the memory array. The dual operations feature simplifies the software management of the device by allowing code to be executed from one partition while another partition is being programmed or erased.

The dual operations feature means that while programming or erasing in one partition, read operations are possible in another partition with zero latency (only one partition at a time is allowed to be in program or erase mode).

If a read operation is required in a partition, which is programming or erasing, the program or erase operation can be suspended.

Also, if the suspended operation is erase then a program command can be issued to another block, so the device can have one block in erase suspend mode, one programming, and other partitions available for read operations.

For the complete list of dual operations allowed, refer to the device datasheet.

**Table 142 — Simultaneous operations allowed in the same partition**

Device Status	Operations allowed in the same partition			
	Read <sup>(1)</sup>	Non-Authenticated Program <sup>(2)</sup>	Non-Authenticated Block Erase	Authenticated Operations <sup>(3)</sup>
Idle	Yes	Yes	Yes	Yes
Programming <sup>(4,5)</sup>	No	No	No	No
Erasing <sup>(6)</sup>	No	No	No	No
Program suspended	Yes <sup>(7)</sup>	No	No	No
Erase suspended	Yes <sup>(8)</sup>	Yes <sup>(9)</sup>	No	No
Authenticated operation suspended <sup>(3)</sup>	Yes <sup>(7)</sup>	No	No	No
Memory Data Digest	No	No	No	No

NOTE 1: Depending on the Overlay Window status and the target read address, data may come from the memory array or from the overlay window.

NOTE 2: Non-Authenticated Program operations include: Single Word Program, Single Word Overwrite, Buffered Program, Buffered Overwrite.

NOTE 3: Authenticated Operations include: Authenticated Single Word Program, Authenticated Single Word Overwrite, Authenticated Buffered Program, Authenticated Buffered Overwrite, Authenticated Block Erase, Memory Data Digest, Write Security Register, Read Security Register, Write Counter Digest.

NOTE 4: Programming is defined by the execution of one of the following operations: Single Word Program, Single Word Overwrite, Buffered Program, Buffered Overwrite, Authenticated Single Word Program, Authenticated Single Word Overwrite, Authenticated Buffered Program, Authenticated Buffered Overwrite.

NOTE 5: Programming may occur during erase suspended.

NOTE6: Erasing states is defined by the execution of one of the following operations: Block Erase, Authenticated Block Erase.

NOTE 7: LPDDR2-NVM will output invalid data if the read operation occurs in the memory area that is being programmed.

NOTE 8: LPDDR2-NVM will output invalid data if the read operation occurs in the block that is being erased.

NOTE 9: Not allowed in the block that is being erased.

## C.7 Dual operations with Authenticated Command (cont'd)

**Table 143 — Simultaneous operations allowed in other partitions**

Device Status	Operations allowed in another partition			
	Read <sup>(1)</sup>	Non-Authenticated Program	Non-Authenticated Block Erase	Authenticated Operations
Idle	Yes	Yes	Yes	Yes
Programming <sup>(2)</sup>	Yes	No	No	No
Erasing	Yes	No	No	No
Program suspended	Yes	No	No	No
Erase suspended	Yes	Yes	No	No
Authenticated operation suspended <sup>(3)</sup>	Yes	No	No	No
Memory Data Digest	Vendor Specific	No	No	No

NOTE 1: Depending on the Overlay Window status and the target read address, data may come from the memory array or from the overlay window.

NOTE 2: Programming may occur during erase suspended.

NOTE 3: The following authenticated operations can be suspended: Authenticated Single Word Program, Authenticated Single Word Overwrite, Authenticated Buffered Program, Authenticated Buffered Overwrite, Authenticated Block Erase, Memory Data Digest.

## Annex D (informative) Differences between Document Revisions

### D.1 Initial Release JESD209-2

LPDDR2 Standard Released as JESD209-2.

### D.2 Updated Standard to JESD209-2A

LPDDR2 Standard Updated as JESD209-2A.

**Table 144 — Changes from JESD209-2 to JESD209-2A**

Changes	Sections Effected	Description of Changes
Added RZQI to Mode Register 0	"Power Ramp and Device Initialization" on page 29 "Mode Register Assignment in LPDDR2 SDRAM/NVM(Common part)" on page 33 MR0, page 35 MR10, page 41	Added Optional RZQI information to Mode Register 0 to determine the connection of ZQ-pin
Clarified Row Data Buffer Write policy	"Overlay Window" on page 48	Row Data Buffers are considered to be Write through structures. All writes to the Overlay Window is completed when the issuing Write Command is completed.
Clarified BST during tRP for LPDDR2-NVM	"LPDDR2-N: Burst Read operation followed by Activate or Preactive" on page 107	Clarification that a BST command is allowed during the tRP period for LPDDR2-NVM.
Clarified device temperature monitoring during power down	"Temperature Sensor" on page 130	The LPDDR2 device shall monitor the device temperature and update MR4 during idle and active power down, and in self-refresh states according to tTSI.
Clarified tMRW in timing diagrams	"LPDDR2-N: Burst Write Followed by MRW: WL = 1, BL = 4" on page 134 "LPDDR2-N: Burst Read followed by MRW: RL = 3, BL = 4" on page 134	Replaced T8 in both timing diagrams with Tx to clarify that tMRW lasts for greater than 3 cycles.
Replaced precharge power down with idle power down in text	"Power-down" on page 139	The precharge power down state in LPDDR2 was renamed to idle power down. This change is semantic.
Removed CKE from notes below Input Signal Figure	"LPDDR2-200 to LPDDR2-400 Input Signal" on page 166 "LPDDR2-466 to LPDDR2-1066 Input Signal" on page 165	CKE is a LVCMOS input signal and does not belong in this input signal diagram.
Changed switching definition for IDD4R and IDD4W	"Definition of Switching for IDD4R" on page 186 "Definition of Switching for IDD4W" on page 186	Changed the definition of the CA3-CA9 inputs during the N+1 and N+2 cycles in order to maintain accesses to the same banks/RBs during the Read/Write burst measurement
Added IDD3NS and IDD2NS to IDD specifications parameters	"LPDDR2 IDD Specification Parameters and Operating Conditions" on page 187	Added IDD2NS and IDD3NS to the IDD specification table in order to have IDD measurement conditions for the non-power down clock stop mode.
Fixed error in LPDDR2-N program/erase currents	"LPDDR2 IDD Specification Parameters and Operating Conditions" on page 187	Removed CKE is HIGH from the LPDDR2-N program/erase currents. CKE is LOW is the current condition.
tJIT(duty) definition updated	"Definition for duty cycle jitter tJIT(duty)" on page 192 "LPDDR2 AC Timing Table*9" on page 197	Updated Clock Duty Cycle Jitter definition and added table entry.
Removed tCK, tCH, tCL, and tHP table entries	"LPDDR2 AC Timing Table*9" on page 197	tCK, tCL, tCH, and tHP definitions are redundant to the tCK(avg), tCL(avg), and tCH(avg) definitions.



**Table 144 — Changes from JESD209-2 to JESD209-2A**

Changes	Sections Effected	Description of Changes
Clarify Deep Power-Down Entry	<a href="#">“LPDDR2-SX: Deep Power-Down” on page 146</a>	Entry into Deep Power-Down is only from the idle state.
Added Package diagrams	<a href="#">“Package ballout &amp; addressing” on page 2</a>	Added PoP, MCP, and Discrete packages for LPDDR2
Changed tTSI timing variable	<a href="#">“Temperature Sensor” on page 130</a>	Changed tTSI from 16ms to 32ms.
Changed Overlay Window Location 0x03E - 0x03F	<a href="#">Overlay Window: Control Register Offsets and Definitions on page 49</a>	Changed these locations from Reserved to Write-Only Reserved
Fixed typo in Self-Refresh diagram notes	<a href="#">“LPDDR2-SX: Definition of tSRF” on page 120</a>	Fixed typo for the refresh window symbol. Changed tREF to tREFW.
Fixed Typo in Bank-Masking section for LPDDR2-S4	<a href="#">“LPDDR2-S4: Partial Array Self-Refresh: Bank Masking” on page 127</a>	Fixed typo in the wording on the Bank Masking section for PASR for LPDDR2-S4.
Added clarification for Overlay Window in LPDDR2-NVM Flow Charts	<a href="#">“Overlay Window Enable and Disable” on page 59</a>	Added the following sentence to notes for the flowcharts for LPDDR2-NVM: “Enabling the Overlay Window is not mandatory if the Overlay Window is already open. “
Added clarification for MRR to MRW and MRR to Write timing	<a href="#">Figure 79 on page 128</a>	MRR to MRW and MRR to Write timing clarified.

**D.3 Updated Standard to JESD209-2B**

LPDDR2 Standard Updated as JESD209-2B.

**Table 145 — Changes from JESD209-2A to JESD209-2B**

Changes	Sections Effected	Description of Changes
Fixed power down diagrams to show appropriate timing from CKE going LOW to CK “don’t care” and exiting PD	<a href="#">“LPDDR2-SX: Self-Refresh Operation” on page 126</a> <a href="#">“LPDDR2-SX: Basic power down entry and exit timing diagram” on page 139</a> <a href="#">“LPDDR2-N: Basic power down entry and exit timing diagram” on page 140</a> <a href="#">“LPDDR2-SX: Deep power down entry and exit timing diagram” on page 146</a>	Clock may be stopped only when CK <sub>t</sub> is LOW. Figure previously implied that clock may be stopped when CK <sub>t</sub> was HIGH. Two valid clocks must be issued prior to exiting Power Down states.
Timing diagram had incorrect axis labels	<a href="#">“Differential Output Slew Rate Definition” on page 174</a>	Fixed axis labels. VOH(AC) -> VOHdiff(AC), VREF -> 0, VOL(AC) -> VOLdiff(AC)
Fixed typo in notes	<a href="#">“162-ball x16/x32 LPDDR2 and SDR-Flash package ballout” on page 9</a>	Incorrect row numbers in note 1 for package ballout. Fixed to indicate 20 rows instead of 17.
Clarified pad sequence	<a href="#">“LPDDR2 Pad Sequence” on page 12</a>	Added note to clarify pad sequence. CA and DQ pads are on opposite sides of the die.
Clarified Read to Precharge with truncated burst	<a href="#">“LPDDR2-SX: Burst Read operation followed by Precharge” on page 111</a>	Added text clarifying that the effective BL shall be used when calculating Read to Precharge.
Added Section on Row Data Buffer Incoherency	<a href="#">“Row Data Buffer Incoherency” on page 80</a>	Added text to explain a situation with Row Data Buffer Incoherency when the device is programmed
Removed “Enable Overlay Window” and “Disable Overlay Window” from NVM flowcharts	<a href="#">“Block Lock Command Flowchart” on page 61,</a> <a href="#">“Block Unlock Flowchart” on page 63,</a> <a href="#">“Block Lock-Down Command Flowchart” on page 65,</a> <a href="#">“Block Erase Flowchart” on page 67,</a> <a href="#">“Single Word Program Flowchart” on page 69,</a> <a href="#">“Single Word Overwrite Flowchart” on page 71,</a> <a href="#">“Buffered Program Flowchart” on page 73,</a> <a href="#">“Buffered Overwrite Flowchart” on page 75,</a> <a href="#">“Program/Erase Resume Command Flowchart” on page 78</a>	Removed “Enable Overlay Window” and “Disable Overlay Window” and related note from NVM flow charts. This was done to simplify the flow charts and to avoid confusion about when to open and close the overlay window.
Clarified MRR and MRW in NVM Truth Table	<a href="#">“Current State Row Buffer n - Command to Row Buffer m” on page 158</a>	MRR is allowed for Preactivating state, while MRW is not. Also corrected note numbers in table.
Clarified that BL in Read to Activate for NVM.	<a href="#">“LPDDR2-N: Burst Read operation followed by Activate or Preactive” on page 107</a>	BL is the effective BL for Read to Activate calculation for NVM.
Clarified “effective BL” in timing diagrams for Read to Activate and Write to Activate for NVM	<a href="#">“LPDDR2-N: Burst write followed by Activate: WL = 1, BL = 4” on page 96,</a> <a href="#">“LPDDR2-N: Burst read operation followed by Activate: RL = 3, BL = 4” on page 107,</a> <a href="#">“LPDDR2-N: Burst write followed by Activate: WL = 1, BL = 4” on page 109</a>	Added notes to timing diagrams clarifying that the BL used in the calculations should be the effective BL when a read or write burst is truncated.
Fixed error in formula for NVM Write to Activate	<a href="#">“LPDDR2-N: Activate Command” on page 83</a>	Corrected formula for Write to Activate timing. The previous equation was missing a “+1”.

**Table 145 — Changes from JESD209-2A to JESD209-2B**

Changes	Sections Effected	Description of Changes
Values for tJIT(cc) were swapped for 400 and 1066 values	<a href="#">“LPDDR2 AC Timing Table*9” on page 197</a>	Values for tJIT(cc) for 400 and 1066 were incorrect and now are corrected.
Added notes for NVM flow charts	<a href="#">“Program/Erase Suspend Request Flowchart” on page 77</a> , <a href="#">“Abort Request Flowchart” on page 79</a>	Added notes for two NVM flowcharts that were missing the OW notes.
Fixed typos in Package Ballouts	<a href="#">“LPDDR2 12x12 PoP 1-channel x32 package ballout using MO-273” on page 5</a> , <a href="#">“79-ball x16 LPDDR2 0.5mm pitch package ballout (Discrete/MCP)” on page 7</a>	Changed INT#, WP# to INT, WP# in 12x12 PoP 1-channel ballout and fixed DQ15 typo in 79-ball x16 MCP.

## D.4 Updated Standard to JESD209-2C

LPDDR2 Standard Updated as JESD209-2C.

**Table 146 — Changes from JESD209-2B to JESD209-2C**

Changes	Sections Effected	Description of Changes
Added min tCK values for tZQCS and tZQCL. Changed max to min for tZQ values.	<a href="#">“LPDDR2 AC Timing Table*9” on page 197</a>	Specified minimum tCK values for tZQCS and tZQCL to 6 tCK. Editorial change of tZQ values from maximum to minimum.
tPOFF value changed.	<a href="#">“Timing Parameters Power-Off” on page 32</a> <a href="#">“Power-off Sequence” on page 32</a> <a href="#">“Uncontrolled Power-Off Sequence” on page 32</a>	Changed tPOFF value from maximum 20ms to maximum 2s.
Added clarifying notes for MR0, RZQI.	<a href="#">“Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM” on page 33</a>	RZQI codes clarified in MR0.
Updated VOHDIFF(AC) and VOLDIFF(AC) to match single ended values	<a href="#">“Differential AC and DC Output Levels” on page 172</a>	VOHDIFF(AC) updated from $+.25*VDDQ$ to $+.2*VDDQ$ to align with VOH(AC) VOLDIFF(AC) updated from $+.25*VDDQ$ to $-.2*VDDQ$ to align with VOL(AC)
Updated Notes for Status Register.	<a href="#">“Status Register details” on page 53</a>	Removed conflicting note for the use of the Abort command.
Updated Note 12 in AC Timing Table	<a href="#">“LPDDR2 AC Timing Table*9” on page 197</a>	Clarified that both analog (ns) and min tCK values shall be used when the min tCK column applies.
Corrected typos in 162-ball and 180-ball MCP ballmaps	<a href="#">“162-ball x16/x32 LPDDR2 and SDR-Flash package ballout” on page 9</a> <a href="#">“180-ball x16/x32 LPDDR2, SDR-Flash, and e-MMC package ballout” on page 10</a>	The 162-ball MCP ball B3 changed to DQS instead of DQ5 and ball B4 changed to DAT7 instead of DAT2. The 180-ball MCP ball B3 changed to DQS instead of DQ5.
Added section for RPMB for LPDDR2-NVM devices	<a href="#">“LPDDR2-N: Replay Protected Memory Block (RPMB)” on page 230</a>	Replay Protected Memory Block is an optional feature for LPDDR2-NVM devices.
CS_N and CKE clarification in Command Truth Table	<a href="#">“Command Truth Table” on page 149</a>	CS_N is registered on the rising edge of clock and is don't care for the falling edge of clock. CKE timing clarified. When CKE changes, from HIGH to LOW or LOW to HIGH, it is don't care on the falling edge of clock.
Added CKE timing clarification.	<a href="#">“LPDDR2 CKE Input Setup and Hold Timing” on page 85</a>	CKE input timing diagram clarifies CKE input timing usage.

**Table 146 — Changes from JESD209-2B to JESD209-2C**

Changes	Sections Effected	Description of Changes
Suspend register clarification	<a href="#">“Suspend Register” on page 51</a>	Replaced “allowed” with “effective”. Writes to this register are only effective when embedded operation is in progress.
Abort register clarification	<a href="#">“Abort Register” on page 52</a>	Replaced “allowed” with “effective”. Writes to this register are only effective when embedded operation is in progress. Also, noted that the embedded operation may have completed successfully before the abort could have taken effect.
IDD specification note clarification	<a href="#">“LPDDR2 IDD Specification Parameters and Operating Conditions” on page 187</a>	Added clarification for Note 8 that out-load load is 5pF.

**D.5 Updated Standard to JESD209-2D**

LPDDR2 Standard Updated as JESD209-2D.

**Table 147 — Changes from JESD209-2C to JESD209-2D**

Changes	Sections Effected	Description of Changes
Fixed notation for active low signals	"LPDDR2 12x12 PoP 1-channel x32 package ballout using MO-273" on page 5	Changed "#" with "_n"
Added 121-Ball MCP Ballout	"121-ball x16 LPDDR2, SDR Flash-NVM, and e-MMC package ballout" on page 11	Added 121-ball LPDDR2 x16 / Flash Ballout
Removed RTT waveform	"Power Ramp and Device Initialization" on page 29 "Power Ramp and Initialization" on page 226	Removed RTT waveform from Figure 6 on page 31
Clarified MR4 OP<2:0> bits value after power-up	"Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM" on page 33	Added the text in red ink to NOTE 2 "... OP<2:0> bits are undefined after power-up" see MR4 on page 39
Fixed ESSB and PSSB value in error condition table	"Block Erase Command" on page 66	Fixed ESSB and PSSB Status Register bits value in case of Erase command issued during suspend.
Fixed PSSB value in error condition tables	"Single Word Program Command" on page 68 "Single Word Overwrite Command" on page 70 "Buffered Program Command" on page 72 "Buffered Overwrite Command" on page 74	Fixed PSSB Status Register bit value in case of command issued during program suspend. Added a note about ESSB value.
Added RDB invalidation step in LPDDR2-NVM flowcharts	"Block Erase Command" on page 66 "Single Word Program Command" on page 68 "Single Word Overwrite Command" on page 70 "Buffered Program Command" on page 72 "Buffered Overwrite Command" on page 74	Added a new step in the flowcharts and a note.
Clarified clock requirement for self refresh exit	"LPDDR2-SX: Self Refresh operation" on page 125	Improved the text as follows. "First, the clock shall be stable and within specified limits for a minimum of 2 tCK <del>clock cycles</del> prior to the positive clock edge that registers CKE <del>going back HIGH</del> ."
Fixed tCK(MIN) and tCK(MAX)	"Input clock stop and frequency change" on page 147	Substituted tCK(MIN) with tCK(abs)min Removed tCK(MAX)
Fixed VILdiff(dc) and VILdiff(ac) max values	"Differential signal definition" on page 167	Changed the sign to VILdiff(dc) and VILdiff(ac) max values, and completed note 1.
Fixed tCKmin	"IDD Specifications" on page 187	Substituted all "tCKmin" with "tCK(avg)min" in the LPDDR2 IDD Specification Parameters and Operating Conditions Table on page 187
Clarified temperature range for IDD values	"IDD Specifications" on page 187	Clarified temperature range for IDD values. Delete reference to note 4 from IDD6ET.
Removed some OW registers for RPMB	"Overlay Window: Control Register Offsets and Definitions" on page 230	Removed the following OW registers: Authentication Configuration Reg, RPMB ID Regs, RPMB Start Address Regs, RPMB Start Address Regs. Updated note 1.
Removed some Command Result values	"Command Result" on page 232	Removed the following values because they never occur: 0x82, 0x83, 0x8A, 0x8B. Added note 1, note 2 and note 6. Modified note 4. Made some minor editorial changes.

**Table 147 — Changes from JESD209-2C to JESD209-2D**

Changes	Sections Effected	Description of Changes
Added description for some OW Regs.	"Nonce Register" on page 233, "MAC Register" on page 234	Added description for Nonce Register and MAC Register
Clarified Write Counter Reg. description	"OW Write Counter Register" on page 233	Clarified the purpose of Write Counter Register and its value after power up or reset. Made few editorial changes.
Clarified Authentication Key Configuration Register description	"Authentication Key Configuration Register" on page 235	Clarified the register value when the device is delivered. Made few editorial changes.
Clarified RPMB ID, RPMB Start Address, RPMB End Address	"RPMB ID, RPMB Start Address, RPMB End Address" on page 236	Made some editorial changes to improve the description.
Added RPMB Configuration Register	"RPMB Configuration Register" on page 236	Added RPMB Configuration Register which includes enable bit and lock-down bit.
Clarified MAC calculation bytes order	"Message Authentication Code Calculation" on page 237	The MAC calculation bytes order table has been split in two tables. Changed note 6. Removed column for Command Result Digest.
Added Read Security Registers command	"LPDDR2 RPMB Commands" on page 239	Added command code.
Removed Command Result Digest Command	"LPDDR2-NVM RPMB commands" on page 239 "Dual operations with Authenticated Command" on page 264	Command Result Digest command has been removed.
Changed Security Register program method	"Write Security Register Command" on page 240	Defined a new method for programming Security Registers.
Added several new Authenticated commands	"LPDDR2-NVM RPMB commands" on page 239 "Read Security Register Command" on page 243, "Authenticated Block Erase Command" on page 249, "Authenticated Single Word Program Command" on page 251, "Authenticated Single Word Overwrite Command" on page 255, "Authenticated Buffered Overwrite Command" on page 260	The following commands have been added: Read Security Register, Authenticated Block Erase, Authenticated Single Word Program, Authenticated Single Word Overwrite, Authenticated Buffered Overwrite.
Changed Status Register error conditions	"Write Counter Digest Command" on page 245	Added error conditions table. Added RDB invalidation step in flowchart. Made some editorial changes.
Changed Status Register error conditions	"Memory Data Digest Command" on page 247	Added error conditions table. Added RDB invalidation step in flowchart. Made some editorial changes.
Fixed PSSB value in error condition table	"Authenticated Buffered Program Command" on page 258	Fixed PSSB Status Register bit value in case of command issued during program suspend. Added a note about ESSB value. Added address failure error condition for Command Result Register. Added RDB invalidation step in flowchart.

**D.6 Updated Standard to JESD209-2E**

LPDDR2 Standard Updated as JESD209-2E.

**Table 148 — Changes from JESD209-2D to JESD209-2E**

Changes	Sections Effected	Description of Changes
Added VACC = VAP acceleration power supply value	<a href="#">“Absolute Maximum DC Ratings” on page 160</a> <a href="#">“Recommended DC Operating Conditions” on page 161</a>	Added VACC absolute maximum value = 7V in <a href="#">Table 68 on page 160</a> , and note 6.  Added VACC = VAP in <a href="#">Table 71 on page 161</a> , and note 3.
Fixed tERR(8per) value for DDR667	<a href="#">“AC Timings” on page 197</a>	tERR(8per) value for DDR667 has been changed from 256 ps to 266 ps.
Clarified Command Result Reg. definition	<a href="#">“Command Result Register” on page 231</a>	Clarified that bit 7 of Command Result Register provides information about the internal Write Counter
Removed the text about the internal Write Counter	<a href="#">“OW Write Counter Register” on page 233</a>	The description of the internal Write Counter has been moved to a dedicated paragraph. Changed the paragraph heading to “OW Write Counter”
Added the “Write Counter” paragraph	<a href="#">“Write Counter, Authentication Key and RPMB Resource” on page 235</a> <a href="#">“Write Counter” on page 235</a>	Most of the text was previously included Write Counter paragraph in the section “Map of Control Registers”.
Clarified write counter update	<a href="#">“Write Counter Digest Command” on page 245</a>	Clarified that the sentence about Write Counter Update refers to the OW Write Counter and not the internal Write Counter
Fixed command code value for Memory Data Digest command	<a href="#">“Memory Data Digest Command” on page 247</a>	Fixed a typo in the description of the command sequence: according to <a href="#">Table 129 on page 239</a> , the command code value is 0x00A6 and not 0x00A8.
Clarified which Write Counter shall be used during MAC calculation	<a href="#">“Authenticated Block Erase Command” on page 249</a> <a href="#">“Authenticated Single Word Program Command” on page 251</a> <a href="#">“Authenticated Single Word Overwrite Command” on page 255</a> <a href="#">“Authenticated Buffered Program Command” on page 258</a> <a href="#">“Authenticated Buffered Overwrite Command” on page 260</a>	Added a sentence to clarify that the OW Write Counter shall be used in the MAC calculation for command authentication.
Clarified Write Counter values used during comparison	<a href="#">“Authenticated Block Erase Command” on page 249</a> <a href="#">“Authenticated Single Word Program Command” on page 251</a> <a href="#">“Authenticated Single Word Overwrite Command” on page 255</a> <a href="#">“Authenticated Buffered Program Command” on page 258</a> <a href="#">“Authenticated Buffered Overwrite Command” on page 260</a>	Clarified that during the write counter comparison, the device shall compare OW Write Counter Register content with the internal Write Counter value.
Clarified Security Register Mapping	<a href="#">“Write Security Register Command” on page 240</a> <a href="#">“Read Security Register Command” on page 243</a>	Added <a href="#">“Security Register Mapping for Write Security Reg. Command” on page 240</a> and <a href="#">“Security Register Mapping for Read Security Reg. Command” on page 243</a>



## D.7 Updated Standard to JESD209-2F

LPDDR2 Standard Updated as JESD209-2F.

**Table 149 — Changes from JESD209-2E to JESD209-2F**

Changes	Sections Effected	Description of Changes
Added 14x14 2 channel PoP ballot	<a href="#">“LPDDR2 14x14 PoP 2-channel 2x32 package ballout” on page 3</a>	Added 14x14 PoP 2-channel ballout
Added 6Gb Density for LPDDR2-S2 and LPDDR2-S4 devices	<a href="#">“LPDDR2 SDRAM Addressing” on page 15</a> <a href="#">“LPDDR2-SX Refresh Requirements by Device Density” on page 196</a> <a href="#">“Functional description” on page 21</a>	Added 6Gb density for LPDDR2-S2 and LPDDR2-S4 devices
Clarified Overshoot and Undershoot voltage levels	<a href="#">“AC Overshoot/Undershoot Specification” on page 175</a> <a href="#">“Overshoot and Undershoot Definition” on page 175</a>	Clarified maximum and minimum VSS and VDD values for the Undershoot and Overshoot specification.





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## Standard Improvement Form

## JEDEC

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The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

☐ Requirement, clause number \_\_\_\_\_

☐ Test method number \_\_\_\_\_ Clause number \_\_\_\_\_

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other \_\_\_\_\_

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2. Recommendations for correction:

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3. Other suggestions for document improvement:

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Submitted by

Name: \_\_\_\_\_

Phone: \_\_\_\_\_

Company: \_\_\_\_\_

E-mail: \_\_\_\_\_

Address: \_\_\_\_\_

City/State/Zip: \_\_\_\_\_

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