Furkan SALIK - 150200056

1.a) For the first 2Kx8 chip, since , 11 bits are required for addressing inside the chip. So, from the address to reside within this chip. The same thing also applies for the second 2Kx8 chip, but this time most significant 5 bits are . So, address range of the second chip is from to . The same procedure applies until the last 2Kx8’s address range is from to **.** For the 4Kx8 chip which is the seventh one, it can be thought as the composition of two 2Kx8 chips. For this reason, first part of the address range would be from to , and the second part would be from to . So in total, the seventh chip’s address range would be from to . And for the last chip, similarly it can be thought as the composition of eight 2Kx8 chips. Following a similar approach as in assigning the address range of the seventh chip, the address range of the eighth chip would be from to .

To summarize, address ranges of the chips are:

1. 2Kx8: **$0000-$07FF**
2. 2Kx8: **$0800-$0FFF**
3. 2Kx8: **$1000-$17FF**
4. 2Kx8: **$1800-$1FFF**
5. 2Kx8: **$2000-$27FF**
6. 2Kx8: **$2800-$2FFF**
7. 4Kx8: **$3000-$3FFF**
8. 16Kx8: **$4000-$7FFF**

|  |  |
| --- | --- |
| 2Kx8 | $0000 |
| $07FF |
| 2Kx8 | $0800 |
| $0FFF |
| 2Kx8 | $1000 |
| $17FF |
| 2Kx8 | $1800 |
| $1FFF |
| 2Kx8 | $2000 |
| $27FF |
| 2Kx8 | $2800 |
| $2FFF |
| 4Kx8 | $3000 |
| $3FFF |
| 16Kx8 | $4000 |
| $7FFF |

1.b) Decoder has inputs , which are bits of the address bus, and outputs from to . Decoder’s enable input must be to disallow addresses more than $7FFF.

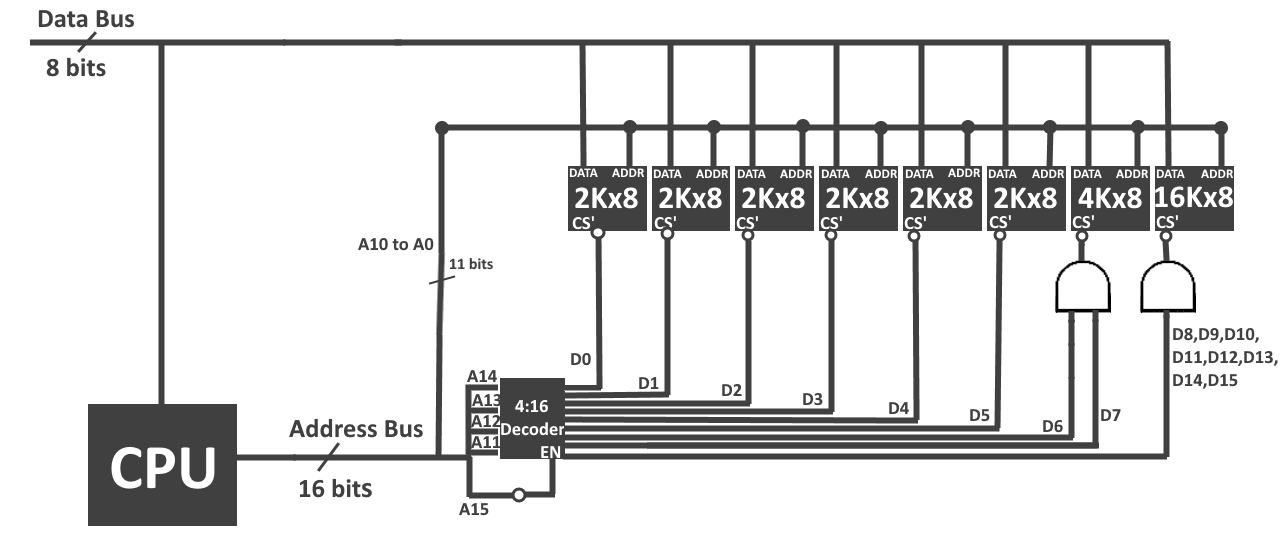
Considering the address ranges;

For the selection of the first 2Kx8 chip, bits from to are , so

Similarly, in the second chip, bits to are , therefore

Following the same procedure,

For the 4Kx8 chip, two different to bits exist. These are and . So,

For the 16Kx8 chip, eight different to bits exist. These are , ,,, , , , . So,

Note that in the diagram, **4:16 Decoder**’s outputs are active low, meaning that only the selected output is 0, and other outputs are 1.

2.a) If two 4Kx4 chips are used in parallel, it can be regarded as a 4Kx8 chip. Both of the chips’ address selection would be same. Only difference would be that most significant 4 bits of the data bus would be wired to one, and least significant 4 bits would be wired to another.

Address Ranges:

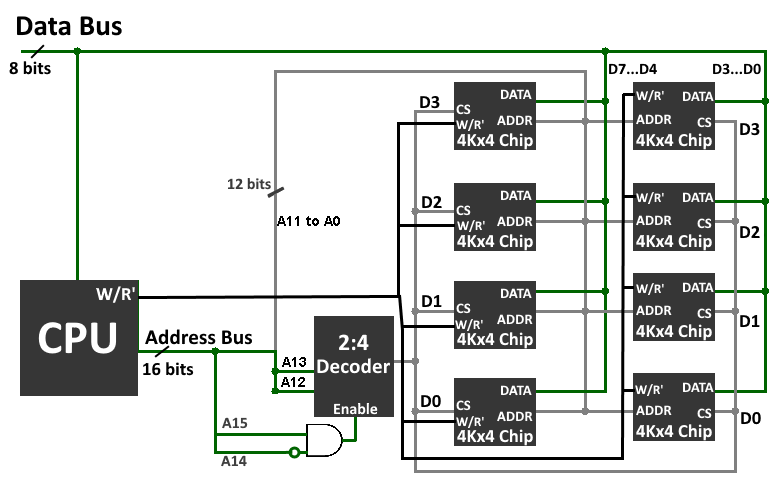
4Kx4: **$8000-$8FFF**

4Kx4: **$9000-$9FFF**

4Kx4: **$A000-$AFFF**

4Kx4: **$B000-$BFFF**

(Note that the parallel pairs have the same address, and it is exactly same for the parallel part.)

2.b)

**2:4 Decoder** is used to supply the chip select inputs of the chips. It takes and bits of the address bus. It determines which chip will be selected using these 2 bits. Also, it is enabled only if is 1, meaning that if the given address is in the range **$8000-$BFFF**.

12 bits of the address bus are used to specify which address will be used inside the chips. Address bus bits from to are used for this.

Also, an important thing to note is that, most significant 4 bits of the data bus are assigned to the chips on the left, and least significant 4 bits are assigned to the chips on the right.