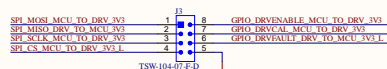


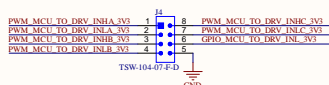
Input & Output



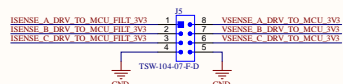
SPI & DRV IO



PWM



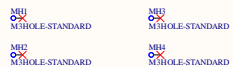
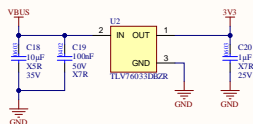
Current & Voltage Sense



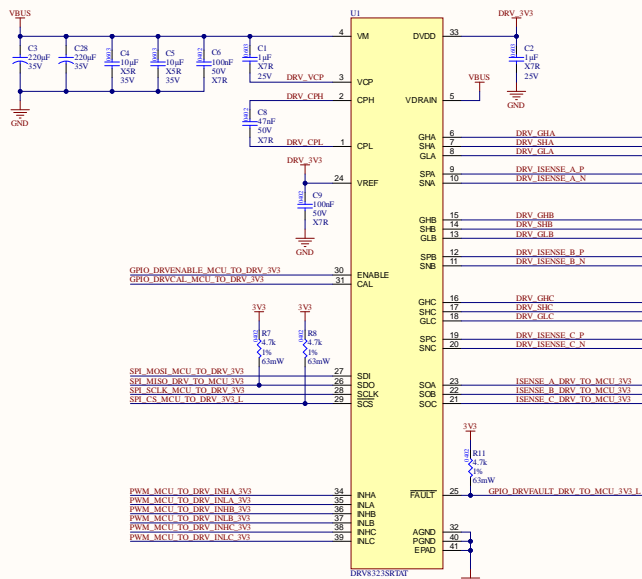
Temperature & 3V3



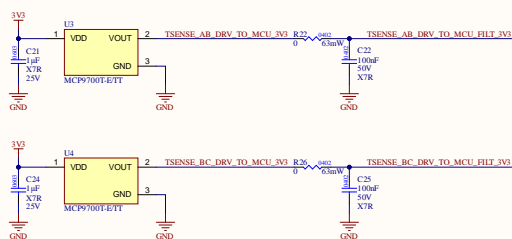
VBUS to 3V3 LDO



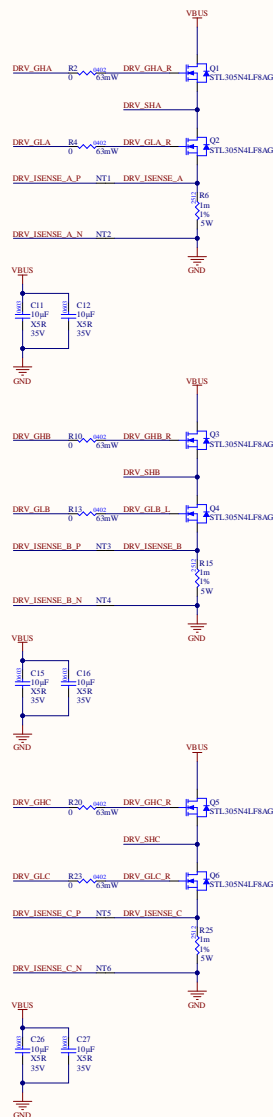
BLDC Gate Driver



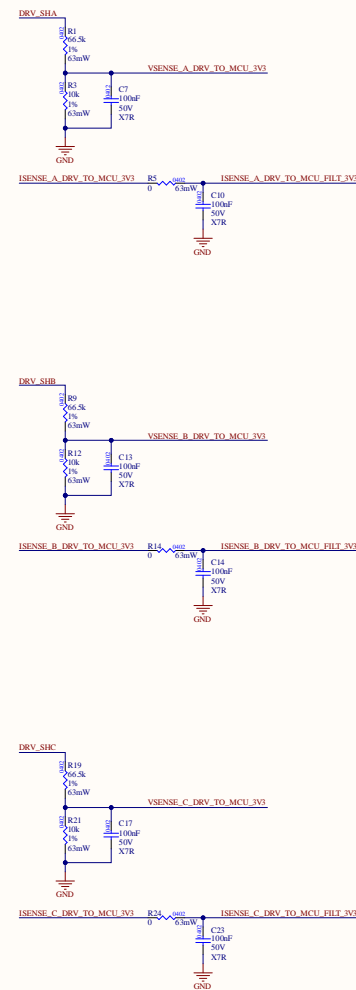
Temperature Sense



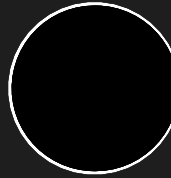
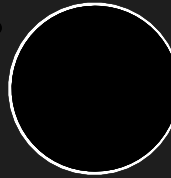
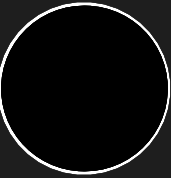
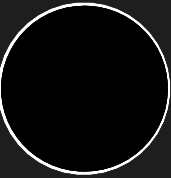
Half-Bridges (3x)



Phase Current & Voltage Sense (3x)



APPROVALS	DATE	PROJECT	Altium	
ENGR.				
DWG.		PROJECT REVISION	127520	127520
CHK.		TITLE	* Schematic SchDoc	
REFERENCE DOCUMENTS				
BOM				
ASSY DWG.		SIZE	CAGE CODE	DWG NO.
FAB DWG.		C		
PCB DWG.		SCALE	FILE NAME	SHEET 1 OF 1

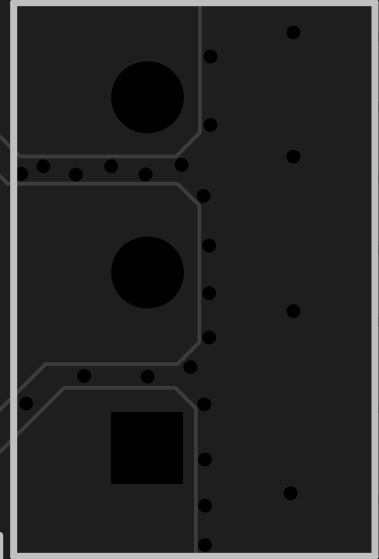
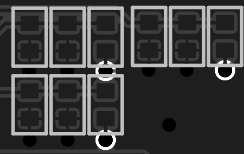
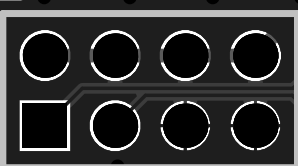
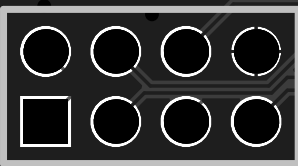
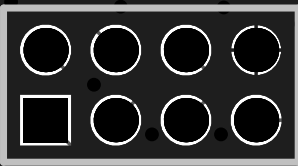
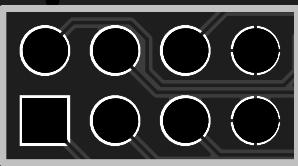


J5

J3

J4

J6



+

-

C

B

A

3

3

3

3

Board Stack Report