Date: 09.04.2019

Student Names: Salih Can Özçelik / Muhammed Halas
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Group ID: 6
Session ID: 2

CMPE 240 Experiment 5 Preliminary Work

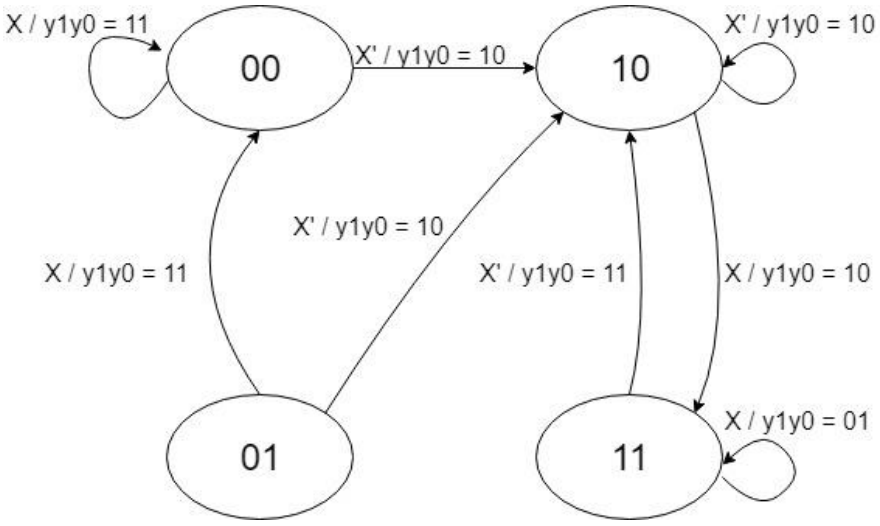
1. State Register Inputs: Clock, next state (d1,d0)
2. State Register Outputs: current state (n1,n0),
3. Combinational Block Inputs: X, current state (n1,n0)
4. Combinational Block Outputs: next state (d1,d0), outputs(y1,y0)
5. Obtain the truth table.

n1	n0	X	d1	d0	y1	y0
0	0	0	1	0	1	0
0	0	1	0	0	1	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
1	0	0	1	0	1	0
1	0	1	1	1	1	0
1	1	0	1	0	1	1
1	1	1	1	1	0	1

6. Is this a Moore or Mealy Machine? (No explanation, only short answer)

   Mealy Machine

7. Draw the finite state machine.



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Since the initial state is given to be ‘00’, FSM simplifies to this one.(Can’t reach state ‘01’.)