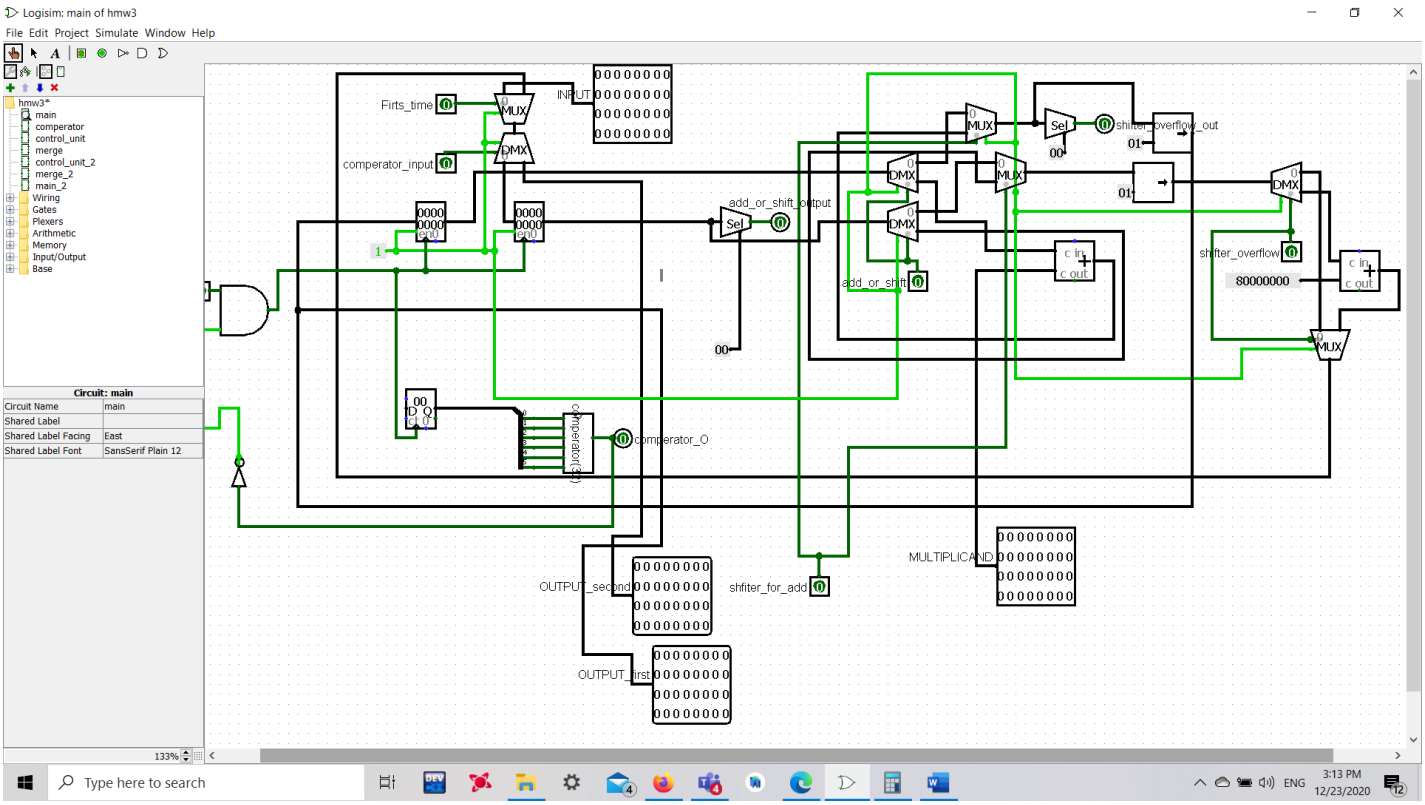
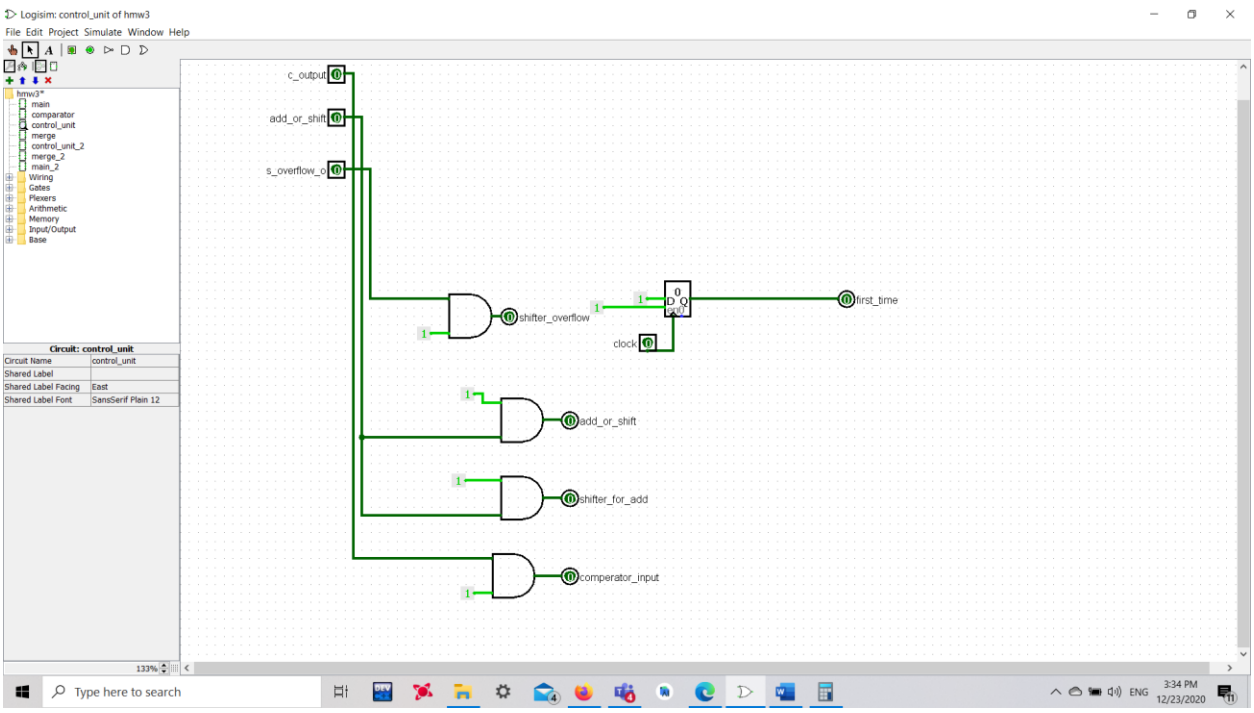
DATAPATH

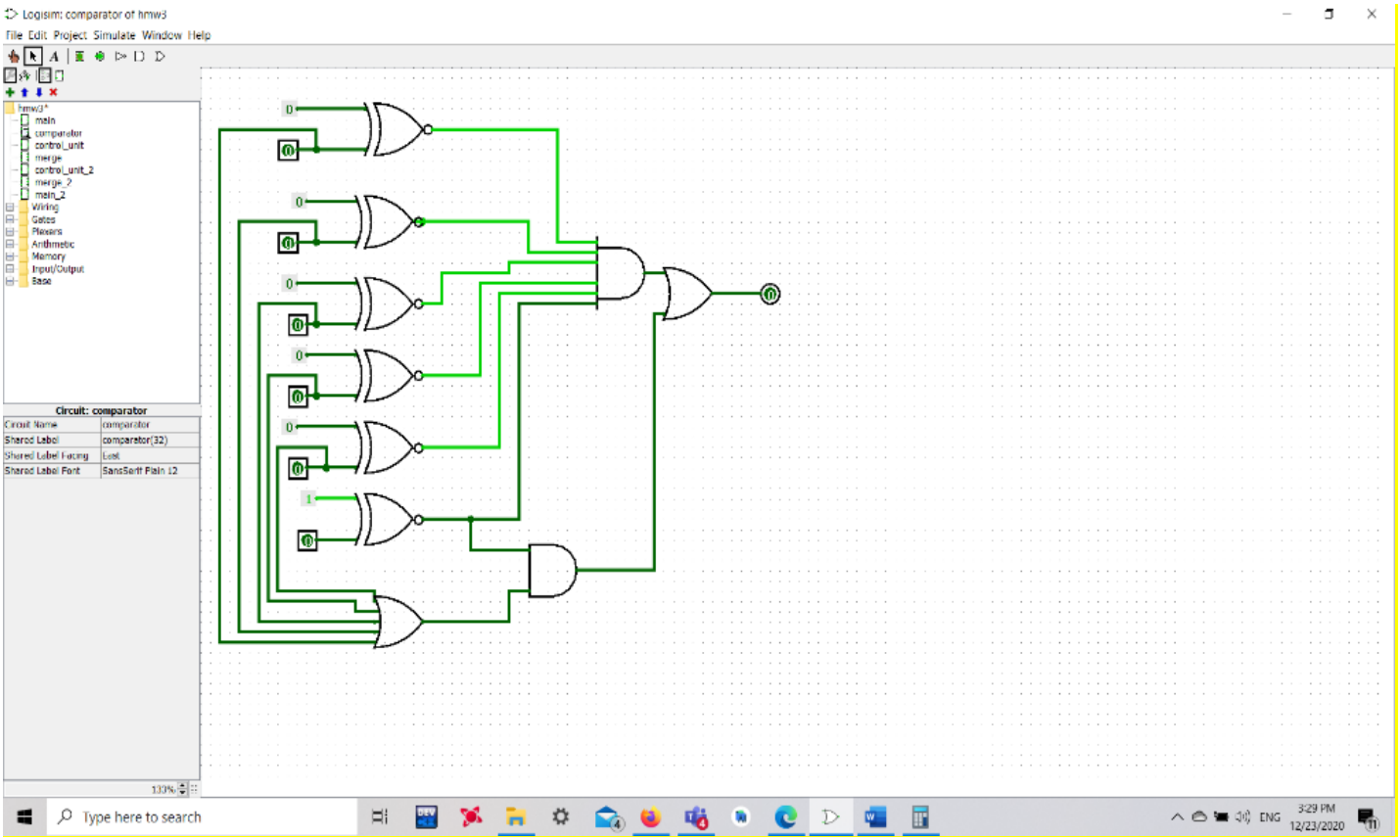

Logisim: main of hmw3
File Edit Project Simulate Window Help
hmw3*
main
comperator
control_unit
merge
control_unit_2
merge_2
main_2
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Circuit: main
Circuit Name main
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
Firts_time
INPUT
comperator_input
add_or_shift_output
add_or_shift
shifter_overflow_out
shifter_overflow
80000000
comperator_O
OUTPUT_second
OUTPUT_first
shifter_for_add
MULTIPLICAND
133%
Type here to search
ENG
3:13 PM
12/23/2020

Control Unit

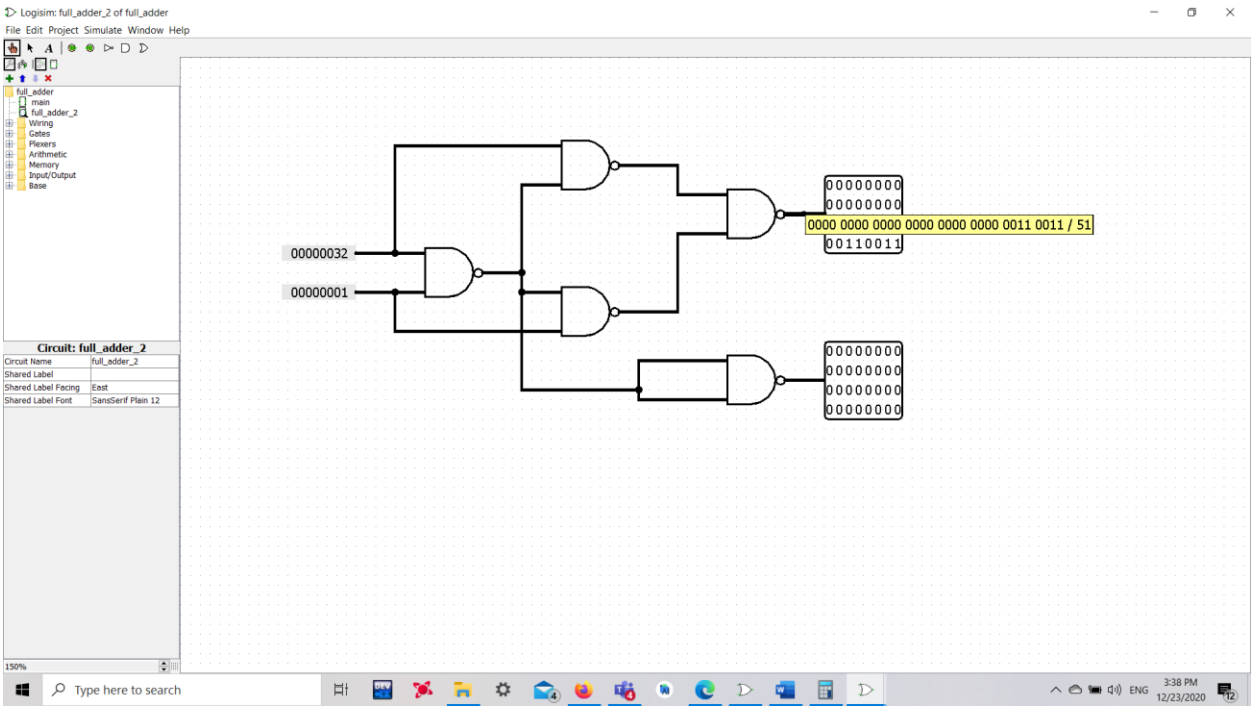


Bonus:

Comparator



Full_adder


Logisim: full_adder_2 of full_adder
File Edit Project Simulate Window Help
full_adder
main
full_adder_2
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Circuit: full_adder_2
Circuit Name full_adder_2
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
150%
00000032
00000001
00000000
00000000
0000 0000 0000 0000 0000 0000 0011 0011 / 51
00110011
00000000
00000000
00000000
00000000
Type here to search
ENG
3:38 PM
12/23/2020

DATAPATH:

Firs_time:

Buradaki datapati basitce aciklamak gerekirse first time 0 iken sayi registira yuklenir.

Sonra first time 1 olur.

Add_or_shift_output =0 :

Eger sayinin LSB'si 0 ise hem register 2(resimde soldaki) hem register 1 shift edilir(ikiside 32 bit).

Add_or_shift_input = 0

Shifter_for_add = 0

Add_or_shift_output=1:

Eger sayinin LSB'si 1 ise reg 1 multiplicant ile toplanir sonra iki register da shift edilir.

Shifter_overflow_out=0:

Sifir olmasi eger shift edilecekse overflow olmadigi anlamina gelir.

ornek:

now:

1000 0000 0000 0000 0000 0000 0000 0000 (reg1)

1000 0000 0000 0000 0000 0000 0000 0000 (reg2)

Next: (overflow yok sadece sifir geliyo)

0100 0000 0000 0000 0000 0000 0000 0000 (reg1)

0100 0000 0000 0000 0000 0000 0000 0000 (reg2)

Shifter_overflow_out=1:

Sifir olmasi eger shift edilecekse overflow oldugu anlamina gelir.

ornek:

now: (overflow var buyuk sayinin lsb'si 1 kucuk sayinin msb'sine kaymali)

1000 0000 0000 0000 0000 0000 0000 0001 (reg1)

1000 0000 0000 0000 0000 0000 0000 0000 (reg2)

next:

0100 0000 0000 0000 0000 0000 0000 0000 (reg1)

1100 0000 0000 0000 0000 0000 0000 0000 (reg2)

Comparator_o:

Bu output counter 32 ve 32'den buyuk olursa comperator_inputu 1 yapar. Sonucu registera basar.

Bonus: (Comparator kendi tasarimim) -> kullanildi calisiyor.

Adder:(kendi tasarimim)-> kullanilmadi ama testleri gecti calisiyor.

Clock:

Burada sekile dikkatle bakilirsa counter 32 saydiktan sonra eksilere indigi icin comparator_o'yu not gate'dan gecirirp clockla andledik boylece sonuc ekranda sabit bi sekilde kaliyor.

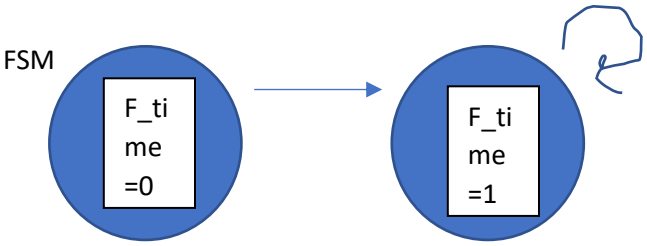
CONTROL_UNIT:

Combinational part:

Sekilden anlasilacagi uzere burada add_or_shift,c_output,s_overflow_out gibi inputlarimiz var bunlari and gatelerde sokup outputlara verdik burada sequential bi durum yok.

Sequencil part:

Buradaki first_time input'umz sequential calismaktadir tasarimi asagidadir.



Truth table:

PS		NS	
S0		V0	F_TIME
0		1	0
1		1	1

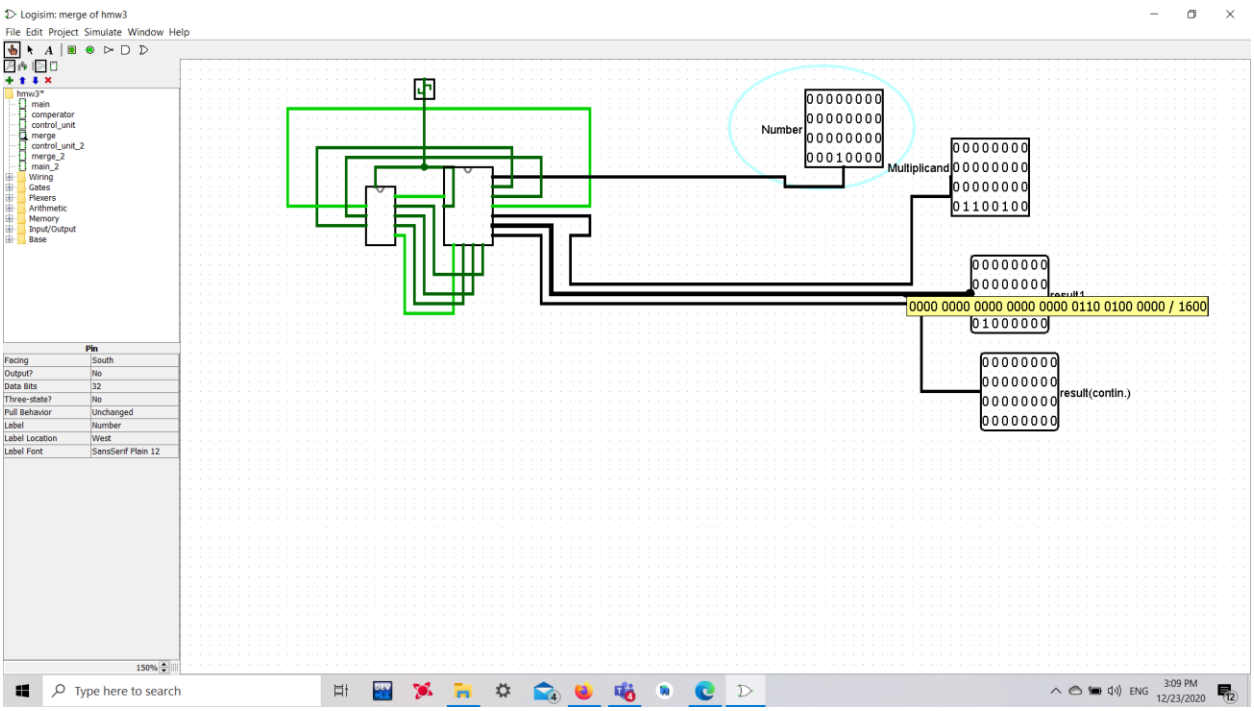
V0= 1

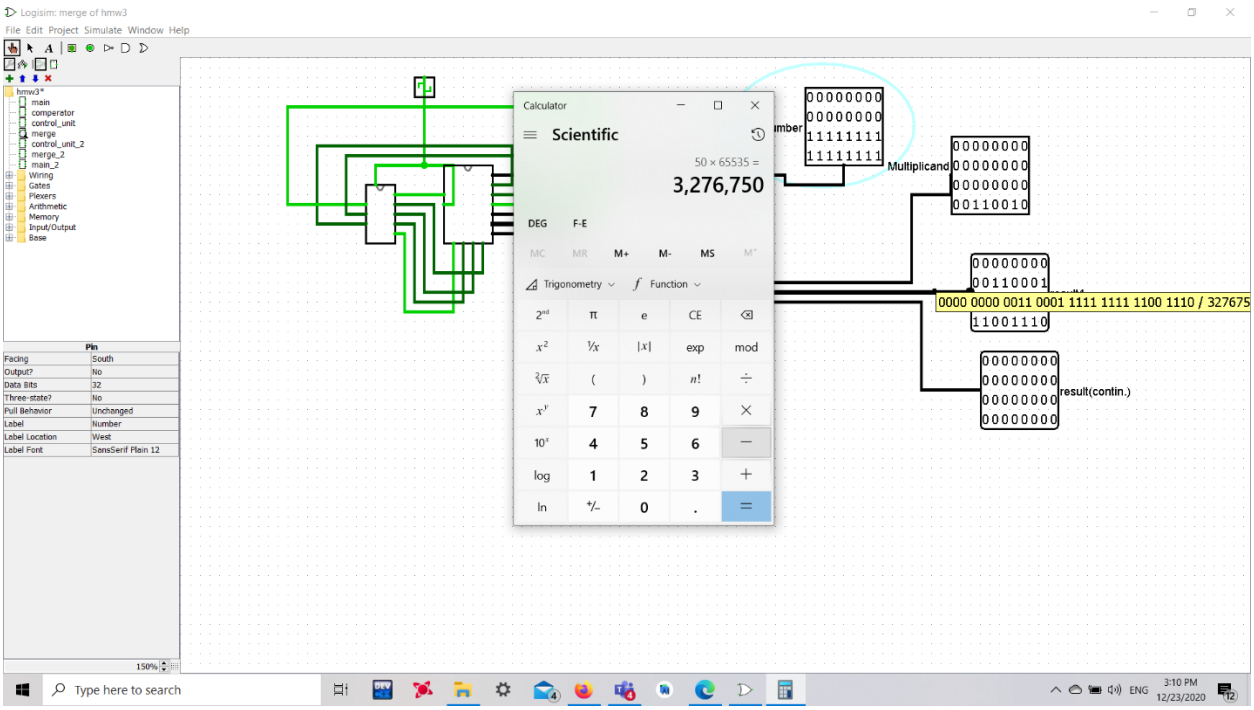
F_TIME=s0

TEST_CASES:

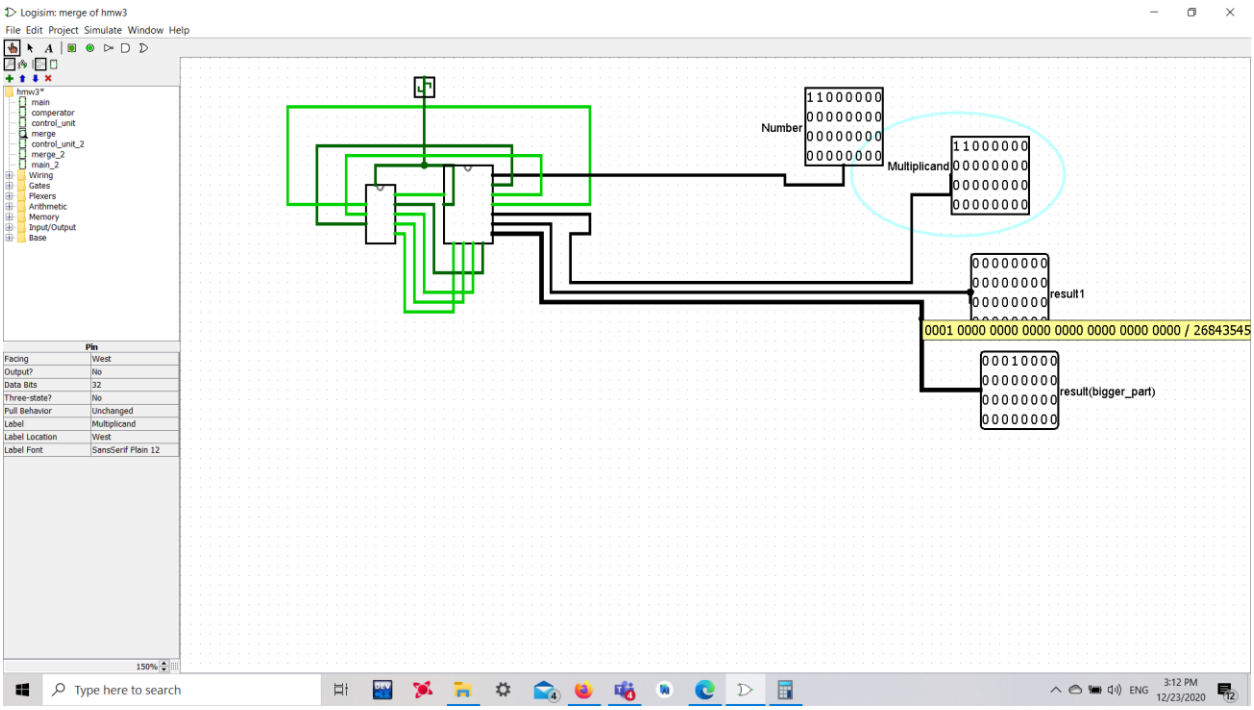
4.1kz ile test edilmistir digger clocklar ile de denenebilir sorun cikmamistir.

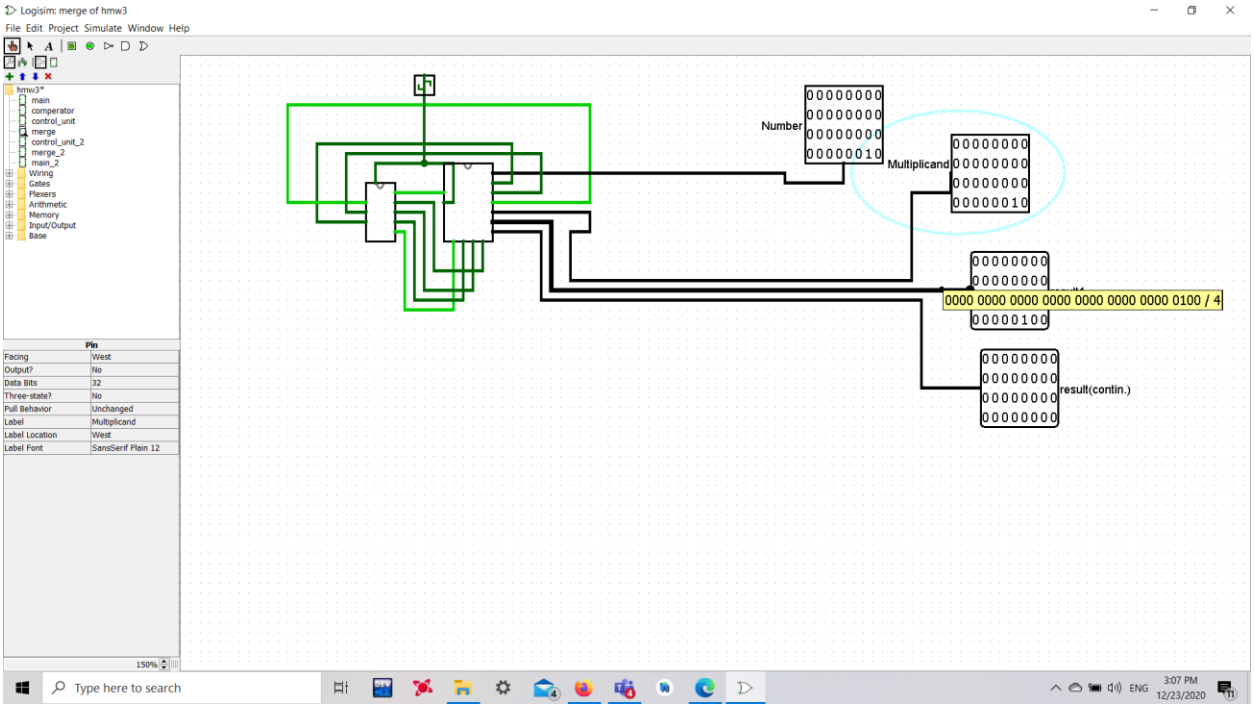
Result bigger part ilk 32 bit result 1 kalan 32 bit.

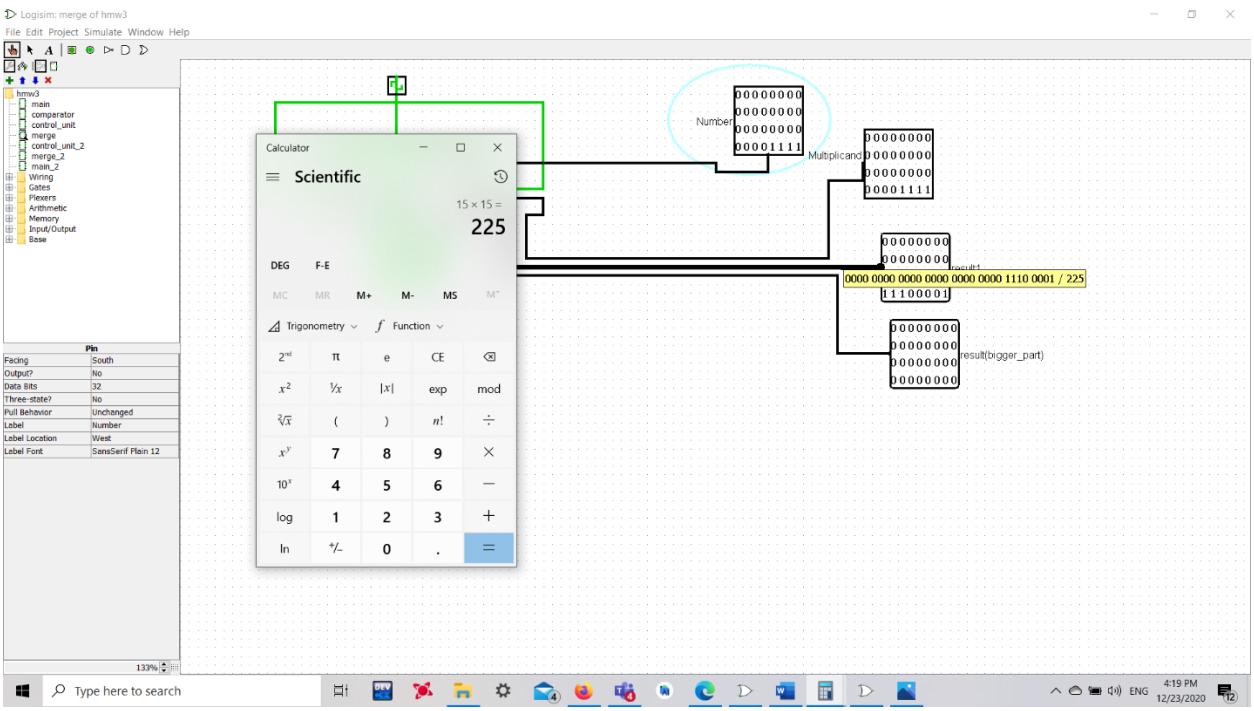

Logisim: merge of hmw3
File Edit Project Simulate Window Help
hmw3*
main
comperator
control_unit
merge
control_unit_2
merge_2
main_2
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing South
Output? No
Data Bits 32
Three-state? No
Pull Behavior Unchanged
Label Number
Label Location West
Label Font SansSerif Plain 12
Number
00000000 00000000 00000000 00010000
Multiplicand
00000000 00000000 00000000 01100100
00000000 00000000
0000 0000 0000 0000 0000 0110 0100 0000 / 1600
01000000
00000000 00000000 00000000 00000000
result(contin.)
150%
Type here to search
ENG
3:09 PM
12/23/2020


Logisim: merge of hmw3
File Edit Project Simulate Window Help
hmw3*
main
comperator
control_unit
merge
control_unit_2
merge_2
main_2
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing South
Output? No
Data Bits 32
Three-state? No
Pull Behavior Unchanged
Label Number
Label Location West
Label Font SansSerif Plain 12
Calculator
Scientific
50 × 65535 =
3,276,750
DEG
F-E
MC MR M+ M- MS M˅
Trigonometry
Function
00000000 00000000 11111111 11111111
Multiplicand
00000000 00000000 00000000 00110010
00000000 00110001
0000 0000 0011 0001 1111 1111 1100 1110 / 327675
11001110
00000000 00000000 00000000 00000000
result(contin.)
150%
Type here to search
ENG
3:10 PM
12/23/2020

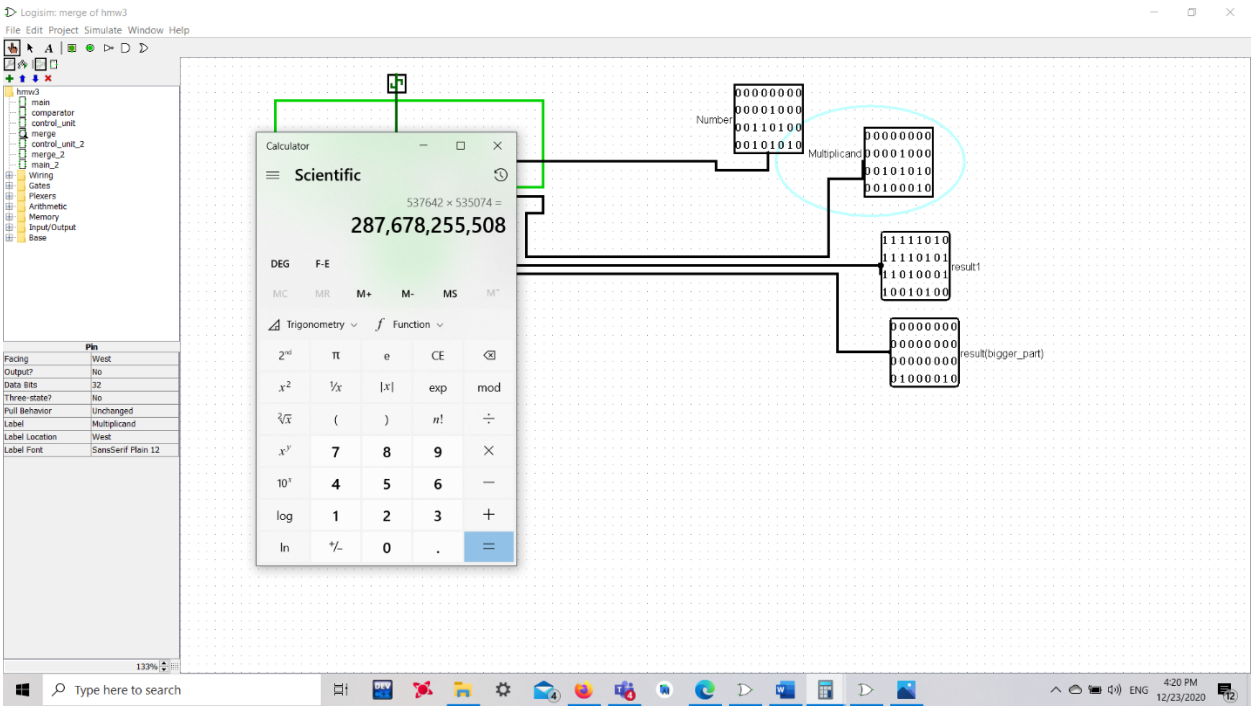
Result1 deki sifirlar eklenmeli 64 bitlik output yok biliyosunuz. Ornek sonda var denendi.

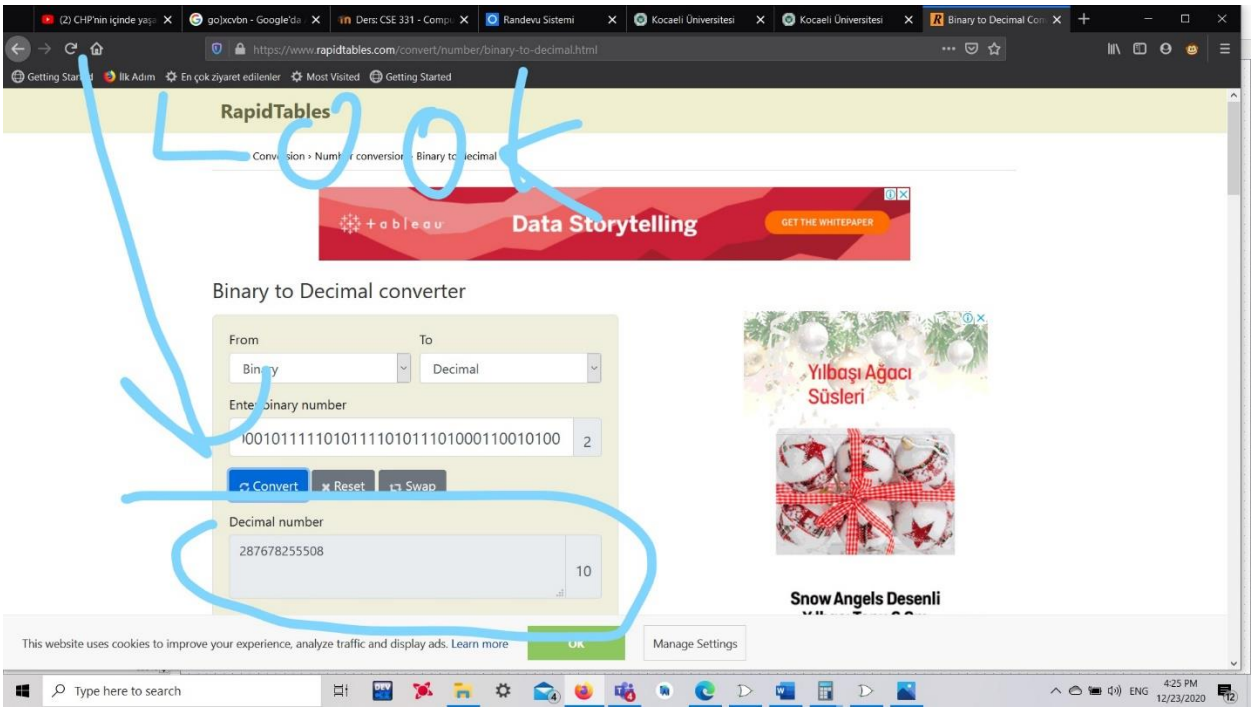




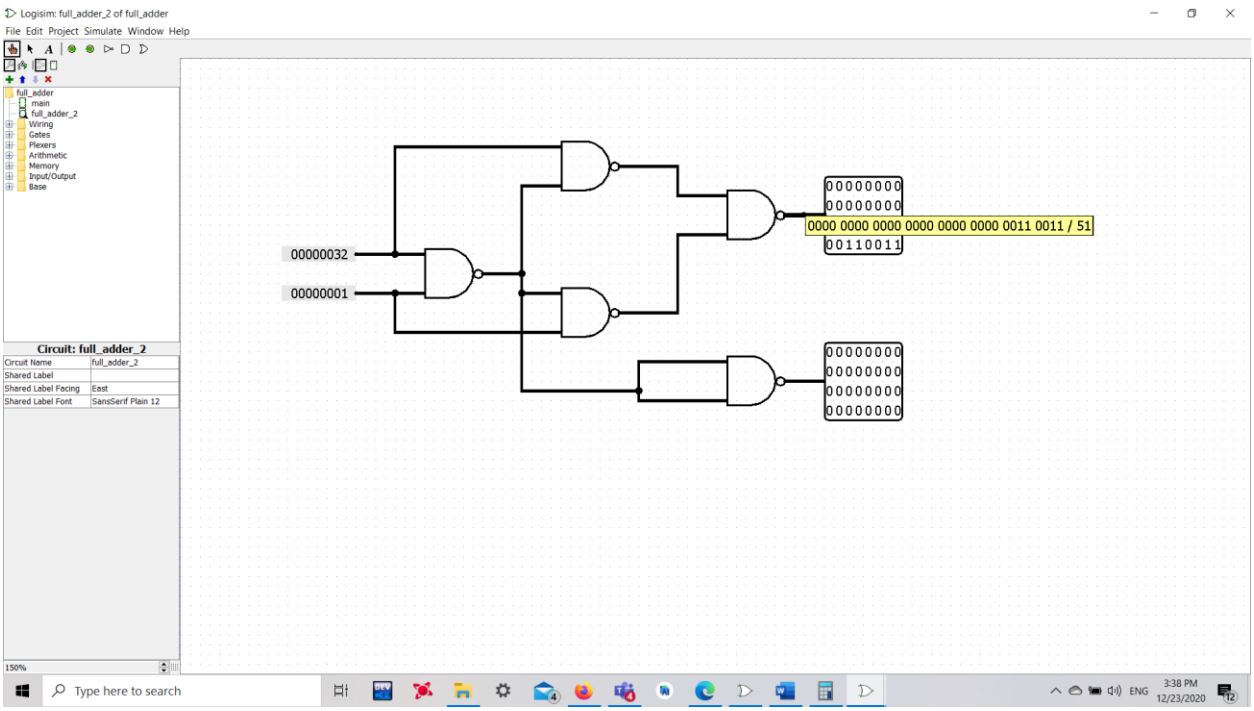


Result bigger part ilk 32 bit result 1 kalan 32 bit




RapidTables
Data Storytelling
GET THE WHITEPAPER
Binary to Decimal converter
From
To
Decimal
Enter binary number
10010111110101111010111010000110010100
2
Convert
Reset
Swap
Decimal number
287678255508
10
Yılbaşı Ağacı Süsleri
Snow Angels Desenli
This website uses cookies to improve your experience, analyze traffic and display ads. Learn more
OK
Manage Settings
Type here to search

Adder test:


Logisim: full_adder_2 of full_adder
File Edit Project Simulate Window Help
full_adder
main
full_adder_2
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Circuit: full_adder_2
Circuit Name
full_adder_2
Shared Label
Shared Label Facing
East
Shared Label Font
SansSerif Plain 12
00000032
00000001
00000000
00000000
0000 0000 0000 0000 0000 0000 0011 0011 / 51
00110011
00000000
00000000
00000000
00000000
150%
Type here to search