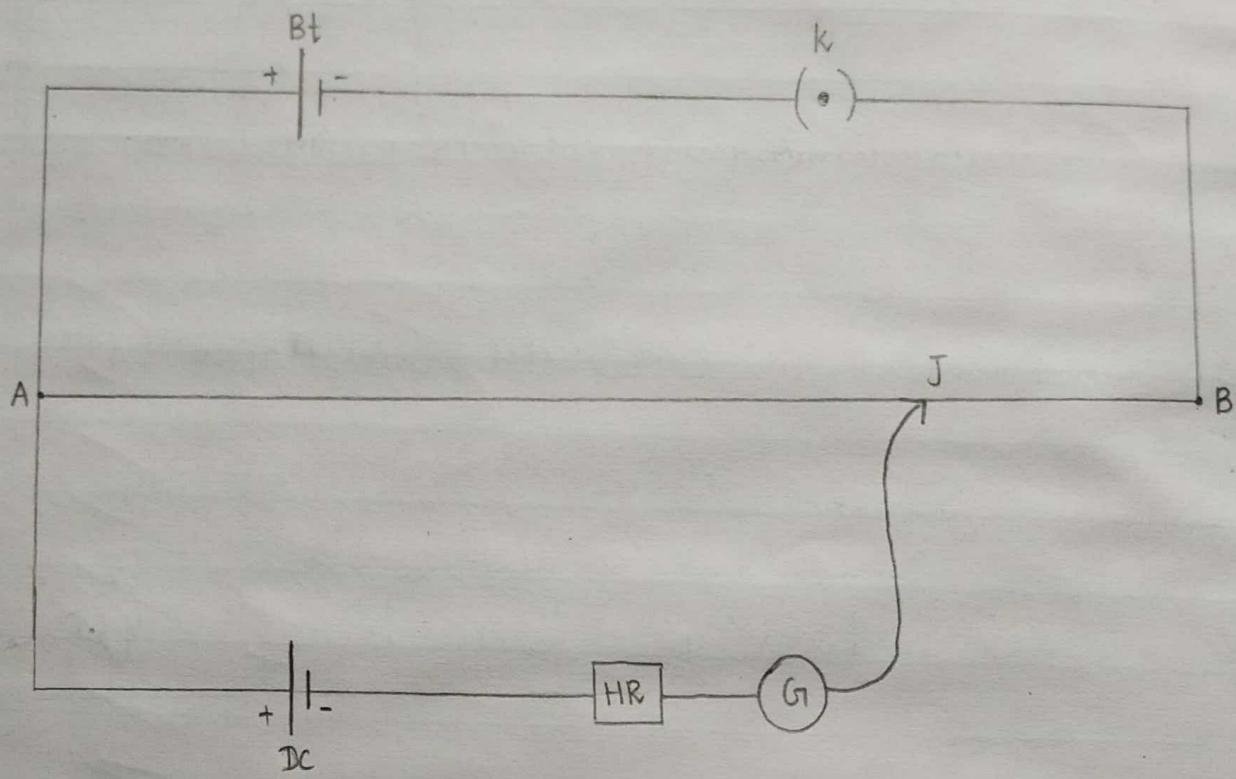
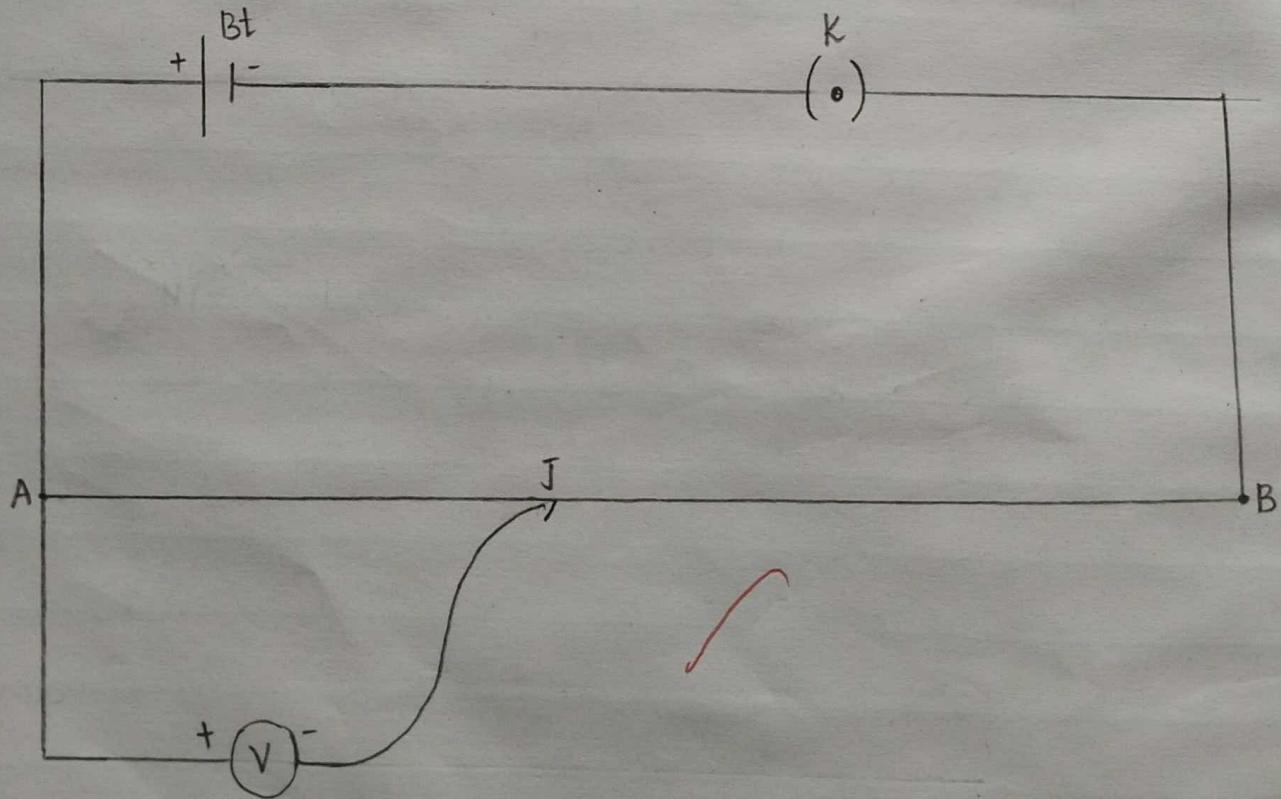


CIRCUIT DIAGRAM

PRIMARY CIRCUIT :-



SECONDARY CIRCUIT :-



Ex. No.: 01
13/09/2021

POTENTIOMETER - CALIBRATION OF LOW RANGE VOLTMETER

AIM :-

To calibrate a low range voltmeter (0-3V) using a potentiometer.

APPARATUS REQUIRED:-

Potentiometer, high resistance, pulley key, voltmeter, Daniel cell, connecting wires, battery, galvanometer, jockey, power supply.

FORMULA:-

$$V' = 1.08 \times \left(\frac{l_2}{l_1} \right) (V)$$

where,

V' = calculated voltage (V)

l_1 = balancing length of Daniel cell $\times 10^{-2}$ m

l_2 = balancing length of different voltage $\times 10^{-2}$ m

MODEL GRAPH-I:-

CALIBRATION GRAPH

PROCEDURE:

The potentiometer terminal A and B are connected in series with the rheostat an circuit the daniel cell is connected in the Galvanometer and high resistance as shown in figure. the positive terminal as daniel cell must be connected to the positive and A of the potentiometer wire the jockey is pressed at various points and the balancing length is found out when galvanometer shows zero reading.

Now the potentiometer wire has a potential difference of 1.08 volts for of length the potential difference for cm of the potentiometer wire .

$$= \frac{1.08}{l_0} \text{ volts}$$

MODEL GRAPH-II:-

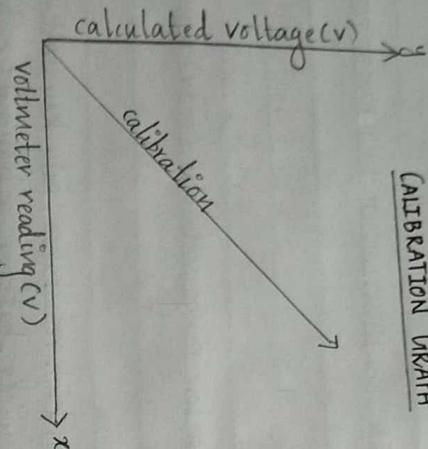
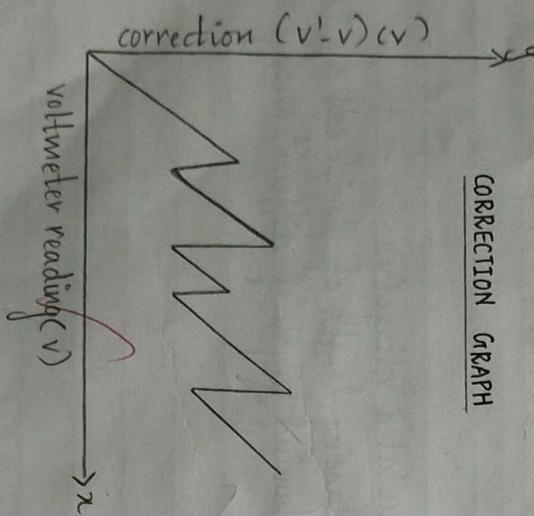
CORRECTION GRAPH

Now the secondary circuit is removed and low range voltmeter is connected in the place with its positive and connected to positive terminal A of the potentiometer wire the voltmeter with show a reading when the jockey is moved. pressing at various point till the voltmeter reads 0.1V. The balancing length l is found at measuring from the positive and A similarly voltmeter reads 0.2, 0.3, 0.4, ... 1.2 volts.

If l_1 is the balancing length when voltmeter reads V volts, the correct potential difference across l is given by

$$V_1 = \frac{1.08}{l_0} \times l_1 \text{ volt}$$

Now, the correcting to the applied for energy voltmeter reading is thus calculated and tabulated.



ABULATION:

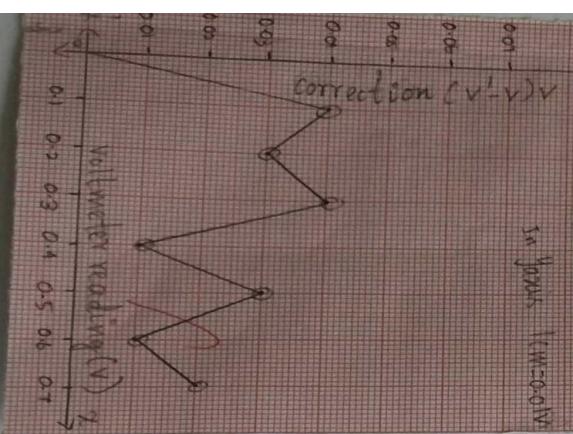
Balancing Length of Daniel Cell $l_1 = \underline{80.5 \times 10^{-2} \text{ m}}$

Voltmeter reading (v)	Balancing length $\times 10^{-2} \text{ m}$ (l_2)	$v' = 1.08 \times \left(\frac{l_2}{l_1}\right)(v)$	correction $(v' - v)$ (v)
0.1	10.5	0.14	0.04
0.2	17.15	0.23	0.03
0.3	25.6	0.34	0.04
0.4	31.3	0.41	0.01
0.5	39.6	0.53	0.03
0.6	45.7	0.61	0.01
0.7	54.3	0.72	0.02

Scale
in Km = 0.1 V

$$\text{Cell } \lambda_1 = 80.5 \times 10^{-2} \text{ m}$$

$\frac{R_2}{R_1}(\nu)$	Correction $(\nu' - \nu)$
0.14	0.04
0.23	0.03
0.34	0.04
0.41	0.01
0.53	0.03
0.61	0.01
0.72	0.02



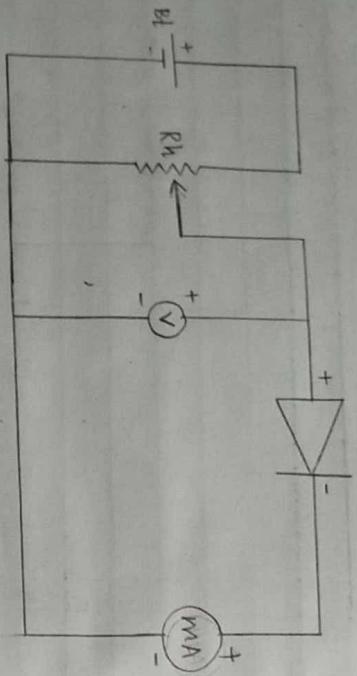
RESULT:-

The given low range voltmeter is calibrated using potentiometer. The calibration and correction graphs are drawn

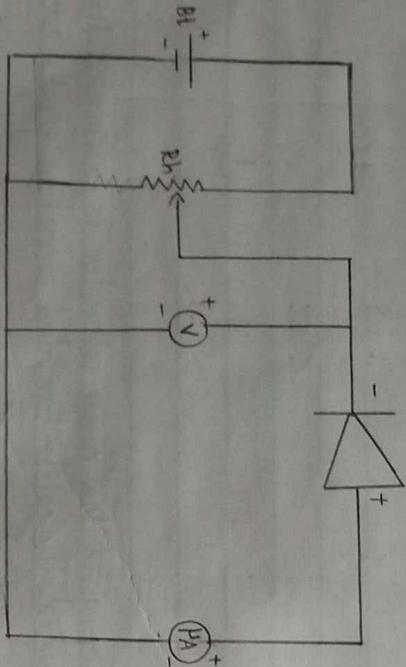
CIRCUIT DIAGRAM

(2)

FORWARD BIAS:



REVERSE BIAS:



Ex. No.: 02

20/09/2021

CHARACTERISTIC OF SEMICONDUCTOR DIODE

AIM:

To study the characteristic of the semi conductor diode

APPARATUS REQUIRED:

Semiconductor diode, voltmeter, milliammeter, microammeter, Battery, connecting wires, power supply, rheostat.

FORMULA:

$$\text{Forward Resistance } R_f = \frac{\Delta V_f}{\Delta I_f} (\Omega)$$

$$\text{Reverse Resistance } R_r = \frac{\Delta V_r}{\Delta I_r} (k\Omega)$$

Where,

ΔV_f = change in forward bias voltage (V)

ΔI_f = change in forward bias current (mA)

ΔV_r = change in reverse bias voltage (V)

ΔI_r = change in reverse bias current (μ A)

TABULATION-I

FORWARD BIAS:

(1)

Forward Bias voltage (V)	Forward Bias current (mA)
0	0
0.1	0
0.2	0
0.3	0
0.4	0
0.5	0
0.6	0
0.7	0
0.8	0
0.9	0
1	5
1.1	10
1.2	15
1.3	20
1.4	25
1.5	30
1.6	35
1.7	40
1.8	45
1.9	50

PROCEDURE:-

FORWARD BIAS:

(2)

The connection are made as shown in the figure. Since, the 'P' region of the semiconductor diode is connected to the position of the battery it is said to be forward biased. The forward bias voltage is increased from 0.1V to 1V in steps of 0.1V and in each case of the milliammeter reading is noted.

REVERSE BIAS:

The connection are made as shown in the figure. Hence, the 'N' region to semiconductor diode is connected to the position of positive of the battery voltage from 0 to 3V in steps 0.5V to microammeter reading is noted.

A graph is drawn taking the voltage V along x -axis and the current (I) along y -axis the step that the slope of the current is gives the resistance in particular bias.

CALCULATION-I

FORWARD BIAS:

$$R_f = \frac{\Delta V_f}{\Delta I_f}$$

$$= \frac{1.5 - 1}{2.5 - 10 \times 10^{-3}} = 3.33 \Omega$$

✓

$R_f = 3.33 \Omega$

FORWARD BIAS:

✓

$R_f = 3.33 \Omega$

TABULATION - II

REVERSE BIAS :-

Reverse Bias voltage (v)	Reverse Bias current (μA)
0	0
0.2	6
0.4	10
0.6	12
0.8	14
1	16
1.2	24
1.4	28
1.6	32
1.8	36

CALCULATION - II

REVERSE BIAS :-

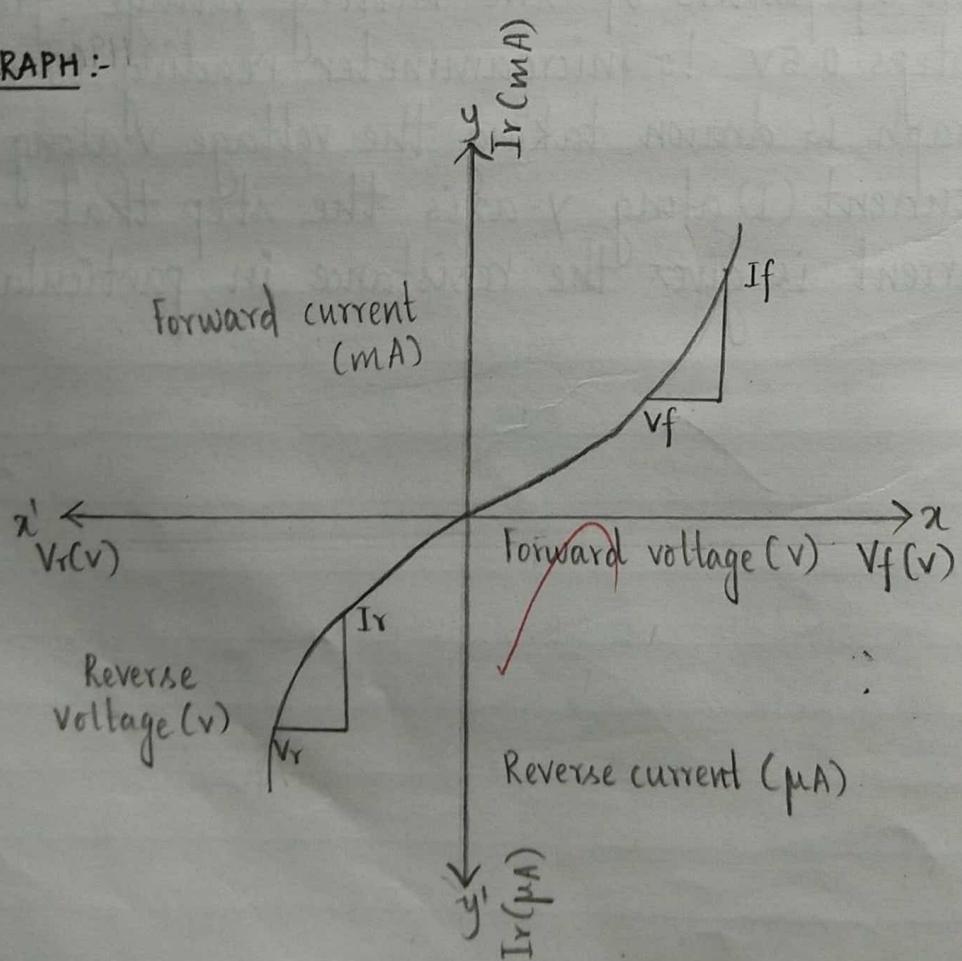
$$R_r = \frac{\Delta V_r}{\Delta I_r}$$

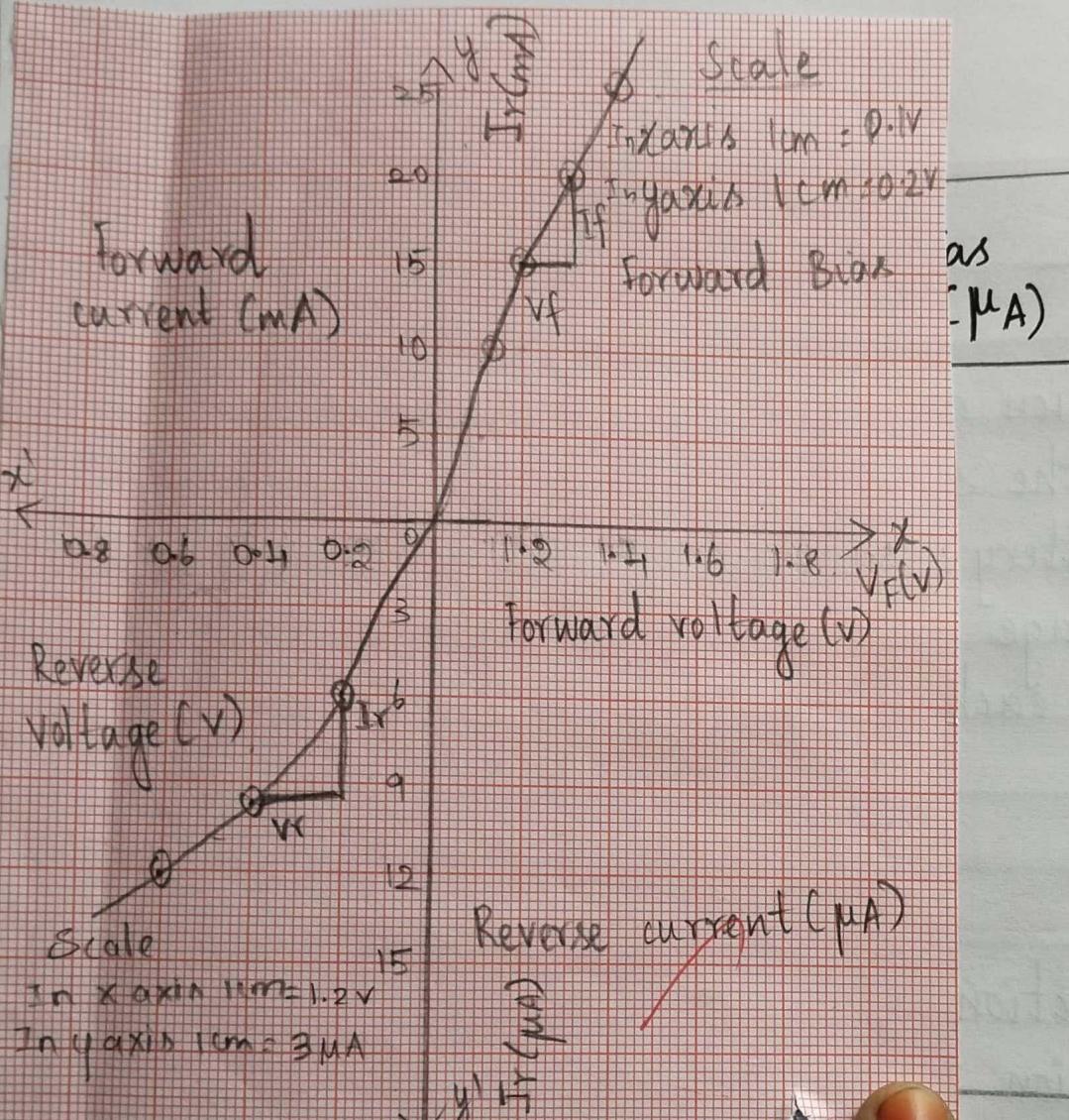
$$= \frac{2 - 1.5}{36 - 26 \times 10^{-6}}$$

$$= 50 k\Omega$$

$$R_r = 50 k\Omega$$

MODEL GRAPH :-





CALCULATION - II

REVERSE BIAS :

$$R_r = \frac{\Delta V_r}{\Delta I_r}$$

$$= \frac{2 - 1.5}{36 - 26 \times 10^{-6}}$$

$$= 50 \text{ k}\Omega$$

$$R_r = 50 \text{ k}\Omega$$

RESULT :-

Thus, the characteristic curve of a semiconductor diode
is studied

bias

1.) Forward Resistance $R_f = 3.33 \Omega$

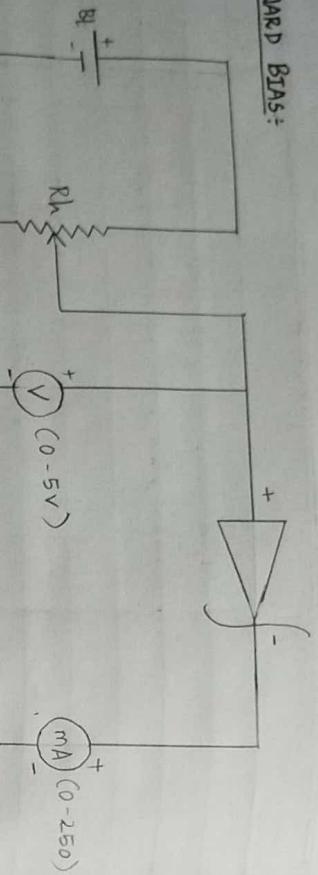
2.) Reverse Resistance $R_r = 50 k\Omega$

bias

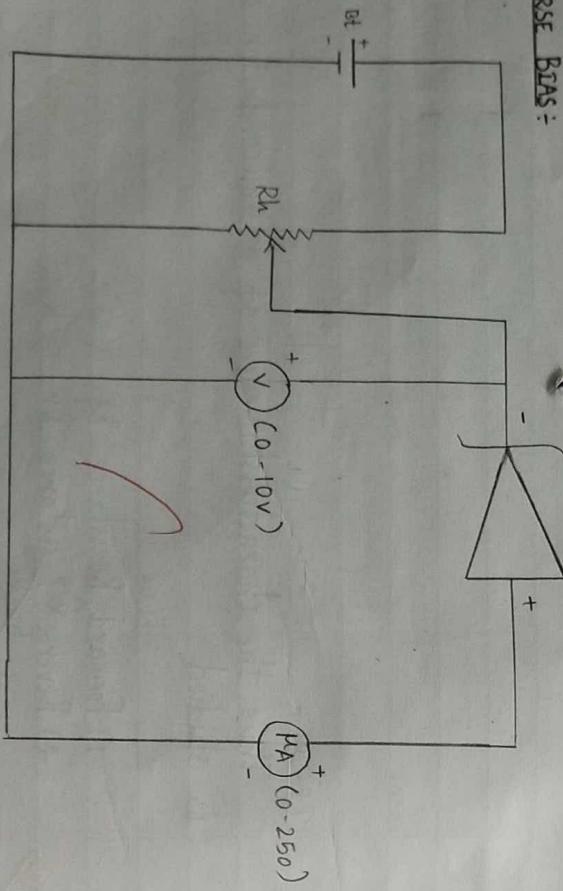
CIRCUIT DIAGRAM

②

FORWARD BIAS:



REVERSE BIAS:



Ex. No.: 03.

13/10/2021

CHARACTERISTIC OF ZENER DIODE

AIM:

To study the characteristic of a Zener Diode

APPARATUS REQUIRED:-

15 volt power supply, zener diode, connecting wires, Battery, voltmeter, Rhostat, microammeter, milliammeter,

FORMULA:

$$\text{Forward Bias Resistance } R_f = \frac{\Delta V_f}{\Delta I_f} (\Omega)$$

where,

ΔV_f = change in forward voltage (v)

ΔI_f = change in forward current (mA)

TABULATION-I

WARD BIAS:

Forward voltage (v)	Forward Current (mA)
0	0
0.1	0
0.2	0
0.3	0
0.4	1
0.5	3
0.6	6
0.7	10

0.5 < 3.5
 (3-1) \times 10

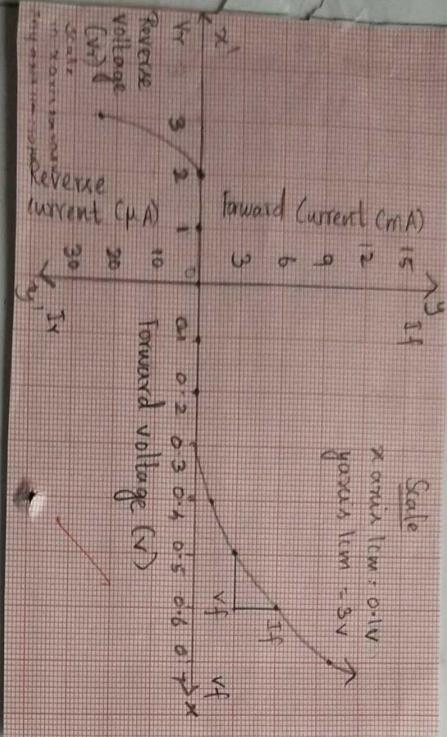
TABULATION-II

REVERSE BIAS:

Reverse Voltage (v)	Reverse Current (I)
0	0
1	0
2	0
3	23

TABULATION-I

FORWARD BIAS:



$$0.5 = 3.4 \\ (3-1) \times 10^{-3}$$

PROCEDURE:-
FORWARD BIAS:-

To study forward bias characteristics of zener diode. The connected are made in shown in figure. The voltage increase from 0 is all step of 0.2 volts. The milliammeter reading are noted in each case for small range of current 0 to mA can be switch over 0 to 50 mA for high range.

REVERSE BIAS:

This circuit is modified as shown in the figure and diode is AB reversed and is almost contact the micro ammeter reading are tabulated. The current graph is drawn by taking voltage in x-axis reverse current in y-axis from forward voltage current in milliammeter the ammeter voltage of reverse can be drawn in the same graph.

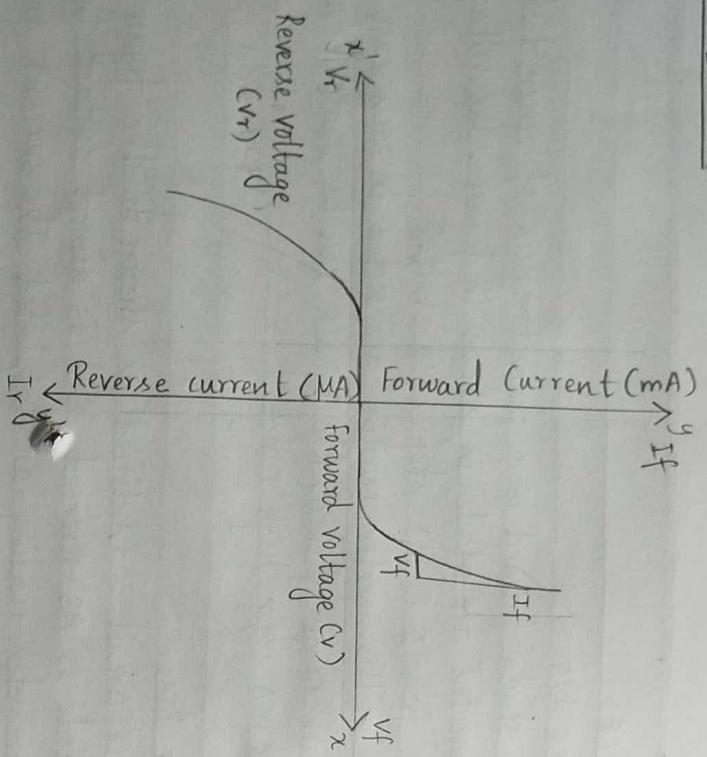
(1b)

TABULATION-II

REVERSE BIAS:

Reverse Voltage (V)	Reverse Current (I)
0	0
1	0
2	0
3	0.23

MODEL GRAPH:



CALCULATION:

$$\text{Bias Forward Resistance } R_f = \frac{\Delta V_f}{\Delta I_f}$$

$$= \frac{0.6 - 0.5}{(6 \cdot 10^{-3}) \times 10^{-3}}$$

$$R_f = \frac{0.1}{3 \times 10^{-3}}$$

$$R_f = 33.3 \Omega$$

$$R_f = 33.3 \Omega$$

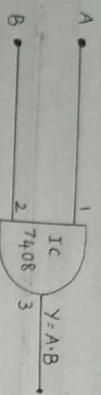
RESULT:

Thus, the characteristics of zener diode is studied and the characteristics curves are drawn. Zener diode breakdown voltage is calculated.

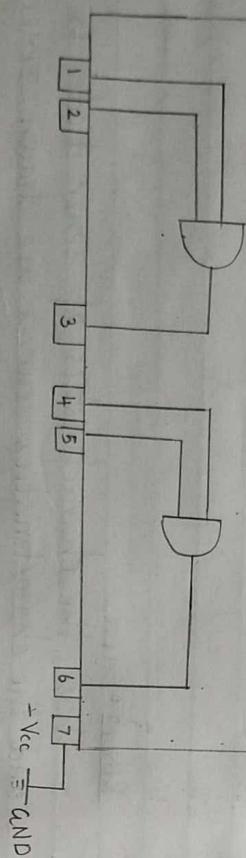
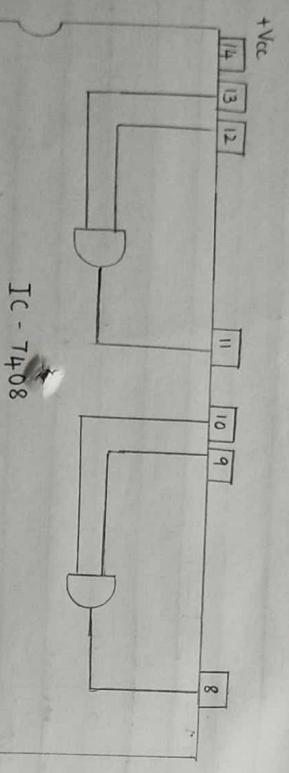
- 1.) Forward Bias $R_f = 33.3 \Omega$
- 2.) Breakdown Voltage $V = 3V$

AND GATE

CIRCUIT DIAGRAM:



PIN CONFIGURATION:



TRUTH TABLE:

		O/p: $Y = A \cdot B$	
A	B	Logic Level	Voltage Level (V)
0	0	0	0.2
0	1	1	0.2
1	0	0	0.2
1	1	1	2.8
		2.8	

Ex. No.: 04

01/11/2021

STUDY OF LOGIC GATES USING IC'S

AIM:

To construct IC Logic gates OR, AND, NOT, NAND, NOR and EX-OR gates are to verify the corresponding truth table.

APPARATUS REQUIRED:

IC 7408, [AND]

IC 7432, [OR]

IC 7404, [NOT]

IC 7400, [NAND]

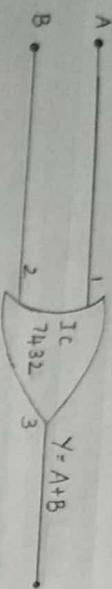
IC 7486, [EX-OR]

IC 7402, [NOR]

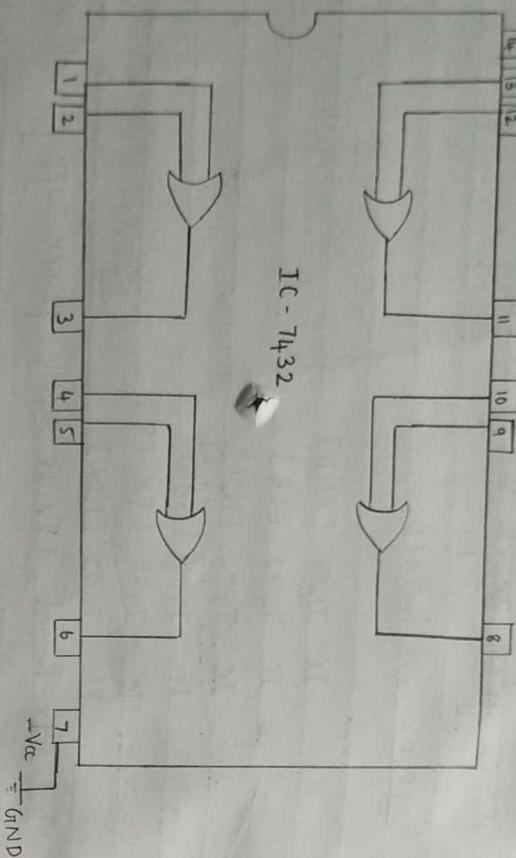
Indicator Record, +5V DC supply, power supply, voltmeter, connecting wires.

OR GATE

CIRCUIT DIAGRAM:



PIN CONFIGURATION:



IC - 7432

TRUTH TABLE:

A	B	Op : $Y = A + B$
0	0	0
1	1	1
1	0	1
0	1	1

OR GATE

PROCEDURE :-

OR GATE:

The IC chip 7432 is fixed on the break board. The negative of the power supply is connected to pin 7 on the +ve is connected to pin A is and is kept at 5 volts. We can construct 4 or gates with on IC chip for the first or gates 112 are inputs and 3 will be outputs to the inputs levels are kept at (0,0), (0,1), (1,0) and (1,1) levels are the corresponding output voltage measured and the truth table is verified. The output is $A + B$, OR functions we can verify the output voltage with OR gates also.

OUTPUT : $Y = A + B$

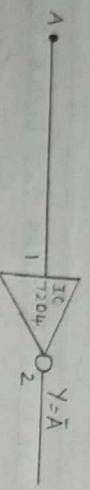
AND GATE:

The IC chips 7408 is fixed on the break board. The pin 7 is connected to +ve and the 14 is connected to +ve of the power supply, which is kept chips at volts, the input levels at 5 volts, we construct 4 and scales with an IC chip, the input levels are kept at (0,0), (0,1), (1,0) and (1,1) the corresponding output are measured and they are found to be $A \cdot B$ and the truth table are verified.

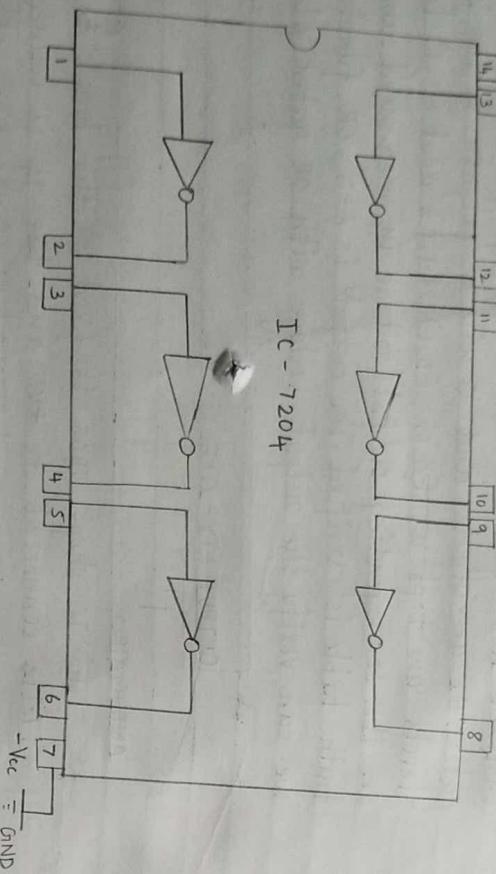
OUTPUT : $Y = A \cdot B$

CIRCUIT DIAGRAM:

NOT GATE



PIN CONFIGURATION:



IC - 7204

OUTPUT: $Y = \bar{A}$

NOT GATE:

The IC chips 7404 is fixed on the break board. The pin 7 is connected to negative and 14 is connected to the +ve of the power supply, which is kept at 5 volts. Here we can get 6 NOT gates when the inputs is '0', we get '1' output and vice versa is the output is found to be \bar{A} .

NOR GATE:
The IC chips 7402 is fixed on the break board. The pin 7 is connected to negative and 14 is connected to the +ve of the power supply, which is kept at 5 volts. Here, we can get 4 NOR gates. The inputs is kept at (0,0), (0,1), (1,0), (1,1) levels. The output is measured and it is found to follows the relation OR and AND, that is $\overline{A+B} = \bar{A} \cdot \bar{B}$. The truth table is also verified.

OUTPUT: $Y = \overline{A+B}$

NAND GATE:

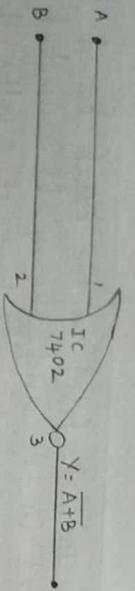
The IC chips 7400 is fixed on the break board. The pin 7 is connected to -ve and 14 is connected to the +ve of the power supply, with the kept at 5 volts we can get 4 NAND gates the inputs is kept at the (0,0), (0,1),

A	O/P: $Y = \bar{A}$
0	1
1	0

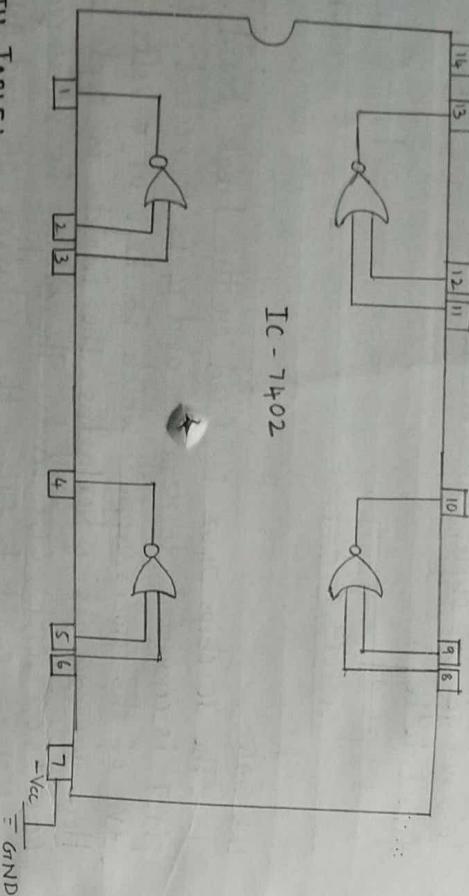
Logic level
Voltage level (V_Y)

NOR GATE

CIRCUIT DIAGRAM:



PIN CONFIGURATION:



IC - 7402

TRUTH TABLE:

O/P: $Y = A + B$		
A	B	Logic Level
0	0	1
1	0	0
0	1	0
1	1	0

O/P: $Y = A + B$		
A	B	Voltage Level (V)
0	0	4.5
1	0	0
0	1	0
1	1	0

OUTPUT: $Y = A \oplus B$

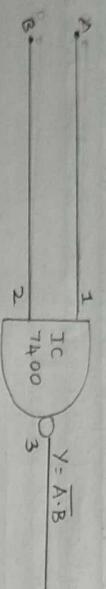
EX-OR:

The IC chips 7486 is fixed on the break board. The pin 7 is connected to -ve and pin 14 is connected to +ve of the power supply, which is kept at 5volts. We can get gate the inputs is kept at (0,0), (0,1), (1,0), and (1,1) levels. The outputs is measured and it is found to follow the relation. The truth table is also verified.

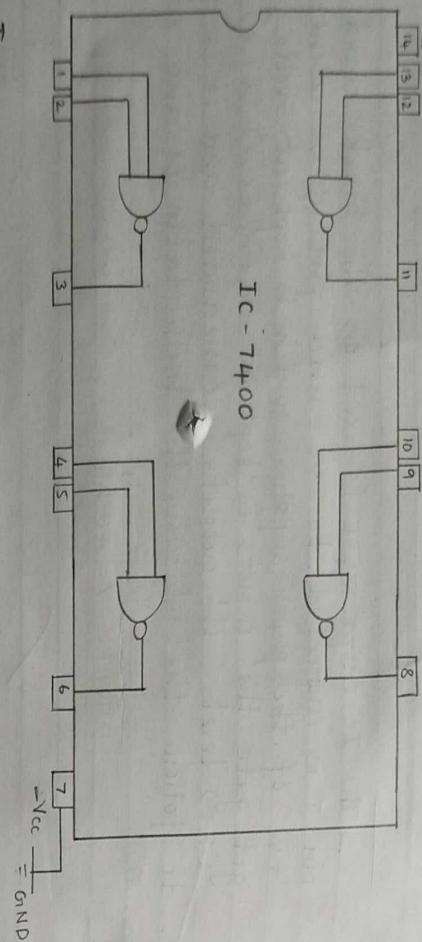
OUTPUT: $Y = A \oplus B$

NAND GATE

CIRCUIT DIAGRAM:



PIN CONFIGURATION :



TRUTH TABLE :-

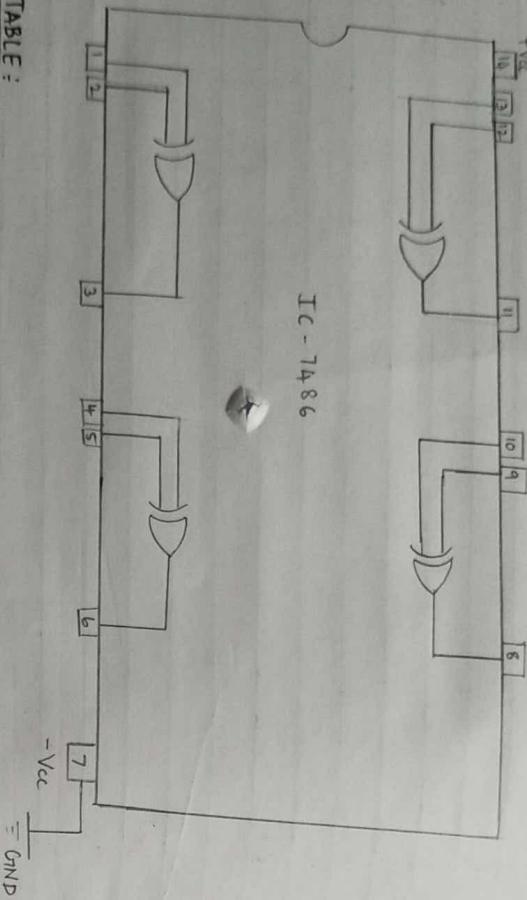
		O/P $\therefore Y = \overline{A \cdot B}$
A	B	Logic Level
0	0	1
0	1	3.2
1	0	3.2
1	1	0

EX-OR GATE

CIRCUIT DIAGRAM :-



PIN CONFIGURATION :-



TRUTH TABLE :-

A	B	O/P: $Y = A \oplus B$	Logic Level
0	0	0	0
0	1	1	3.2
1	0	1	3.2
1	1	0	0

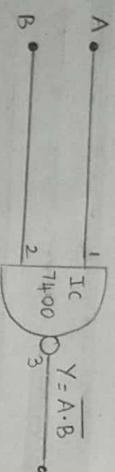
RESULT:-

Thus, the logic gates are constructed using IC chips and the corresponding truth table are verified.

NAND AS UNIVERSAL GATE

NAND GATE:

CIRCUIT DIAGRAM:

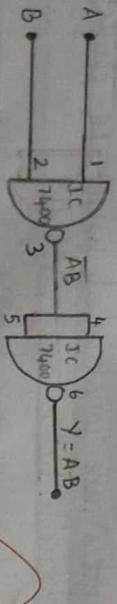


TRUTH TABLE:

		$Y = \overline{A \cdot B}$	
A	B	Logic Level	Voltage Level (V)
0	0	1	3.6
0	1	1	3.6
1	0	1	3.6
1	1	0	0

NAND AS AND GATE:

CIRCUIT DIAGRAM:



TRUTH TABLE:

		O/P: $Y = A \cdot B$	
A	B	Logic Level	Voltage Level (V)
0	0	0	0
0	1	X	3.1
1	0	-	3.1
1	1	1	3.1

Ex. No.: 05
12/11/2021

STUDY AS NAND, NOR GATES AS UNIVERSAL GATES

AIM:
To construct NAND, NOR as universal gates and verify the truth table.

APPARATUS REQUIRED:

Indicator board record, +5v power supply, Voltmeter, connecting wires, IC 7400 (NAND), IC 7402 (NOR), Volt ammeter (0-5V).

PROCEDURE:

NAND and NOR gates can be used to construct other logic gates.

NAND AS UNIVERSAL GATE

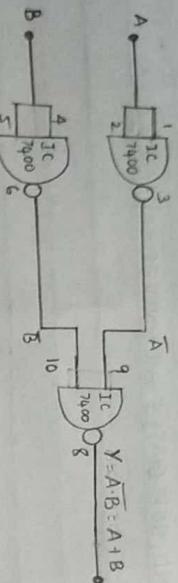
NAND AS AND GATE :

An AND gates can be made out of NAND gate the output of the first NAND gate is $\overline{A \cdot B}$, the second NAND gate then complimentary of a quantity itself. $\overline{\overline{A \cdot B}} = A \cdot B$. therefore NAND gate can be connected to perform and function.

OUTPUT : $Y = A \cdot B$

NAND AS OR GATE:

CIRCUIT DIAGRAM:

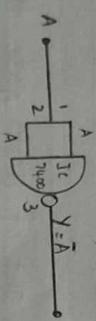


TRUTH TABLE:

		o/p : $Y = A + B$	
A	B	Logic Level	Voltage Level (V)
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	2.2

NAND AS NOT GATE:

CIRCUIT DIAGRAM:



TRUTH TABLE:

		o/p : $Y = \bar{A}$	
A		Logic Level	Voltage Level (V)
0		0	0
1		1	2.2

NAND AS NOT GATE:

The NAND gate can be made out of NAND gate by connecting all the inputs together. If A is zero to the output of the NAND gate is one. If A is one of the output of the NAND gate is zero.

$$\text{OUTPUT : } Y = \bar{\bar{A}}$$

NAND AS NOR GATE:

We can also make an OR gate using NAND gate. Since, the two NAND gate, then produce an output is $\bar{A}\bar{B}$. Since, the final output is A and B, we have shown that NAND gate OR function.

$$\text{OUTPUT : } Y = \bar{A} + \bar{B}$$

NAND AS NOR GATE:

The signal A is applied to one NAND gate and B to another which provided \bar{A} and \bar{B} at their gate output. They are applied to third NAND gate, whose output will be AB. This is set as input to the equivalent is $A + B$.

$$\text{OUTPUT : } Y = \bar{\bar{A}} + \bar{B}$$

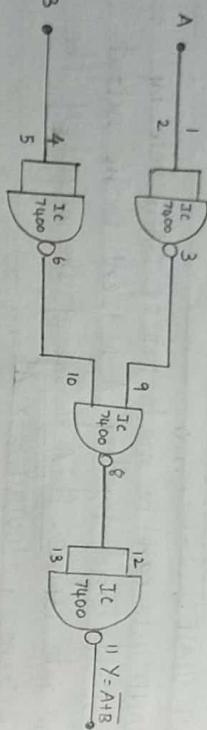
NAND AS EX-OR GATE:

The EX-OR gate has two inputs and one output. The logic of the EX-OR gate is verify using the observed for entry logic. The truth table drawn.

$$\text{OUTPUT : } Y = A \oplus B$$

NAND AS NOR GATE:

CIRCUIT DIAGRAM :-

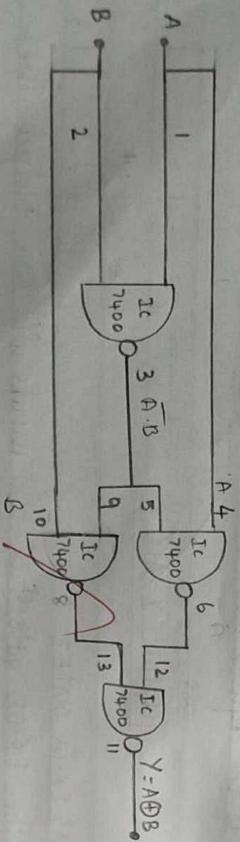


TRUTH TABLE:-

A	B	O/P : $Y = \overline{A+B}$
		Logic Level Voltage (V)
0	0	1
0	1	0
1	0	0
1	1	0

NAND AS EX-OR GATE:

CIRCUIT DIAGRAM:-



NOR AS NOT GATE :-
The NOT GATE has one input and output which denote the complement of the following input. The circuit is constructed as shown in figure the logic is checked using Input and output board and the truth table is verified.

OUTPUT : $Y = \bar{A}$

NOR AS UNIVERSAL GATE

NOR AS AND GATE :-
The AND GATE has two inputs and an output which denotes high only when inputs are high the logic

is verified and the truth table is drawn.

NOR AS OR GATE:

The OR gate has two inputs and an output. The output is high, if anyone of the inputs are high. If both the inputs are high, the output is also high.

OUTPUT : $Y = A + B$

NOR AS EX-OR GATE:-

The EX-OR gate has two inputs and an outputs. The logic of EX-OR gate is verified using input and output

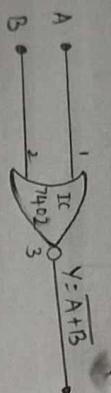
6

TRUTH TABLE :- [NAND AS EX-OR GATE]

		O/P :- $Y = A \oplus B$
A	B	Logic Level Voltage level(V)
0	0	0
0	1	3.6
1	0	3.6
1	1	0

NOR AS UNIVERSAL GATE

NOR GATE :
CIRCUIT DIAGRAM:



is board, the truth table is drawn and the output is verified.

OUTPUT :- $Y = A \oplus B$

NOR GATES AS NAND GATE :
A NAND gate is an AND gate followed by NOT gate. So connect the output of AND gate to a NOT gate, overall output is that of a NAND gate. To make a NOR gate perform the NAND function, we must invert all inputs to the NOR gate as well as the NOR gate's output. For a two - input gate, this requires three more NOR gates connected as inverters.

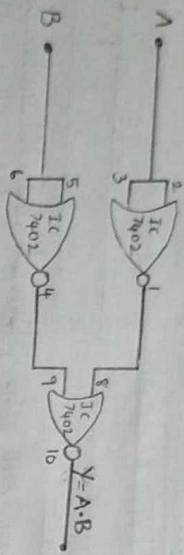
OUTPUT :- $Y = \overline{A \cdot B}$

TRUTH TABLE :

		O/P :- $Y = \overline{A \cdot B}$
A	B	Logic Level Voltage level(V)
0	0	4.2
0	1	0
1	0	0
1	1	0

NOR AS AND GATE :

CIRCUIT DIAGRAM :

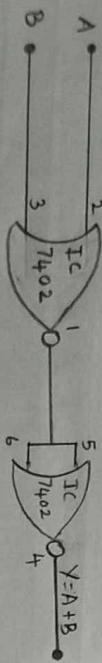


TRUTH TABLE :

A	B	O/P : $Y = A \cdot B$	Logic level	Voltage (V)
0	0	0	0	0
0	1	0	0	0
1	0	0	0	0
1	1	1	1	4.2

NOR AS OR GATE :

CIRCUIT DIAGRAM :



TRUTH TABLE :

A	B	O/P : $Y = A + B$	Logic level	Voltage (V)
0	0	0	0	0
0	1	1	1	4.2
1	0	1	1	4.2
1	1	1	1	4.2

NOR AS NOT GATE :

CIRCUIT DIAGRAM :

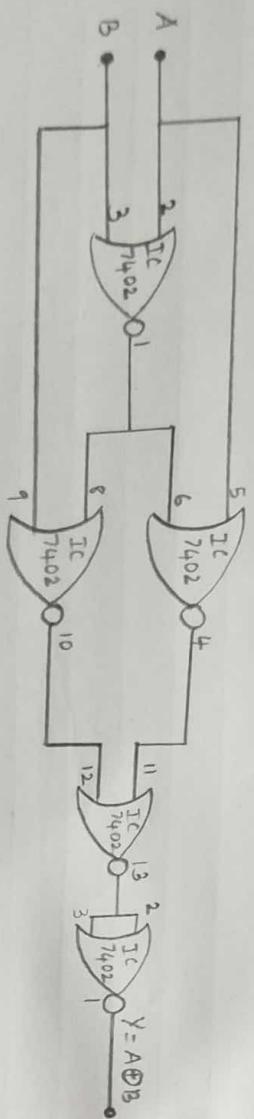


TRUTH TABLE:

A	O/P : $Y = \bar{A}$ Logic Level	Voltage Level (V)
0	1	4.2
1	0	0

NOR AS EX-OR GATE :

CIRCUIT DIAGRAM:



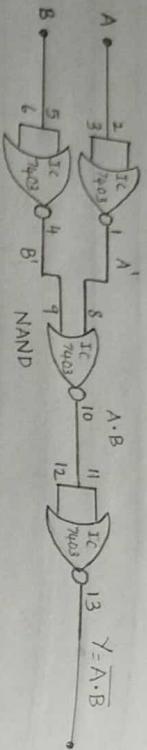
TRUTH TABLE:

A	B	O/P : $Y = A \oplus B$ Logic Level	Voltage Level (V)
0	1	1	3.2
1	0	1	3.2
0	0	0	0
1	1	0	0

NOR AS NAND GATE :

CIRCUIT DIAGRAM :

(10)



TRUTH TABLE :

A	B	O/P: $Y = \overline{A \cdot B}$	
A	B	Logic Level	Voltage Level (V)
0	0	1	4.2
1	0	1	4.2
0	1	1	4.2
1	1	0	0

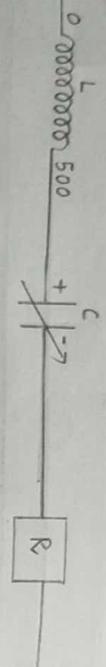
RESULT :

Thus, NAND, NOR as universal gate are constructed and their truth tables are verified.

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(4.2)

CIRCUIT DIAGRAM:-



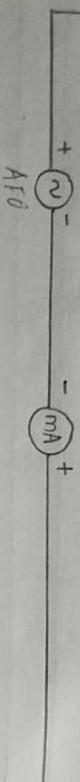
Ex. No.: 06

19/11/2021 LCR - SERIES RESONANCE CIRCUIT

AIM:-

To construct a series resonance circuit and to draw a curve of resonance circuit and to find the quality factor of the coil.

MODEL GRAPH:-



APPARATUS REQUIRED:-
Inductance coil, capacitance box, Resistance box, AC william -meter, AFC (Audio Frequency Oscillator), connecting wires, power supply

FORMULA:-

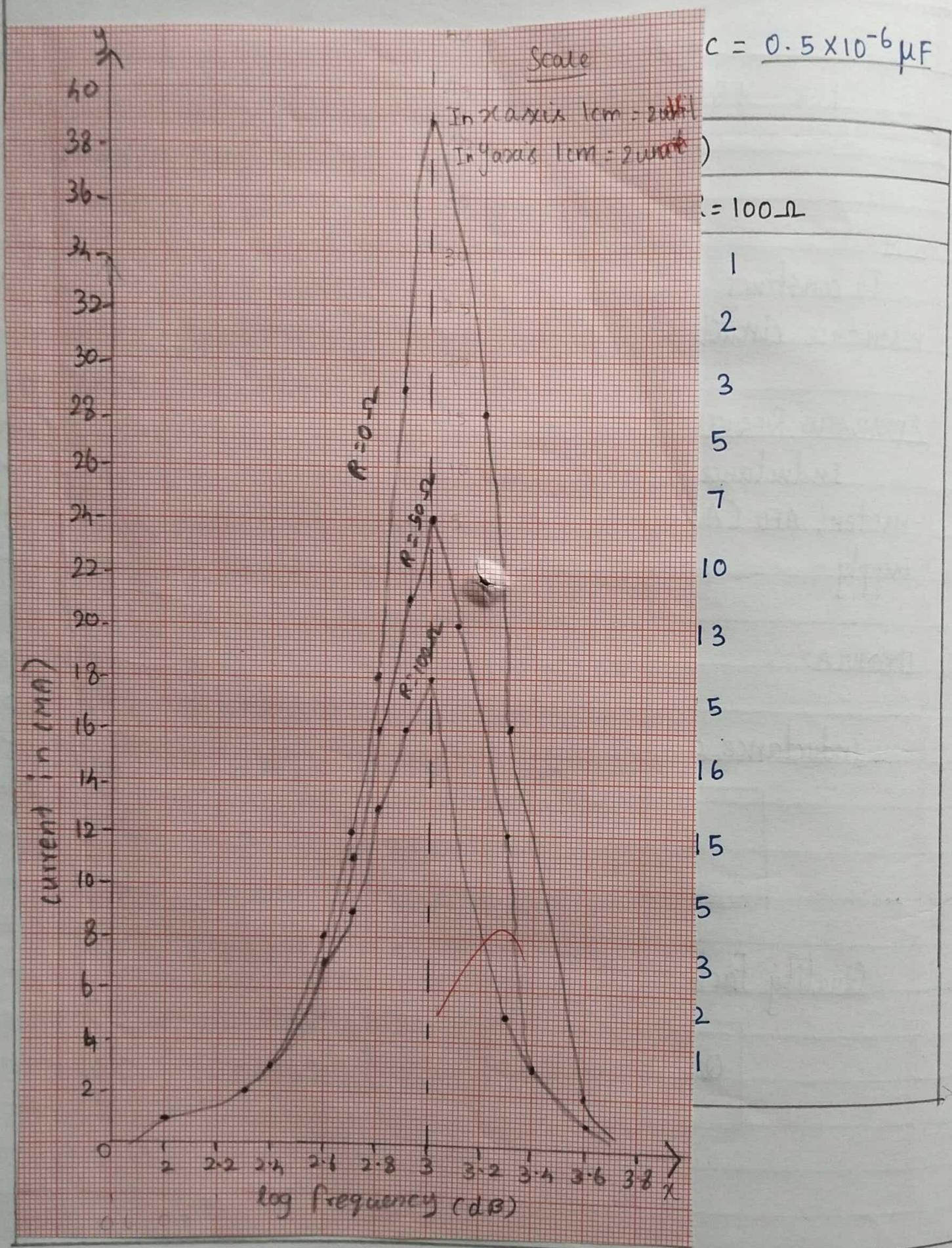
Inductance of the coil :-

$$L = \frac{1}{4\pi^2 f r^2} \text{ (Henry)}$$

Quality Factor of the coil :-

$$Q = \frac{L \times 2\pi \times f_r}{r} \text{ (No unit)}$$

TABULATION :



$$r = 10.9 \Omega$$

$$c = 0.5 \times 10^{-6} \mu F$$

Resonance Frequency :

$$f_r = \frac{1}{2\pi\sqrt{LC}} \text{ (Hz)}$$

PROCEDURE :

The connections are made as shown in the figure. A resistance in the circuit of 50Ω is included in the resistance box. The oscillation is switched on and the frequency is varied note down the a.c frequency. A graph is drawn by taking frequency of ac inputs. The frequency corresponding to the maximum current reading is bound to be the resonance frequency. The experiment is repeated for different values.

In the formula Inductance, Quality factor and Resonance frequency of the coil.

where,

L = Inductance of a coil (Henry)

C = Capacitance of a coil (μF) as condenser (μF)

r = Resistance of a Inductance (ohm)

f_r = Resonance Frequency (Hz)

Q = Quality factor of the coil (No unit)

Frequency (Hz)	Log Frequency (dB)	Current in (mA)			Resonance Frequency (Hz)
		R = 0Ω	R = 50Ω	R = 100Ω	
100	2	1	1	1	
200	2.3010	2	2	2	
300	2.4771	3	3	3	
400	2.6020	5	5	5	
500	2.6989	8	7	7	
600	2.778	12	11	10	
700	2.845	18	16	13	
800	2.903	29	21	15	
900	2.9542	39	24	16	
1000	3	28	20	15	
2000	3.3010	6	6	5	
3000	3.4771	3	3	3	
4000	3.6020	2	2	2	
5000	3.6989	1	1	1	

CALCULATION:

Inductance of the coil :

$$L = \frac{1}{4\pi^2 f_r^2 C} \text{ Henry} = \frac{1}{4(3.14)^2 (900)^2 \times 0.5 \times 10^{-6}}$$

$$= \frac{1}{39.4384 \times 810000 \times 0.5 \times 10^{-6}}$$

$$L = 0.0626 \text{ Henry}$$

Quality factor of the coil :

$$Q = \frac{L \times 2\pi \times f_r}{Y} \text{ (No unit)}$$

$$= \frac{0.0626 \times 2 \times 3.14 \times 900.053}{10.6}$$

$$Q = 33.3808 \text{ (No unit)}$$

Resonance frequency :

$$f_r = \frac{1}{2\pi\sqrt{LC}} \text{ Hz}$$

$$= \frac{1}{2 \times 3.14 \sqrt{0.0626 \times 0.5 \times 10^{-6}}} \text{ Hz}$$

$$f_r = 900.053 \text{ Hz}$$

RESULT:

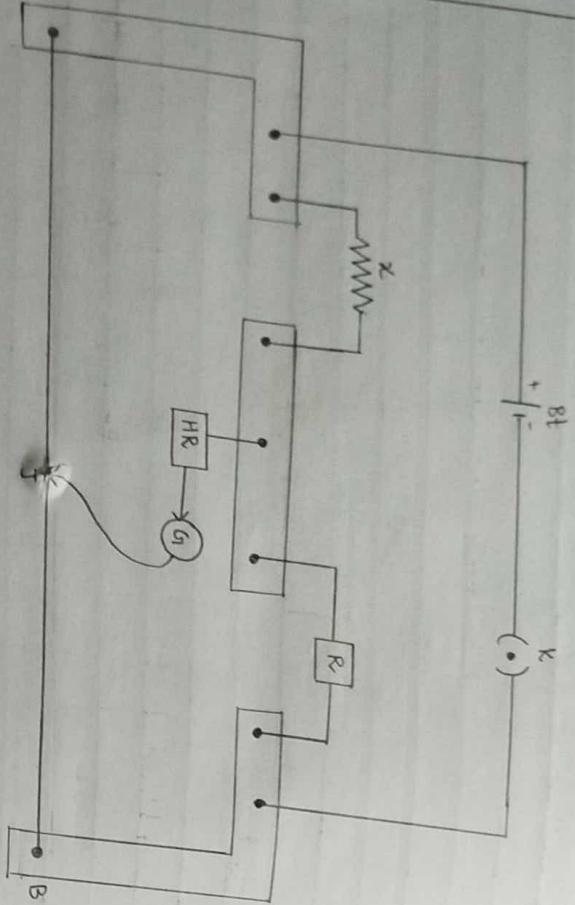
The series resonance circuit is constructed and the resonance curve is drawn and the quality factor of the coil is found.

1.) Inductance of the coil $L = 0.0626 \text{ Henry}$

2.) Quality Factor of the coil $Q = 33.3808 \text{ (No unit)}$

3.) Resonance frequency $f_r = 900.053 \text{ Hz}$

CIRCUIT DIAGRAM:



Ex. No.: 07
06/12/2021

METER BRIDGE - DETERMINATION OF SPECIFIC RESISTANCE

AIM:

To determine the resistance of a given coil of the wire and calculate the specific resistance of the material of the wire.

APPARATUS REQUIRED:

Meterbridge, resistance box, jockey, galvanometer, high resistance, plug key, coil of wire, Lechalanche cell, battery, power supply, unknown resistance.

FORMULA:

The Specific resistance of the given coil of the wire :

$$\rho = \frac{\pi r^2 \alpha}{l} (\Omega/m)$$

where,

r = Radius of the given coil of the wire (m)

α = Resistance of the given coil of the wire (Ω)

ρ = Specific resistance of the given material of the given coil of wire (Ω/m)

l = Length of the given coil of the wire (m)

TABULATION - I

To find the resistance of the given coil of the wire

$$l_2 = \frac{100 - l_1}{2} \quad x = \frac{3.2415}{l_2} \Omega$$

R (Ω)	x in left gap $x_1 = R(l_1/l_2)$	x in right gap $x_2 = R(l_2/l_1)$		
l_1 (m)	l_2 (m)	l_1 (m)	l_2 (m)	C (Ω)
3.0	48.5	51.5	2.8252	58.4
3.1	49.2	50.8	3.002	51.5
3.2	50	50	3.2	48.5
3.3	51.2	48.8	3.462	49.3
3.4	52.6	47.4	3.772	48.8
			$x_1 = 3.2522$	51.2
				3.4622
				3.752
			$x_2 = 3.2308$	

PROCEDURE:

A resistance box is connected in the right gap and the given coil of the wire of the unknown resistance x in the left gap Lechalanche cell is connected in the A & B of the Bridge wire through a plug key in one terminal of the high resistance is connected in the middle strip and the other terminal to the jockey through the galvanometer.

A suitable resistance say 5 ohms introduced in the resistance box and the circuit is closed the jockey is pressed near A and then near B. If the deflection are in the opposite direction the corrections are corrects.

The jockey is now pressed at the middle of the bridge wire at the metre axis if the resistance in R is adjusted until the deflection in the galvanometer is almost zero, the value of three given of the resistance in the resistance box should be around this value.

The jockey along the wire and the balance point T for which there is no deflection in the galvanometer is found the new balance length AT and BJ are measured as l_1 and l_2 respectively.

Then,

$$\frac{x}{R} = \frac{l_1}{l_2}$$

$$x = R \frac{l_2}{l_1}$$

The experiment is repeated for two or more value of R .

TABULATION-II

To find the radius of the wire using screw gauge.

$$L_C = \frac{0.01 \text{ mm}}{100 \times 10^{-2} \text{ m}}$$

$$Z_e = -\frac{1}{4} \text{ div}$$

$$L = \frac{100 \times 10^{-2}}{\text{div}}$$

$$Z_C = +\frac{1}{\text{div}}$$

Pitch Scale Reading ($\times 10^{-3}$ mm)	Head Scale (Co-incidence div (HSC) X mm)	$OR = PSR \pm (HSC \times \frac{L_C}{10^{-3} \text{ m}}) \times 10^{-3} \text{ m}$	$LR = OR \pm (Z_C \times L_C) \times 10^{-3} \text{ m}$
0	54	0.54	0.58
0	55	0.55	0.59
0	55	0.55	0.59
0	53	0.53	0.57

Then,

$$\frac{x}{R} = \frac{l_2}{l_1}$$

$$x = R \frac{l_2}{l_1}$$

The reading are tabulated and the mean value of x is found. The determine the specific resistance of the given wire the length L of the given wire is measured the radius of the wire is found with a screw gauge by measuring it at various point along the wire.

The specific resistance ρ of the material of the wire is calculated from the relation.

$$\rho = \frac{\pi r^2 x}{l} (\Omega \text{m})$$

$$r = 0.291 \times 10^{-3} \text{ m}$$

$$d = \frac{2.33}{4}$$

$$\frac{d}{2} = \frac{0.5825}{2}$$

Now x and R interchanged and now balance point J is found. The balance point J is founded. The Balance length AJ and JB are measured as l_1 and l_2 respectively.

CALCULATION :-

$$l = 100 \times 10^{-2} \text{ m}$$

$$r = 0.291 \times 10^{-3} \text{ m}$$

$$\chi = 3.2415 \Omega$$

$$\rho = \frac{\pi r^2 \chi}{l} (\Omega \text{m})$$

$$\rho = \frac{3.14 \times (0.29 \times 10^{-3})^2 \times 3.2415}{100 \times 10^{-2}}$$

$$\rho = \frac{86.1909 \times 10^{-7}}{100}$$

$$\rho = 8.61 \times 10^{-7} \Omega \text{m}$$

RESULT :-

1.) Resistance of the given coil of the wire :- $\chi = 3.2415 \Omega$

2.) The specific resistance of the given coil of the wire :-

$$\rho = 8.61 \times 10^{-7} \Omega \text{m}$$