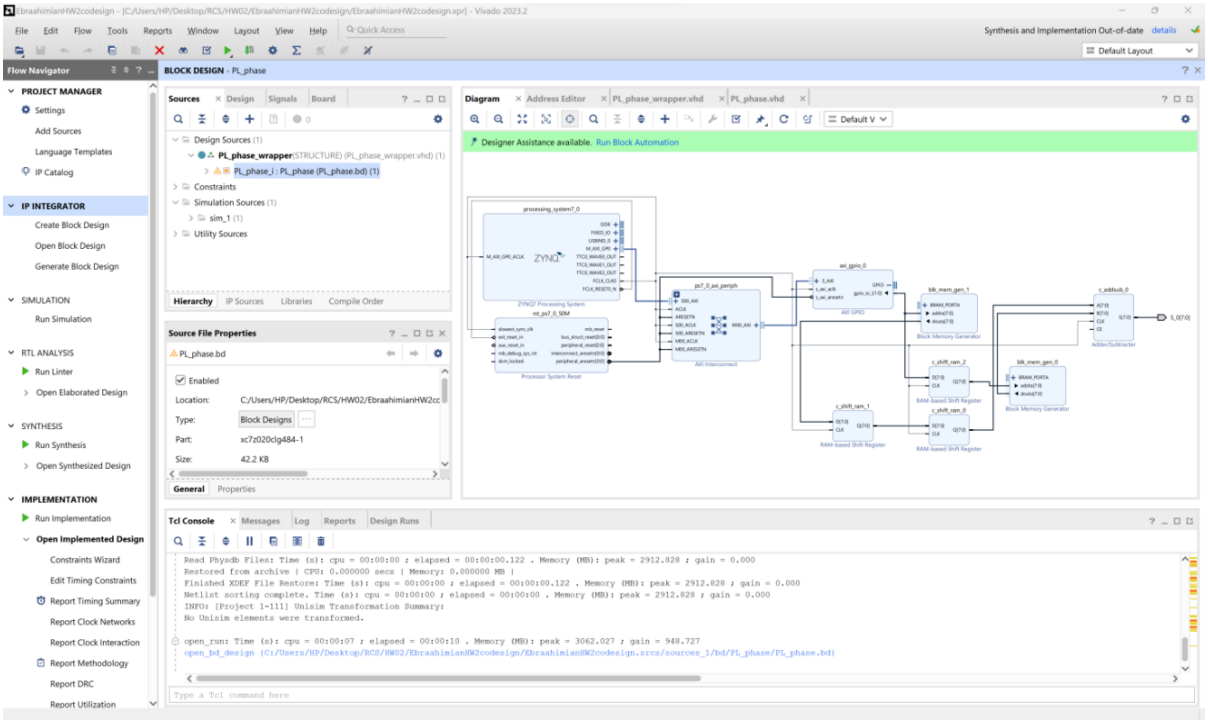
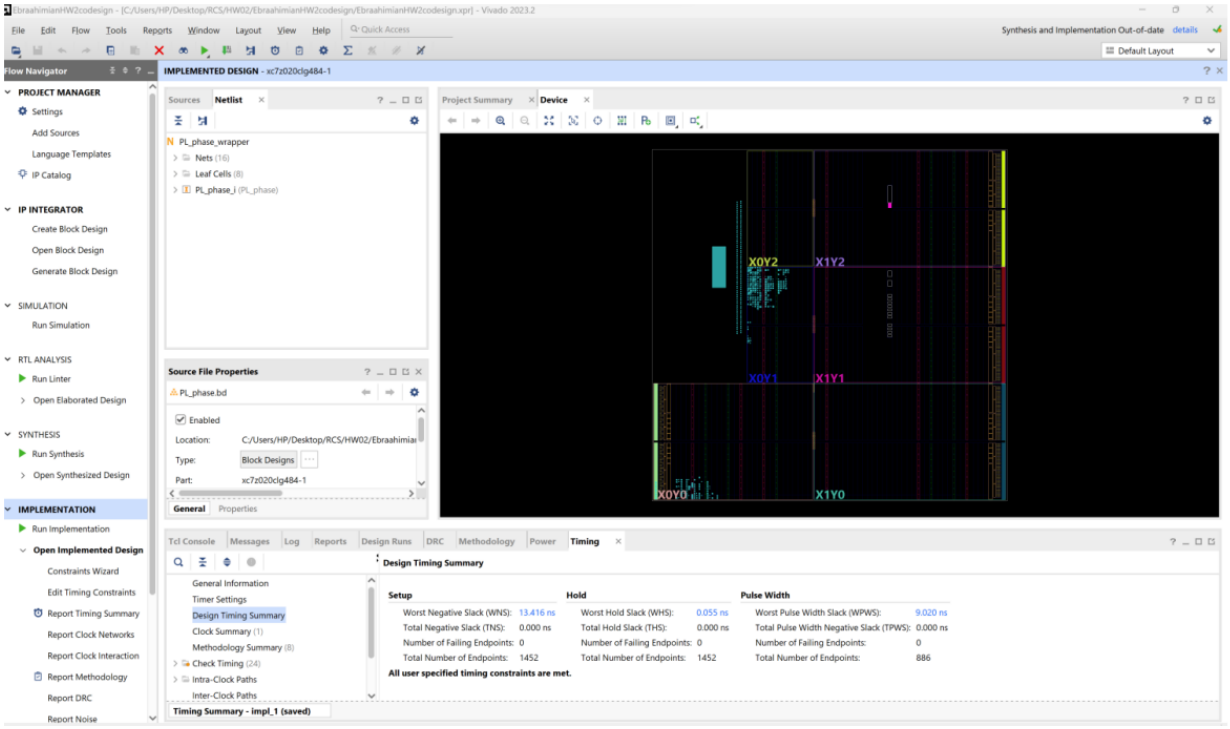
The goal of the task is to **implement an operation that includes multiplication** by 2 (left shift) along with an Integer adder. The system's display should be capable of showing 6 digits with an optionally displayable decimal point. To achieve the display of the value **4× sin ($x$)+sin (2$x$)** where $x$ is an input to the system ranging from 0 to 180, a specific approach must be followed. The implementation of these steps has been carried out in two ways:

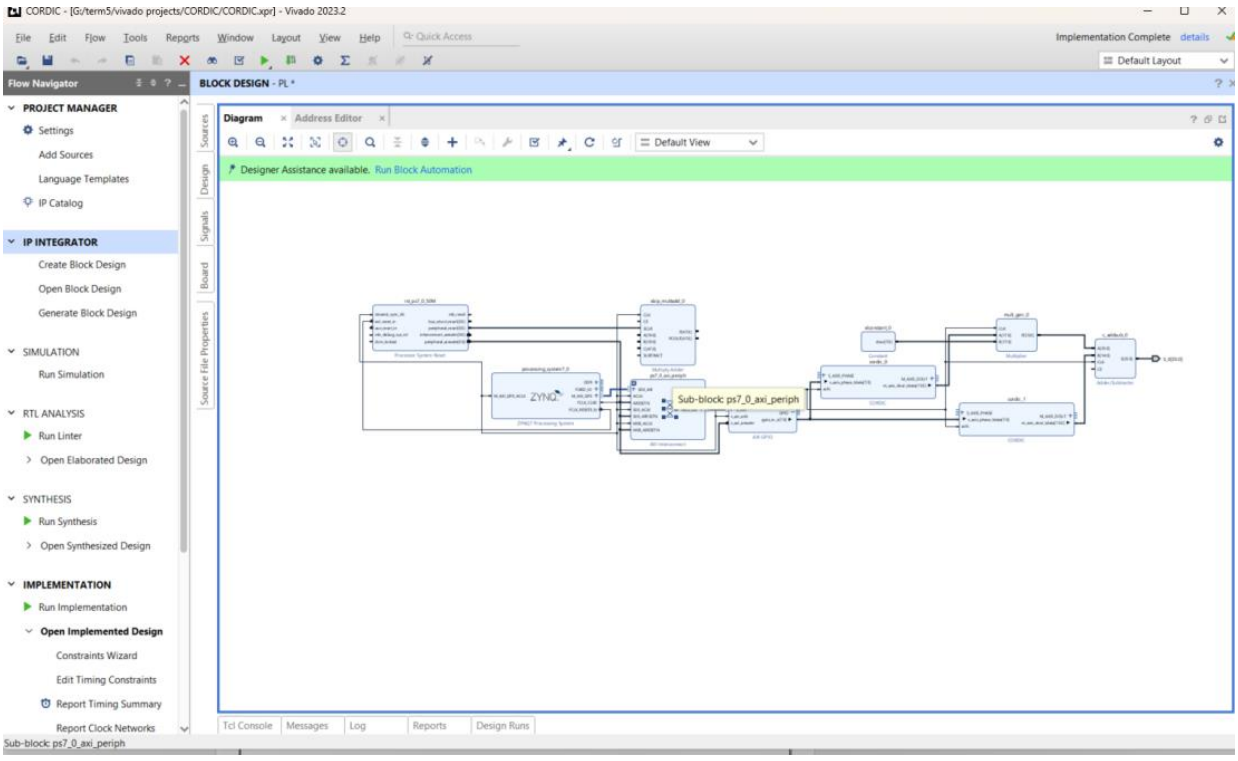
1. Through register shifting, memory blocks, and an adder.

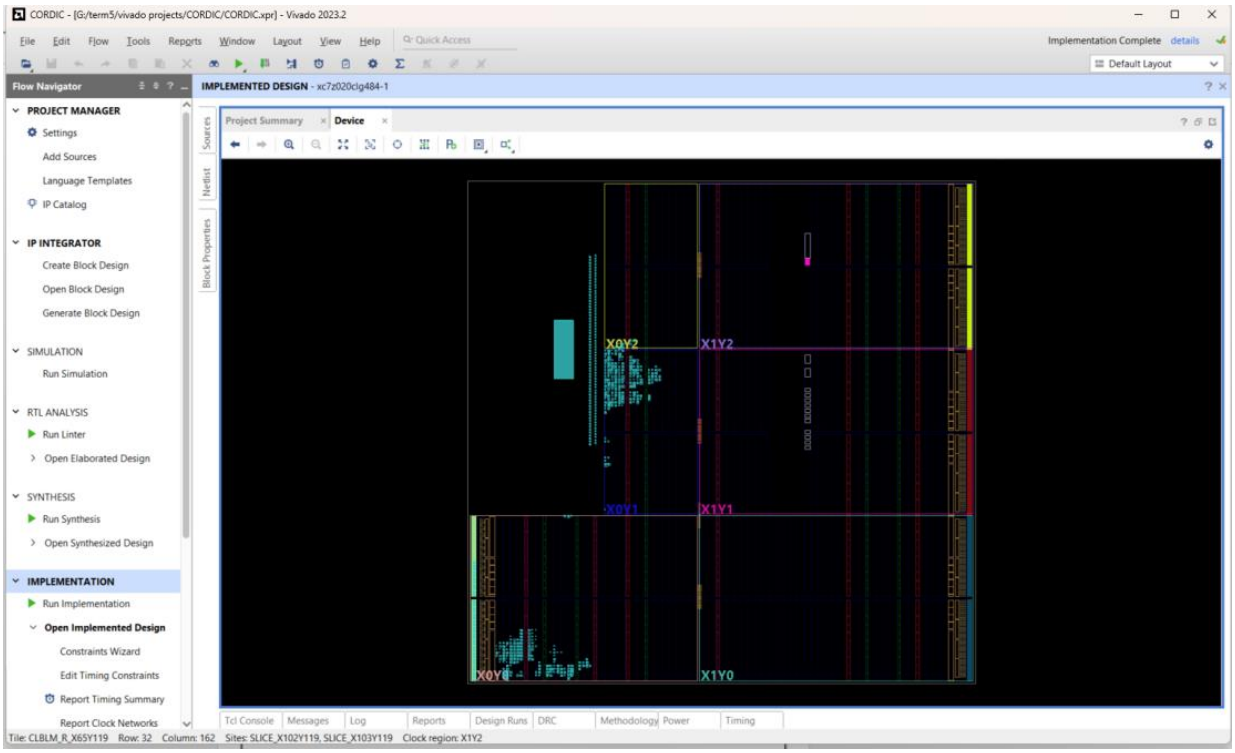
2. Through a CORDIC block, a multiplier, a fixed input value, and an adder.

Initially, a **7000 Zynq board was created**, followed by the creation of a GPIO AXI and establishing the necessary connections. Then, an 8-bit memory block was created, and a connection was made between the shift registers. Subsequently, two serial shift registers were used to perform the multiplication by 4. Finally, the two obtained values were fed into the inputs of the adder. In the first approach, the system uses register shifting and memory blocks to perform the required calculations. By implementing an 8-bit memory block and connecting it with shift registers, multiplication is efficiently executed through shift operations. The values obtained from these shifts are then summed using an Integer adder.




Flow Navigator
IMPLEMENTED DESIGN - xc7z020clg484-1
PROJECT MANAGER
IP INTEGRATOR
SIMULATION
RTL ANALYSIS
SYNTHESIS
IMPLEMENTATION
Sources
Netlist
PL_phase_wrapper
Nets (16)
Leaf Cells (8)
PL_phase_i (PL_phase)
Source File Properties
PL_phase.bd
Enabled
Location: C:/Users/HP/Desktop/RCS/HW02/EbraahimiaI
Type: Block Designs
Part: xc7z020clg484-1
General
Properties
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Methodology Summary (8)
Check Timing (24)
Intra-Clock Paths
Inter-Clock Paths
Setup
Worst Negative Slack (WNS): 13.416 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 1452
Hold
Worst Hold Slack (WHS): 0.055 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 1452
Pulse Width
Worst Pulse Width Slack (WPWS): 9.020 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 886
All user specified timing constraints are met.
Timing Summary - impl_1 (saved)


CORDIC - [G:/term5/vivado projects/CORDIC/CORDIC.xpr] - Vivado 2023.2
Implementation Complete
Flow Navigator
BLOCK DESIGN - PL *
PROJECT MANAGER
IP INTEGRATOR
SIMULATION
RTL ANALYSIS
SYNTHESIS
IMPLEMENTATION
Diagram
Address Editor
Default View
Designer Assistance available. Run Block Automation
Sub-block: ps7_0_axi_periph
Tcl Console
Messages
Log
Reports
Design Runs
Sub-block: ps7_0_axi_periph


CORDIC - [G:/term5/vivado projects/CORDIC/CORDIC.xpr] - Vivado 2023.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete details
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7z020clg484-1
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Project Summary
Device
Sources
Netlist
Block Properties
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Tile: CLBLM_R_X65Y119 Row: 32 Column: 162 Sites: SLICE_X102Y119, SLICE_X103Y119 Clock region: X1Y2