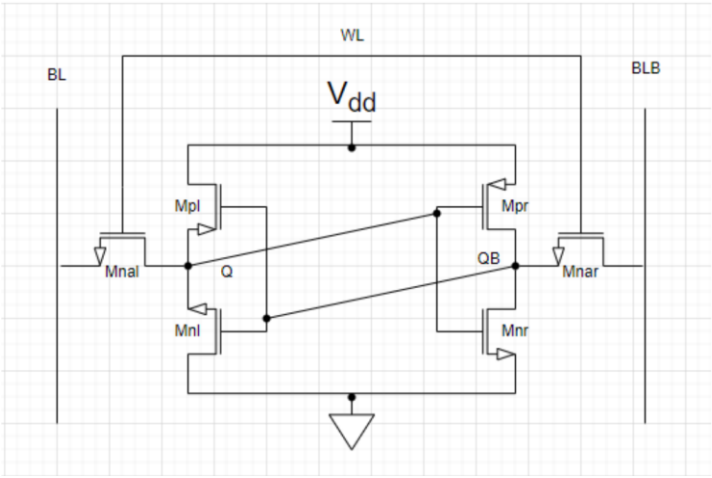
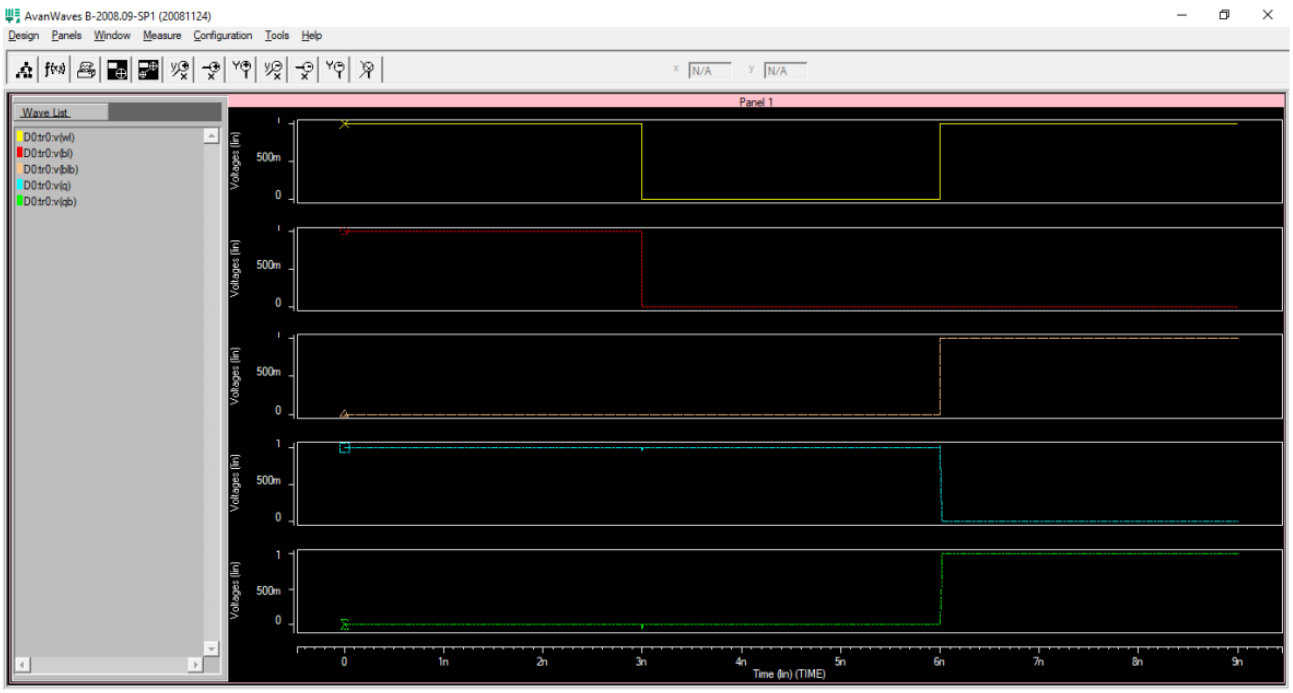
The simulation of the 6T/10T-SRAM cell in HSPICE

An image of the designed circuit with the names of the nodes and the size of the transistors (6T):



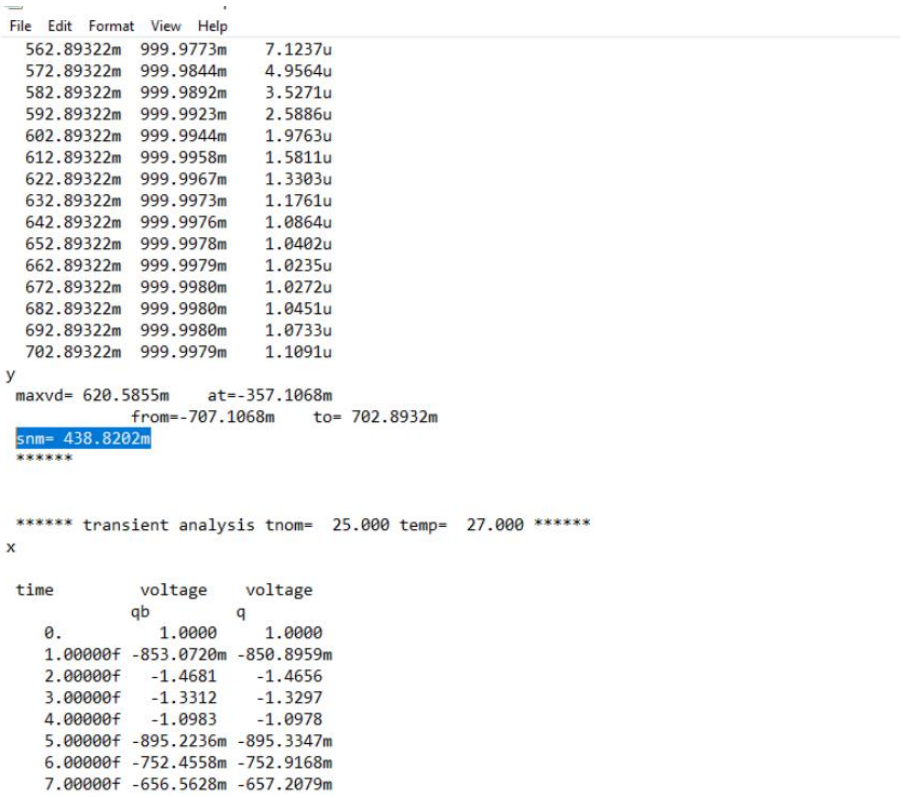
Images showing the correctness of the operation (waveforms) are required as part of the response for this step.



The noise margin of an SRAM cell, or SNM, indicates the sensitivity of an SRAM cell to noise. SNM is defined as the difference between the minimum amount of electric charge required to retain a bit in the SRAM cell and the amount of injected electric charge that can cause the cell to change state. Based on this definition, the following formula can be used to calculate the SNM of an SRAM cell in general:

$$SNM = \frac{(V_{min} - V_m)}{\sigma}$$

In this formula, V_{min} is the minimum bitline voltage that can maintain the electric charge on the cell, and V_m is the average bitline voltage calculated based on the cell's state. Additionally, σ represents the standard deviation of the bitline voltage. According to this formula, SNM is maximized when V_m is equal to 0.5 V_{min}, meaning the average bitline voltage is half of the minimum bitline voltage.



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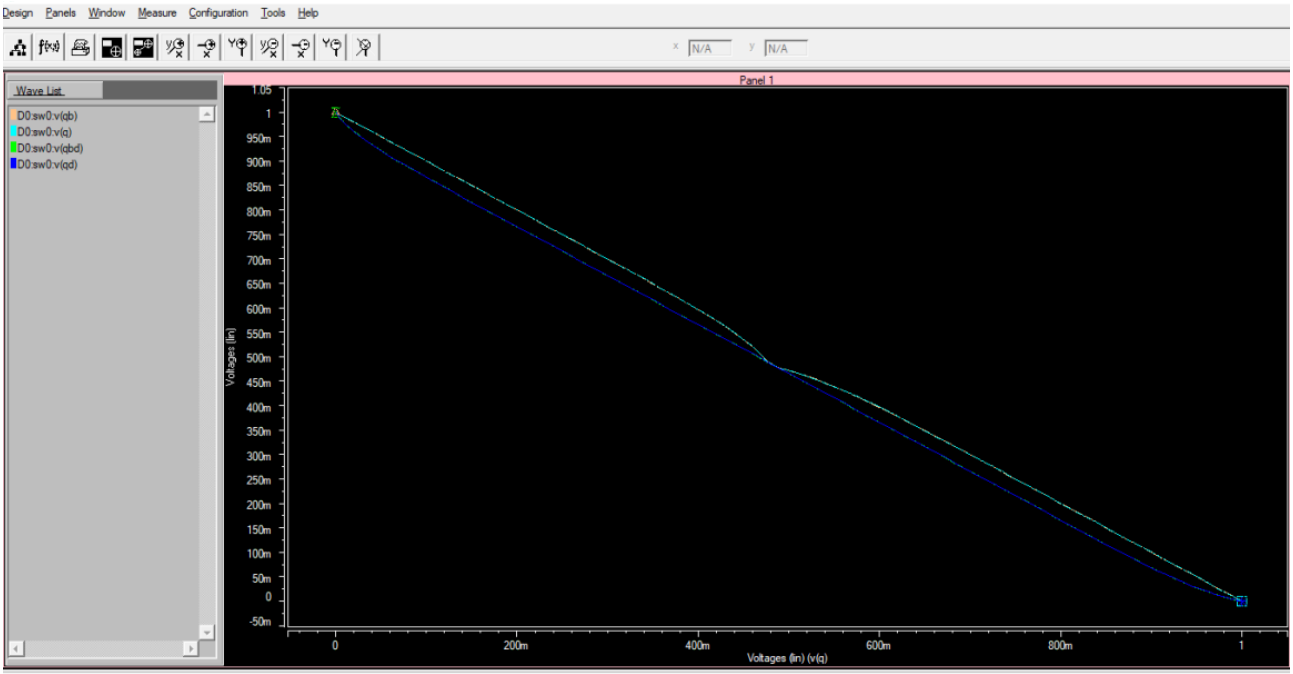
File  Edit  Format  View  Help
  562.89322m  999.9773m    7.1237u
  572.89322m  999.9844m    4.9564u
  582.89322m  999.9892m    3.5271u
  592.89322m  999.9923m    2.5886u
  602.89322m  999.9944m    1.9763u
  612.89322m  999.9958m    1.5811u
  622.89322m  999.9967m    1.3303u
  632.89322m  999.9973m    1.1761u
  642.89322m  999.9976m    1.0864u
  652.89322m  999.9978m    1.0402u
  662.89322m  999.9979m    1.0235u
  672.89322m  999.9980m    1.0272u
  682.89322m  999.9980m    1.0451u
  692.89322m  999.9980m    1.0733u
  702.89322m  999.9979m    1.1091u
y
 maxvd= 620.5855m    at=-357.1068m
            from=-707.1068m    to= 702.8932m
 snm= 438.8202m
 ******

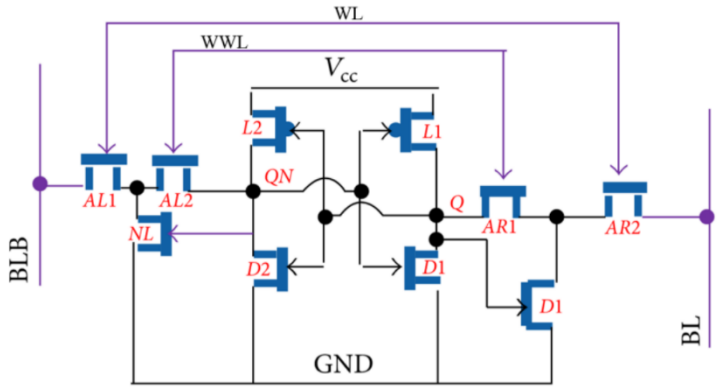

 ****** transient analysis tnom=  25.000 temp=  27.000 ******
x

 time         voltage    voltage
             qb         q
    0.          1.0000     1.0000
   1.00000f -853.0720m -850.8959m
   2.00000f   -1.4681    -1.4656
   3.00000f   -1.3312    -1.3297
   4.00000f   -1.0983    -1.0978
   5.00000f -895.2236m -895.3347m
   6.00000f -752.4558m -752.9168m
   7.00000f -656.5628m -657.2079m
```

The **butterfly** diagram corresponding to the simulation:



An image of the designed circuit with the names of the nodes and the size of the transistors (10T):



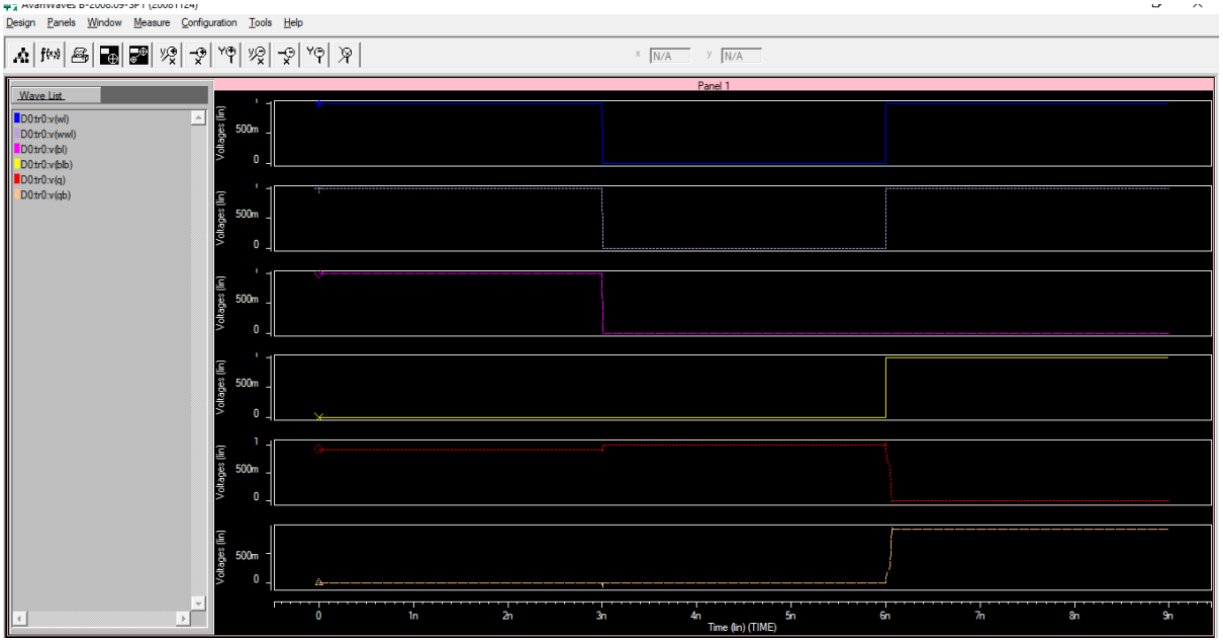
Read Mechanism of a 10-Transistor SRAM Cell

- To read data, first activate the wordline.

- Then, activate the bitline corresponding to the bits you want to read.
- At this stage, some of the main transistors of the cell are activated, and the electric charge is transferred from the main transistors through the access transistors to the bitline.
- The electric charge on the bitline is measured using a voltage sensor. The value of this voltage depends on the amount of data stored in the cell.
- To preserve the data, the electric charge on the bitline must be refreshed after reading. This is done by reactivating the wordline and updating the bitline corresponding to the bits that need refreshing.
- Once the reading and data refresh process is complete, the cell is ready for the next read operation.

Write Mechanism of a 10-Transistor SRAM Cell

- To write data, first activate the wordline.
- The data to be written is transferred to the cell via the corresponding bitline.
- Then, by changing the state of the bitline corresponding to the bits to be updated, the electric charge is transferred to the cell through the access transistors.
- To preserve the data, the electric charge on the bitline must be correctly set. This is done by adjusting the bitline state so that the electric charge on the bitline exceeds a certain threshold, thereby updating the data in the cell.
- To store the data, the enable line of the cell must be deactivated.
- Once the data write process is complete, the cell is ready for the next write operation.



Butterfly diagram 10T**:**