

MCKV INSTITUTE OF ENGINEERING



Estd. 1999

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Laboratory Instruction Sheets

Digital Electronics Laboratory

ES-EC392

MCKV INSTITUTE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Digital Electronic Laboratory ES-EC392

Experiment No. 1: Realization of Basic gates (AND,OR,NOT) from Universal Gates(NAND & NOR).

Objectives: To realize the operation of basic gates(AND,OR,NOT) using Universal logic gates.

Theory:

Universal Gates

A universal gate is a gate which can implement any Boolean function without need to use any other gate. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

NAND Gate

The NAND gate represents the complement of the AND operation. Its name is an abbreviation of NOT AND. The symbol for the NAND gate consists of an AND symbol with a bubble on the output, denoting that a complement operation is performed on the output of the AND gate.



NAND		
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

The NOR gate represents the complement of the OR operation. Its name is an abbreviation of NOT OR. The symbol for the NOR gate consists of an OR symbol with a bubble on the output, denoting that a complement operation is performed on the output of the OR gate.



NOR		
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

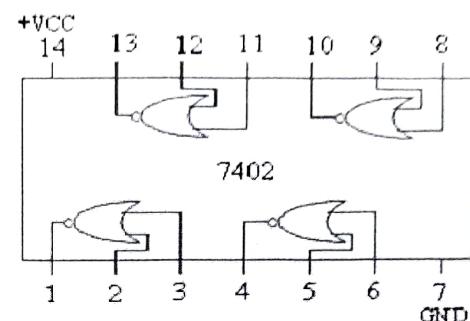
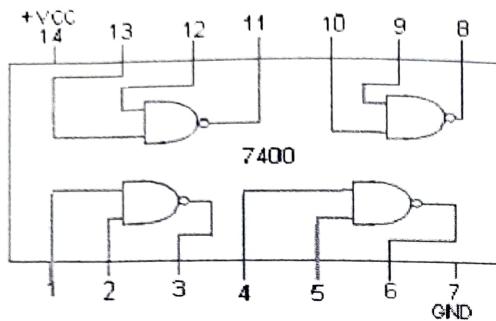
Truth tables :

NOT	
A	Y
0	1
1	0

OR		
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

AND		
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Internal Configuration of IC's 7400 and 7402:

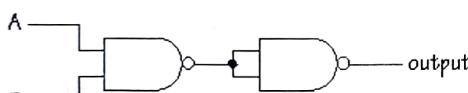


Circuit Diagram :

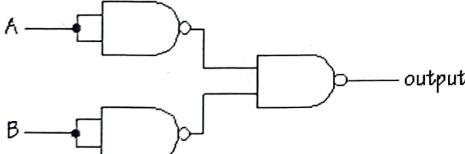
NOT gate



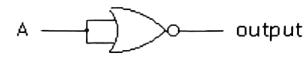
AND gate



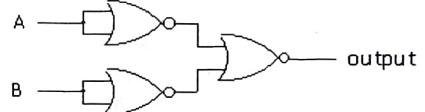
OR gate



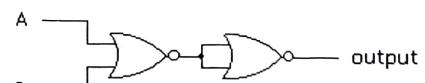
NOT gate



AND gate



OR gate



Equipments Required:

1. Bread board.
2. +5 volt dc supply.
3. Connecting wires.
4. Components.
 - a. IC's - 7400, 7402.
 - b. Resistors.
 - c. LED's.

Experimental Procedure :

1. Low levels refer to 0 volt and high voltage refers to +5 volt.
2. Verify the truth table.

Results/Observations: All the truth tables are verified experimentally.

Remarks :

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Experiment No. 2: Implementation of the given Boolean function using logic gates in both SOP and POS forms.

Objectives: To Implement the given Boolean function using logic gates in both SOP and POS forms.

- i) $AB+BC$
- ii) $(A+B).(B+C)$

Theory:

Sum Of Products Form (SOP):

The **sum-of-products** (SOP) form is a method (or form) of simplifying the Boolean expressions of logic gates. In this SOP form of Boolean function representation, the variables are operated by AND (product) to form a product term and all these product terms are ORed (summed or added) together to get the final function. Each ANDed term in SOP form is called Minterm.

Product Of Sum Form (POS):

The product of sums form is a method (or form) of simplifying the Boolean expressions of logic gates. In this POS form, all the variables are ORed, i.e. written as sums to form sum terms. All these sum terms are ANDed (multiplied) together to get the product-of-sum form. This form is exactly opposite to the SOP form. So this can also be said as "Dual of SOP form". Each ORed term in POS form is called Maxterm.

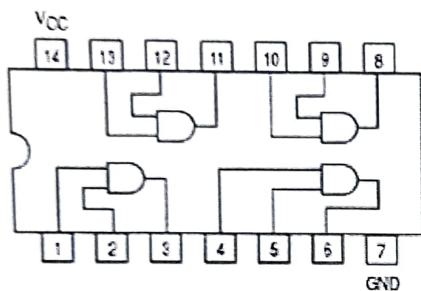
Truth tables :

A	B	C	$Q=AB+BC$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

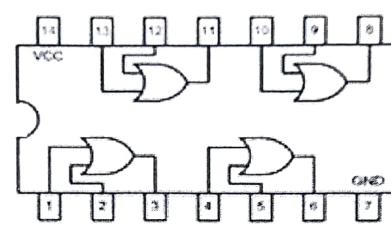
(5)

A	B	C	$Q = (A+B)(B+C)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Internal Configuration of IC's 7408 and 7432:

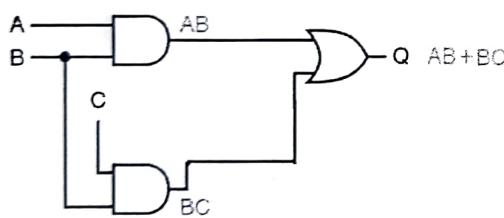


IC 7408

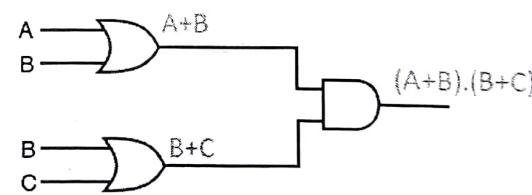


IC 7432

Circuit Diagram :



SOP Form



POS Form

Equipments Required:

1. Bread board.
2. +5 volt dc supply.
3. Connecting wires.
4. Components.
 - a. IC's - 7408, 7432.
 - b. Resistors.
 - c. LED's.

Experimental Procedure :

1. Low levels refer to 0 volt and high voltage refers to +5 volt.
2. Verify the truth table.

Results/Observations: All the truth tables are verified experimentally.

Remarks :

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Experiment No 3: Design and Verify Adder, Subtractor circuit.

Objective: To construct simple arithmetic circuits-Adder, Subtractor.

Theory:

HALF ADDER- adder takes two inputs A and B and produces a sum S bit and a carry out bit. This operation is called half addition and the circuit to realize it is called a half adder.

FULL ADDER- full adder takes two inputs A and B and a Carry input and produces the Sum and Carry outputs.

HALF SUBTRACTOR- subtracting a single-bit binary value B from another A (I.e. A -B) produces a difference bit D and a borrow out bit B-out. This operation is called half subtraction and the circuit to realize it is called a half subtractor.

FULL SUBTRACTOR- subtracting two single-bit binary values, B, BORin from a single-bit value A produces a difference bit D and a borrow out BORout bit.

Truth Table:

HALF ADDER

INPUT		OUTPUT	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

HALF SUBTRACTOR

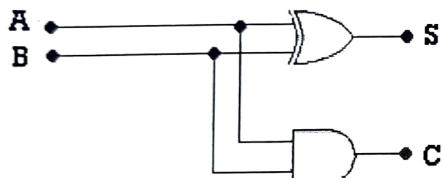
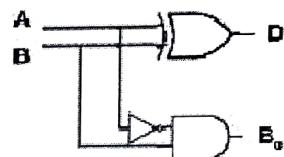
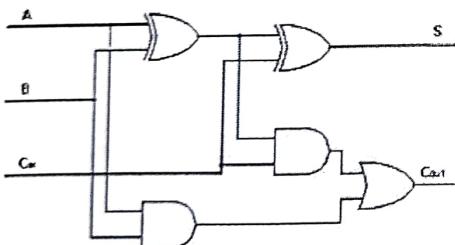
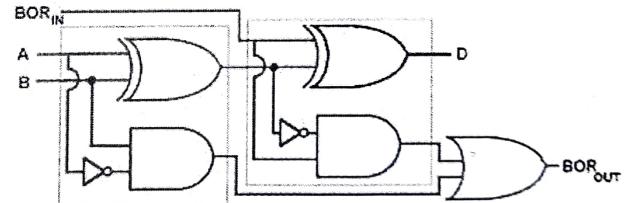
INPUT		OUTPUT	
A	B	D	B _o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

FULL ADDER

INPUT			OUTPUT	
A	B	C _{in}	S	C _{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL SUBTRACTOR

INPUT			OUTPUT	
A	B	BOR _{in}	D	BOR _{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Circuit Diagram:Half AdderHalf SubtractorFull AdderFull SubtractorEquipments Required:

1. Bread Board
2. + 5V supply
3. Connecting wires.
4. Components
 - a) IC's 7486, 7408, 7404, 7432
 - b) Resistors
 - c) LED's

Experimental Procedure:

1. Simplify the truth table and get the Boolean function to design the circuit using Karnaugh map.
2. Set up the circuit, apply the inputs and observe the output.
3. Verify the operation of the circuit.
4. Low levels refer to 0 volt and high voltage refers to +5 volt.

Result/Observation: All the truth tables are verified experimentally.

Remarks:

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Experiment No. 4 : Implementation and Verification of Decoder, Encoder, Multiplexer, Demultiplexer Circuit

Objective: To implement and verify simple Decoder, Encoder, Multiplexer and Demultiplexer.

Theory:

Decoder:

A n-to- 2^n decoder takes an n-bit input and produces 2^n outputs. The n inputs represent a binary number that determines which of the 2^n output is uniquely true. Decoders are simply a collection of logic gates which are arranged in a specific way so as to breakdown any combination of inputs to a set of terms that are all set to '0' apart from one term.

Encoder:

The decimal to binary encoder usually consists of 10 input lines and 4 output lines. Each input line corresponds to the each decimal digit and 4 outputs correspond to the BCD code. This encoder accepts the decoded decimal data as an input and encodes it to the BCD output which is available on the output lines.

Multiplexer:

A multiplexer, abbreviated mux, is a device that has multiple inputs and one output. A data selector, more commonly called a Multiplexer. They connect or control, multiple input lines called "channels" consisting of either 2, 4, 8 or 16 individual inputs, one at a time to an output. Multiplexers are used as one method of reducing the number of logic gates required in a circuit or when a single data line is required to carry two or more different digital signals.

Generally, multiplexers have an even number of data inputs (2^n), a number of select lines (n) that correspond with the number of data inputs and according to the binary condition of these select lines, the appropriate data input is connected directly to the output.

Demultiplexer:

The process of getting information from one input and transmitting the same over one of many outputs is called Demultiplexing. If you recall the Multiplexer tutorial, there we discussed the concept of Multiplexing. Demultiplexing is just the opposite of that. A Demultiplexer is a combinational logic circuit that receives the information on a single input line and transmits the same information over one of 'n' possible output lines. In order to select a particular output, we have to use a set of Select Lines and the bit combinations of these select lines control the selection of specific output line to be connected to the input at a given instant.

Truth Table:

Decoder (2:4)

INPUT		OUTPUT			
X	Y	B ₀	B ₁	B ₂	B ₃
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Multiplexer (2:1)

Select line	Output
S	Y
0	I ₀
1	I ₁

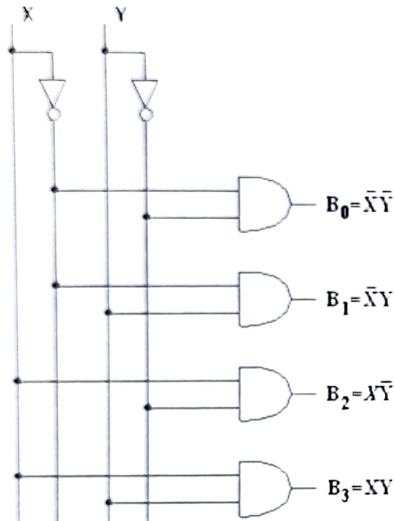
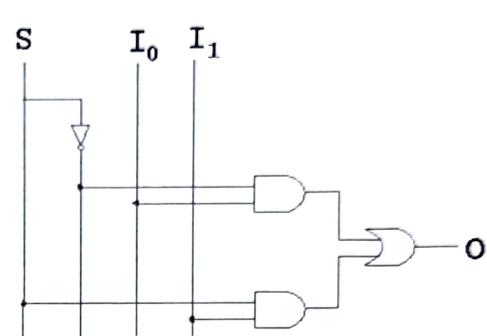
$$Y = S'I_0 + SI_1$$

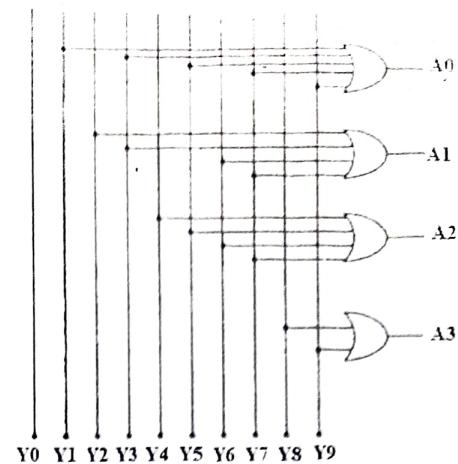
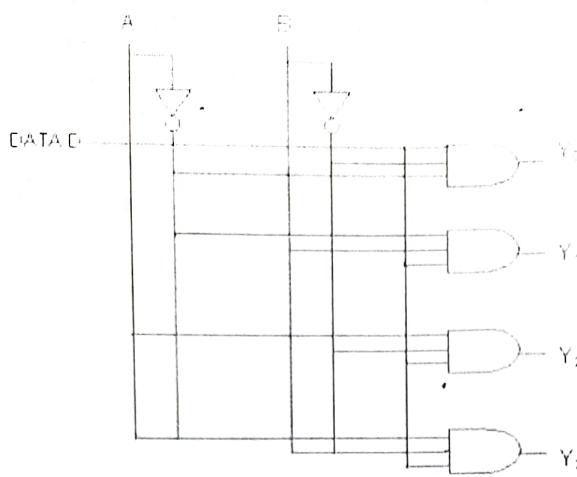
Decimal to BCD Encoder

INPUTS										OUTPUTS			
Y ₉	Y ₈	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀	A ₃	A ₂	A ₁	A ₀
0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	1	0	0	1

Demultiplexer

Input	Select Lines	Output Lines
I	S ₁ S ₀	D ₀ D ₁ D ₂ D ₃
I	0 0	1 0 0 0
I	0 1	0 1 0 0
I	1 0	0 0 1 0
I	1 1	0 0 0 1

Circuit Diagram:Decoder (2:4)Multiplexer (2:1)DemultiplexerDecimal to BCD Encoder



Equipments Required:

1. Bread Board.
2. +5V supply.
3. Connecting wires.
4. Components
 - a. IC's 7404, 7408, 7432.
 - b. Resistors.
 - c. LED's.

Experimental Procedure:

1. Set up the circuit, apply the inputs and observe the output.
2. Verify the operation of the circuit.
3. Low levels refer to 0 volt and high voltage refers to +5 volt.

Result/Observation: All the truth tables are verified experimentally.

Remarks:

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Experiment No 5: Verification of the state tables of RS-JK, D and T flip-flops using Universal logic gates.

Objectives: To realize the operation of RS-JK, D and T flip-flops using Universal logic gates.

Theory :

Sequential Logic Basics

In Sequential Logic the change of state depends not only on the actual inputs being applied to their inputs at that time, but also on the previous output states. Sequential logic circuits are generally termed as *two state* or Bistable devices which can have their output or outputs set in one of two basic states, a logic level "1" or a logic level "0" and will remain unchanged indefinitely in this current state or condition until some other input trigger pulse or signal is applied which will cause the bistable to change its state once again.

The word "Sequential" means that things happen in a "sequence", one after another and in Sequential Logic circuits, the actual clock signal determines when things will happen next. Simple sequential logic circuits can be constructed from standard Bistable circuits such as Flip-flops, Latches and Counters and which themselves can be made by simply connecting together universal NAND Gates and/or NOR Gates in a particular combinational way to produce the required sequential circuit.

There are mainly four types of flip flops that are used in electronic circuits. They are

1. The basic Flip Flop or S-R Flip Flop
2. Delay Flip Flop [D Flip Flop]
3. J-K Flip Flop
4. T Flip Flop

SR Flip-Flop

The SR flip-flop can be considered as one of the most basic sequential logic circuit possible. This simple flip-flop is basically a one-bit memory bistable device that has two inputs, one which

will "SET" the device (meaning the output = "1"), and is labeled S and another which will "RESET" the device (meaning the output = "0"), labeled R.

Then the SR description stands for "Set-Reset". A basic NAND gate SR flip-flop circuit provides feedback from both of its outputs back to its opposing inputs and is commonly used in memory circuits to store a single data bit. The term "Flip-flop" relates to the actual operation of the device, as it can be "flipped" into one logic Set state or "flopped" back into the opposing logic Reset state.

JK Flip-flop

This simple JK flip-Flop is the most widely used of all the flip-flop designs and is considered to be a universal flip-flop circuit. The sequential operation of the JK flip-flop is exactly the same as for the previous SR flip-flop with the same "Set" and "Reset" inputs. The difference this time is that the JK flip-flop has no invalid or forbidden input states of the SR Latch (when S and R are both 1).

The circuit includes two 3-input NAND gates. The output Q of the flip flop is returned back as a feedback to the input of the NAND along with other inputs like K and clock pulse [CP]. Similarly output Q' of the flip flop is given as a feedback to the input of the NAND along with other inputs like J and clock pulse [CP].

D Flip-flop

D flip flop is actually a slight modification of the above explained clocked SR flip-flop. The D input is connected to the S input and the complement of the D input is connected to the R input. The D input is passed to the output of the flip flop when the value of CP is '1'.

T Flip-Flop

In T flip flop, "T" defines the term "Toggle". The "T Flip Flop" has only one input, which is constructed by connecting the input of JK flip flop. This single input is called T.

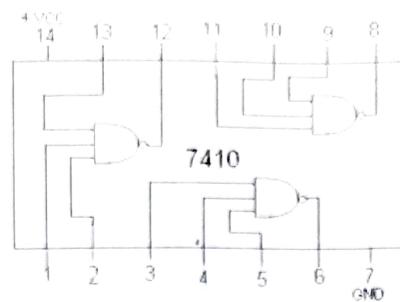
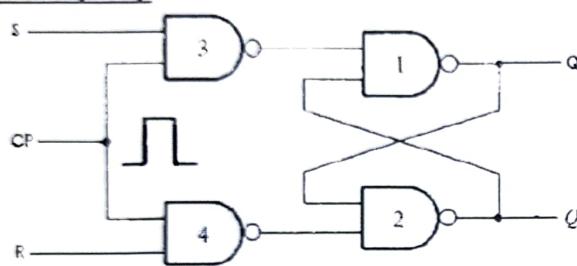
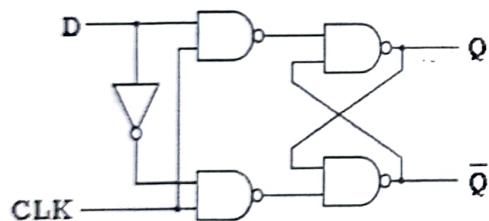
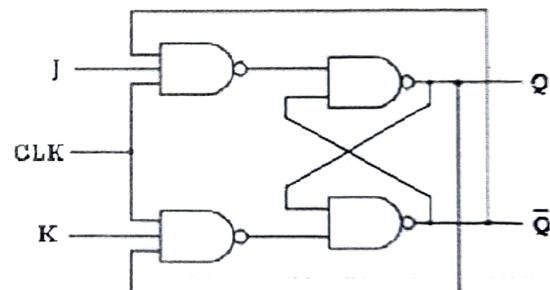
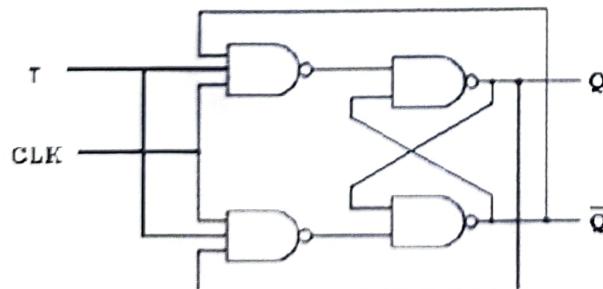
Truth Table:

Clk	S	R	O/P
↑	0	0	No Change
↑	0	1	0
↑	1	0	1
↑	1	1	Forbidden

Clk	J	K	O/P
↑	0	0	No Change
↑	0	1	0
↑	1	0	1
↑	1	1	Toggle

Clk	D	O/P
↑	0	0
↑	1	1

Clk	T	O/P
↑	0	NC
↑	1	Toggle

Internal configuration of Ic 7410:Circuit Diagram:SR FlipFlopD FlipFlopJK FlipFlopT Flip Flop

Equipments Required:

1. Bread Board
2. + 5V supply
3. Connecting wires.
4. Components
 - a. IC's 7400,7410,7404
 - b. Resistors
 - c. Multimeter.
 - d. LED's

Experimental Procedure:

1. Set the Set up the circuit,apply the inputs, and observe the output.
2. Low levels refer to 0 volt and high voltage refers to +5 volt.
3. Verify the trueh table.

Result/Observation : All the truth tables are verified experimentally.

Remarks :

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Experiment No. 6: Design of Shift Register using D Flip Flop

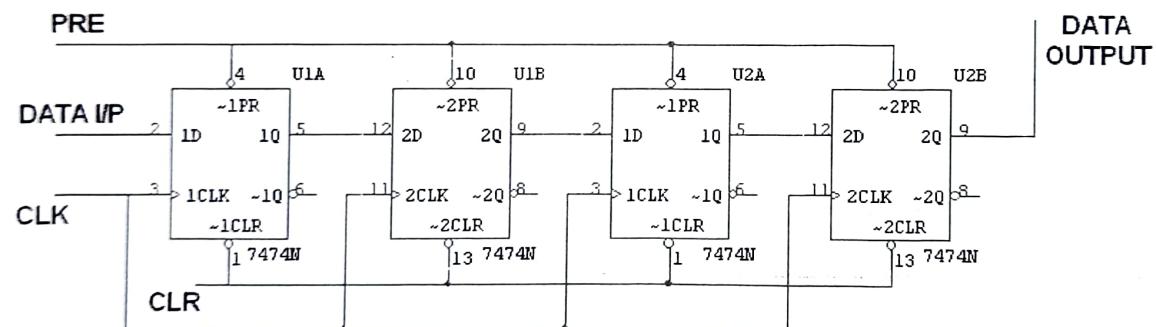
Objective : To design a Shift Register using D Flip Flop and verification of truth table.

Theory:

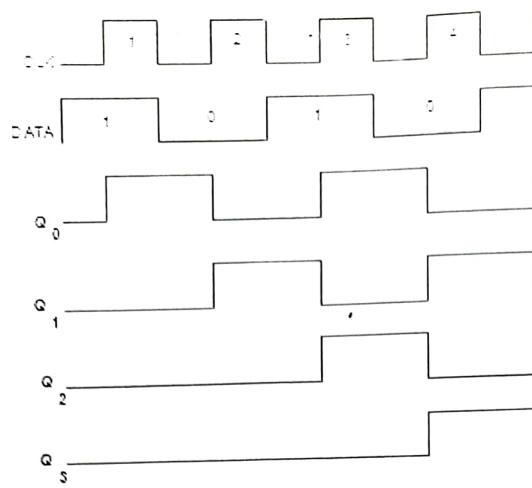
Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. All the flip-flops are driven by a common clock, and all are set or reset simultaneously. The serial in/serial out shift register accepts data serially – that is, one bit at a time on a single line. It produces the stored information on its output also in serial form. The serial in/parallel out shift register accepts data serially – that is, one bit at a time on a single line. It produces the stored information on its output in parallel form. The parallel in/serial out shift register accepts data in parallel. It produces the stored information on its output also in serial form. The parallel in/parallel out shift register accepts data in parallel. It produces the stored information on its output in parallel form.

SERIAL IN SERIAL OUT:

LOGIC DIAGRAM:



OUTPUT WAVEFORM:



Output Waveforms of 4-bit Serial-in Serial-out Register

TRUTH TABLE:

Clk	Serial in	Serial out
1	1	0
2	0	0
3	0	0
4	0	1

Equipments Required:

1. Bread Board
2. + 5V supply
3. Connecting wires.
4. Components
 - a. IC's 7474
 - b. Resistors
 - c. Multimeter.
 - d. LED's

Experimental Procedure:

1. Set the Set up the circuit apply the inputs and observe the output.
2. Low levels refer to 0 volt and high voltage refers to +5 volt.
3. Verify the truth table.

Result/Observation : All the truth tables are verified experimentally.

Remarks :

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Experiment No 7: Realization of Asynchronous Up/Down counter.

Objectives: To realize the operation of Asynchronous Up/Down counter.

Theory :

A counter is a sequential circuit with a set of flip flop which counts the number of pulses given at the clock input. The number of flip-flops determines the count limit or number of states.

$$(\text{No of states} = 2^{\text{no of flip flops}})$$

In asynchronous counter only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop. Asynchronous counters are slower than synchronous counters because of the delay in the transmission of the pulses from flip-flop to flip-flop. Asynchronous counters are also called *ripple-counters* because of the way the clock pulse ripples it way through the flip-flops.

A up /down asynchronous counter must be able to count both up and down. The circuit below is a 2-bit up-down counter. It counts up or down depending on the status of the control signal M. When the M input is at 0, the OR and AND network between FF0 and FF1 will gate the non-inverted output (Q) of FF0 to the clock input of FF1. Thus the counter will count up. When the M input is at 1, the OR and AND network between FF0 and FF1 will gate the inverted output (\bar{Q}) of FF0 to the clock input of FF1. Thus the counter will count down.

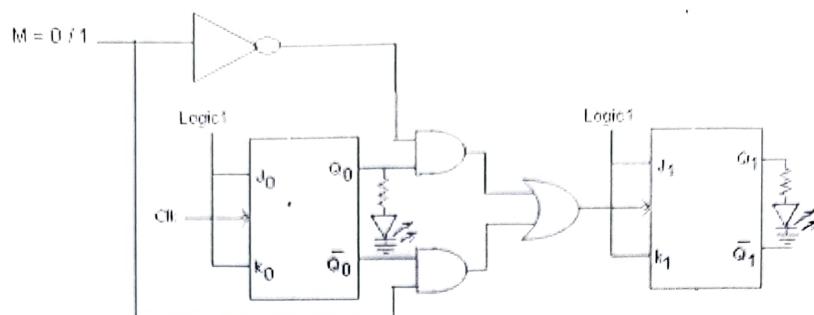
Truth Table:

Up Counter(for M=0)

Clk	Q1	Q0
↓	0	0
↓	0	1
↓	1	0
↓	1	1
↓	0	0

Down Counter (for M=1)

Clk	Q1	Q0
↓	0	0
↓	1	1
↓	1	0
↓	0	1
↓	0	0

Circuit Diagram:Equipments Required:

1. Bread Board
2. + 5V supply
3. Connecting wires.
4. Components
 - a. IC's 7473, 7408, 7432, 7404
 - b. Resistors
 - c. Multimeter.
 - d. LED's

Experimental Procedure:

1. Set the Set up the circuit, apply the inputs and observe the output.
2. Low levels refer to 0 volt and high voltage refers to +5 volt.
3. Verify the operation of the circuit.

Result/Observations : All the truth tables are verified experimentally.

Remarks:

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Experiment No 8 : Realization of Synchronous Up/Down counter.

Objectives: To realize the operation of Synchronous Up/Down counter.

Theory :

A counter is a sequential circuit with a set of flip flop which counts the number of pulses given at the clock input. The number of flip-flops determines the count limit or number of states.

$$(No\ of\ states = 2^{\text{no of flip flops}})$$

Here all the flip-flops are clocked simultaneously by an external clock. Synchronous counters are faster than asynchronous counters because of the simultaneous clocking. Synchronous counters are an example of state machine design because they have a set of states and a set of transition rules for moving between those states after each clocked event.

A up /down synchronous counter must be able to count both up and down. The circuit below is a 2-bit up-down counter. It counts up or down depending on the status of the control signal M. When the M input is at 0, the OR and AND network between FF0 and FF1 will gate the non-inverted output (Q) of FF0 to the J and K inputs of FF1. Thus the counter will count up. When the M input is at 1, the OR and AND network between FF0 and FF1 will gate the inverted output (\bar{Q}) of FF0 to the J and K input of FF1. Thus the counter will count down.

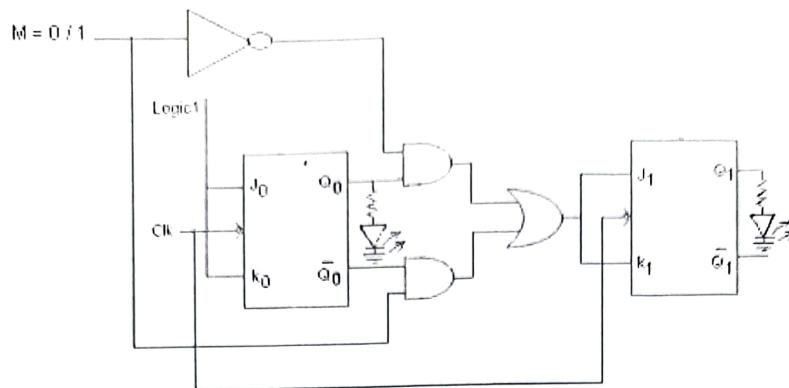
Truth Table:

Up Counter(for M=0)

Clk	Q1	Q0
↓	0	0
↓	0	1
↓	1	0
↓	1	1
↓	0	0

Down Counter (for M=1)

Clk	Q1	Q0
↓	0	0
↓	1	1
↓	1	0
↓	0	1
↓	0	0

Circuit Diagram:Equipments Required:

1. Bread Board
2. + 5V supply
3. Connecting wires.
4. Components
 - a. IC's 7473, 7408, 7432, 7404
 - b. Resistors
 - c. Multimeter.
 - d. LED's

Experimental Procedure:

1. Set the Set up the circuit, apply the inputs and observe the output.
2. Low levels refer to 0 volt and high voltage refers to +5 volt.
3. Verify the operation of the circuit.

Result/Observation : All the truth tables are verified experimentally.

Remarks:

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Experiment No 9: Realization of Ring counter & Johnson's counter.

Objectives: To realize the operation of Ring counter & Johnson's counter.

Theory :

Ring Counter:

Ring counters are implemented using shift registers. It is essentially a circulating shift register connected so that the last flip-flop shifts its value into the first flip-flop. There is usually only a single 1 circulating in the register, as long as clock pulses are applied. (Starts 100>010>001repeat). To initialize the operation of the ring counter, it is necessary to set the first flip-flop and reset second and third flip flops simultaneously as shown in the figure.

Johnson Counter:

The Johnson counter, also known as the twisted-ring counter, is exactly the same as the ring counter except that the inverted output of the last flip-flop is connected to the input of the first flip-flop. Let's say, starts from 000, 100, 110, 111, 011 and 001, and the sequence is repeated so long as there is input pulse. To initialize the operation of the Johnson counter, it is necessary to reset all flip-flops, as shown in the figure.

Observe that neither the Johnson nor the ring counter will generate the desired counting sequence if not initialized properly.

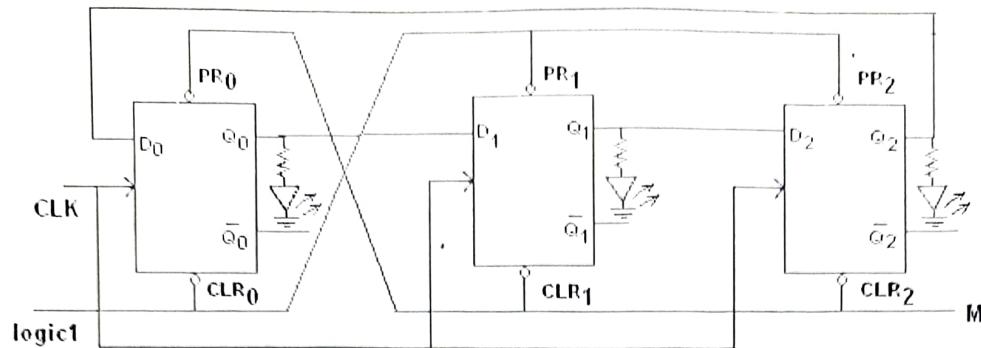
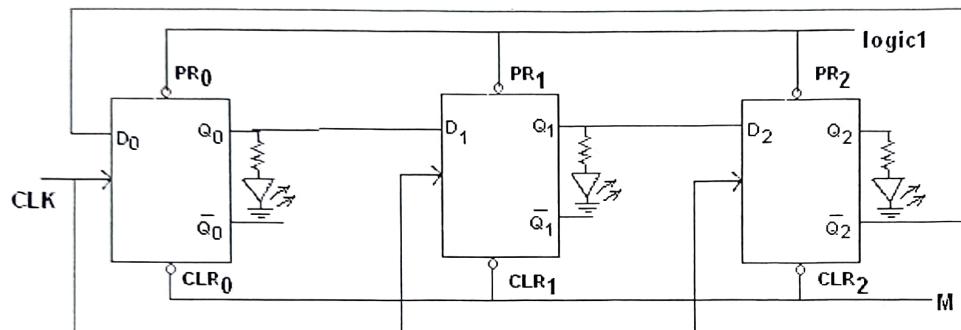
Truth Table:

Ring counter

Q0	Q1	Q2
1	0	0
0	1	0
0	0	1

Johnson counter

Q0	Q1	Q2
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1
0	0	0

Circuit Diagram:Ring CounterJohnson's CounterEquipments Required:

1. Bread Board
2. + 5V supply
3. Connecting wires.
4. Components
 - a. IC's 7474
 - b. Resistors
 - c. Multimeter.
 - d. LED's

Experimental Procedure:

1. Set up the circuit, apply the inputs and observe the output.
2. Switch on the ckt, connect M=0 momentarily then make M=1.
3. Low levels refer to 0 volt and high voltage refers to +5 volt.
4. Verify the operation of the circuit.

Result/Observation : All the truth tables are verified experimentally.

Remarks:

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Experiment No. 10: Study of D/A Converter and A/D Converter Circuit

Objective : To study the characteristics of DAC using R-2R ladder circuit and To study the characteristics of ADC 0804.

DAC:

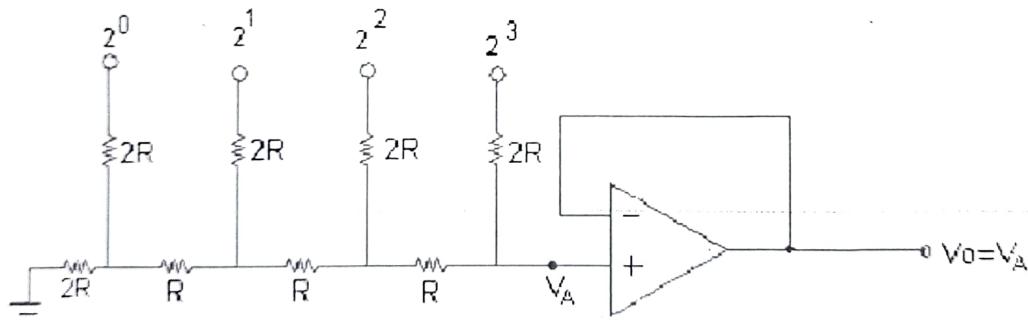
Theory :

Digital to analog and analog to digital conversion form two very important aspects of digital data processing. As an example the output of digital system may be changed to analog form for the purpose of driving a pen recorder. In this case a digital to analog converter (DAC) is necessary. DAC converts a digital signal into an equivalent analog voltage. Two convenient methods of converting digital signals are

1. Binary weighted network. Ω
2. Binary ladder network.

Binary ladder network

The binary ladder is resistive network whose output voltage is a proper sum of the digital inputs. The resistors used here have two values and thus overcomes one of the objections to the binary weighted network. Such a ladder designed for 4 bits, is shown in Figure.



If we study the network, we can conclude that the total equivalent resistance looking from any node (A or B or C or D) back toward the terminating resistor or out toward the digital input is $2R$. This is true regardless of whether the digital inputs are at ground or $+V$. The conclusion is true assuming that the digital inputs are ideal voltage sources.
(Zero internal impedance).

We can use this characteristics to determine the output voltages for various digital inputs.

Starting from LSB each bit of DAC has weight ($V/16$, $(V/8)$, $(V/4)$ and $(V/2)$ Volts respectively, where V is the voltage input to each bit of DAC.

27

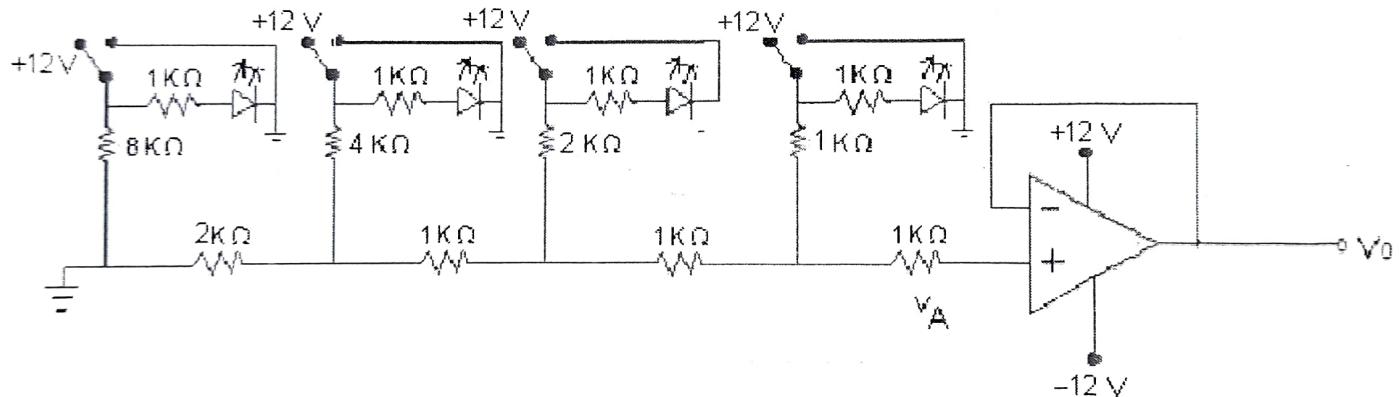
Digital Input	Analog Output
0001	$V/16$
0010	$V/8$
0100	$V/4$
1000	$V/2$

An OPAMP in voltage follower mode can be used at the output as it has high input impedance so that the circuitry connected at the output will not load the resistance network.

Equipments Required:

1. Bread Board
2. + 5V supply
3. Connecting wires.
4. Components
 - a. IC's 741
 - b. Resistors 1kohm, 2kohm
 - c. Multimeter.
 - d. LED's

Circuit Diagram:



(b) Binary Ladder Network

Experimental Results:

No. of Obs.	Digital Input				Analog Output	
	2^3	2^2	2^1	2^0	Calculated Value	Practical Value

ADC:

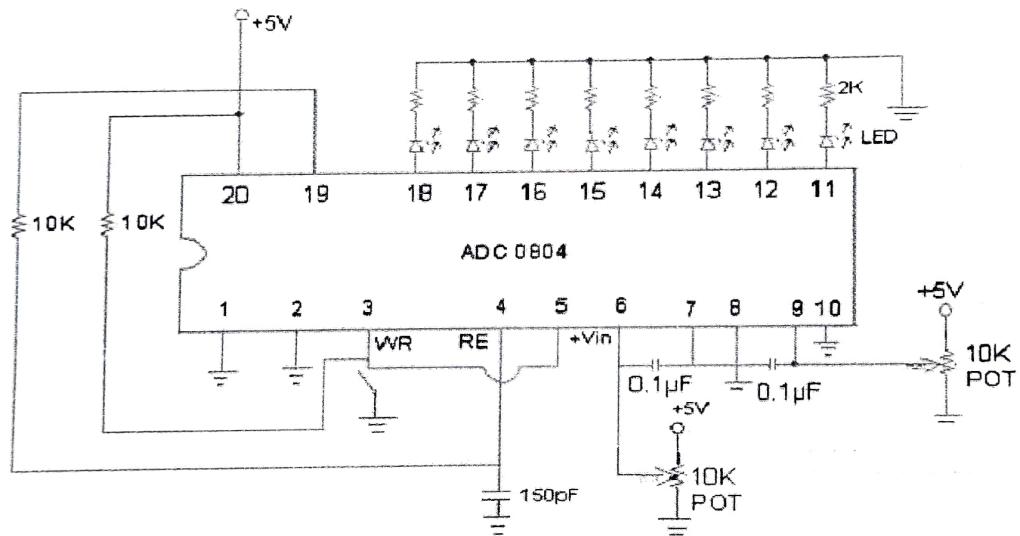
Theory:

(B) The process of converting an analog voltage into an equivalent digital signal is known as analog to digital conversion (ADC). This operation is somewhat more complicated than converse operation of D/A Conversion. A number of different methods have been developed which are

- (C) (a) Simultaneous conversion type
- (D) (b) Ramp type.
- (E) (c) Successive approximation type.
- (F) (d) Integrating type.
- (G) (e) Counter type.
- (H) (f) Dual slope type.

Successive approximation type ADC and integrating type ADC are most common. In our experiment we have used ADC 0804 Chip, which is a successive approximation type ADC. It has 8-bit digital output, one channel analog input; one reference voltage has to be supplied to it.

Circuit Diagram:



Equipments/Components Required for ADC:

1. IC 0804
2. Signal generator
3. Power supply (+5V)
4. Capacitor 150pf
5. Resistor 2KΩ, 10KΩ
6. 10KΩ pot
7. LED

Procedure:

1. Make circuit connection as shown in fig
2. A 2.5V reference dc voltage is to be provided at pin 9 by a $10\text{K}\Omega$ trim pot.
3. A variable voltage (analog input) is provided at pin 6 by a $10\text{K}\Omega$.
4. Analog voltages ranging from 0 to 5 volt is applied to the input of the conversion steps of 0.5 volt and in each step note the digital output.

Experimental results:

Analog input	Digital output								Decimal Equivalent of Digital Output
	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	

Remarks: