Week-13

DLD LAB-13

Flip Flop and Its Types

Objectives:

- To understand concept of Flip Flop, its types and their circuits.
- To validate implementation of circuits using **Circuit Maker 2000**.

Flip-Flop vs Latches

The primary difference between a latch and a flip-flop is a gating or clocking mechanism.

In Simple words. Flip Flops are edge-triggered and a latch is level-triggered.

If you are confused between latch and flip-flop, then you should check this detailed article where we discussed the difference between Latch and flip-flop.

For example, let us talk about SR latch and SR flip-flops. In this circuit when you Set S as active, the output Q will be high and Q' will be Low.

This is irrespective of anything else. (This is an active-low circuit; so active here means low, but for an active high circuit, active would mean high).

Types of Flip-flops

In digital electronics different types of Flip-flops are:

- SR Flip-Flop
- JK Flip-Flop
- D Flip-Flop
- T Flip-Flop

SR Flip-Flop

This is the **most common flip-flop** among all. This simple flip-flop circuit has a set input (S) and a reset input (R). In this system, when you Set “S” as active, the output “Q” would be high, and “Q ‘” would be low.

Once the outputs are established, the wiring of the circuit is maintained until “S” or “R” goes high, or power is turned off.

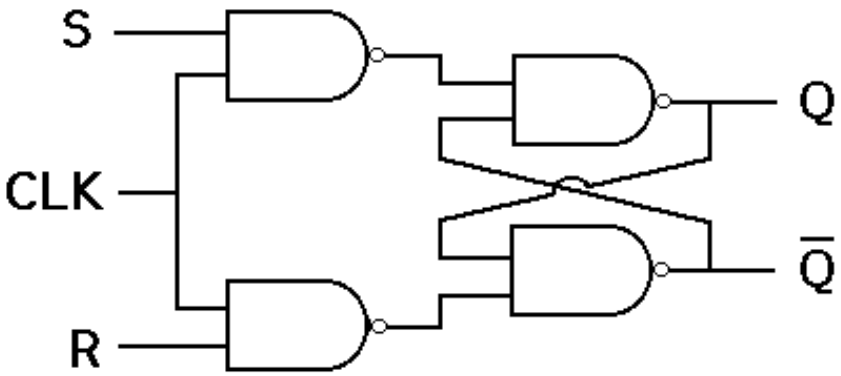
As shown above, it is the simplest and easiest to understand. The two outputs, as shown above, are the inverse of each other.

Truth Table of SR Flip-Flop:

The below table represents the truth table of SR Flip-Flop.

S	R	Q(n+1)	State
0	0	Qn	No change
0	1	0	RESET
1	0	1	SET
1	1	x	INVALID

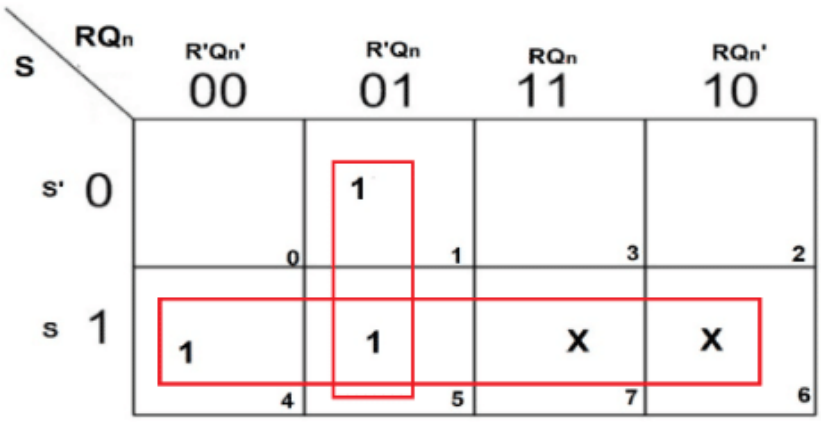
Circuit Diagram of SR Flip-Flop:



Characteristics Table of SR Flip-Flop:

S	R	Qn	Q(n+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

K-Map of SR Flip-Flop:



From the K-map you get 2 pairs. On solving both we get the following characteristic equation:

$$Q(n+1) = S + R'Qn$$

JK Flip-Flop

Due to the undefined state in the SR flip-flops, another flip-flop is required in electronics.

The JK flip-flop is an improvement on the SR flip-flop where S=R=1 is not a problem.

The input condition of J=K=1 gives an output inverting the output state. However, the outputs are the same when one tests the circuit practically.

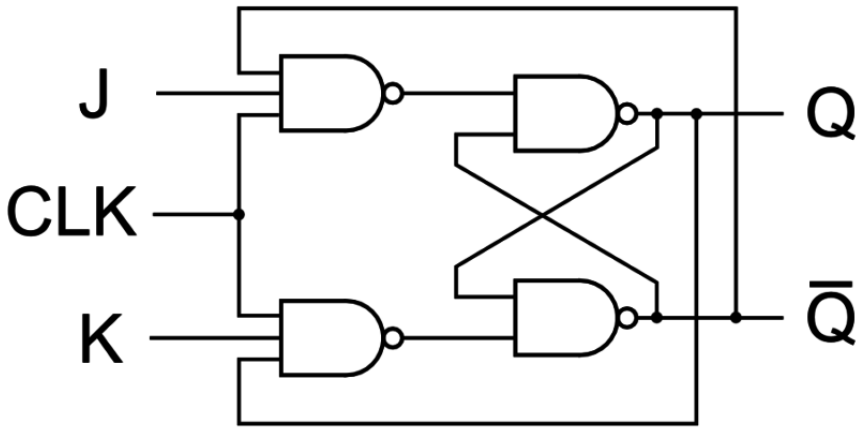
In simple words, If J and K data input are different (i.e. high and low), then the output Q takes the value of J at the next clock edge. If J and K are both low, then no change occurs.

If J and K are both high at the clock edge, then the output will toggle from one state to the other. JK Flip-Flops can function as Set or Reset Flip-flops.

Truth Table of JK Flip-Flop:

J	K	Q(n+1)	State
0	0	Qn	No Change
0	1	0	RESET
1	0	1	SET
1	1	Qn’	TOGGLE

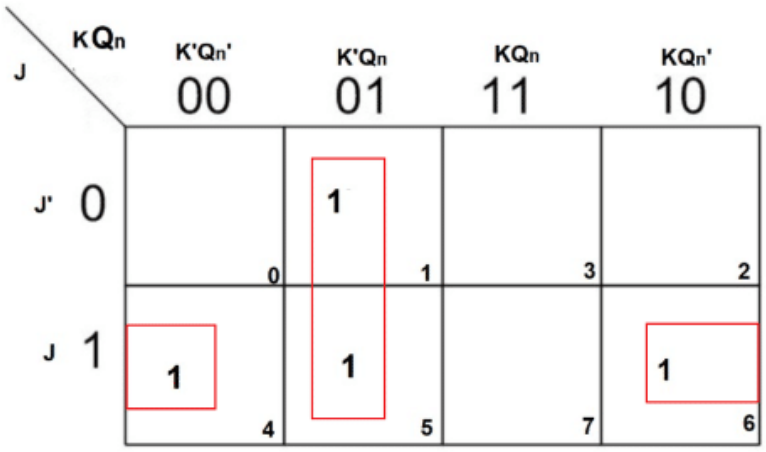
Circuit Diagram of JK Flip-Flop:



Characteristics Table of JK Flip-Flop:

J	K	Qn	Q(n+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

K-Map of JK Flip-Flop:



From the K-map you get 2 pairs. On solving both we get the following characteristic equation:

$$Q(n+1) = JQn' + K'Qn$$

D Flip-Flop

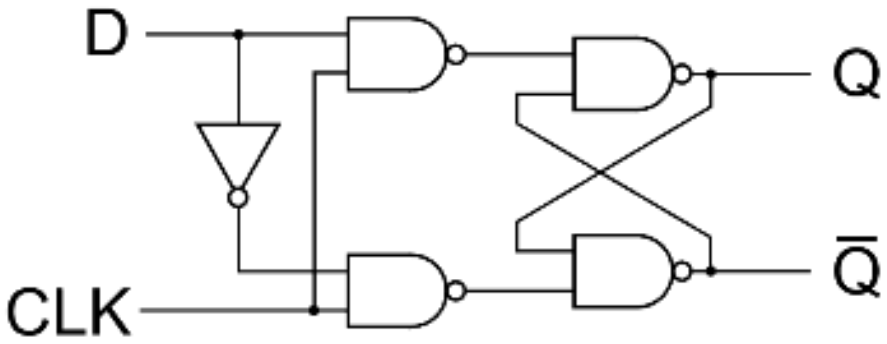
Delay or D flip-flop is a better alternative that is very popular with digital electronics. They are commonly used for counters, shift registers, and input synchronization.

In the D flip-flops, the output can only be changed at the clock edge, and if the input changes at other times, the output will be unaffected.

Truth Table of D Flip-Flop:

CLK	D	Q(n+1)	State
1	0	0	RESET
1	1	1	SET

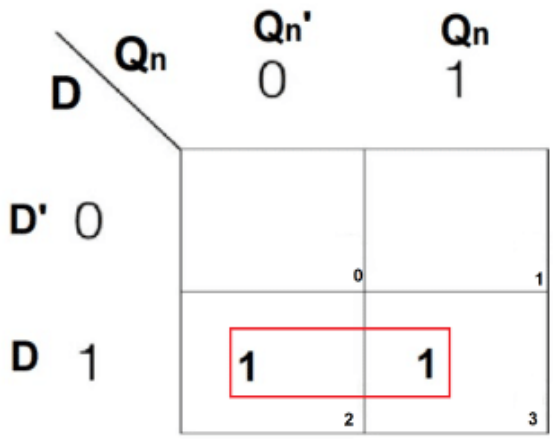
Circuit Diagram of D Flip-Flop:



Characteristics Table of D Flip-Flop:

D	Qn	Q(n+1)
0	0	0
0	1	0
1	0	1
1	1	1

K-Map of D Flip-Flop:



From the K-map you get 2 pairs. On solving both we get the following characteristic equation:

```
Q(n+1) = D
```

T Flip-Flop

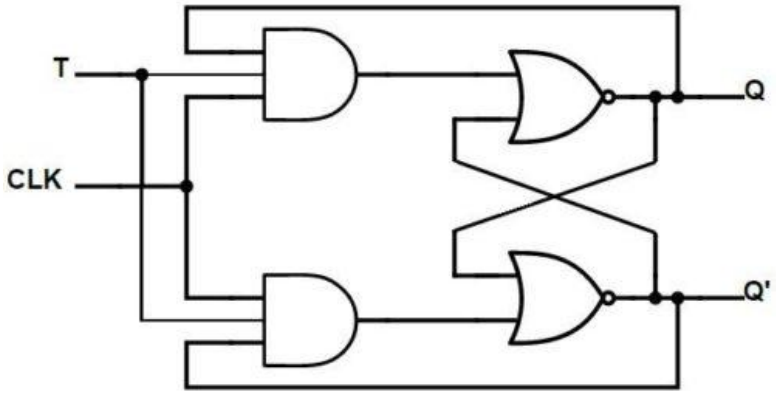
A T flip-flop is like a JK flip-flop. These are single-input versions of JK flip-flops. This modified form of the JK is obtained by connecting inputs J and K together. It has only one input along with the clock input.

These flip-flops are called T flip-flops because of their ability to complement their state i.e. Toggle; hence they are named **Toggle flip-flops**.

Truth Table of T Flip-Flop:

CLK	T	Q(n+1)	State
1	0	Q	NO CHANGE
1	1	Q’	TOGGLE

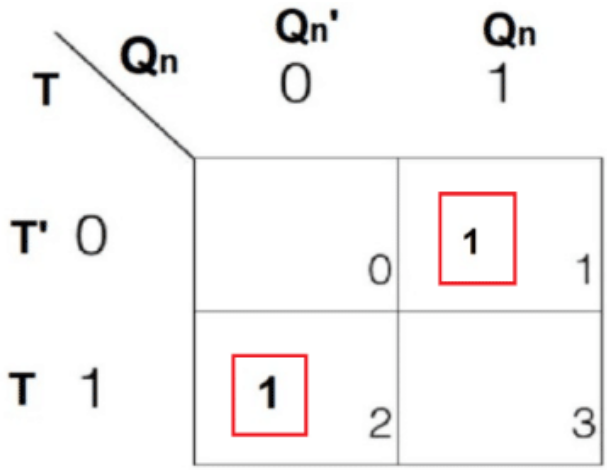
Circuit Diagram of T Flip-Flop:



Characteristics Table of T Flip-Flop:

T	Qn	Q(n+1)
0	0	0
0	1	1
1	0	1
1	1	0

K-Map of T Flip-Flop:



From the K-map you get 2 pairs. On solving both we get the following characteristic equation:

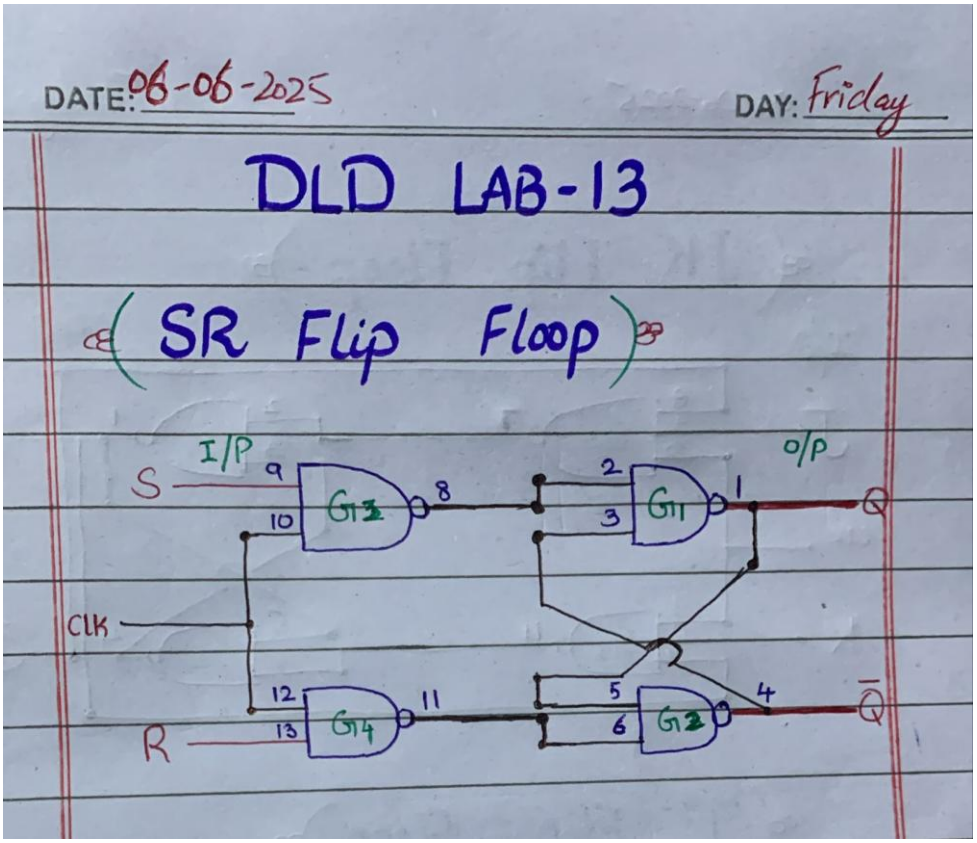
```
Q(n+1) = TQn’ + T’Qn = T XOR Qn
```

LAB TASKS

TASK-01

Do the following for SR Flip-Flop:

a) Draw the Circuit diagram of **SR Flip Flop** on page. Mention/label all inputs and output clearly.

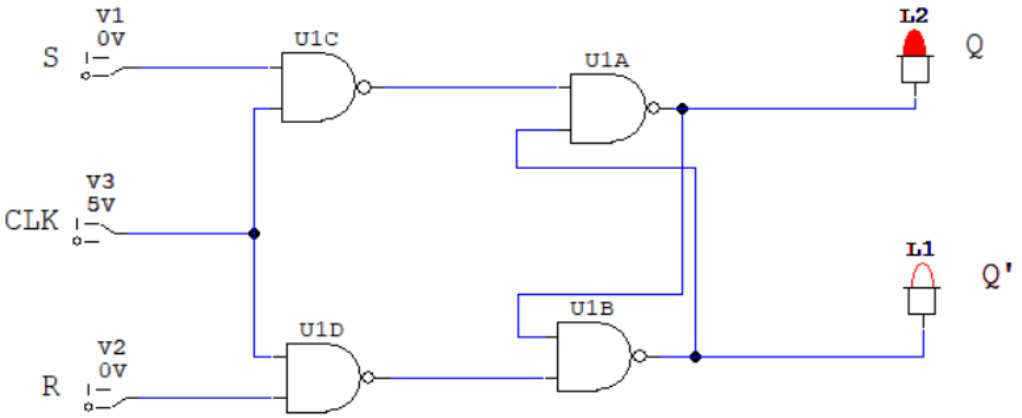


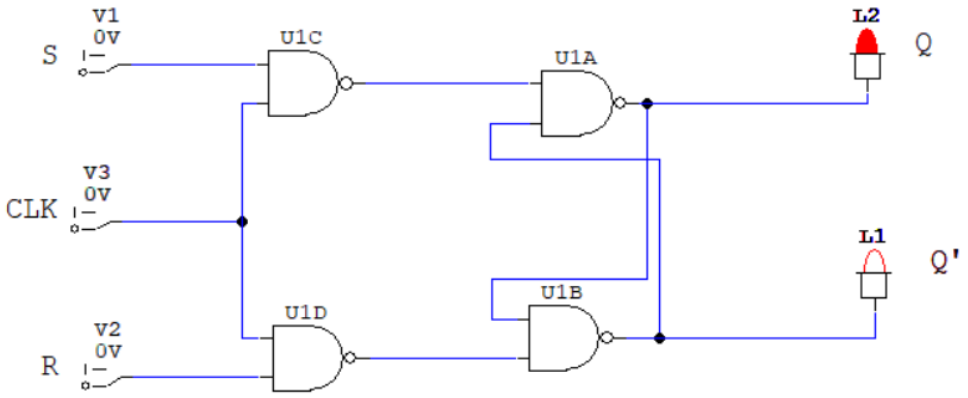
b) Draw the characteristic table.

Ref No	S_4	R_2	Q_{n_1}	$Q(n+1)$/state	
0	0	0	0	0	No change
1	0	0	1	1	
2	0	1	0	0	Reset
3	0	1	1	0	
4	1	0	0	1	Set
5	1	0	1	1	
6	1	1	0	X	Indeterminate
7	1	1	1	X	

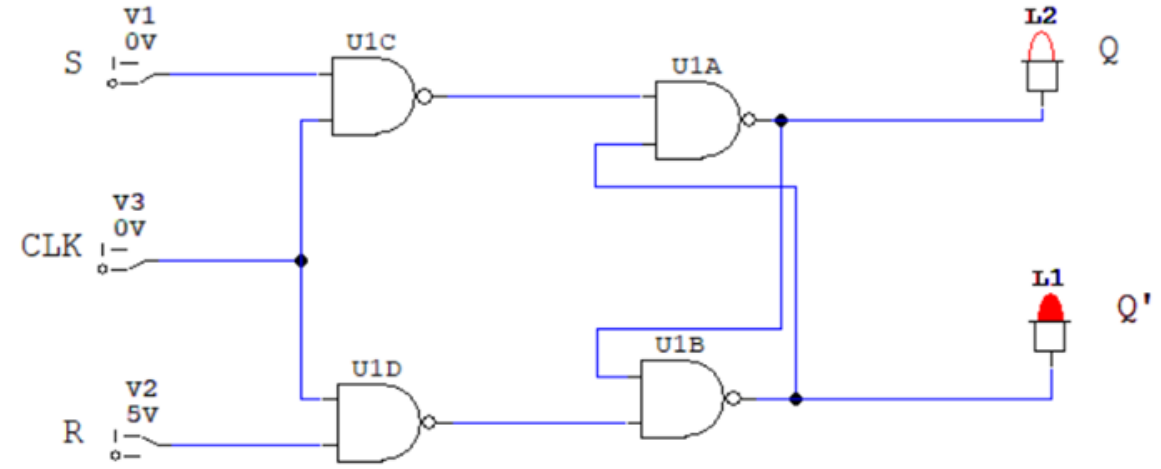
c) Implement circuit of SR Flip-flop on **circuit maker** and verify from Characteristic Table.

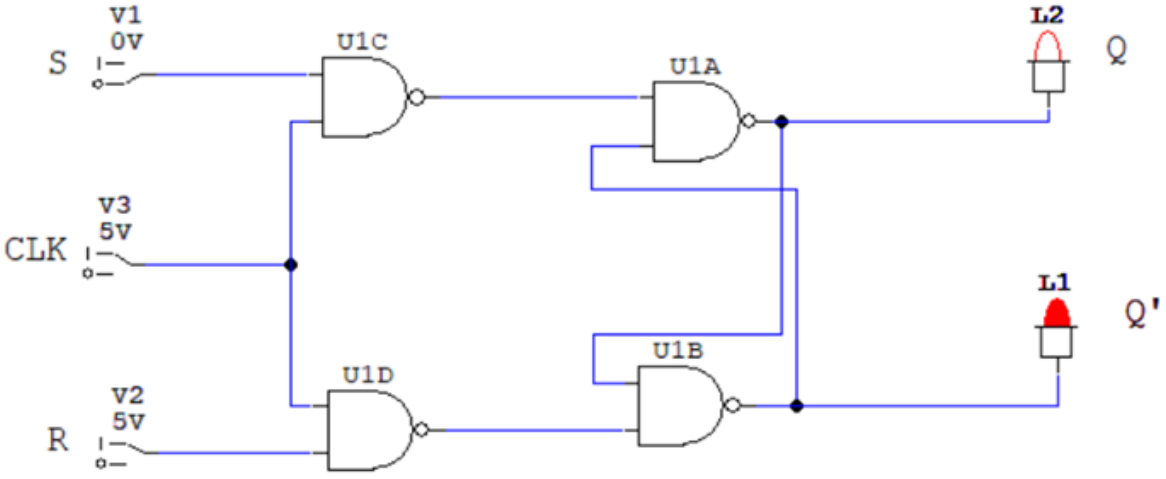
No Change:-



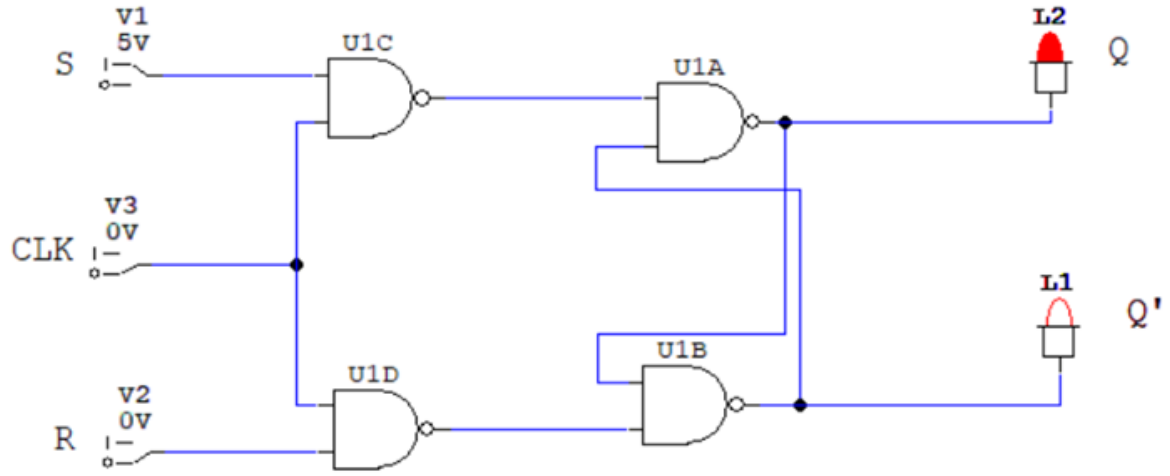

V1
0V
S
U1C
U1A
L2
Q
V3
0V
CLK
L1
Q'
U1B
U1D
V2
0V
R

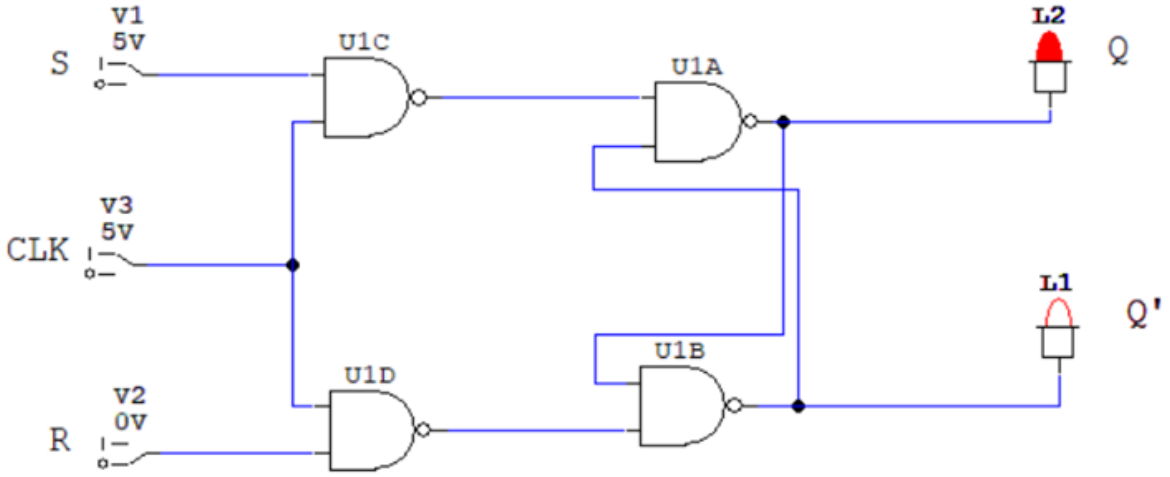
Reset:-


V1
0V
S
U1C
U1A
L2
Q
V3
0V
CLK
L1
Q'
U1B
U1D
V2
5V
R


V1
0V
S
U1C
U1A
L2
Q
V3
5V
CLK
L1
Q'
U1B
U1D
V2
5V
R

Set:-

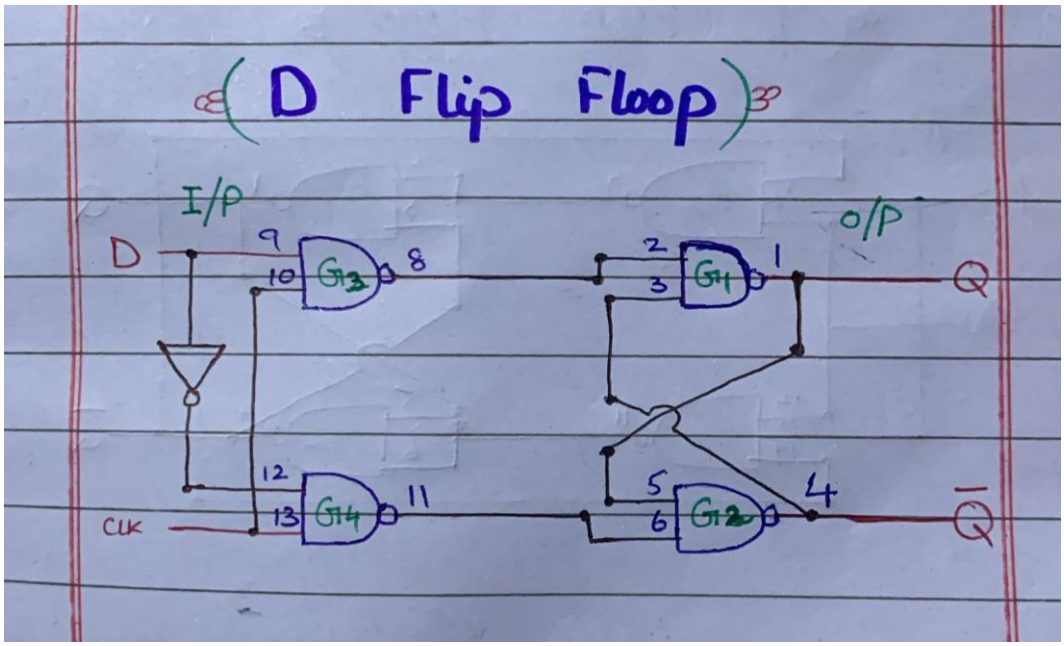

V1
5V
S
U1C
U1A
L2
Q
V3
0V
CLK
L1
Q'
U1B
U1D
V2
0V
R


V1
5V
S
U1C
U1A
L2
Q
V3
5V
CLK
L1
Q'
U1B
U1D
V2
0V
R

TASK-02

Do the following for D Flip-Flop:

a) Draw the Circuit diagram of **D Flip Flop** on page. Mention/label all inputs and output clearly.

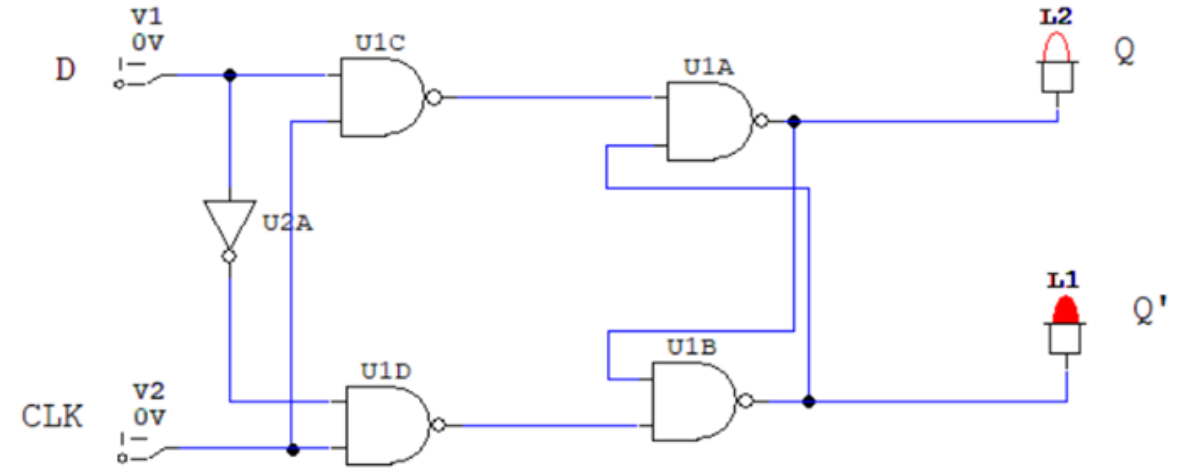


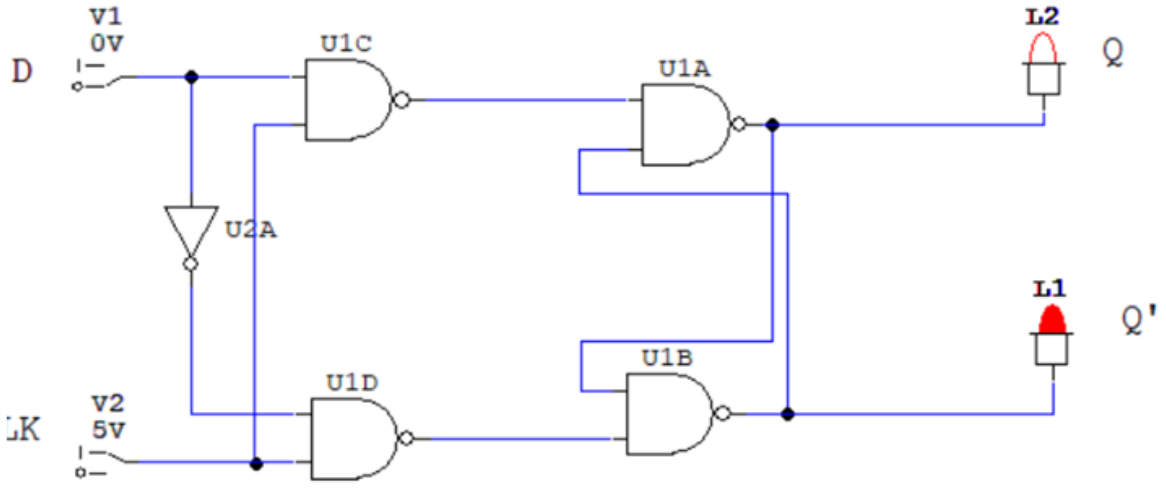
b) Draw the characteristic table.

Ref No.	D_2	Q_n	$Q_{(n+1)}$	state
0	0	0	0	Reset
1	0	1	0	
2	1	0	1	Set
3	1	1	1	

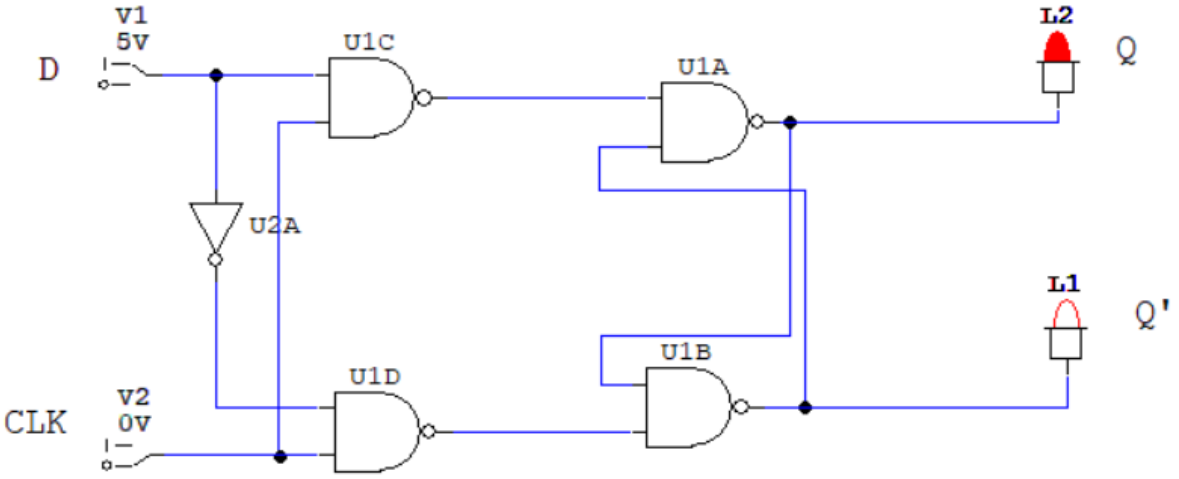
c) Implement circuit diagram of D Flip-flop on **circuit maker** and verify from Characteristic Table.

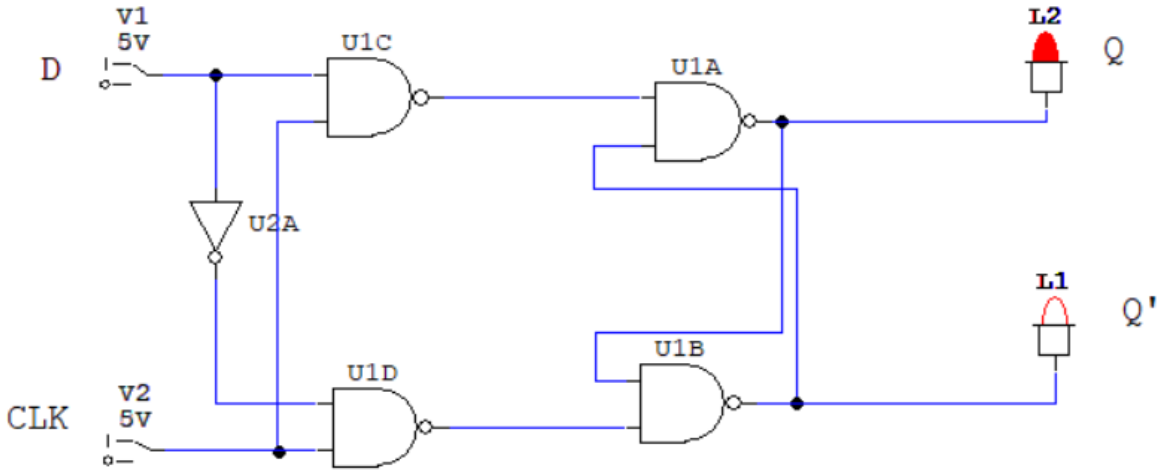
Reset:





Set:-

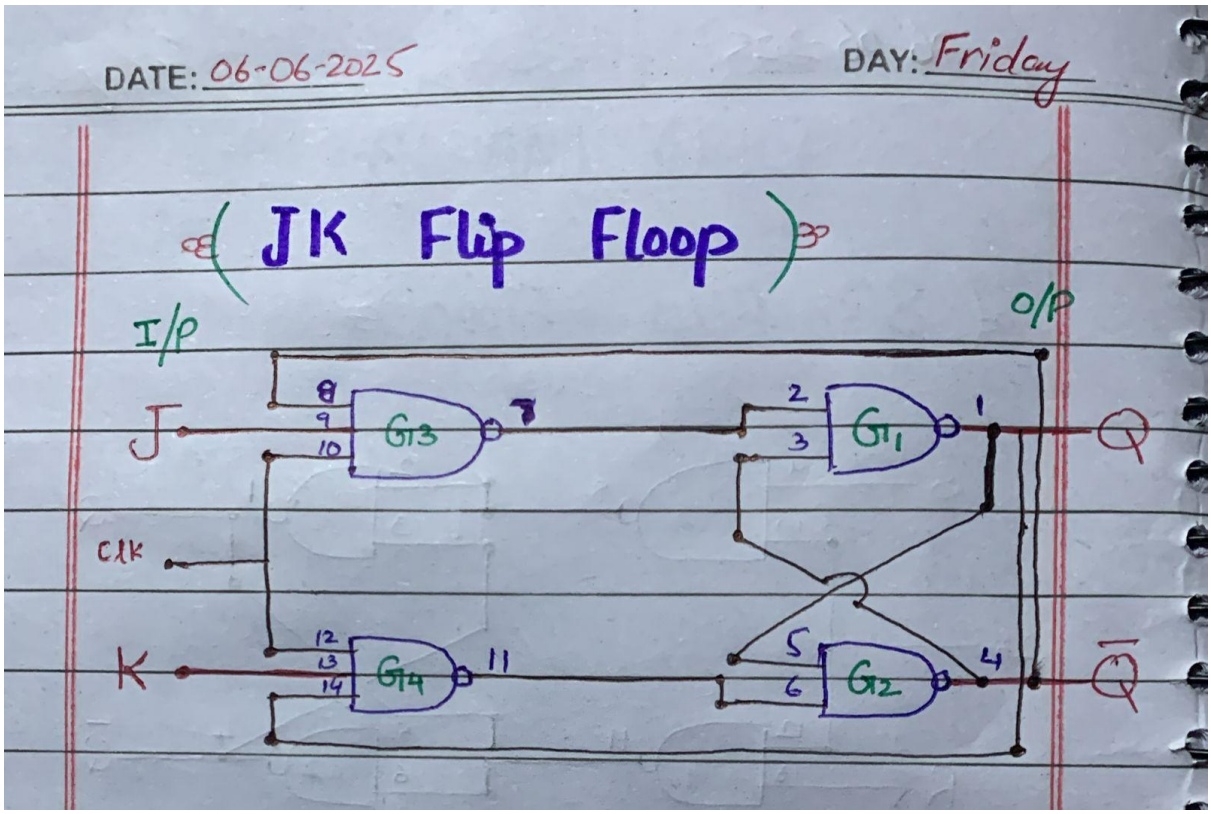

V1
5V
D
U1C
U1A
L2
Q
U2A
L1
Q'
U1B
U1D
V2
0V
CLK


V1
5V
D
U1C
U1A
L2
Q
U2A
L1
Q'
U1B
U1D
V2
5V
CLK

TASK-03

Do the following for JK Flip-Flop:

a) Draw the Circuit diagram of **JK Flip Flop** on page. Mention/label all inputs and output clearly.

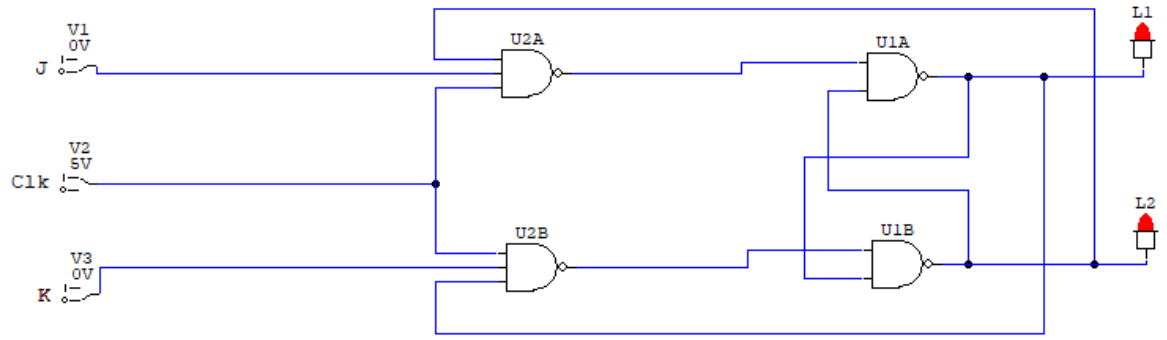


b) Draw the characteristic table.

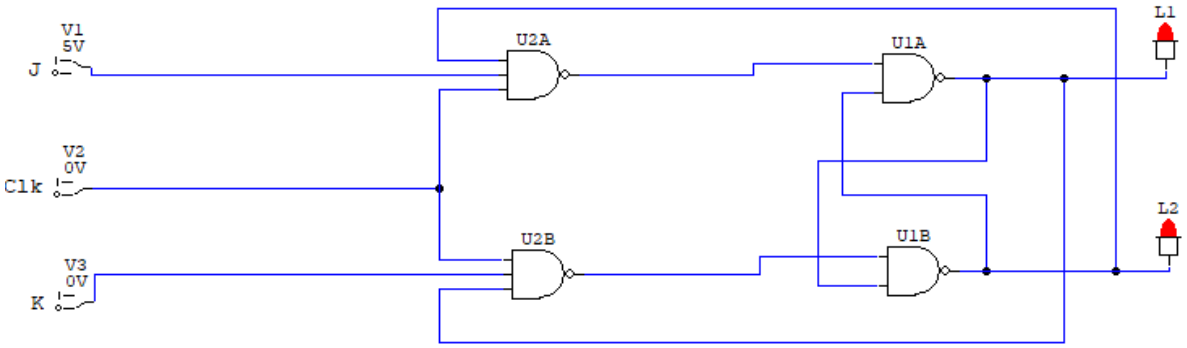
Ref No.	J_4	K_2	Q_{n1}	$Q_{(n+1)}$	State
0	0	0	0	0	No change
1	0	0	1	1	
2	0	1	0	0	Reset
3	0	1	1	0	
4	1	0	0	1	Set
5	1	0	1	1	
6	1	1	0	1	Toggles
7	1	1	1	0	

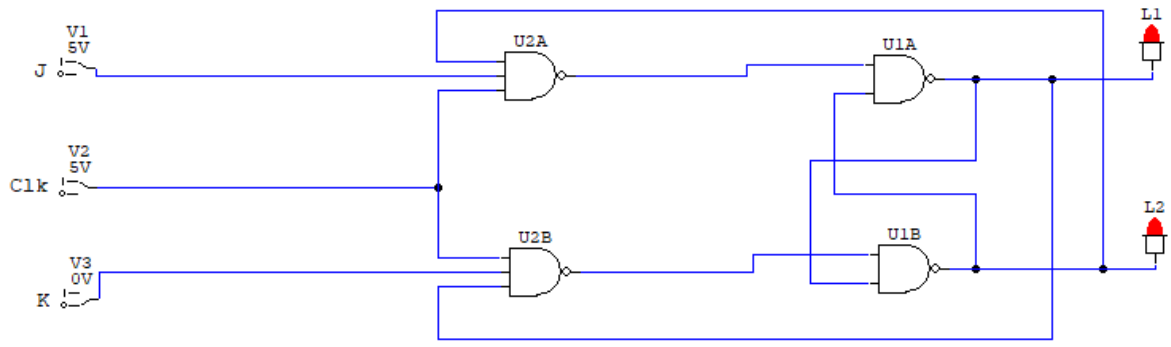
c) Implement circuit diagram of JK Flip-flop on **circuit maker** and verify from Characteristic Table.

No change:-

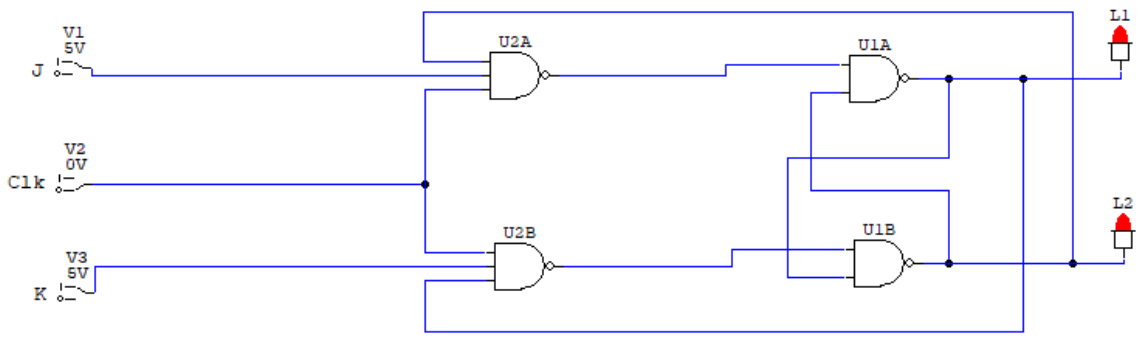


Set:-





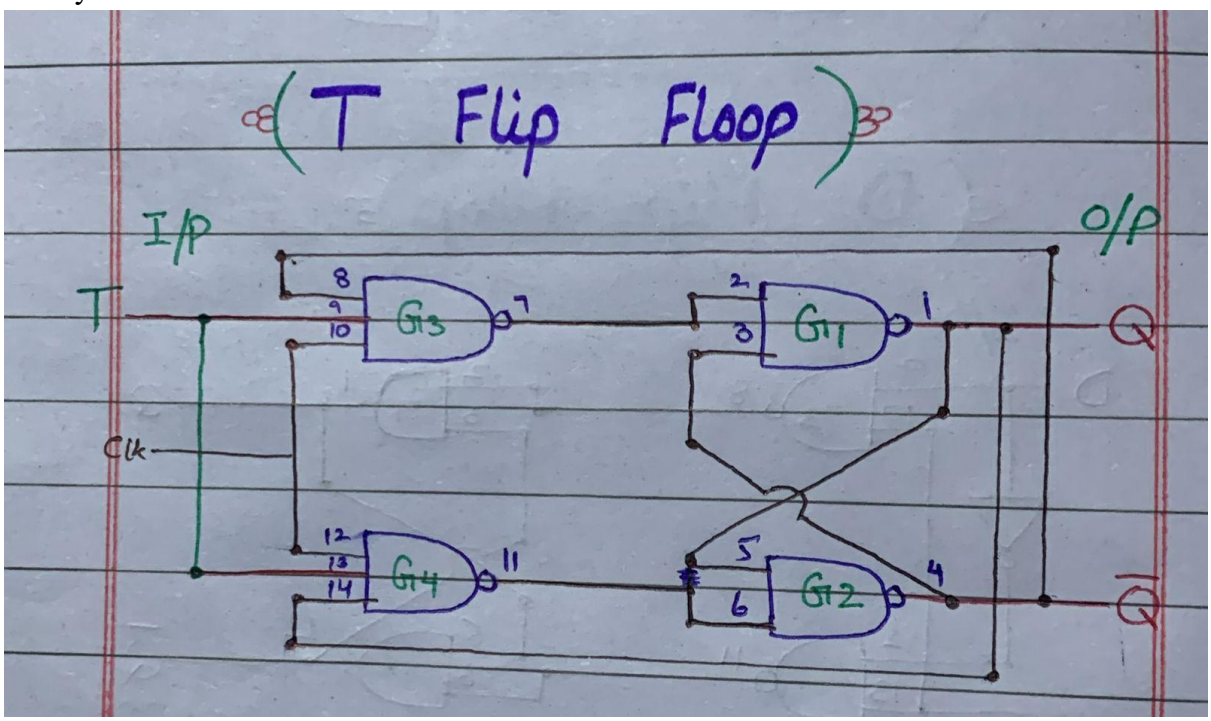
Toggles:-



TASK-04

Do the following for T Flip-Flop:

a) Draw the Circuit diagram of **T Flip Flop** on page. Mention/label all inputs and output clearly.

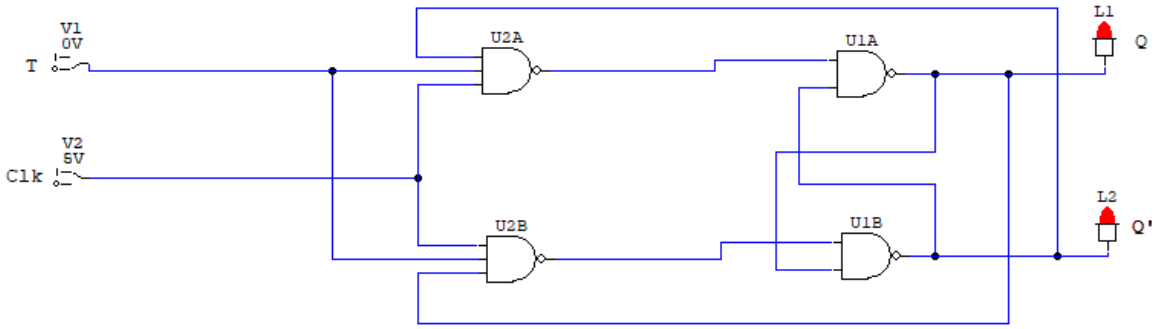


b) Draw the characteristic table.

Ref No.	T_2	Q_n	$Q_{(n+1)}$	state
0	0	0	0	No change
1	0	1	1	
2	1	0	1	Toggles
3	1	1	0	

c) Implement circuit diagram of T Flip-flop on **circuit maker** and verify from Characteristic Table.

No Change:-



Toggles:-