Week-15

DLD LAB-15

Asynchronous Counter and Frequency Divider

Objectives:

- To understand concept of Asynchronous Counter, Frequency Divider and their circuits.
- To validate implementation of circuits using **Circuit Maker 2000**.

Counter

A **Counter** is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit. For example, in UP counter a counter increases count for every rising edge of clock. Not only counting, a counter can follow the certain sequence based on our design like any random sequence 0,1,3,2. They can also be designed with the help of flip flops. They are used as frequency dividers where the frequency of given pulse waveform is divided. Counters are sequential circuit that count the number of pulses can be either in binary code or BCD form. The main properties of a counter are timing, Sequencing, and counting. Counter works in two modes:

1. Up counter
2. Down counter

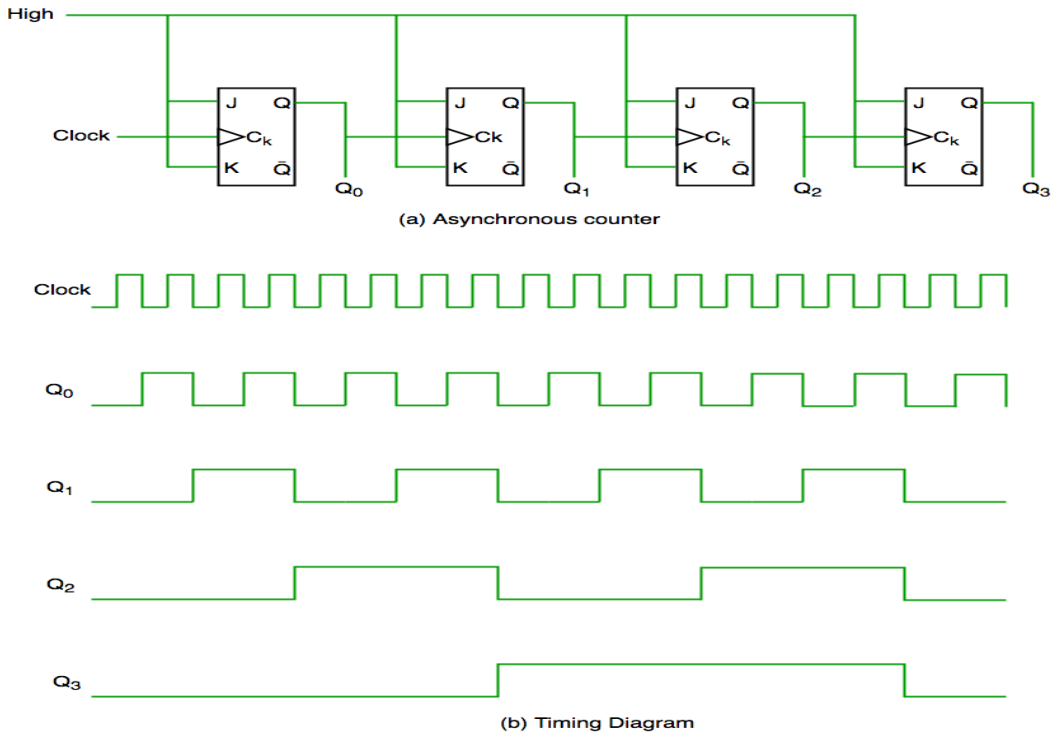
Types of Counters

Counters are broadly divided into two categories:

1. Asynchronous counter
2. Synchronous counter

Asynchronous Counter:

In asynchronous counter we don't use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following flip flop is driven by output of previous flip flops. We can understand it by following diagram:



It is evident from timing diagram that Q0 is changing as soon as the rising edge of clock pulse is encountered, Q1 is changing when rising edge of Q0 is encountered (because Q0 is like clock pulse for second flip flop) and so on. In this way ripples are generated through Q0, Q1, Q2, Q3 hence it is also called **RIPPLE counter.**

Frequency Divider

A **frequency divider** is a circuit that **reduces the frequency** of a clock signal by a certain factor.

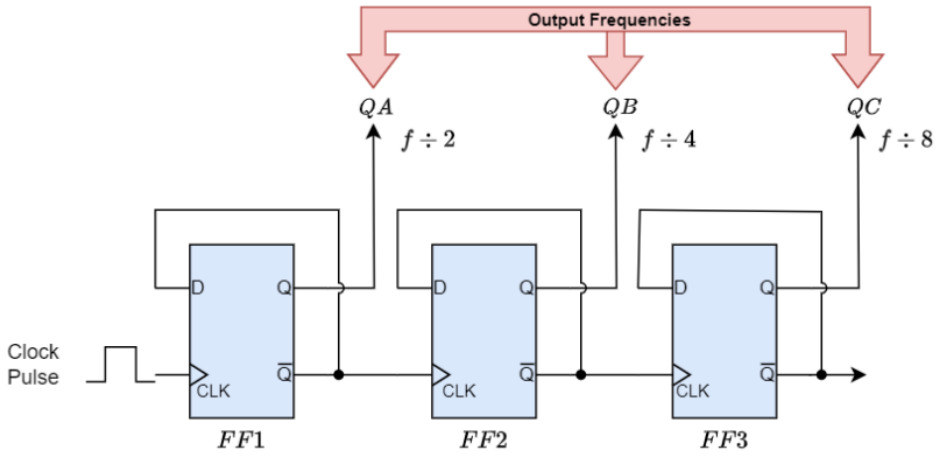
For example:

- Divide-by-2: If input clock is 1 kHz → output is 500 Hz
- Divide-by-4: If input clock is 1 kHz → output is 250 Hz

It's also called a **clock divider** and is commonly built using **flip-flops**.

How It Works (Using Flip-Flops)

- A **T flip-flop** or **JK flip-flop with J = K = 1** toggles output on every clock pulse.
- This toggled output is **half the input frequency**.



LAB TASKS

TASK-01

Design and simulate a 3-bit Asynchronous Up (ripple) counter using flip-flops in Circuit Maker 2000.

Solution:

Components Required (in Circuit Maker 2000)

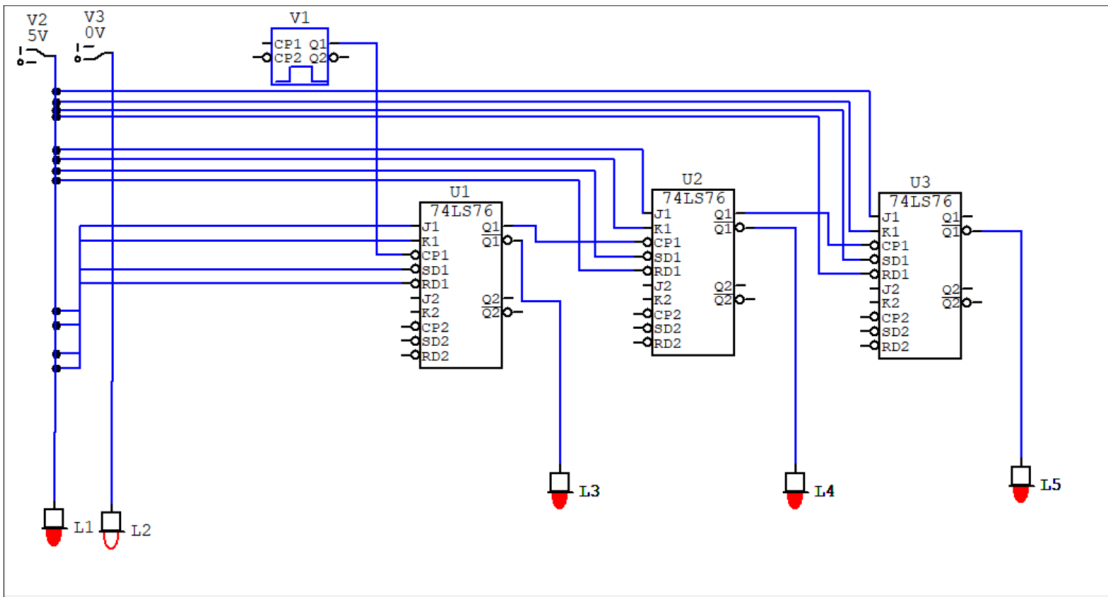
- 3 × JK Flip-Flops (or T Flip-Flops if available)
- 1 × Clock Pulse Source
- Wires for connections
- Logic probes (for outputs Q0, Q1, Q2)

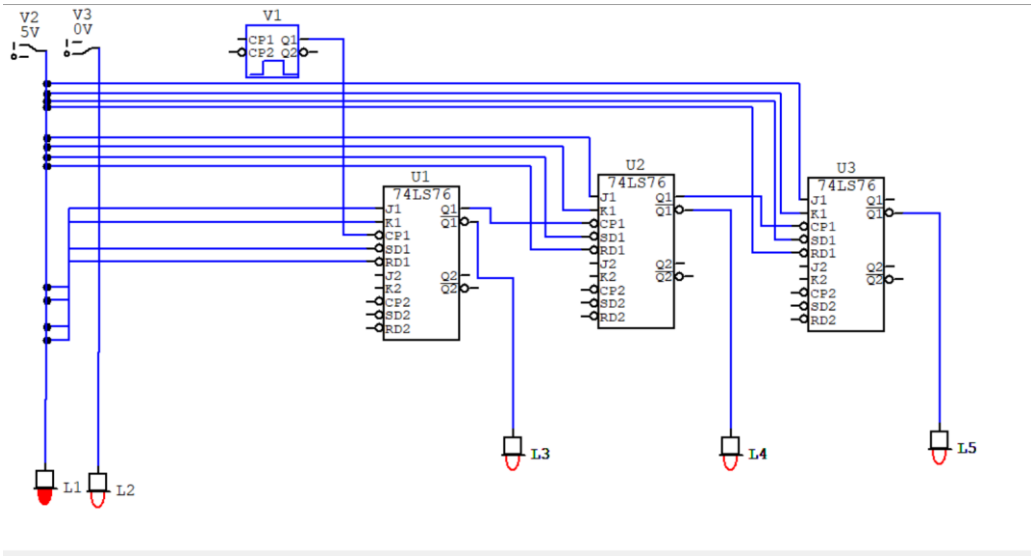
Truth Table of 3-bit Counter:

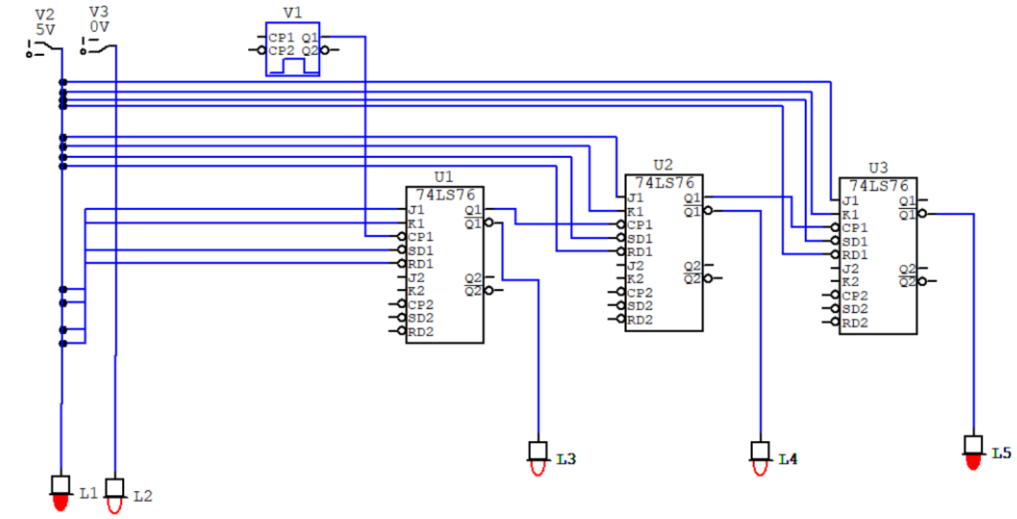
Count	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1

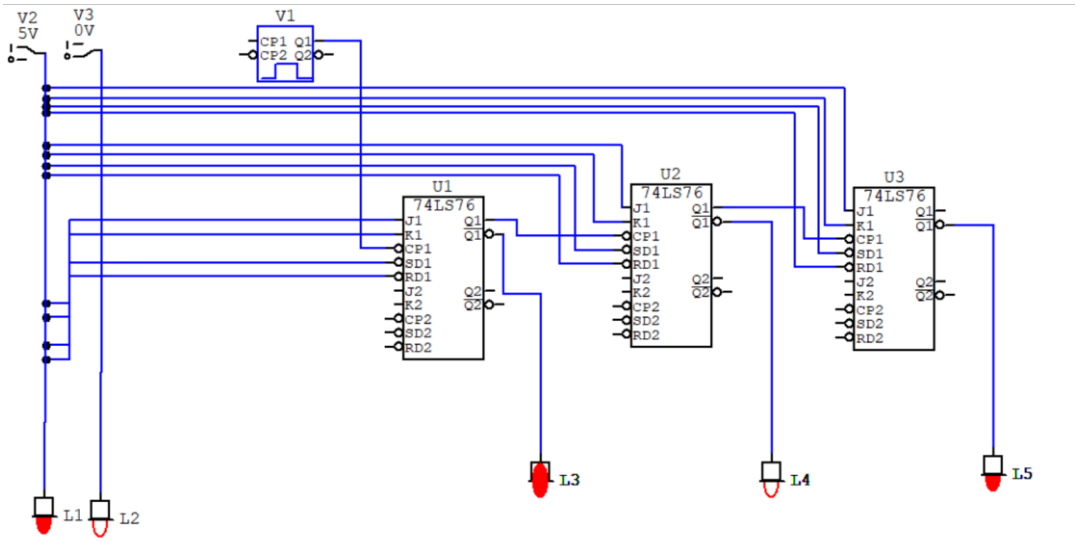
6	1	1	0
7	1	1	1

Circuit in Circuit Maker 2000:









These LEDs will follow **binary counting pattern** like this:

Clock Pulse	L5 (Q3)	L4 (Q2)	L3 (Q1)	Binary
0	OFF	OFF	OFF	000
1	OFF	OFF	ON	001
2	OFF	ON	OFF	010
3	OFF	ON	ON	011
4	ON	OFF	OFF	100
5	ON	OFF	ON	101

6	ON	ON	OFF	110
7	ON	ON	ON	111
8	OFF	OFF	OFF	000

TASK-02

Design and simulate a 4-bit Asynchronous Up (ripple) counter using flip-flops in Circuit Maker 2000.

Solution:

TASK-03

Design a divide-by-2, and divide-by-4 frequency divider using JK flip-flops.

Solution: