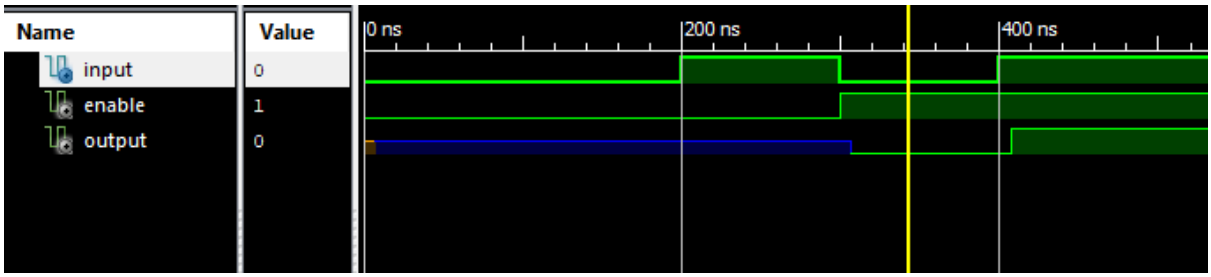
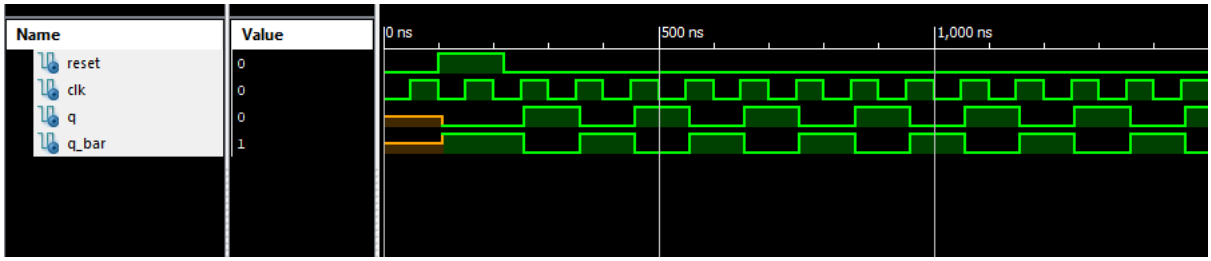
Lab 3 Simulations

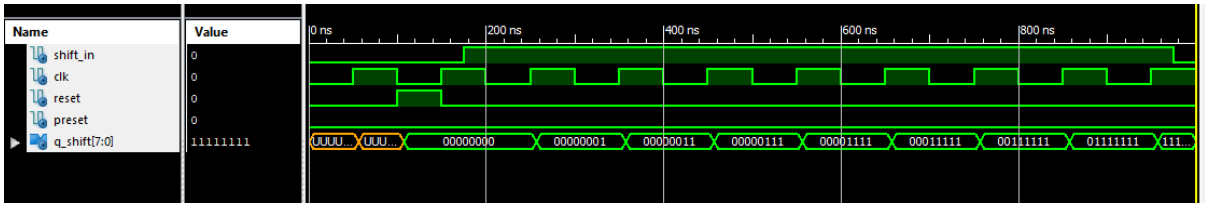
Tri State buffer



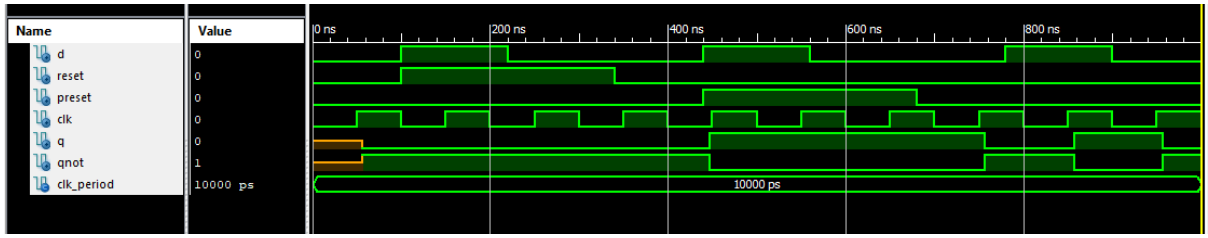
T-type flip-flop



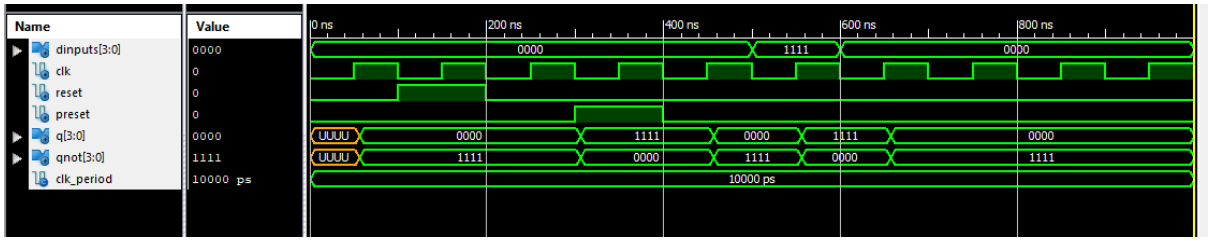
n-bit shift register



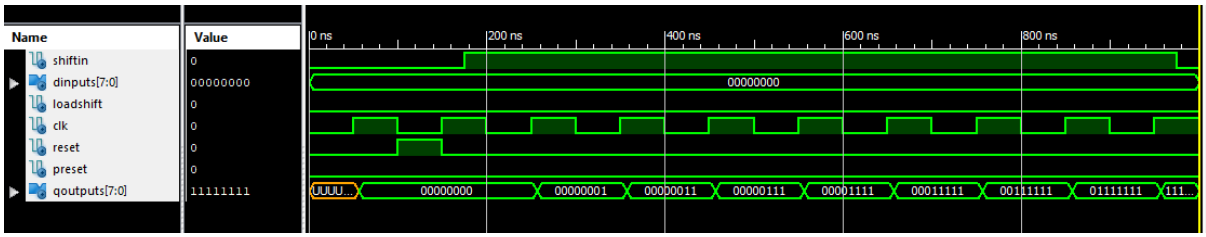
D flip-flop



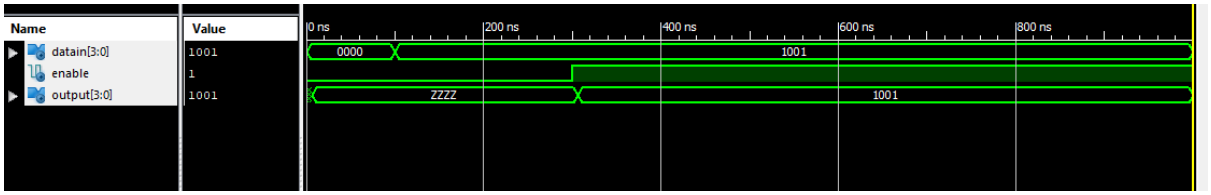
n-bit register



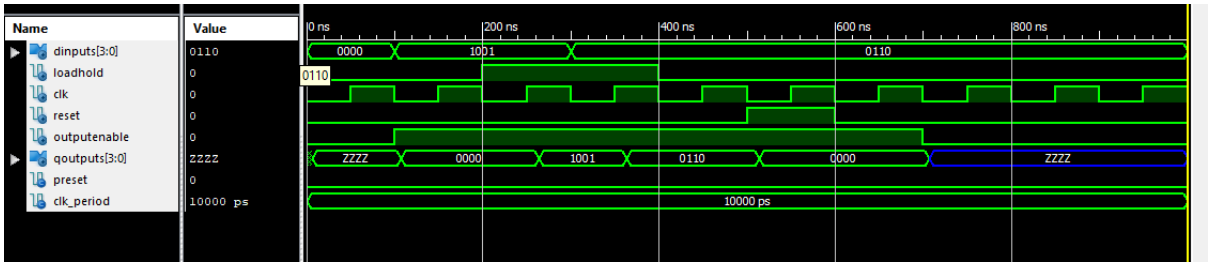
n-bit register with load/~hold control



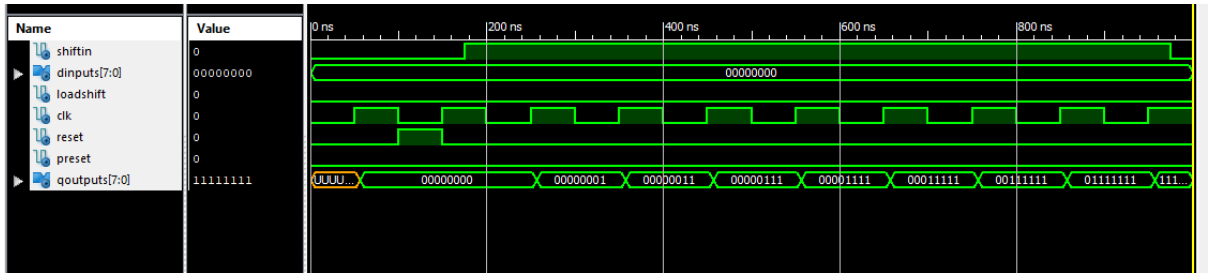
n-bit tri-state buffer



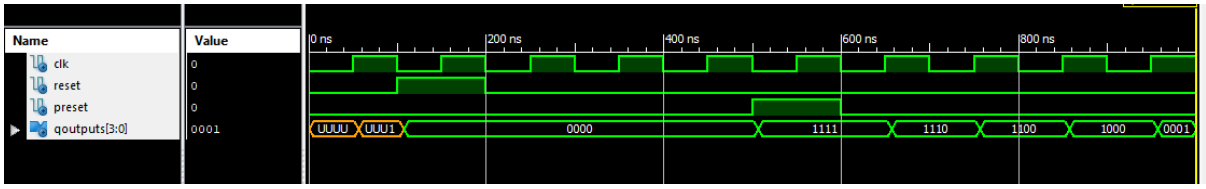
n-bit register load/~hold and tri-state output enable



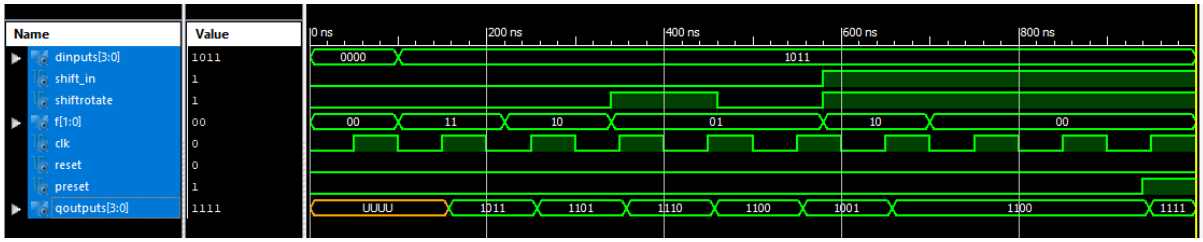
n-bit shift register with parallel load input



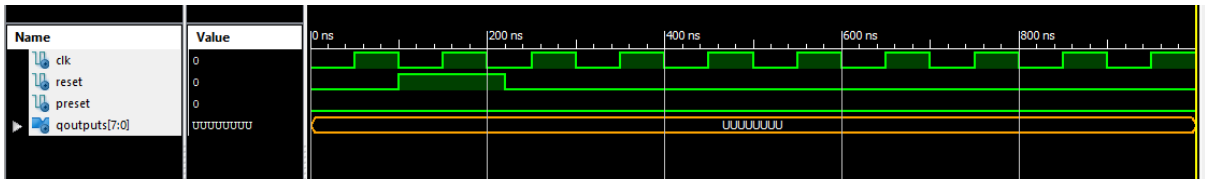
4-bit linear feedback shift register



n-bit universal shift register



n-bit twisted ring counter


Name
Value
clk
reset
preset
qoutputs[7:0]
0
0
0
UUUUUUUU
0 ns
200 ns
400 ns
600 ns
800 ns
UUUUUUUU