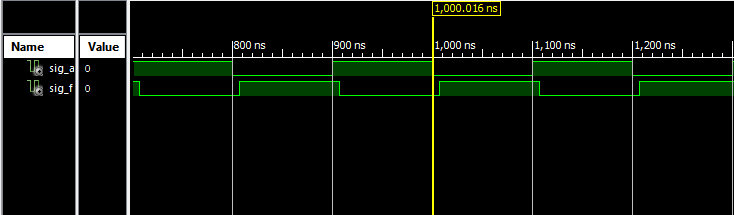
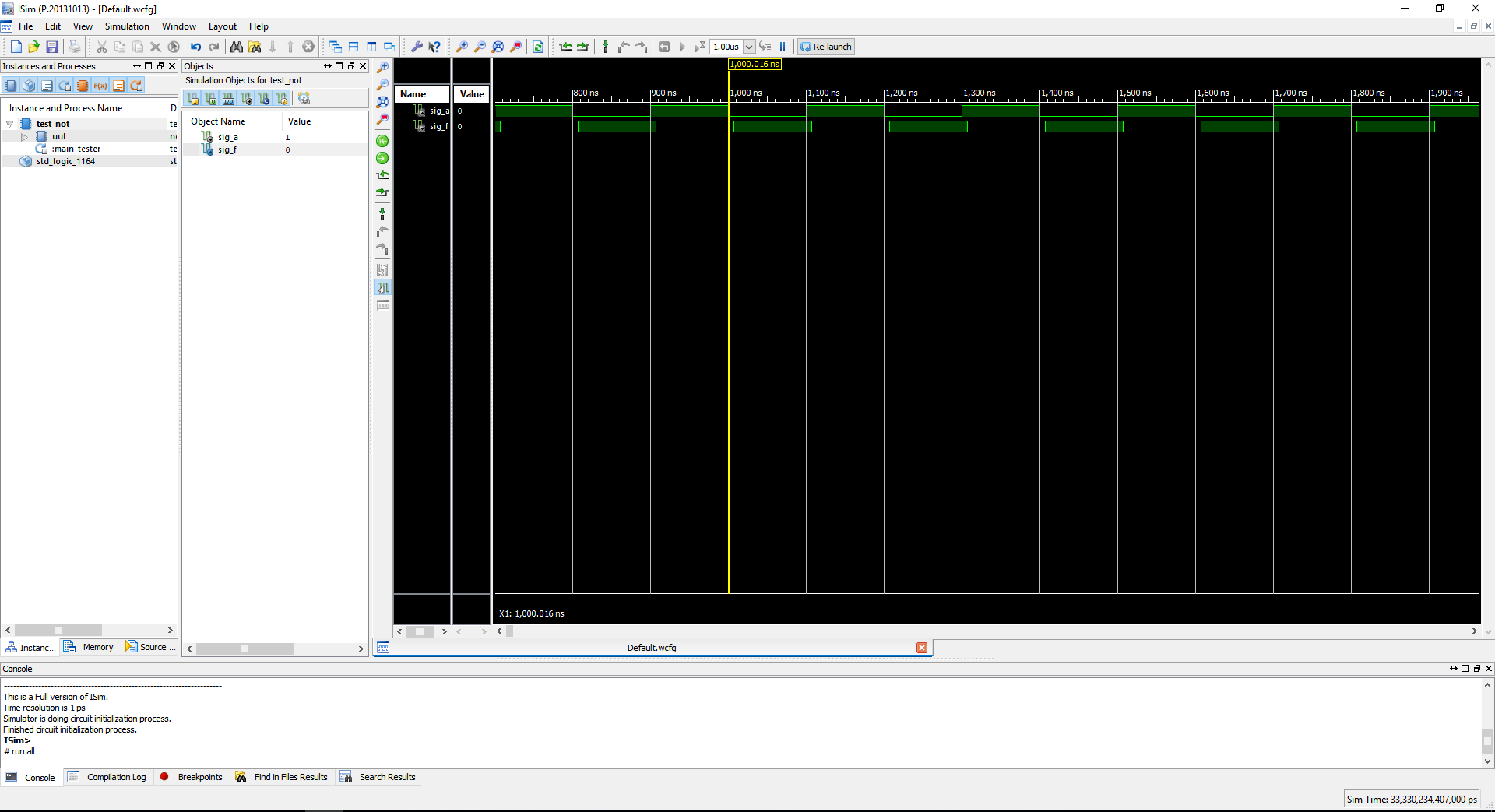
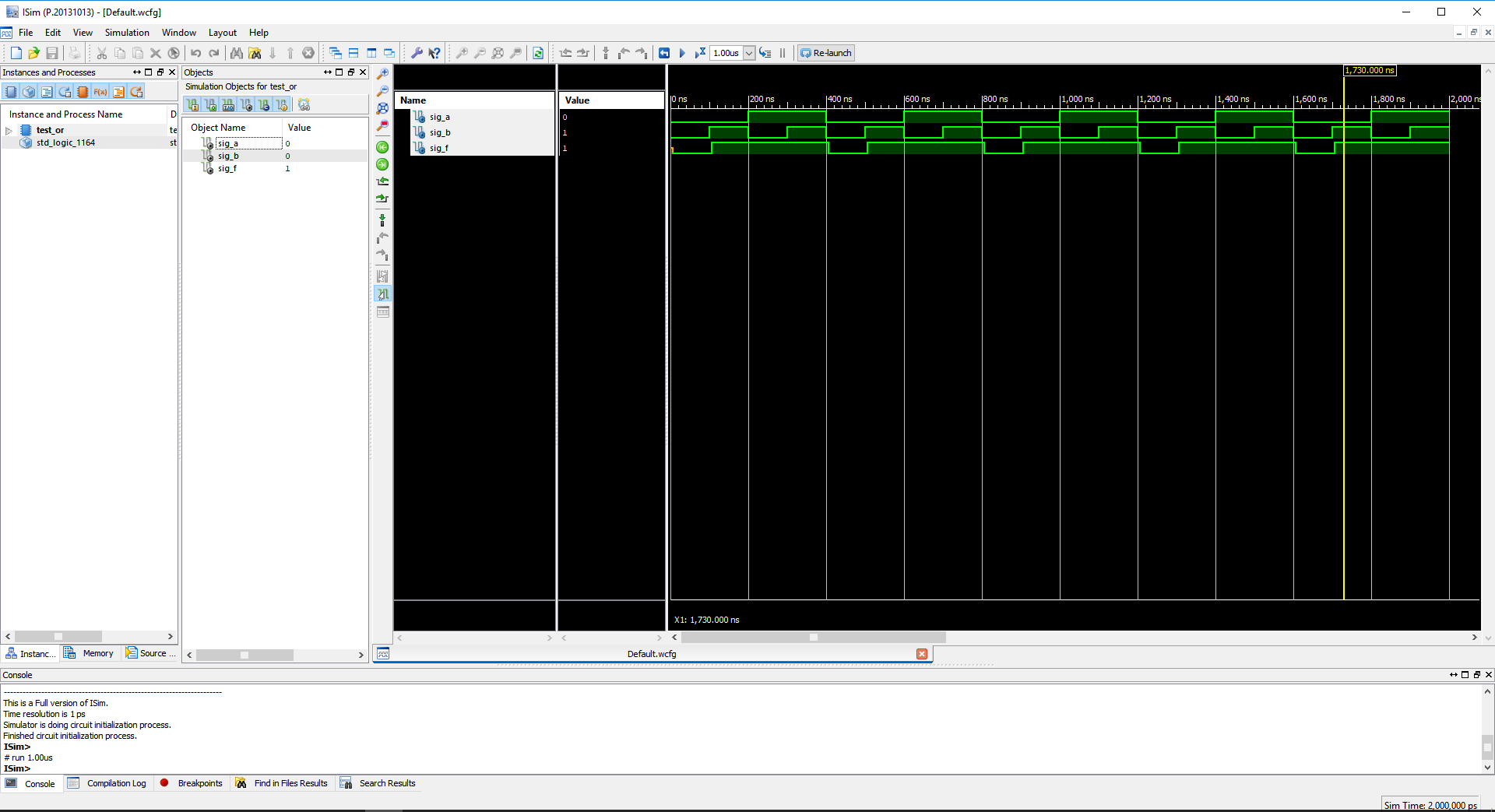
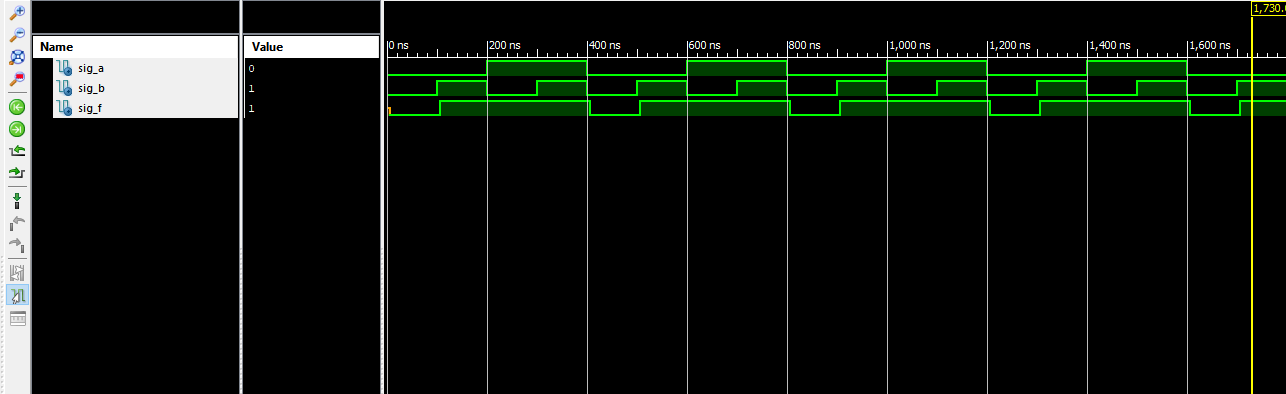
**Lab 1 Simulation**

NOT Gate

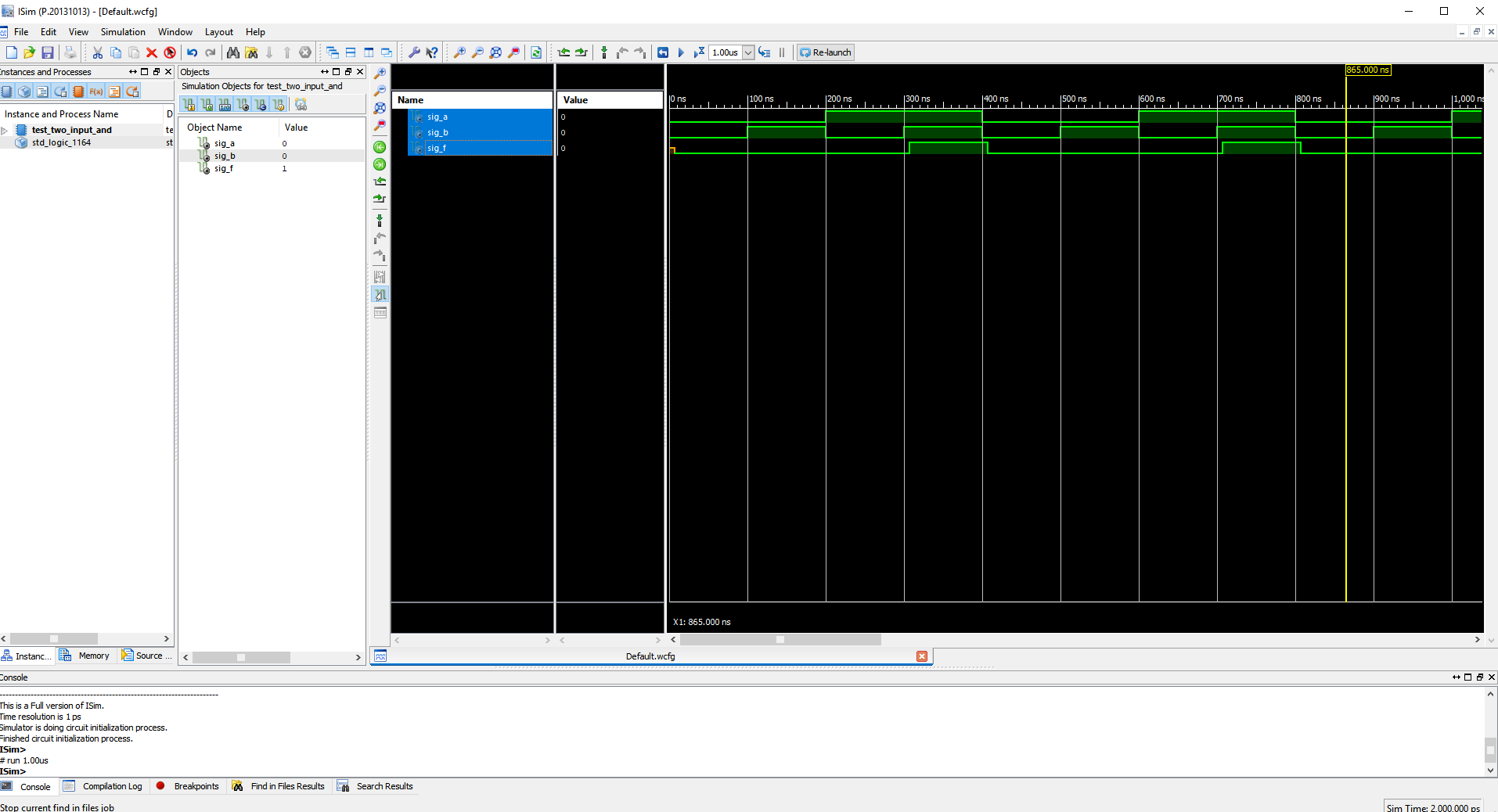


OR Gate



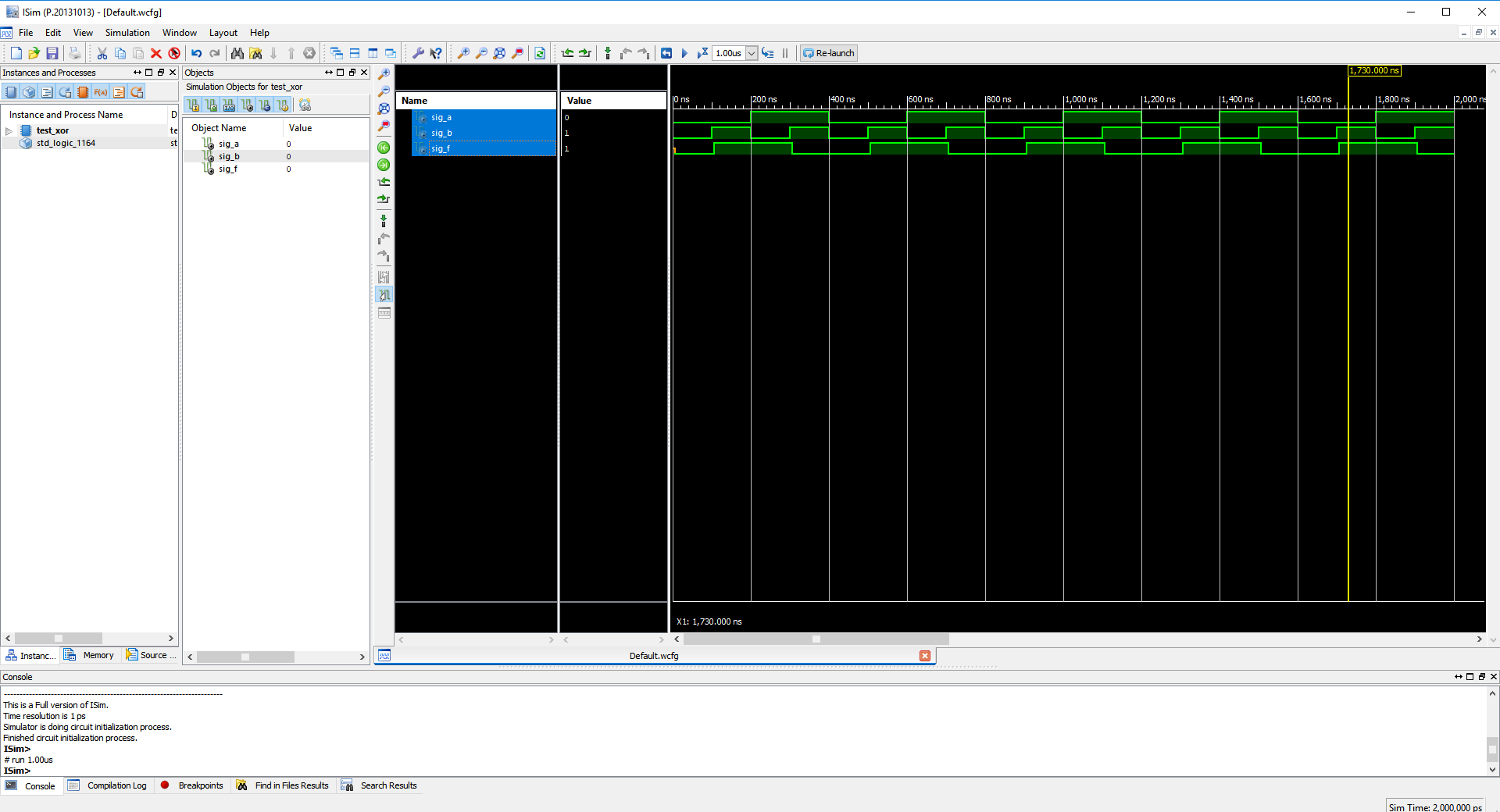


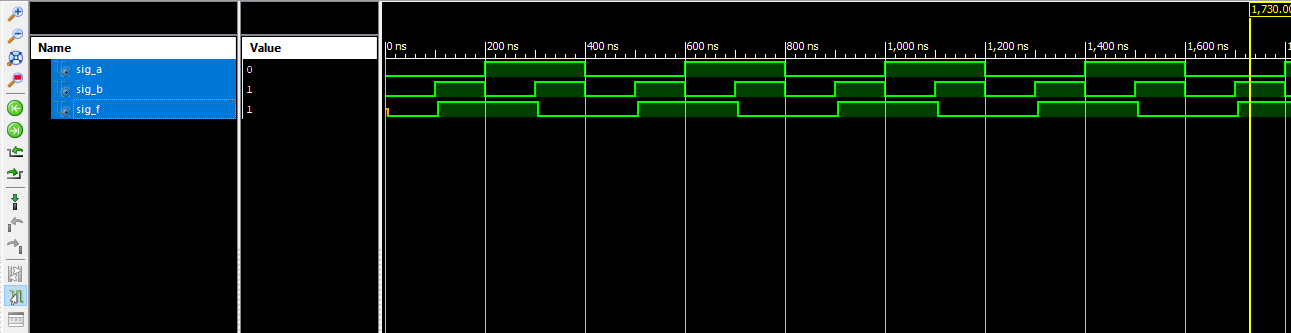
AND Gate



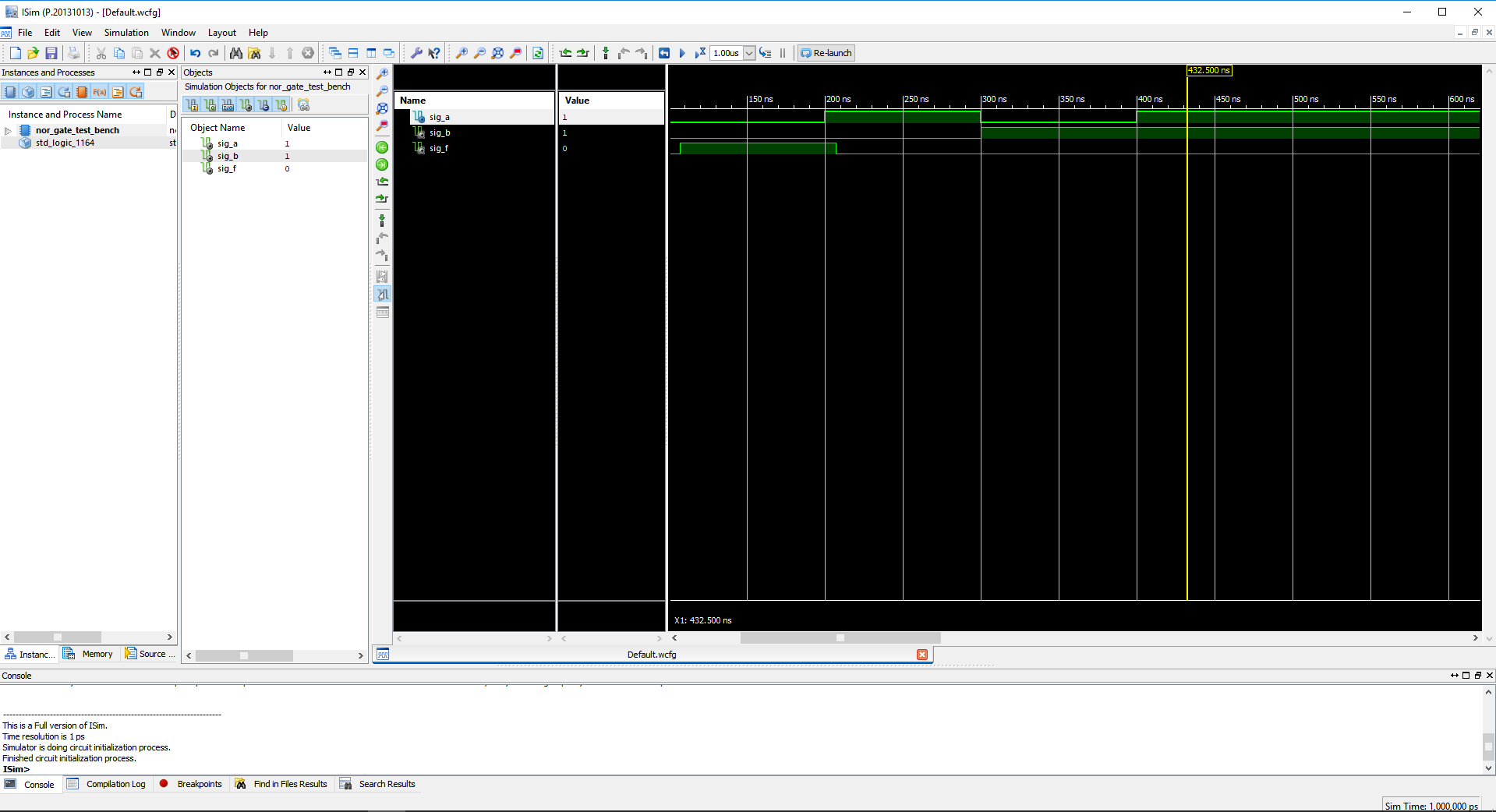


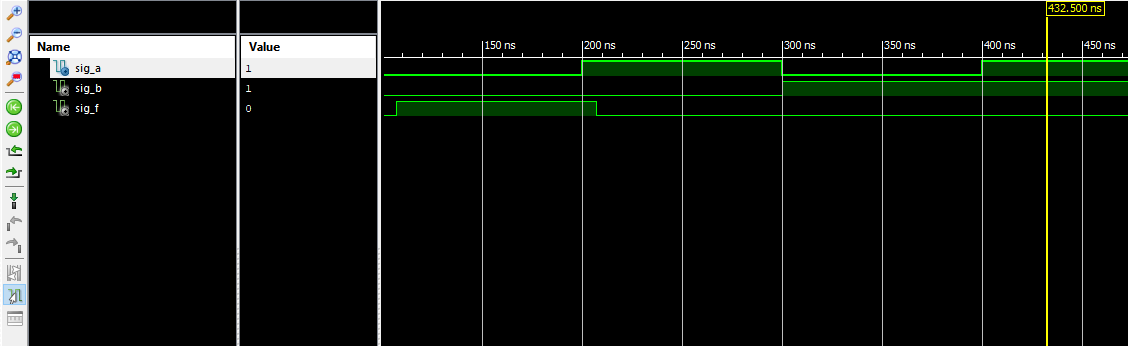
XOR Gate



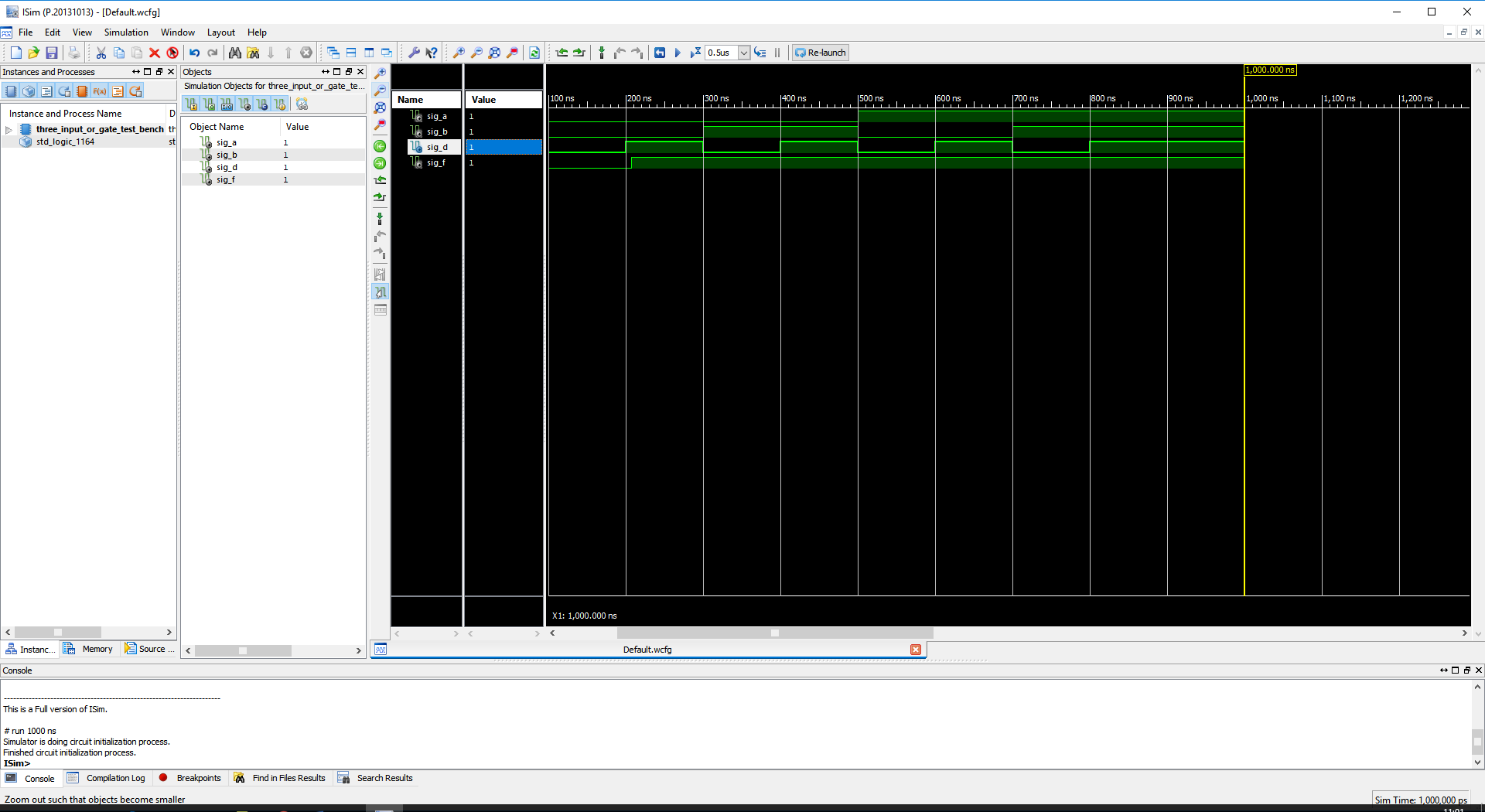


NOR gate



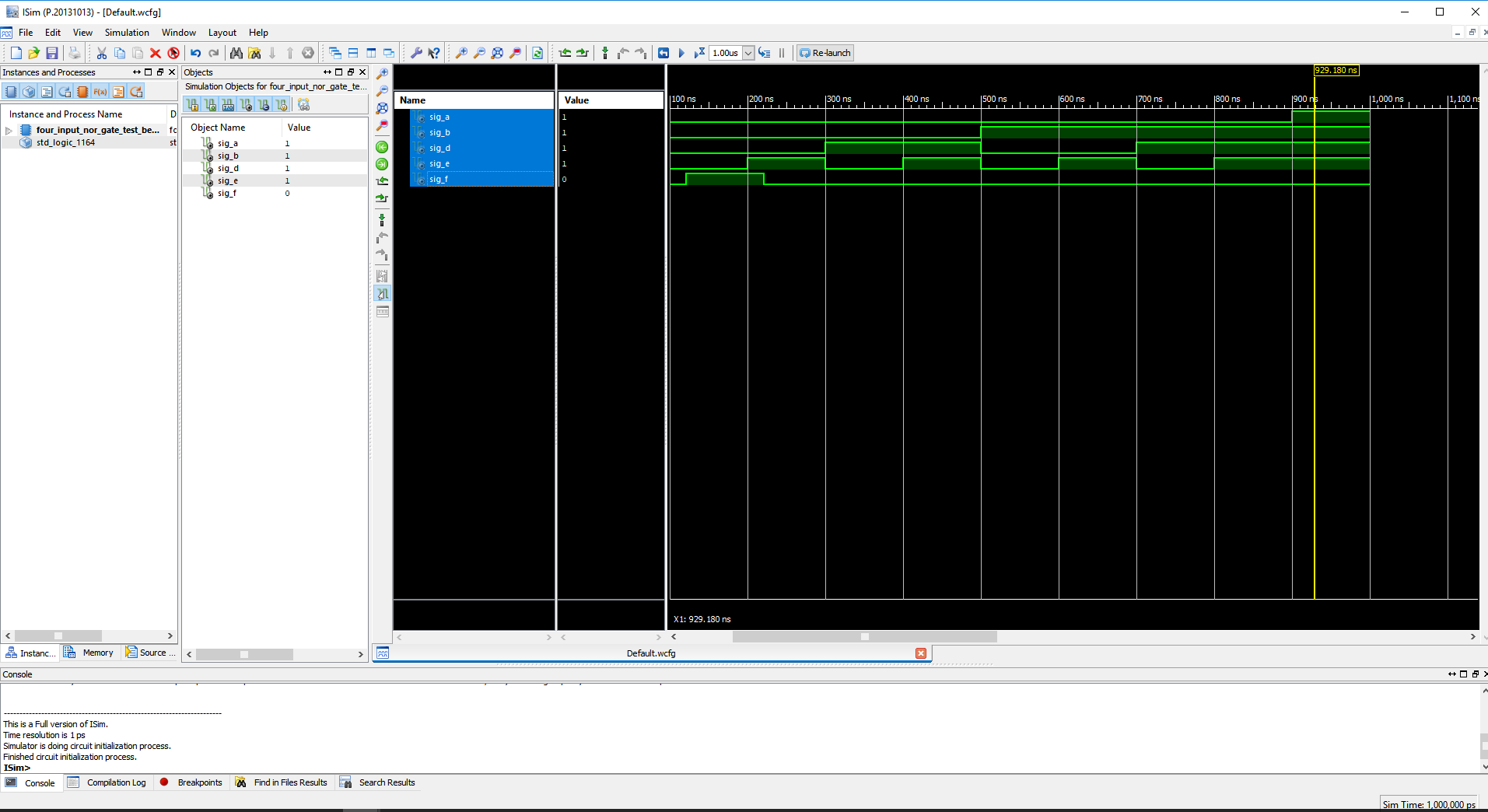


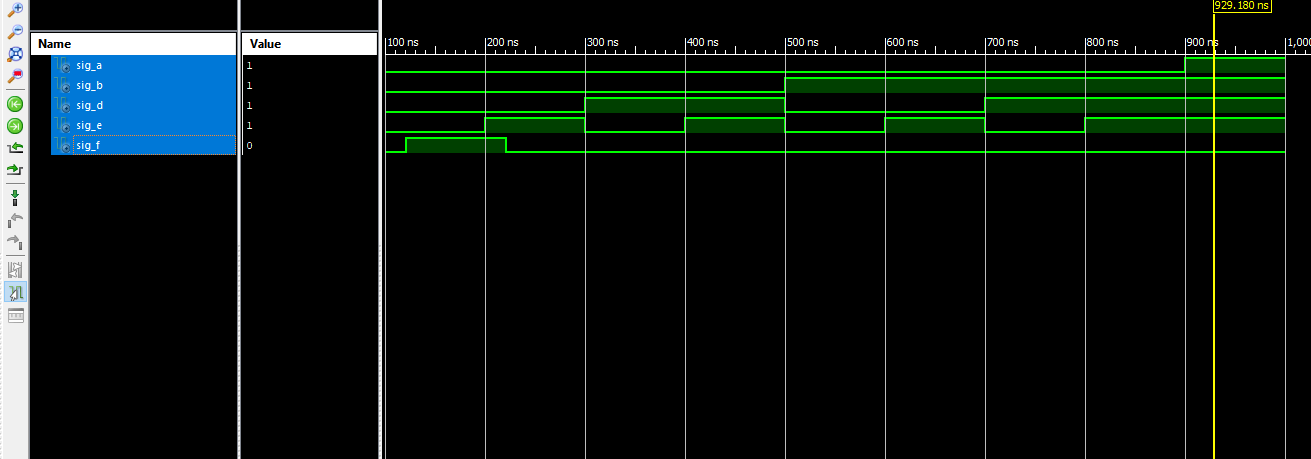
Three input or gate



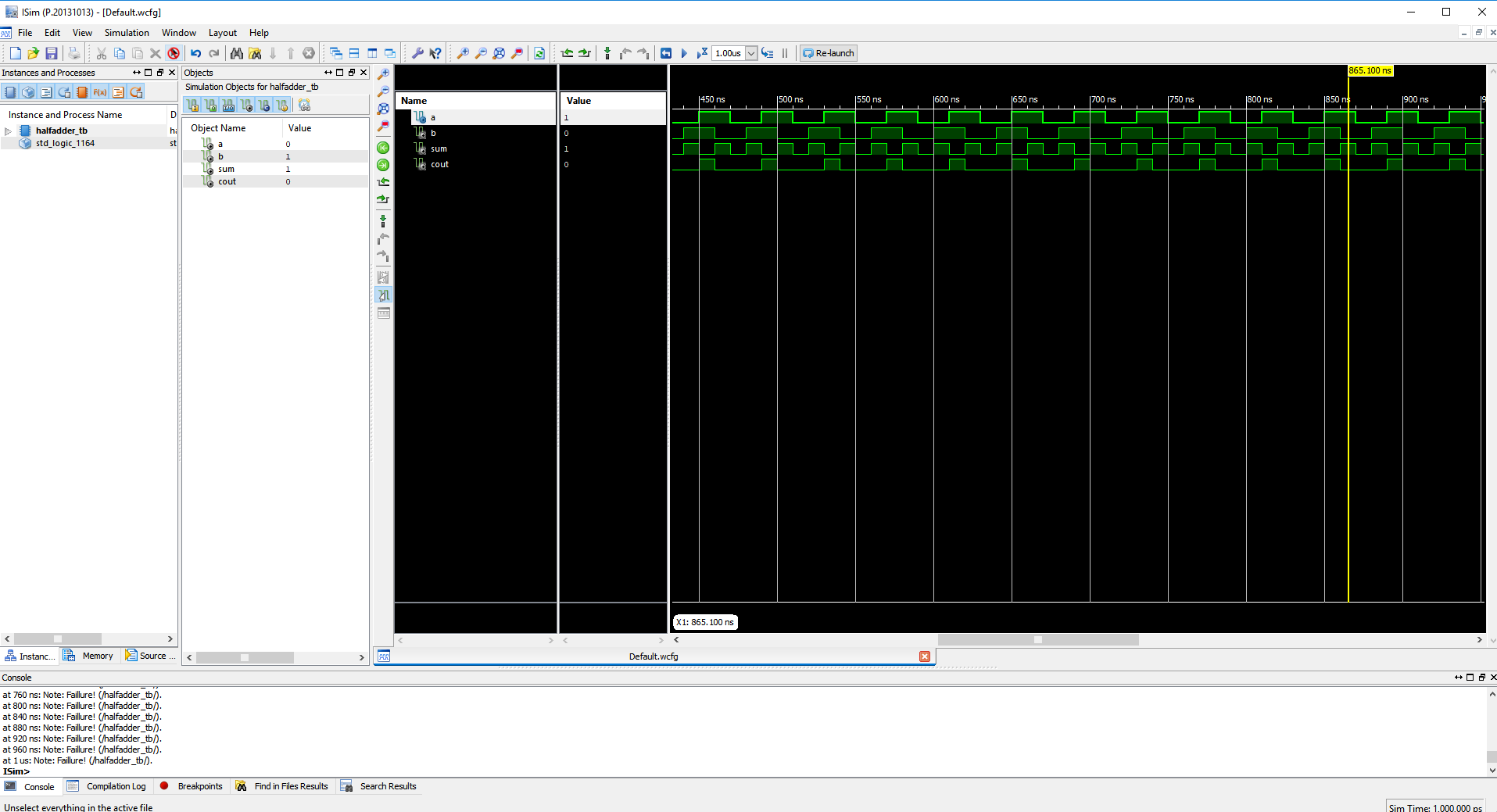


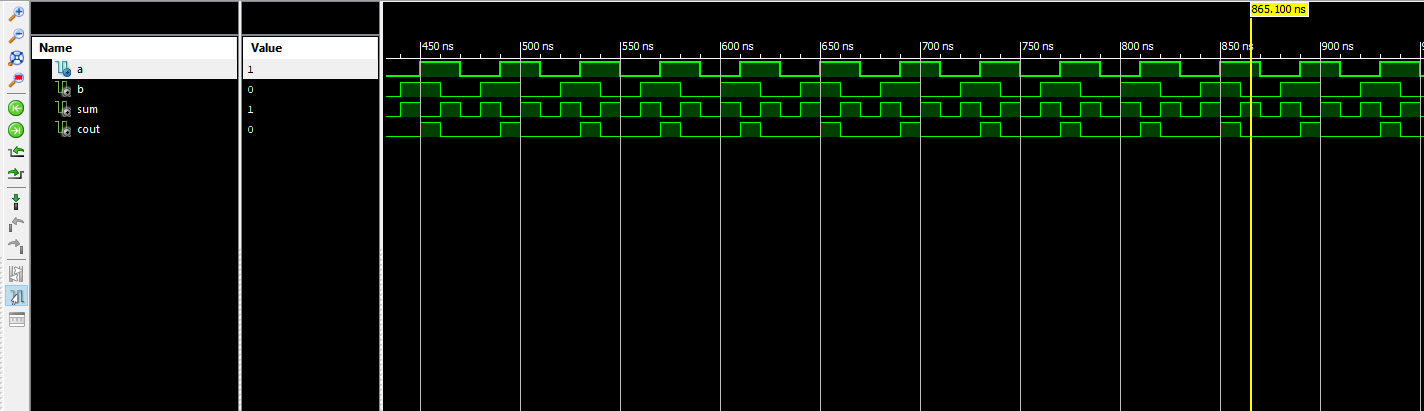
Four input nor



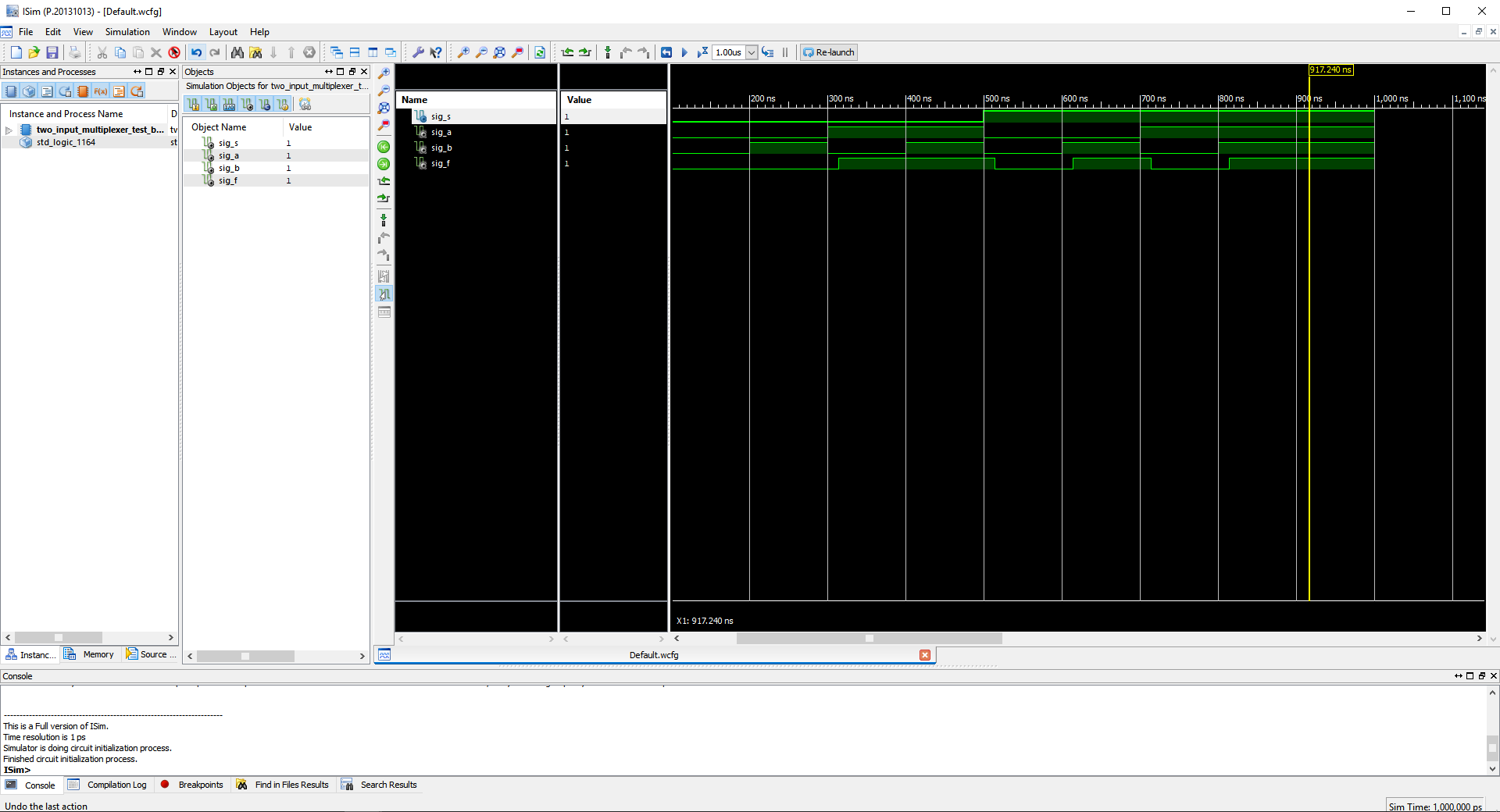


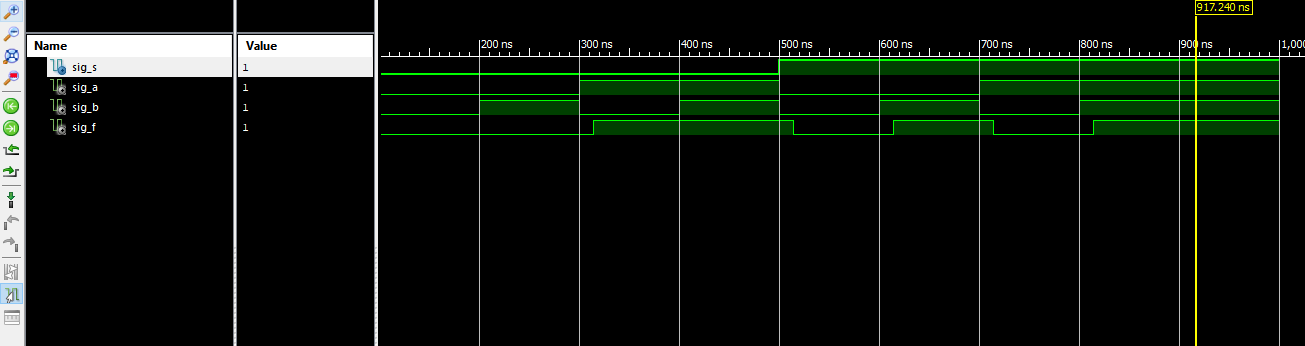
Half adder



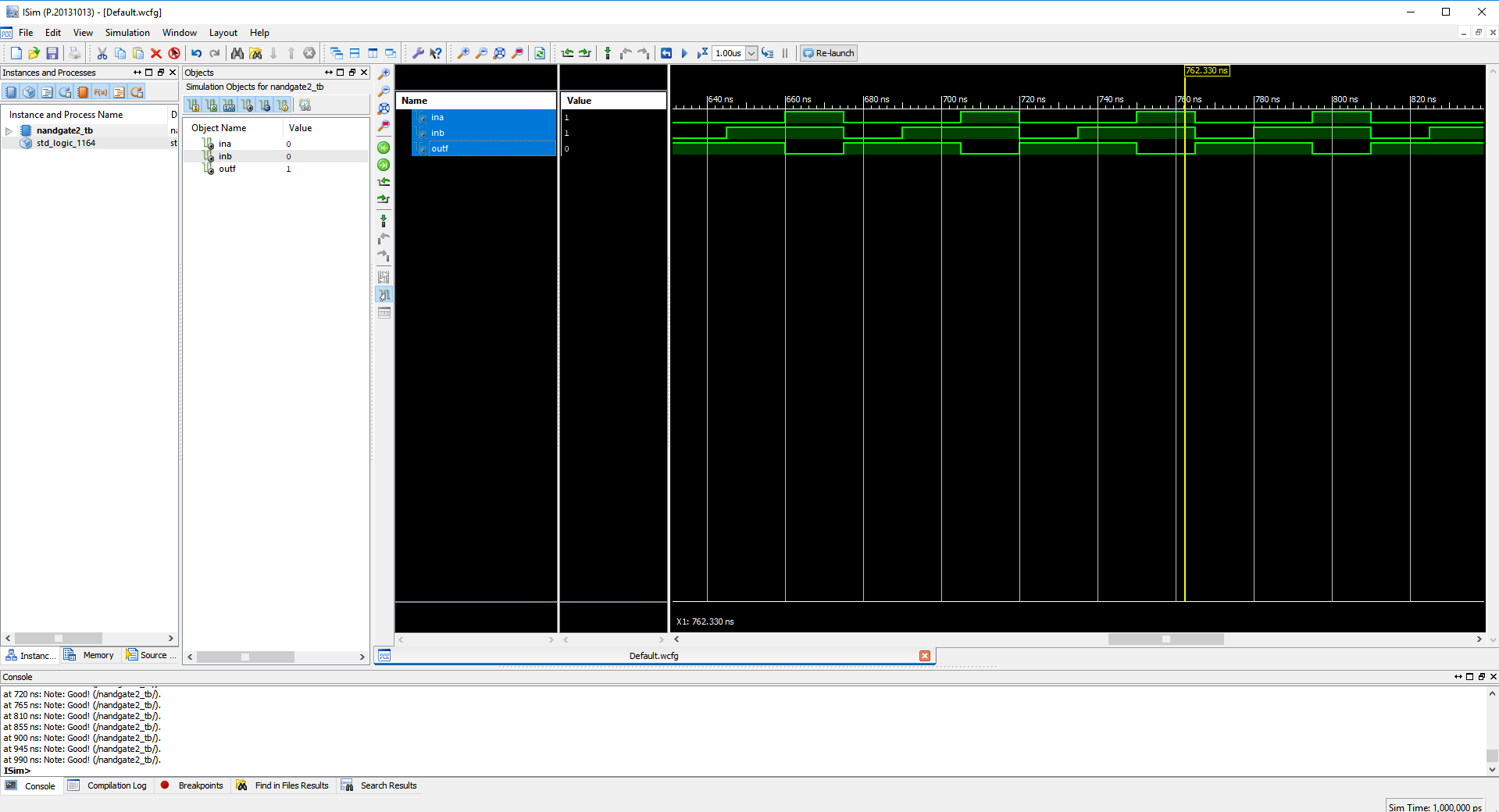


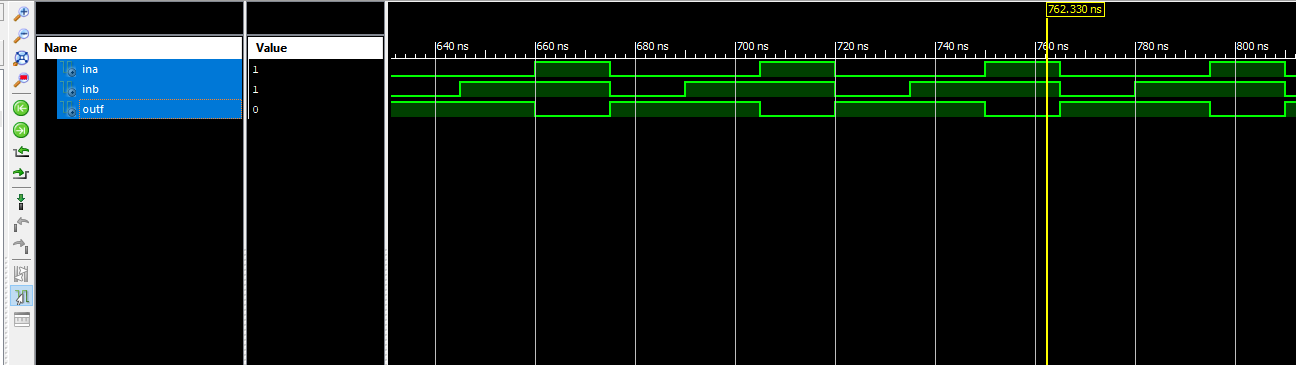
Two input multiplexer





Nand gate





Full adder

