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Lab5 Monday 3:30pm

Experiment (1):

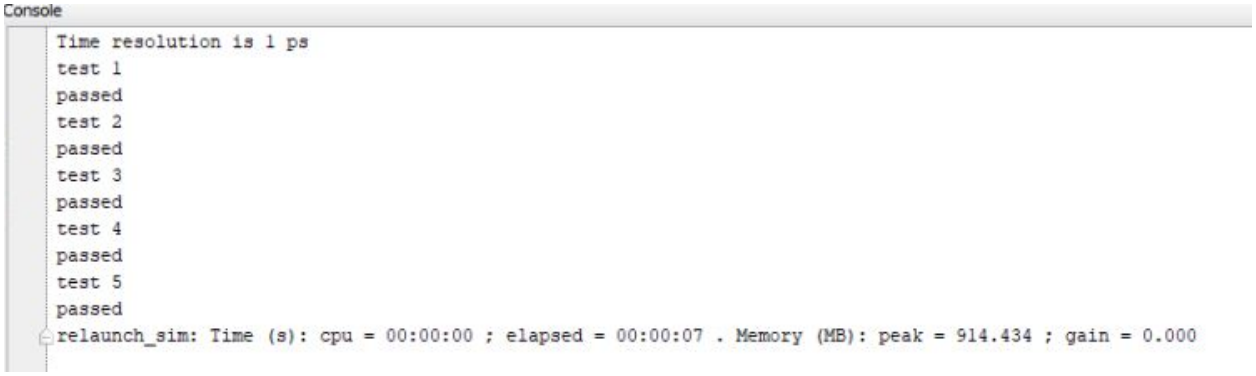
Summary :

In this experiment, we designed a memory instruction unit that takes the instruction encoding. It takes the address from the pc (7bits) and outputs a 32 bit data_out.

Steps:

1. We were provided with the source code in the lab manual
2. We developed a testbench for it that has 5 test cases

Output:



It passed the 5 test cases we assigned to it.

Simulation:

Brief interpretation:

1. We initialized the memory with some values in the source code
2. The values are:

mem[0]=17; mem[1]=9; mem[2]=25; mem[3]=55 ;mem[4]=40;

So the output is right accordingly

Experiment (2):

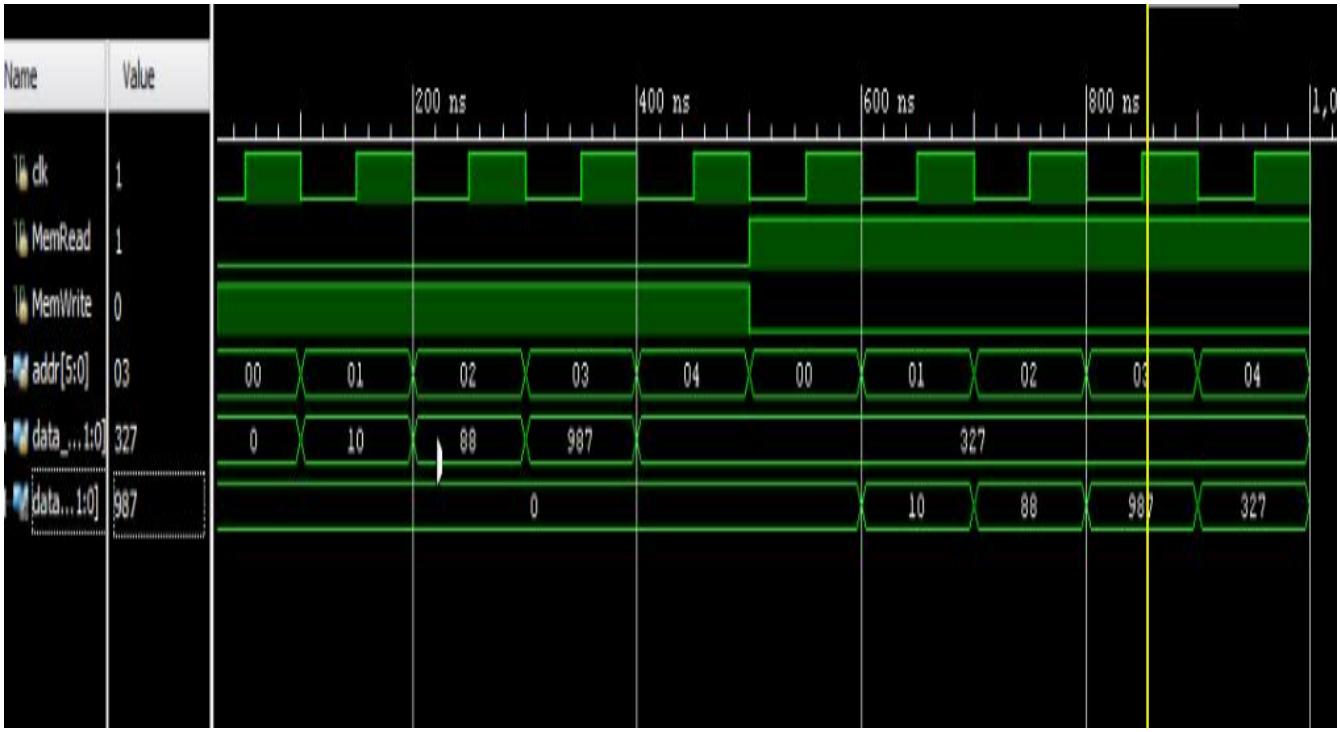
Summary :

In this experiment, we designed a memory module.we implemented a word addressable data memory of 64 words with 6 address bits.

Steps:

1. The full code were provided in the lab manual
2. We developed a testbench for it using 5 test cases
3. We discarded the least significant 2 bits and the ALU computes the byte address of the data item to be loaded or stored, we divided it by 4 before connecting it to the address input of the data memory to convert it to a word address.

Simulation:



Brief interpretation:

1. When enabling memwrite, we are writing on the memory. So data_in are changing according to the imputed values in the testbench
2. When disabling memwrite and enabling memread signals, we are reading the values stored in the memory. So, the output is the value imputed lastly.

As for experiment (3) , we started in it and wrote its code but we are going to develop the testbench next lab :)