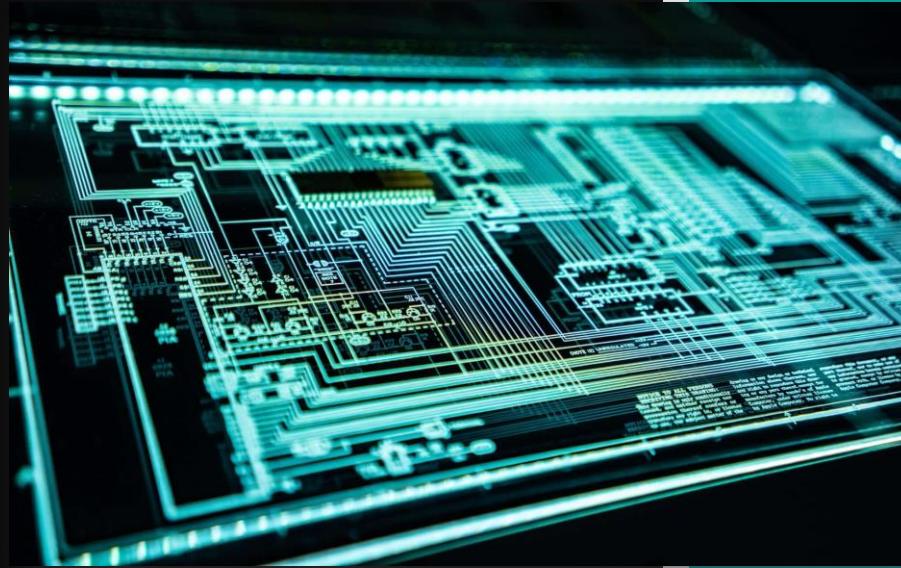


The American University at Cairo

Final Electronics (I) Project Report



Dr. Mohab Anis

TA: Eng. Omar Morsy

Salma Soliman:

900182325

Menna Hasan:

900182848

Abstract

In this project, we aim at designing and simulating circuits that are made out of devices we studied throughout the semester. The first circuit is an application of the (Bipolar Junction Transistor) BJT. It is an audio amplifier. The second circuit is an application of the (Operational Amplifier) OpAmp. It is a square wave generator and integrator circuit. The third circuit is CMOS applications which are some logic gates.

Introduction

This report will discuss in details the process of building some applications that depend on the BJT, the operational amplifier and the MOSFET.

One of the most important applications of the bipolar junction transistor is using it as an amplifier. In this project we aim to design an audio amplifier with specific power and output current characteristics. This could be done in four stages coupled together with capacitors, each with a bipolar junction transistor in the active mode.

The application based on the operational amplifier will be designing wave generators. The first wave generator to be discussed in detail in this report is the square wave generator, and the second is the triangular wave generator.

Last, we design logic gates using electronics components. And this component used is the MOSFET. The gates to be made are NOT, NAND, NOR, AND, OR.

Circuit (1): BJT Application, Audio Amplifier

Design approach:

The design purpose was to achieve:

- $v_o(\text{rms}) = 8 * 0.112 = 0.896 \text{ volts}$
- $i_L(\text{rms}) = 0.112 \text{ A}$

from a voltage input v_i (peak) = 10mV

In multisim, we can measure the value of currents and voltages peak to peak. In addition, peak to peak is better because we can use it to compute the AC gain directly, as it is independent of the DC values.

Therefore, all values were converted to peak to peak values using these formulas

$$V_{\text{rms}} = V_{\text{peak}} * \frac{1}{\sqrt{2}} \text{ (or } 0.7071)$$

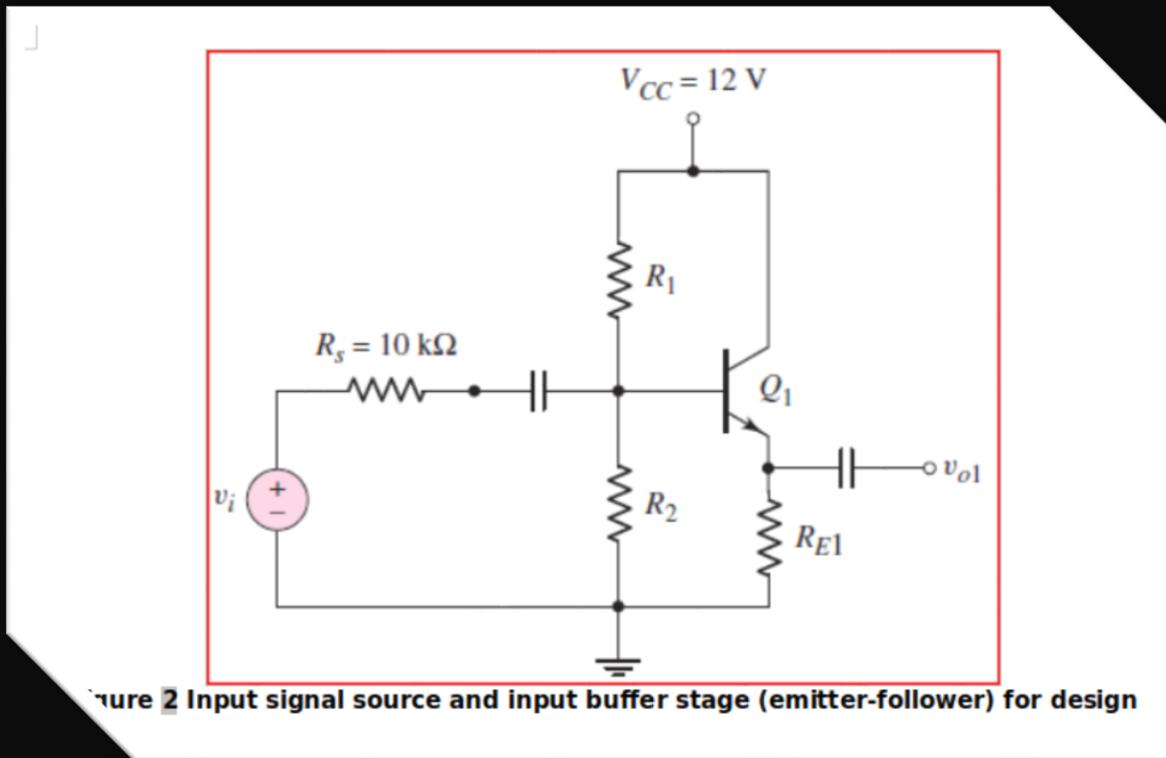
$$V_{\text{rms}} = V_{\text{peak-to-peak}} * \frac{1}{(2\sqrt{2})} \text{ (or } 0.35355)$$

$$V_{\text{rms}} = V_{\text{average}} * \frac{\pi}{(2\sqrt{2})} \text{ (or } 1.1107)$$

Therefore, the values we use are:

- $v_o(\text{peak to peak}) = 2.53 \text{ volts}$
- $i_L(\text{peak to peak}) = 0.3167 \text{ A}$
- $v_i(\text{peak to peak}) = 20 \text{ mV}$

This application is done over three stages. The first stage is a buffer stage. It basically eliminates the effect of the source resistance to supply the gain stage with the most possible portion of the voltage source. This is achieved by taking the output from the emitter part.



R_1 and R_2 :

These resistors form a voltage divider, establishing a voltage-divider bias for the base of transistor Q1. R_2 will develop about 1V. That's enough to forward bias the base junction of Q1, turning the transistor on.

C_1 : This is a coupling capacitor which allows the AC signal to pass but prevents the DC. It protects the microphone's coil from receiving a DC current from the amplifier's bias.

Q1:

This BJT is the heart of the first amplification stage, a common-emitter (CE) voltage amplifier. Its job is to transform variations in the base current caused by the microphone voltage variations arriving over C_1 into current variations through the collector-emitter circuit R_{E1} and C_2 .

Hand written analysis:

in DC

we have $I_{C1} = 1mA$
 $\therefore I_E1 = 1.01 \text{ mA}$

$V_{CE} = 6V$ & $V_C = 6V$

$R_{E1} = \frac{12 - 6}{1.01} = 6k\Omega$

$r_{\pi} = \frac{0.025(100)}{1 \times 10^{-3}} = 2.5k\Omega$

AC

gain = $\frac{V_{o1}}{V_i} \quad \& \quad V_{o1} = 101 i_b (6k)$

$\therefore \text{gain} = \frac{101(6k)(R_m)}{(10k + [R_m \parallel (2.5 + 101(6k))])(102.5k + 101(6k))}$

→ by using different values for $R_m = R_1 \parallel R_2$
we chose $R_m = 100k\Omega$ as it makes $\text{gain} = 0.892$

Back to DC

$\frac{V_m - 6.7}{100k} = I_B \quad \therefore V_m = 7.7$

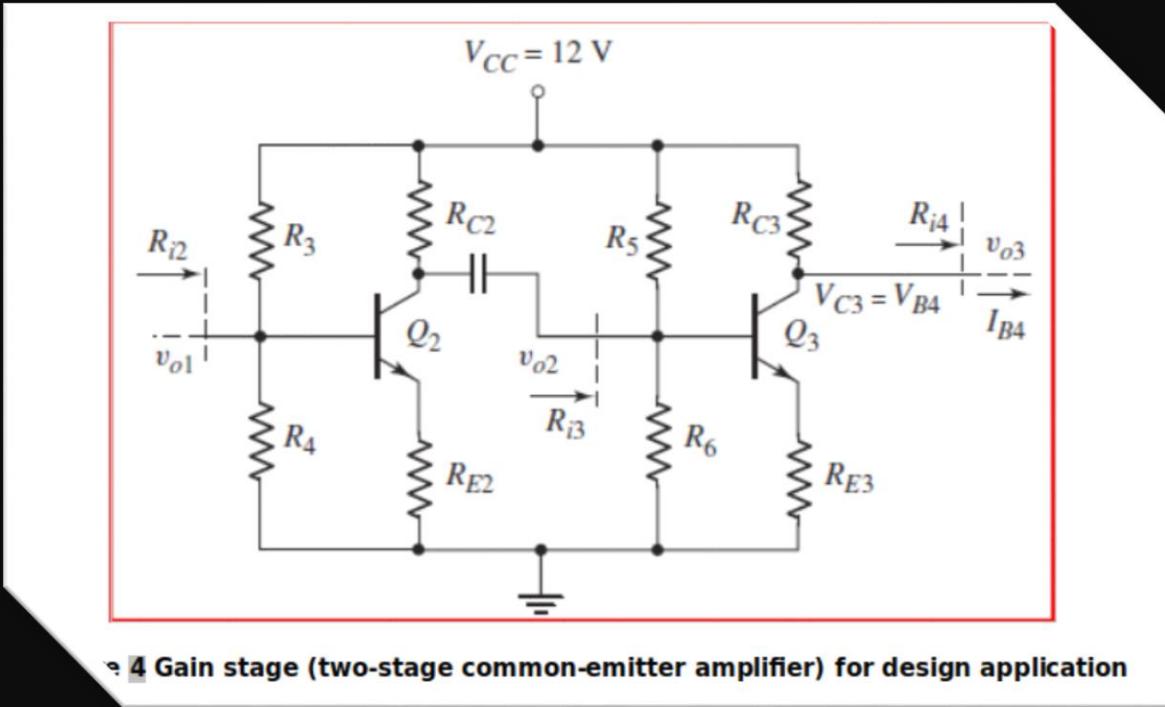
$\therefore V_m = \frac{R_2}{R_1 + R_2} \cdot 12 = 7.7$
 $\therefore \frac{100k \cdot 12}{R_1} = 7.7$

$\therefore R_m = \frac{R_1 R_2}{R_1 + R_2} = 100k$
 $\therefore \frac{R_2}{R_1 + R_2} = \frac{100k}{R_1}$

$\therefore R_1 = 155 \Omega \quad \& \quad R_2 = 280k\Omega$

→ if we want $V_i = 10mV \text{ peak}$
 $\therefore V_{o1} = 8.92mV \text{ peak}$

The gain stage:



Hand written analysis

(Gain Stage)

$$\therefore V_{O_3} = 1.28 \text{ and the Gain} = \frac{V_{O_3}}{V_{O_1}} = \frac{1.28}{8.928 \times 10^{-3}} = 143.36 \approx 144$$

\therefore we will assume that

The first stage gain is 12

and the second stage gain is 12

This is the
whole gain

$$\therefore \frac{V_{O_3}}{V_{O_2}} = 12 = \frac{1.28}{V_{O_2}} \Rightarrow V_{O_2} = 0.1066$$

The same

$$\frac{V_{O_2}}{V_{O_1}} = 12 \Rightarrow \frac{V_{O_2} - V_{O_1}}{8.928 \times 10^{-3}} \Rightarrow V_{O_2} = 0.106$$

Resistors \therefore To get R_{C_3}

$$\therefore V_{E_1} = 6V \quad \therefore V_{B_1} = V_{C_3} = 6.7$$

$$\therefore I_{E_1} = 0.375 A \quad \therefore I_{B_1} = \frac{0.375}{101} = 3.71 mA$$

$$\text{let's assume } I_{\text{total}} = 3.71 mA + \underbrace{0.01667}_{\text{assumed } I_{C_3} = 16.67 mA} = 0.02038$$

$$R_{C_3} = \frac{12 - 6.7}{0.02038} = \boxed{260 \Omega}$$

$$\therefore I_{E_3} = \frac{I_{C_3(B+1)}}{B} = \frac{16.67}{101} = 0.1651 A$$

$$\therefore I_{B_3} = 1.651 \times 10^{-3} A$$

$$\therefore I_{B_3} = 1.651 \times 10^{-3} A$$

$$\frac{V_{O3}}{V_{O2}} = 12$$

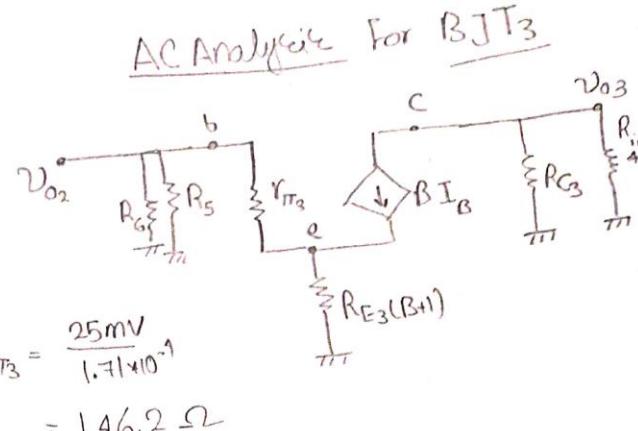
$$\frac{V_{O3}}{V_{O2}} = \frac{\beta (R_{C3} \parallel R_{in})}{r_{\pi_3} + (\beta+1) R_{E3}}$$

$$12 = \frac{100 (R_{E3} \parallel 595.4)}{146.2 + 101 * R_{E3}}$$

$$1467.2 = 146.2 + 101 R_{E3}$$

$$R_{E3} = 13 \Omega \approx 15 \Omega$$

$$\text{assume } R_5 \parallel R_6 = 100 \text{ k}\Omega$$



$$r_{\pi_3} = \frac{25 \text{ mV}}{1.71 \times 10^{-3}} = 146.2 \Omega$$

$$R_{in3} = R_6 \parallel R_5 \parallel (r_{\pi_3} + R_{E3}(B+1))$$

$$= 100 \text{ k} \parallel (146.2 + 15 \times 101) = 1634 \Omega$$

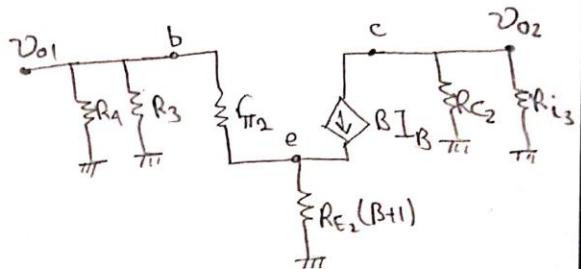
$$\Rightarrow [R_5 = 155 \text{ k}, R_6 = 280 \text{ k}]$$

BJT (2)

$$\text{assume } V_{C2} = 6 \text{ , } I_{C2} = 6 \text{ mA}$$

$$R_{C2} = \frac{12 - 6}{6} = 1 \text{ k}\Omega$$

$$r_{\pi_2} = \frac{B V_{th}}{I_{C2}} = \frac{100 \times 25 \text{ mV}}{6 \text{ mA}} = 416 \Omega$$



$$\frac{V_{O2}}{V_{O1}} = \frac{\beta (R_{C2} \parallel R_{in3})}{r_{\pi_2} + (1+\beta) R_{E2}} = \frac{100 (1 \text{ k} \parallel 1634)}{416 + 101 * R_{E2}} = 12$$

$$R_{E2} = 47 \Omega$$

$$\text{assume } R_3 \parallel R_4 = 100 \text{ k} \Rightarrow [R_3 = 155 \text{ k}, R_6 = 280 \text{ k}]$$

R_{E_1} can be approximated to $6K$, $r_{\pi_i} = 2.5K\Omega$, $R_1 = 155K$, $R_2 = 280K$

$$R_{in} = R_1 \parallel R_2 \parallel (r_{\pi_i} + R_{E_1}(B+1))$$

$$= (100K) \parallel (2.5K + 101 \times 6K)$$

$$= 85.8K\Omega$$

$$V_{o1} = i_b \times R_{E_1}(B+1)$$

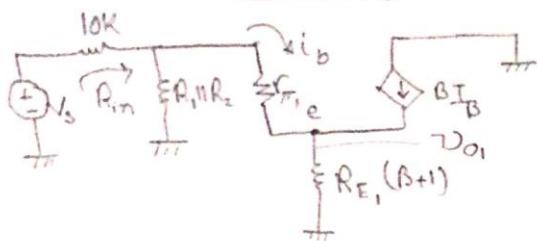
$$i_b = \frac{V_s}{10K + R_{in}} \times \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + r_{\pi_i} + R_{E_1}(B+1)}$$

$$\frac{V_{o1}}{V_s} = A_1 = \frac{R_{E_1}(B+1) \times R_1 \parallel R_2}{(10K + R_{in})(R_1 \parallel R_2 + r_{\pi_i} + R_{E_1}(B+1))}$$

$$= \frac{(6K)(101) \times (100K)}{(10K + 85.8K)(100K + 2.5K + 6K + 101)} = 0.8928$$

$$\text{Since } V_s = 10 \text{ mA} \implies V_{o1} = 89.28 \text{ mV}$$

AC analysis



The output stage:

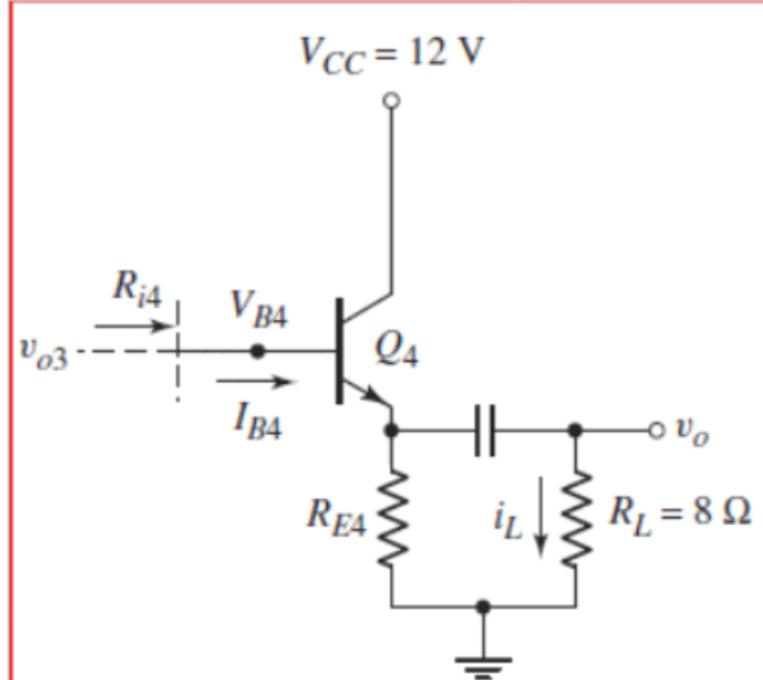


Figure 3 Output stage (emitter-follower) for design application

Hand written analysis

Output Stage

$$V_{o4} = (8)(0.1583) = 1.267 \text{ V}$$

Peak

$$\therefore \frac{V_{o4}}{V_{o3}} = \frac{1.267}{V_{o3}} = 0.99$$

$$\boxed{V_{o3} = \frac{1.267}{0.99} = 1.28}$$

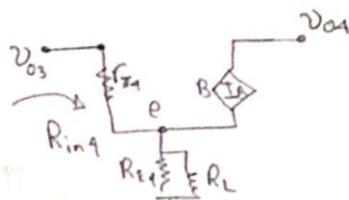
$$\begin{aligned} R_{in4} &= R_L \parallel R_{E4} + r_{\pi4} \\ &= [8 \parallel (16)] \times (101) + \frac{25 \text{ mV}}{0.375} \\ &= \boxed{545.41} \end{aligned}$$

\therefore The output Gain should be 0.99

\therefore We will assume that $R_L = 16 \Omega$ and also assume that $V_{CE4} = 6$

$$\therefore V_{E4} = 12 - 6 = 6 \text{ V}$$

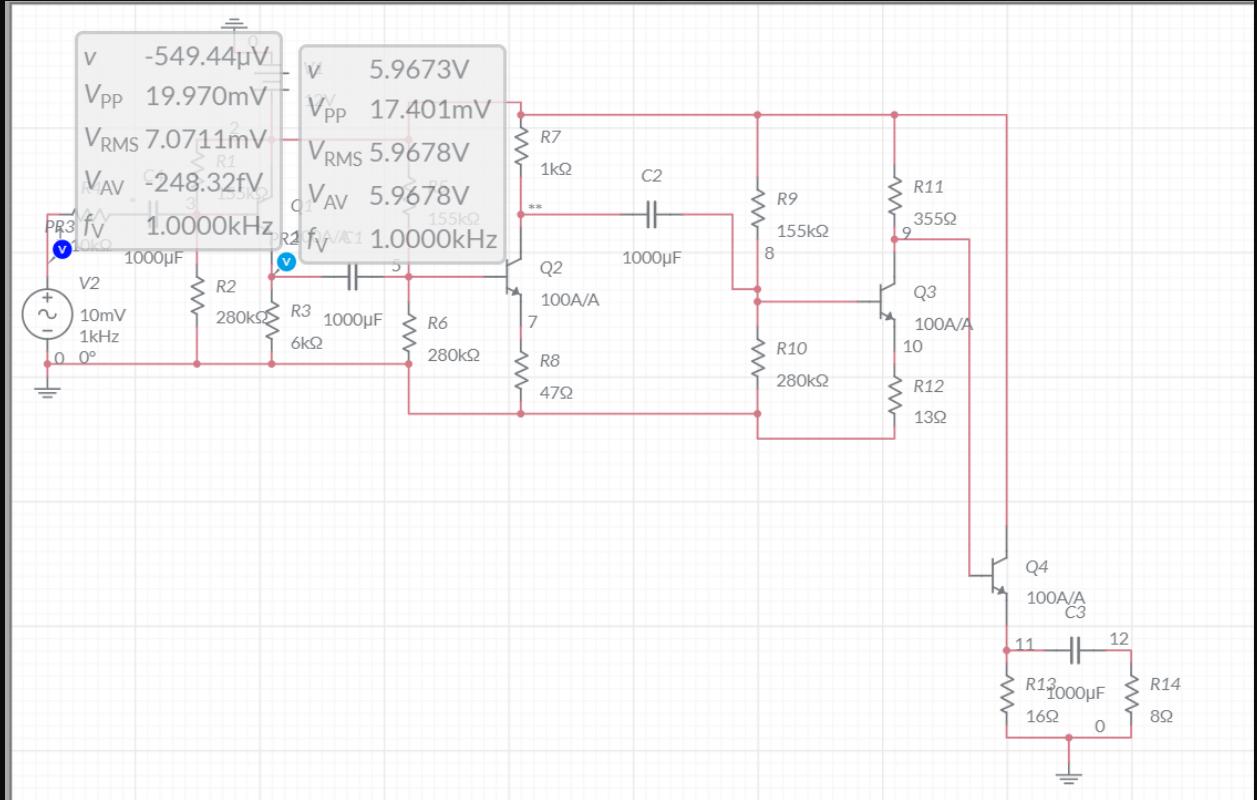
$$\therefore I_{E4} = \frac{12 - 6}{16} = 0.375 \text{ A}$$



Simulation tests and results

Simulation using multisim was used to check each stage individually, then to check the final results

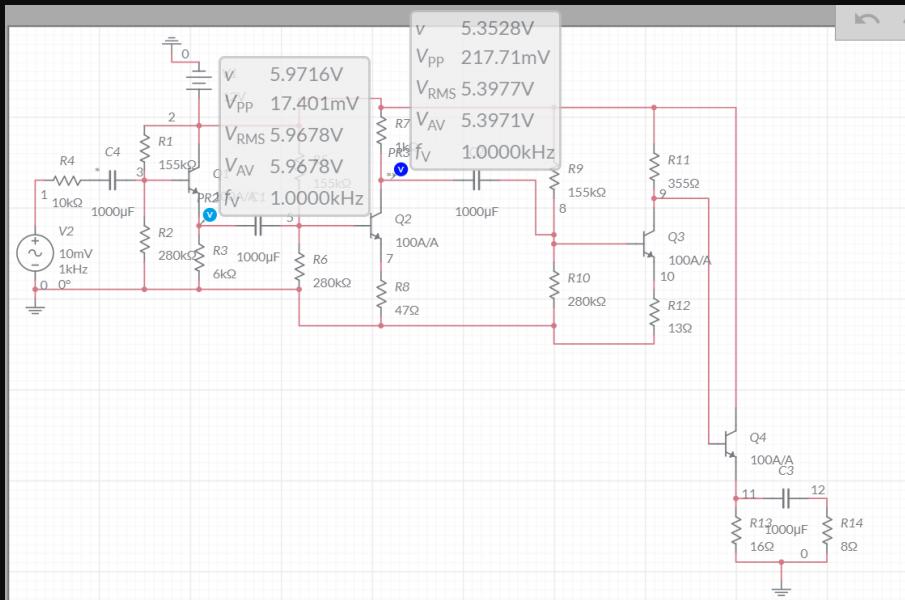
1. Test for checking the first transistor (input stage)



$$\text{Gain} = 0.87$$

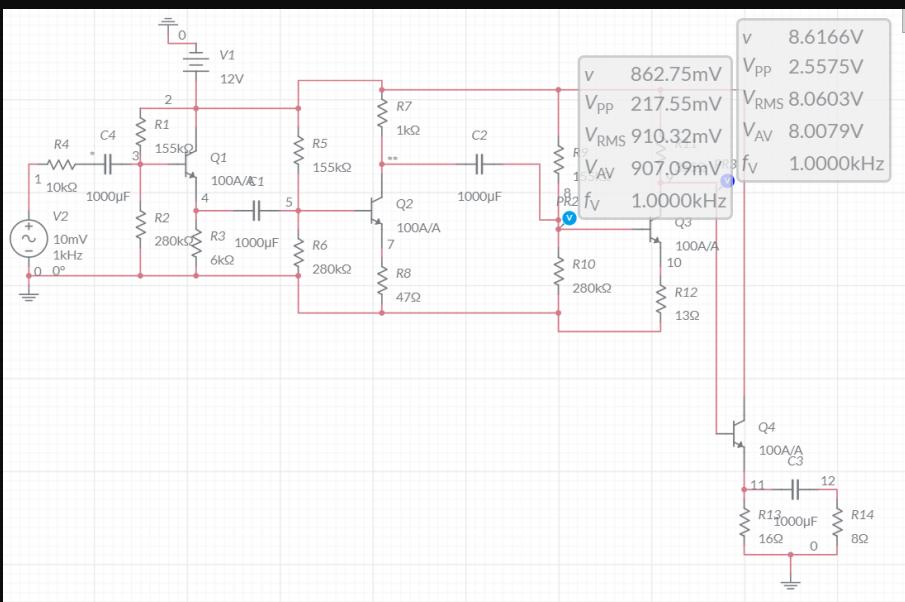
- Value close to the calculations

2. Test for checking the second transistor (gain stage)



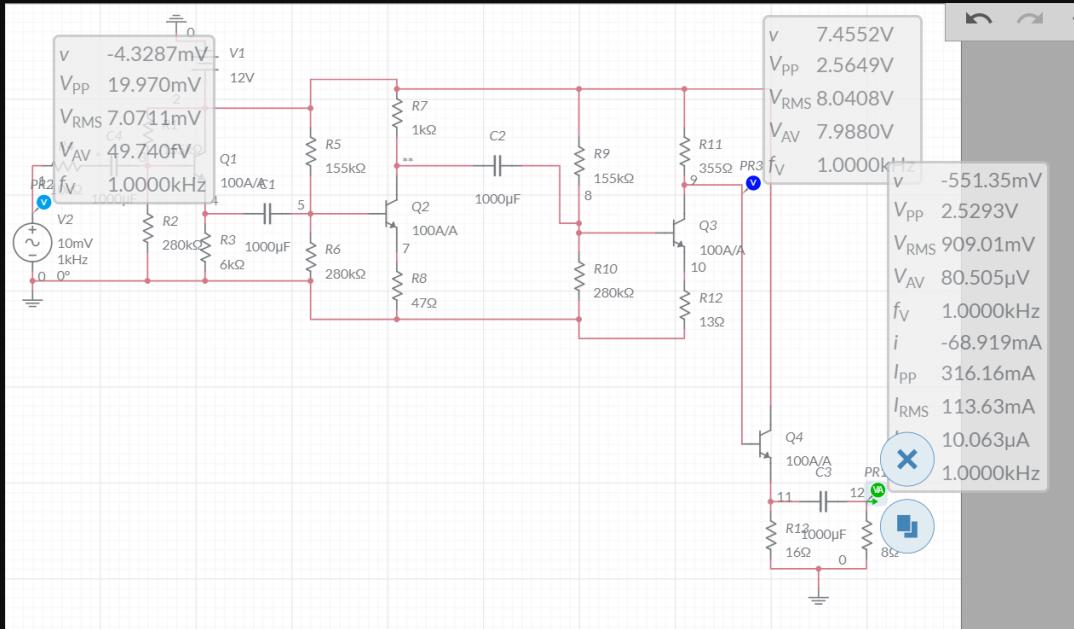
Gain =
12.511
Value close
to the
calculations

3. Test for checking the third transistor (gain stage)



Gain = 11.7
Value close
to the
calculations

4. Test for checking the fourth transistor (output stage)



The expected output values from calculation:

- $v_o(\text{peak to peak}) = 2.53 \text{ volts}$
- $i_L(\text{peak to peak}) = 0.3167 \text{ A}$

The output values in the simulation:

- $v_o(\text{peak to peak}) = 2.5293 \text{ volts}$
- $i_L(\text{peak to peak}) = 0.3161 \text{ A}$

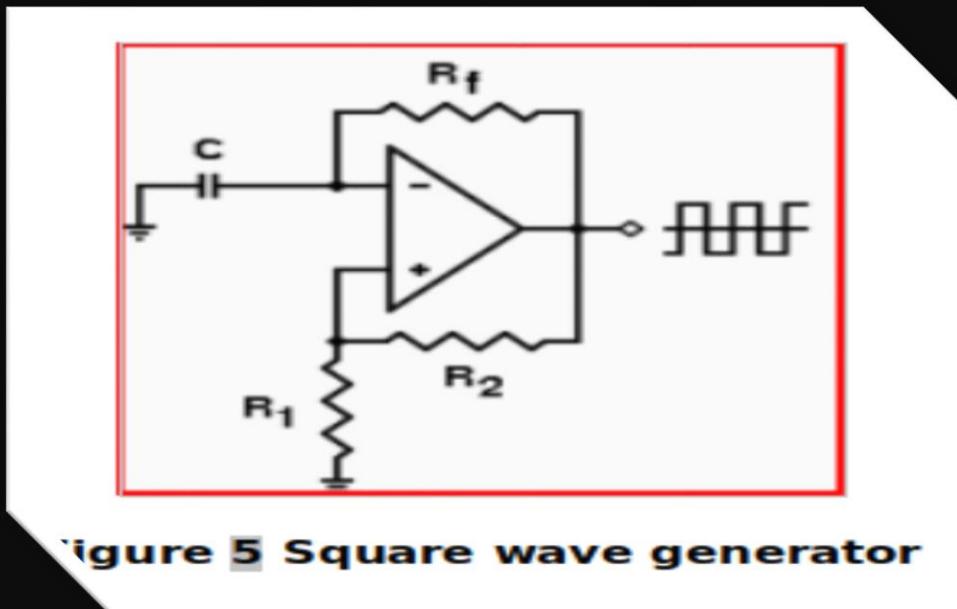
Values are very close to the desired outputs; therefore, the amplifier is performing well.

Note: to achieve those results, trial and error tests were performed after the hand calculation, and the resistor R_{C3} was changed to 355 ohms from the calculated value of 260 ohms. No additional changes were made.

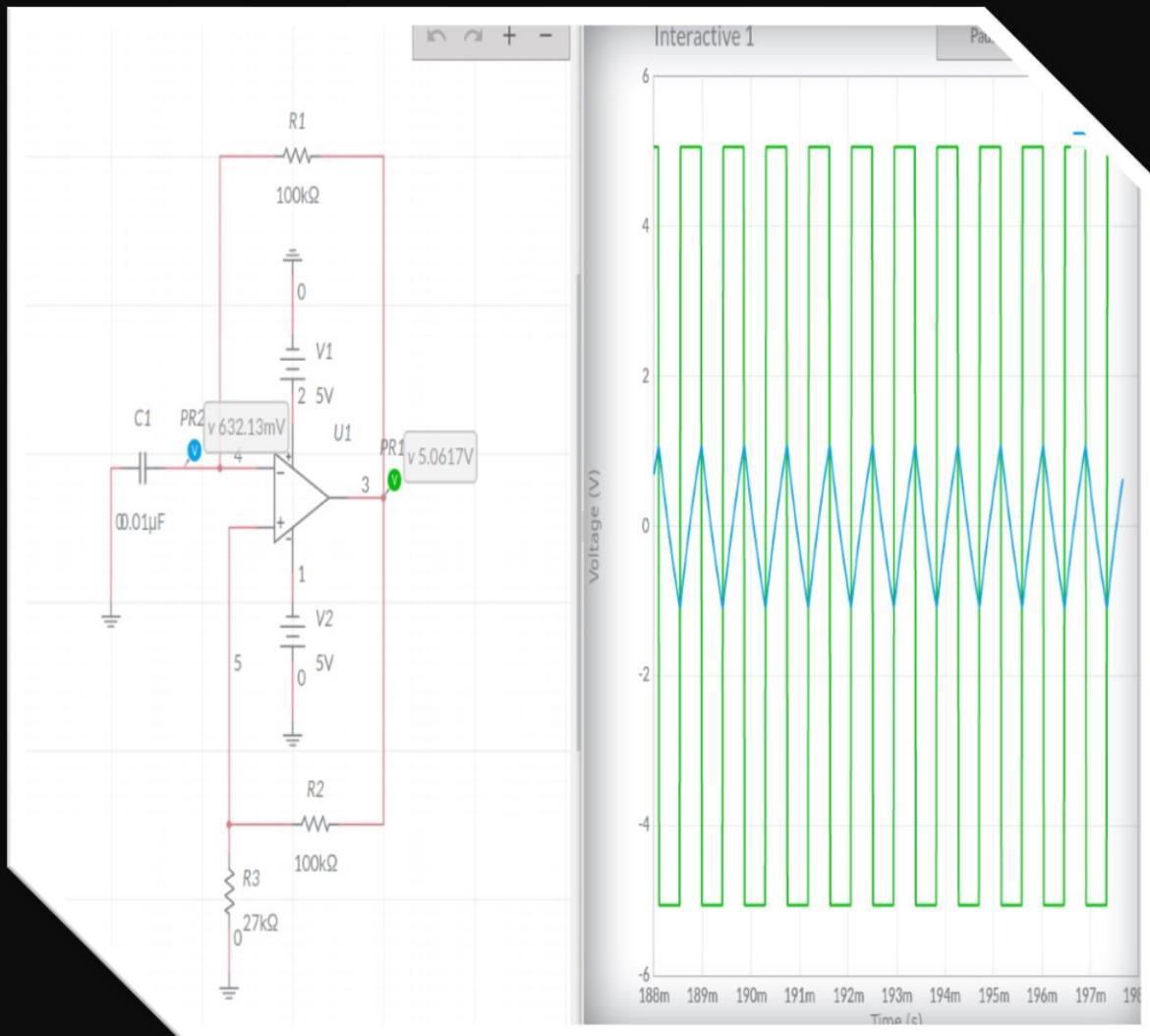
- more tests:
 - more tests were made for the four transistors to check if they operate correctly with different AC inputs, and to make sure they are all in the active mode.

- Input value of the AC voltage was changed to 20mV, 30mV, 40mV (peaks) and results were recorded
- The results has shown that they all operate in the active mode and give gain of 12 ideally, but this gain value changes slightly for other values of input other than 10mV

Circuit (2): a square wave generator



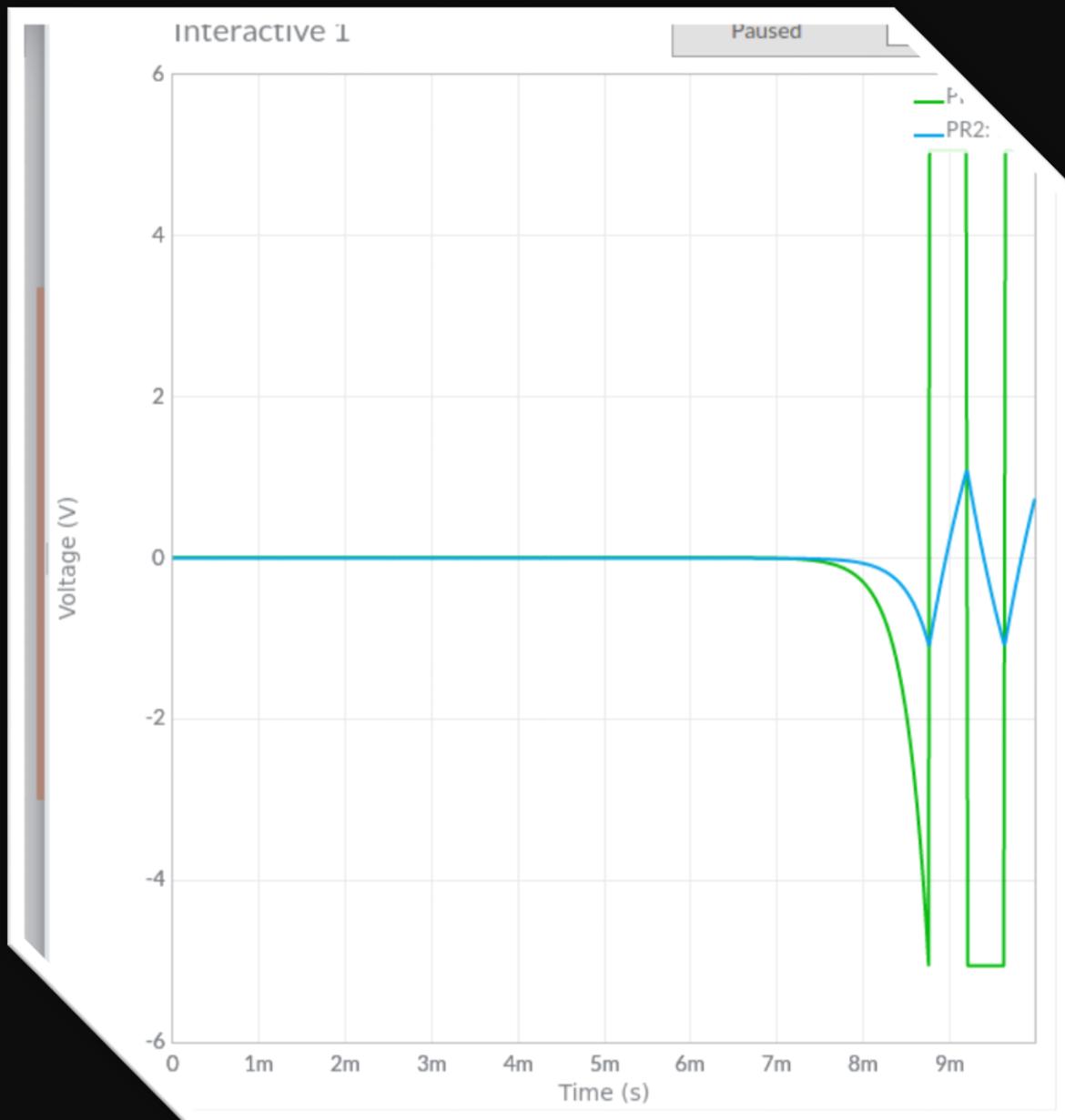
Simulation of the circuit



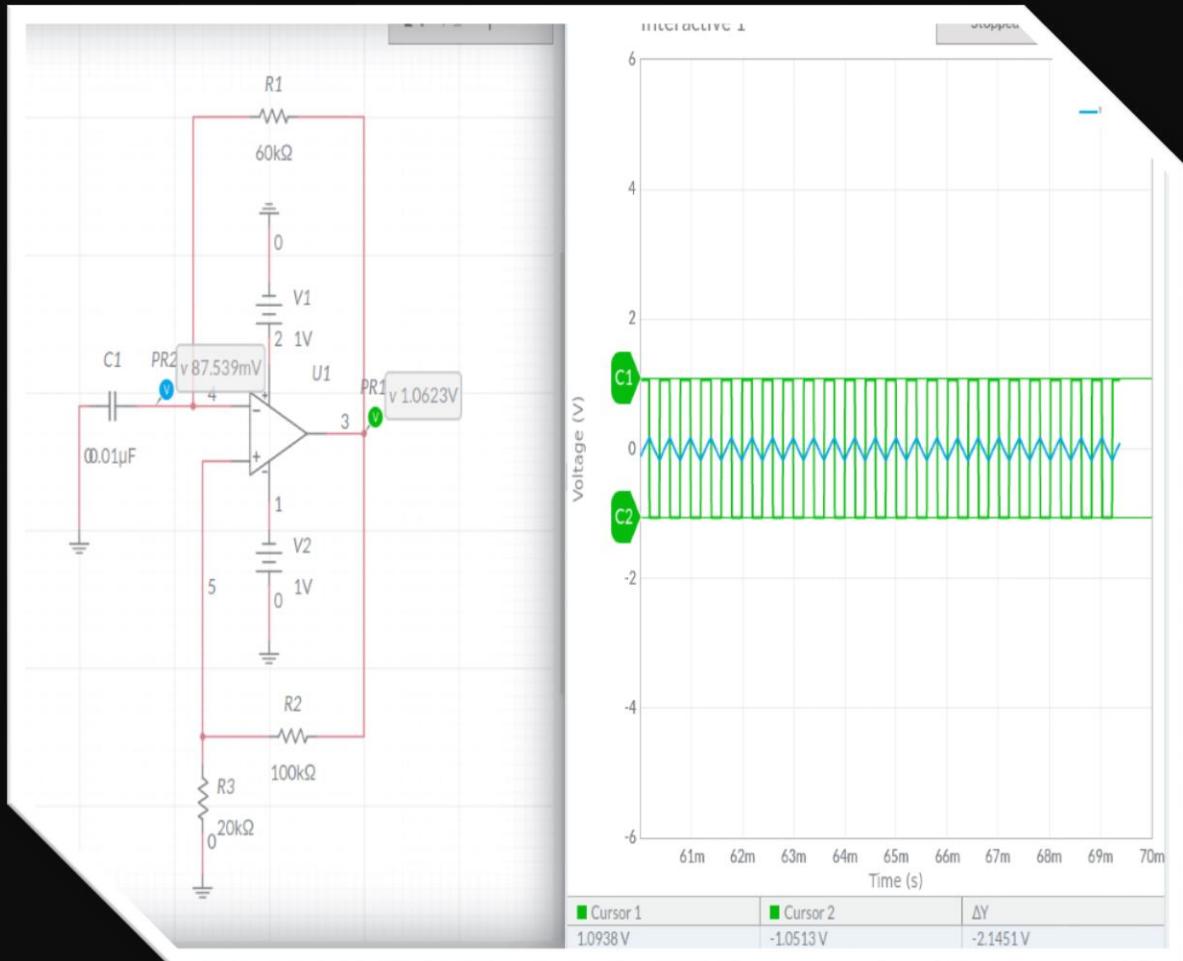
The circuit, indeed, generated a square wave in the input

- Delay

Because the negative feedback path uses a capacitor while the positive feedback path does not, however, there is a time delay before the comparator is triggered to change state.



Changing the amplitude of the square wave was possible through changing the Vcc and -Vcc values of the



The frequency

* calculating the frequency theoretically:

$$\begin{aligned} f_{\text{out}} &= \frac{1}{2R_f \times C \times \ln \left(\frac{2R_1}{R_2} + 1 \right)} \\ &= \frac{1}{2(100 \times 1000)(0.01 \times 10^{-6}) \ln \left(\frac{2(27K)}{100K} + 1 \right)} \\ &= 1157.99 \approx \boxed{1158 \text{ Hz}} \end{aligned}$$

* the frequency after simulating

$$\begin{aligned} \Delta t &= (216.28 - 215.40) \text{ ns} \quad \Rightarrow \Delta t \text{ in one period} \\ &= 0.88 \text{ ms} \\ \therefore f &= \frac{1}{T} = \frac{1}{0.88 \times 10^{-3}} = \boxed{1136.4 \text{ Hz}} \end{aligned}$$

$$\begin{aligned} \text{error} &\pm \frac{|f_{\text{theoretical}} - f_{\text{experimental}}|}{f_{\text{theoretical}}} \times 100\% \\ &= \frac{|1158 - 1136.4|}{1158} \times 100\% = \boxed{1.86\%} \end{aligned}$$

Integrator:

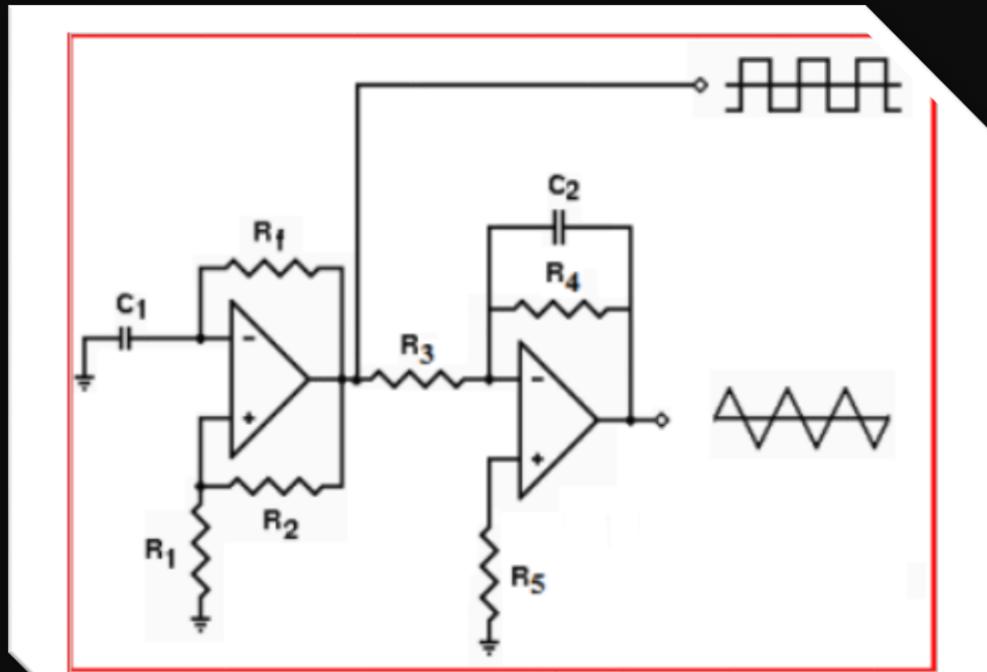
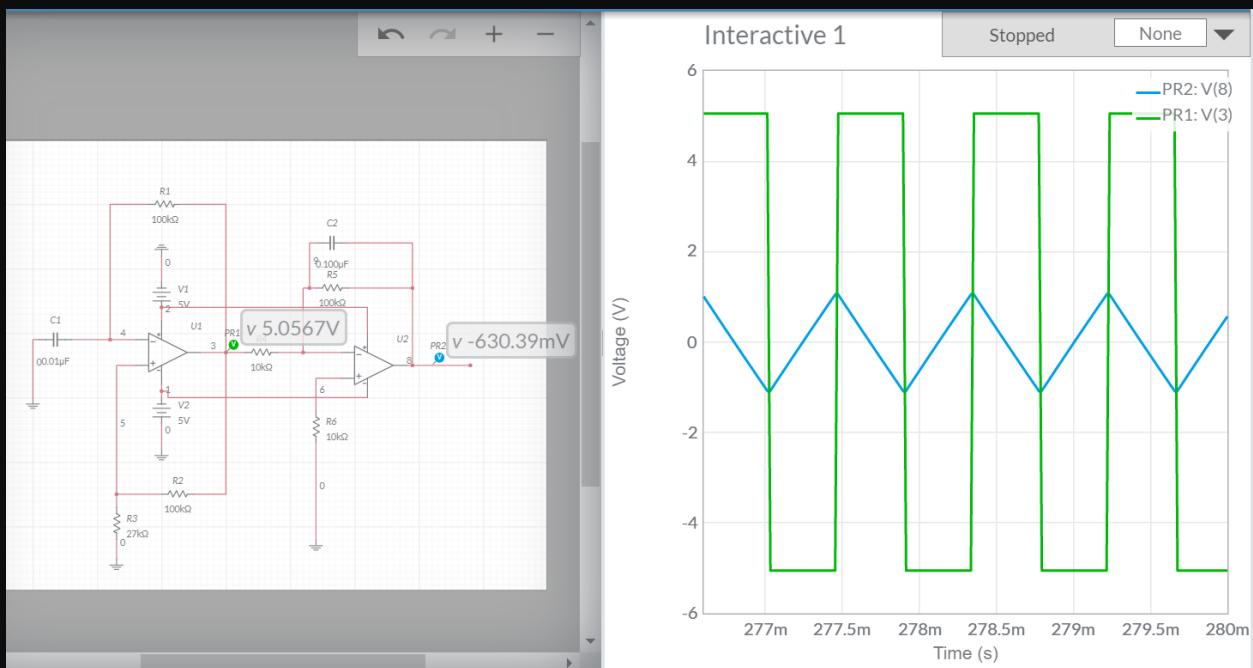


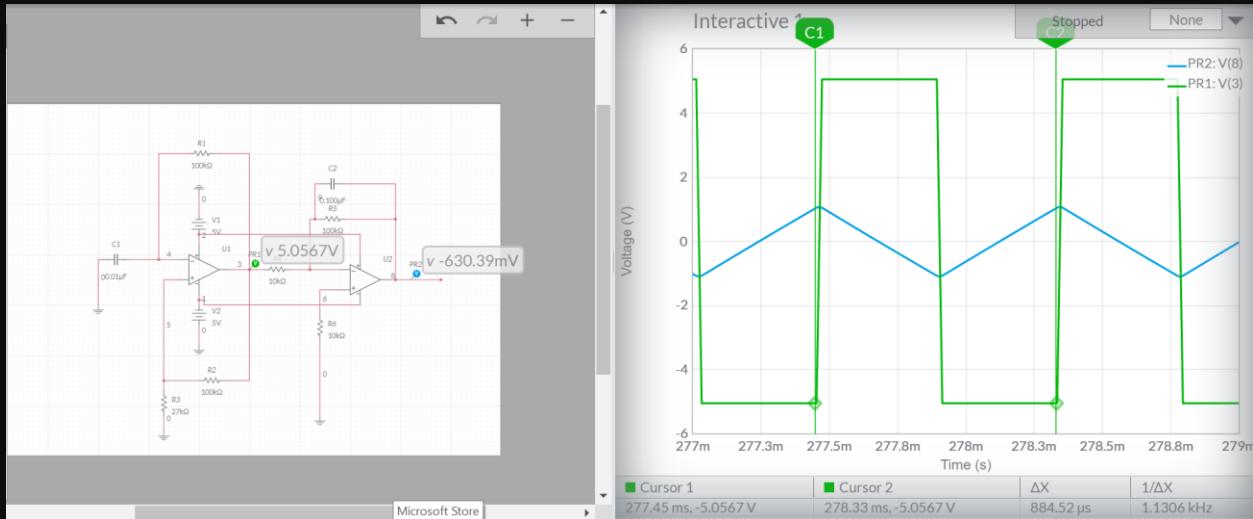
Figure 6 Square and Triangle wave generator

Simulation:

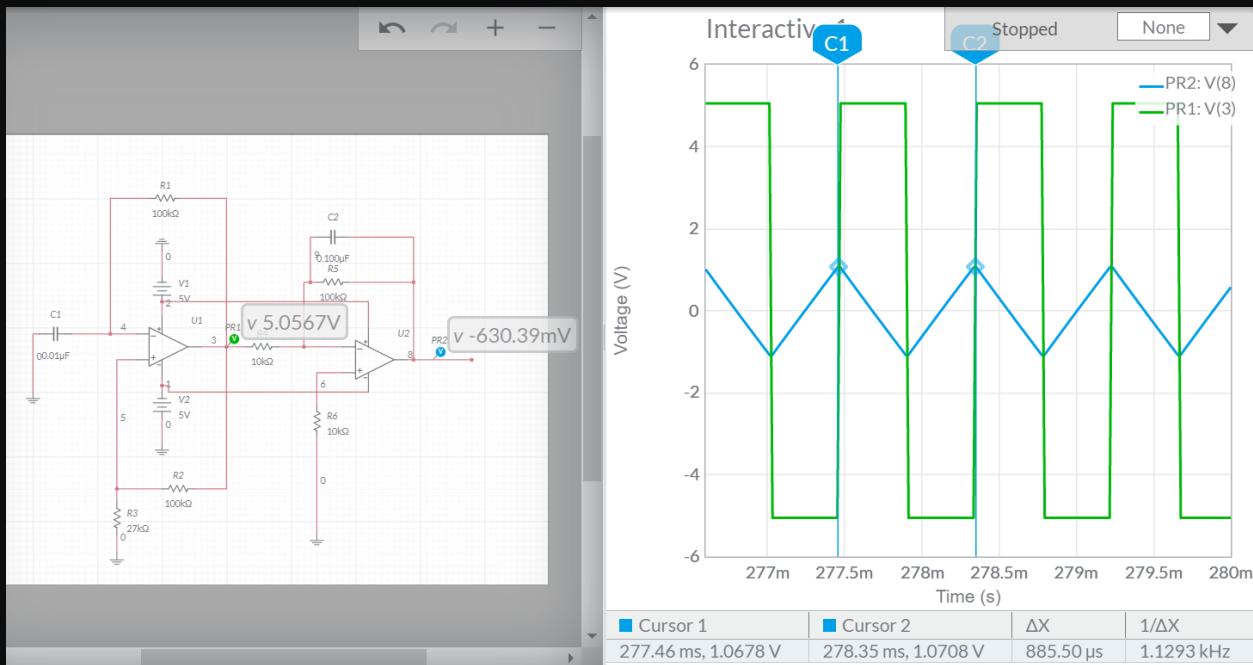


Frequency

For the square wave, frequency was 1130.6 Hz



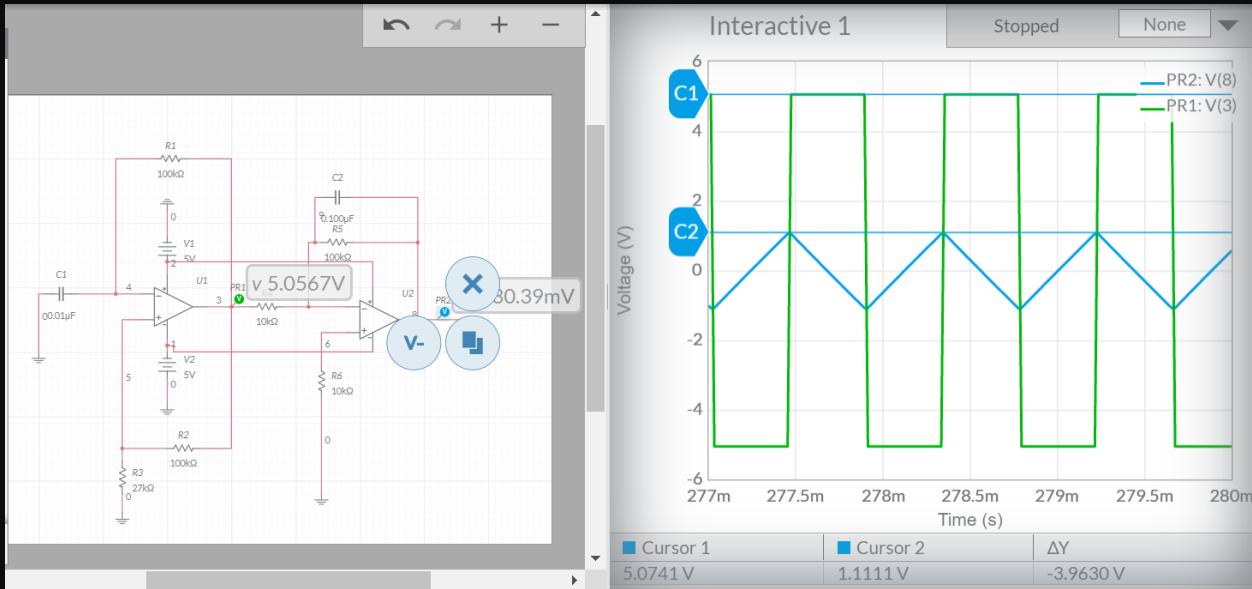
For the triangular wave, frequency was 1129 Hz



Comment:

The frequency of the square wave is as calculated from the formula of the square wave generator, and the frequency of the triangular wave is almost the same because the integrator does not change the frequency.

Amplitude



Square amplitude = 5.07 volts

Triangular amplitude = 1.11 volts

Comment:

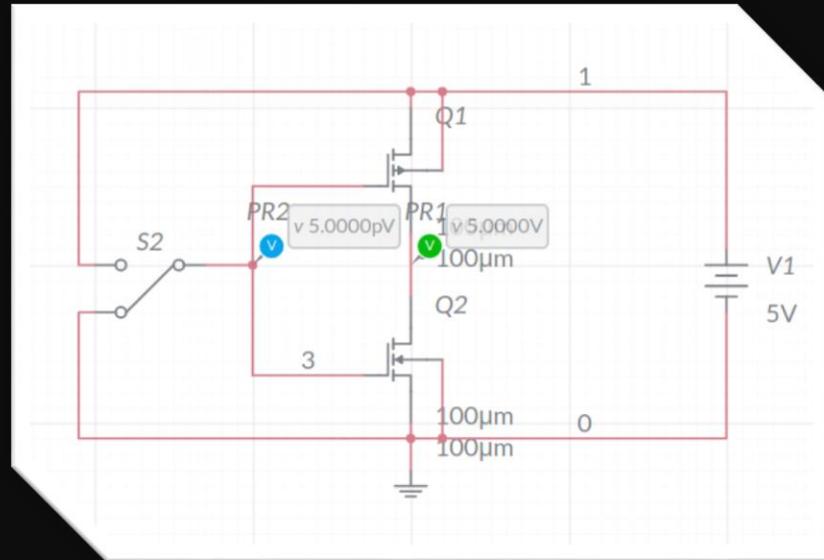
The square wave amplitude is controlled by the Vcc and the -Vcc of the OpAmp. On the other hand, the integrator circuit controls the amplitude by it's an integral equation. The variables that control it are R4, C2, R3.

CMOS application: logic gates implementation

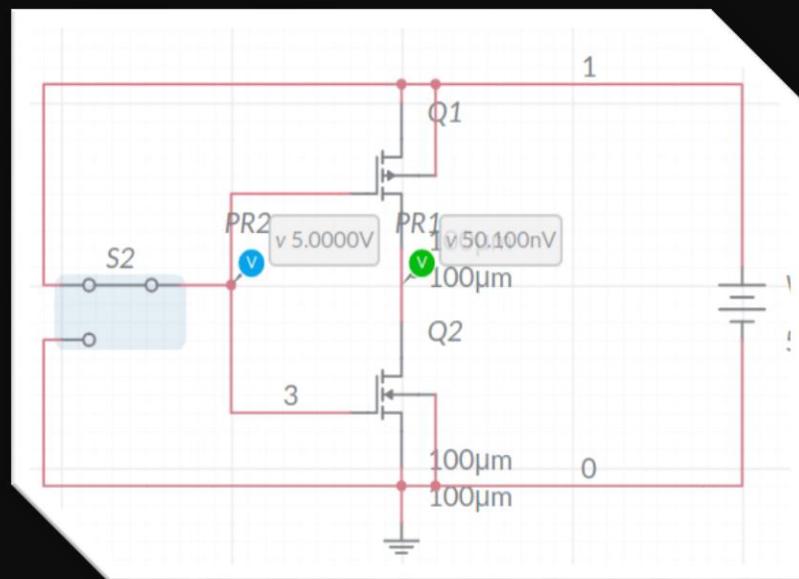
NOT Gate:

Simulation:

in case input = 0



In case input=1



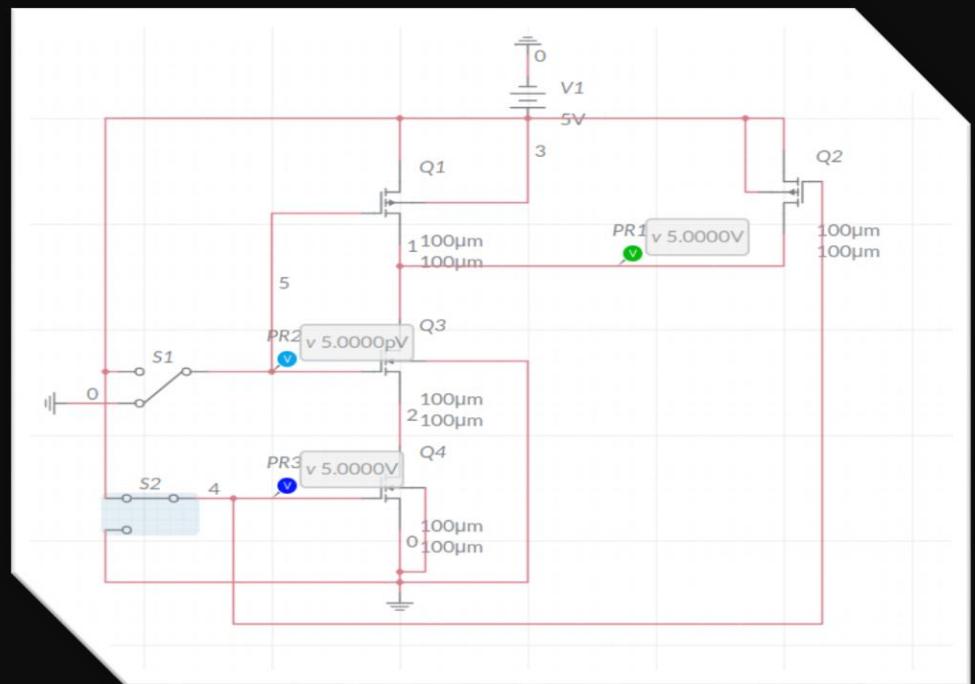
Comment: it follows the truth table

NAND Gate:

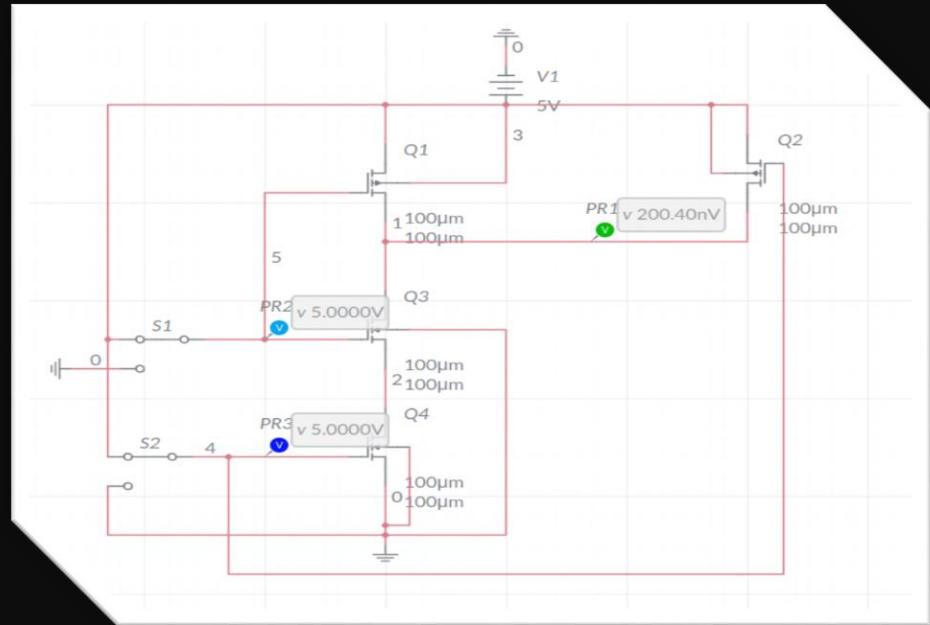
- The truth table

A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

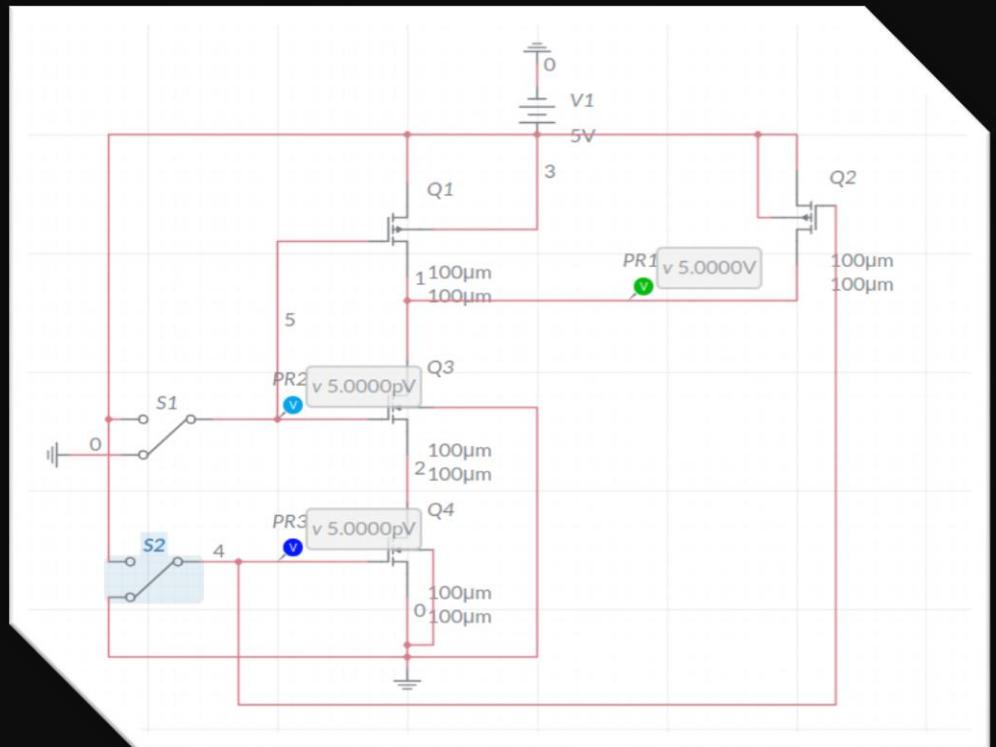
- In case input is 01



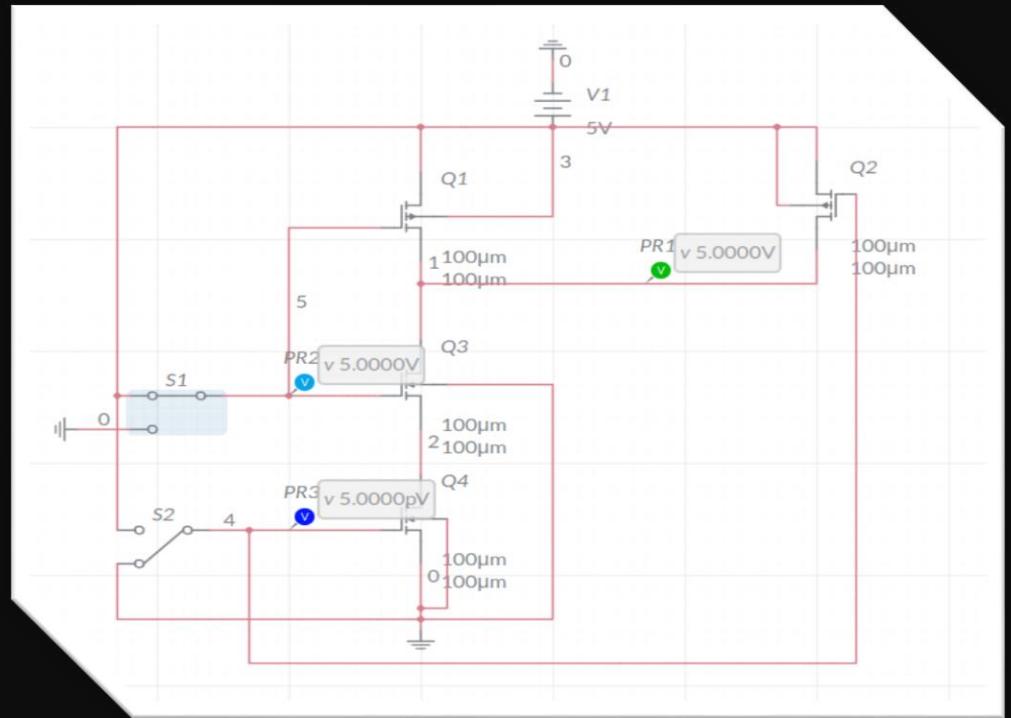
- In case input is 11



- In case input is 00



- In case input is 10



Comments:

The simulation results satisfy the truth table

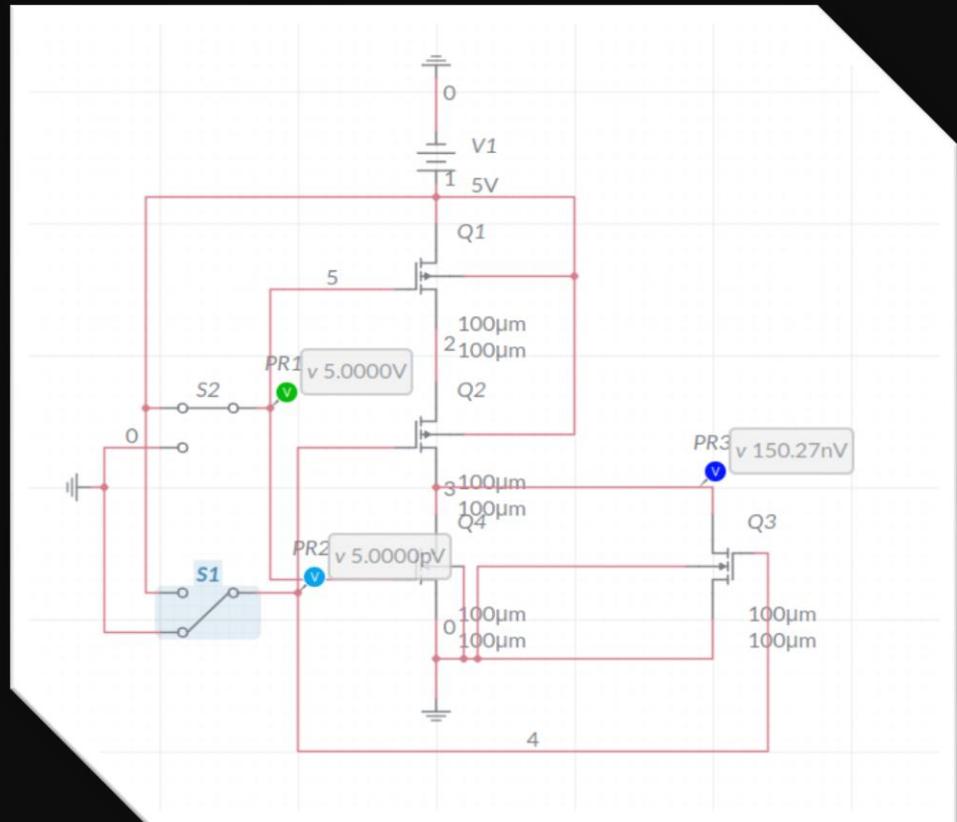
NOR Gate:

The truth table

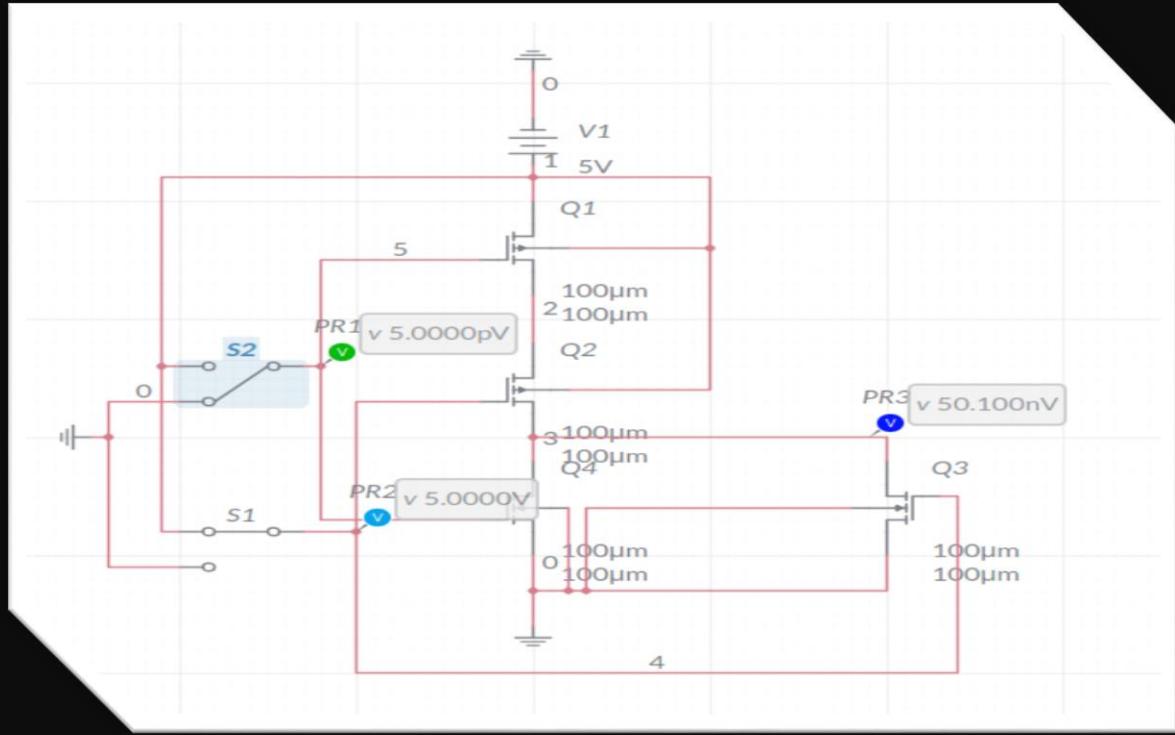
A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

simulation:

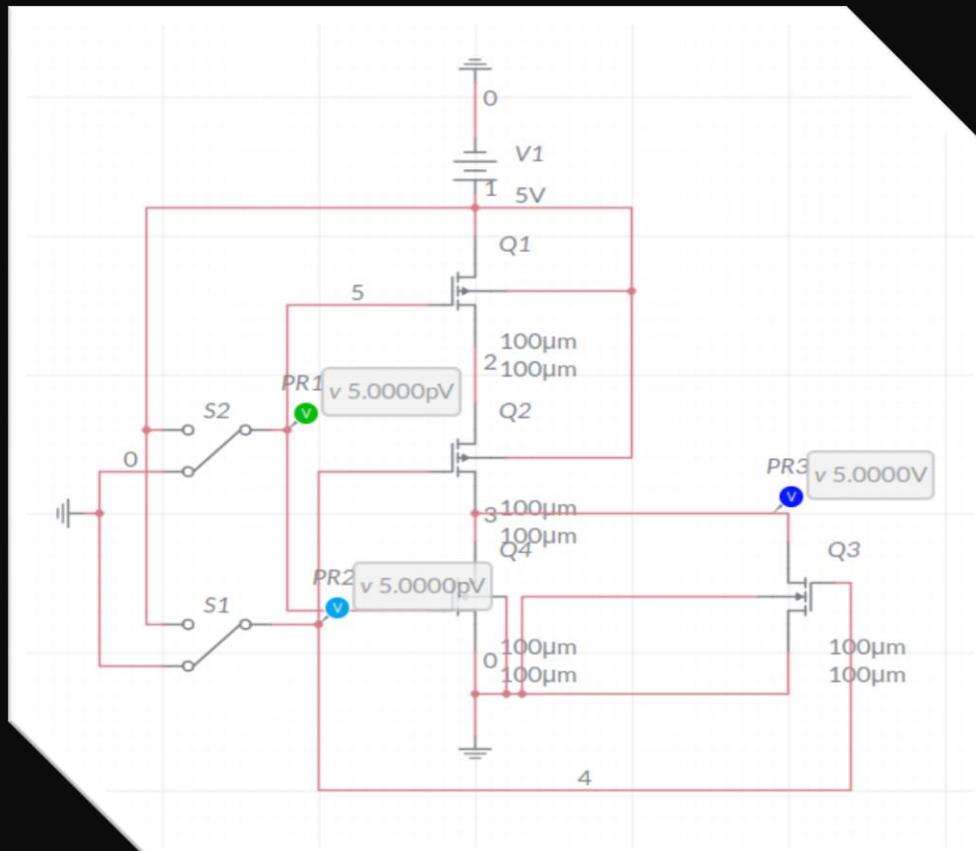
- In case input = 10



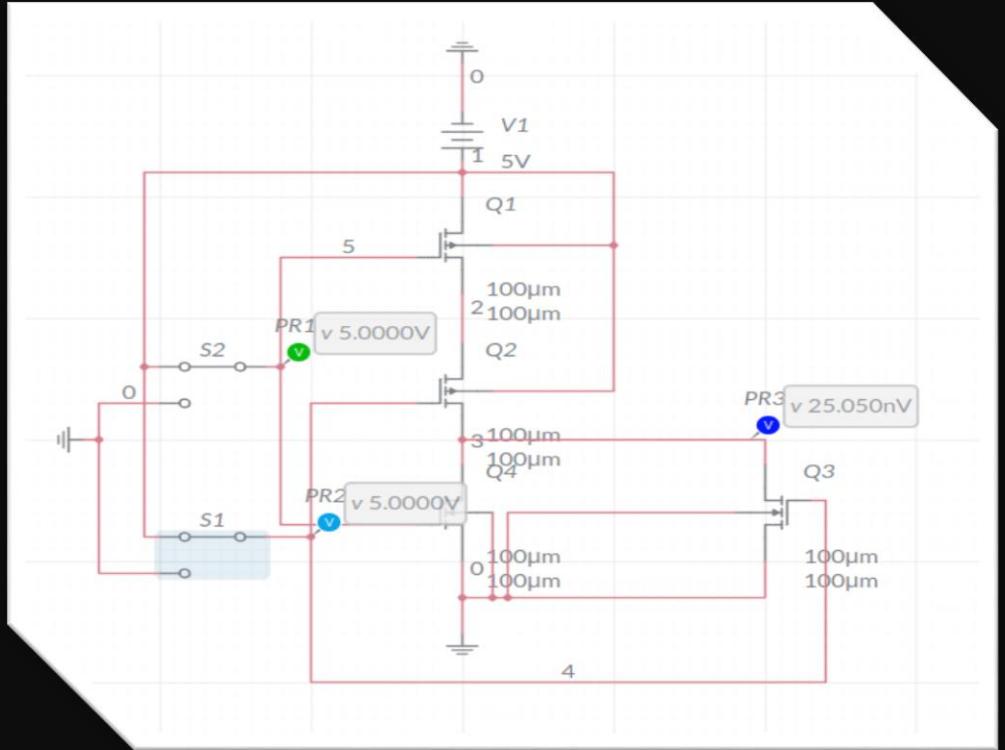
- In case input = 01



- In case input = 00



- In case input = 11



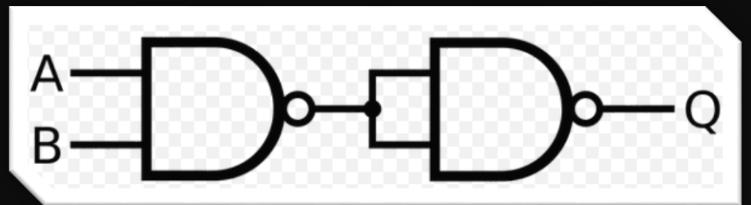
Comments:

The simulation results satisfy the truth table

AND Gate:

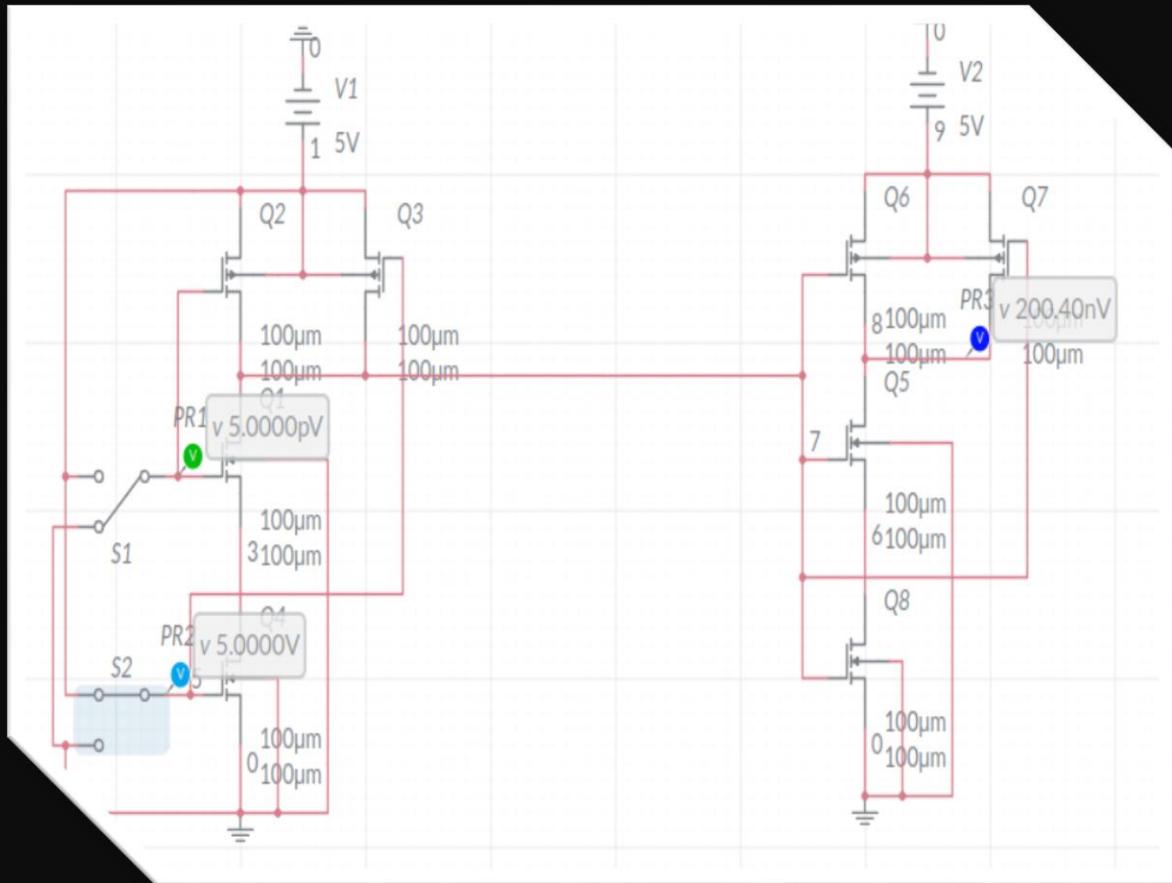
Options for creating AND gate:

- 2 NAND
- 3 NOR
- (1 NAND + 1 NOR (one input))

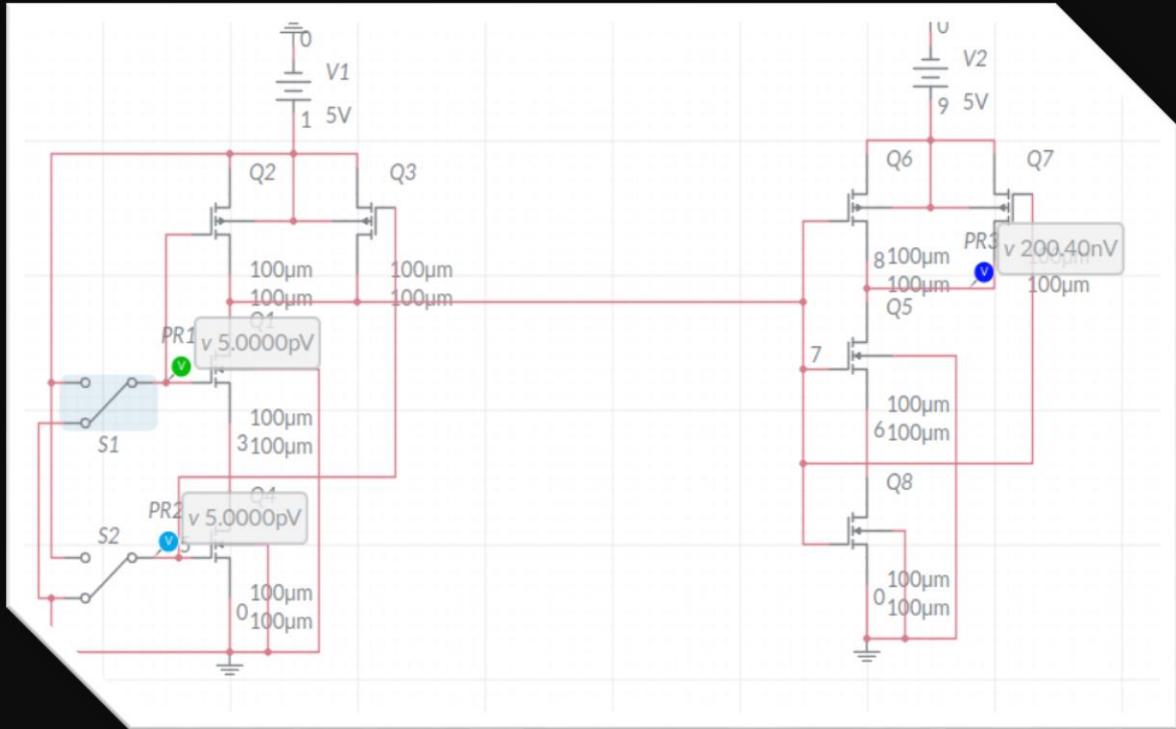


Using 2 NAND:

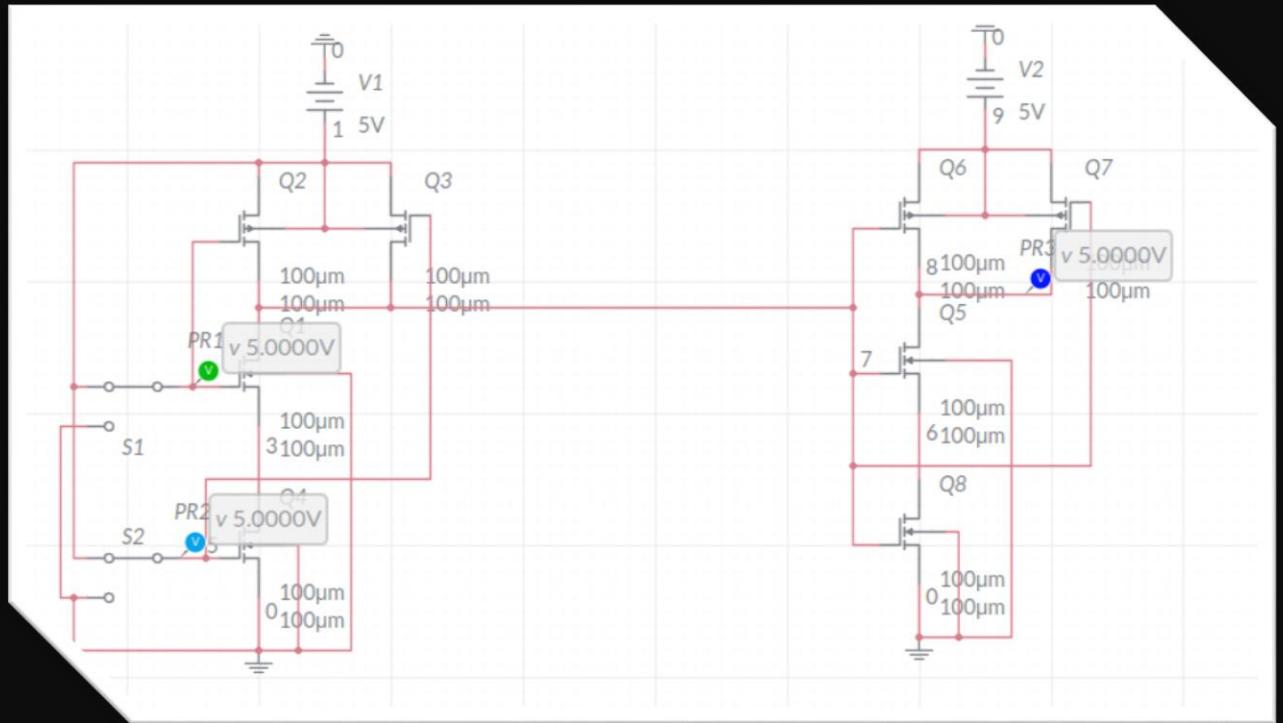
- In case input = 01



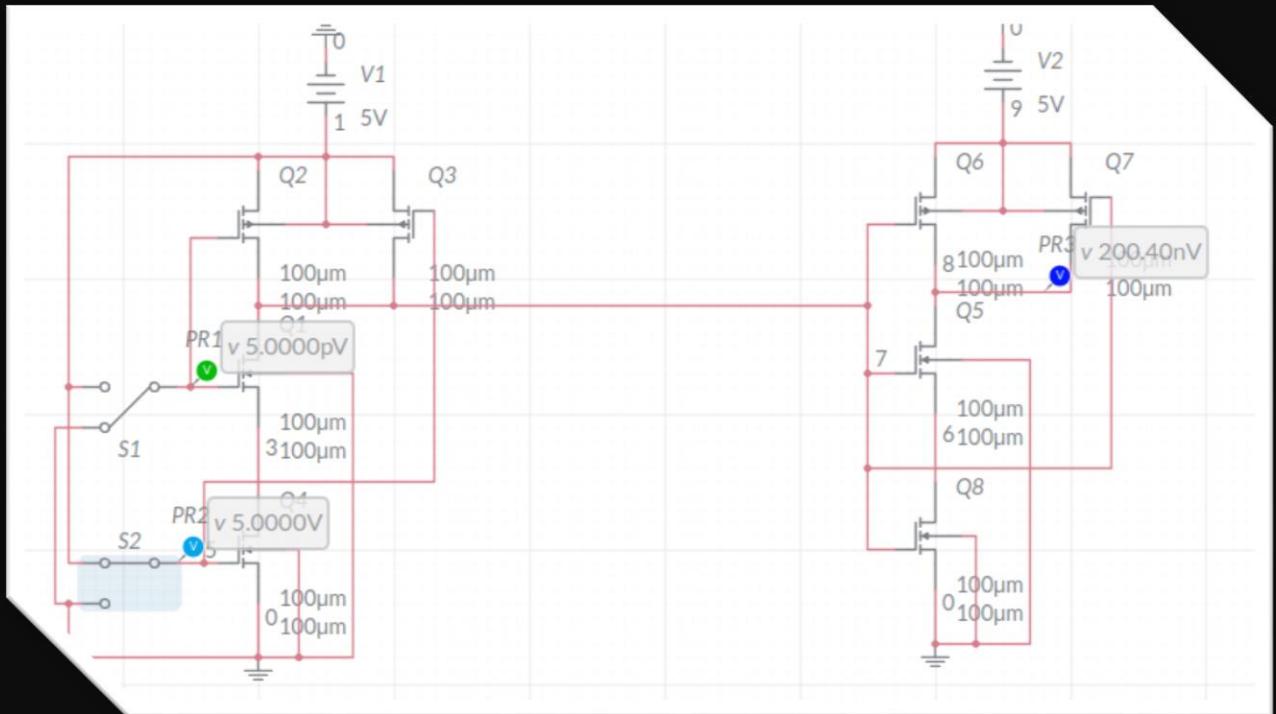
- In case input = 00



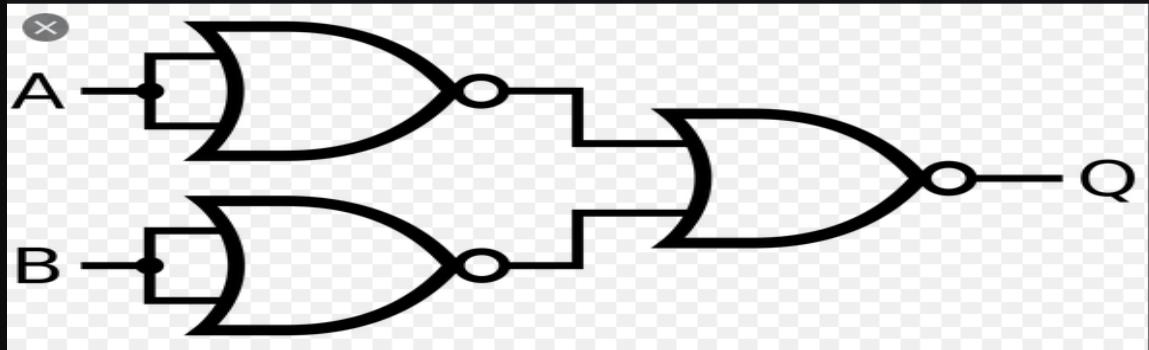
In case input = 11



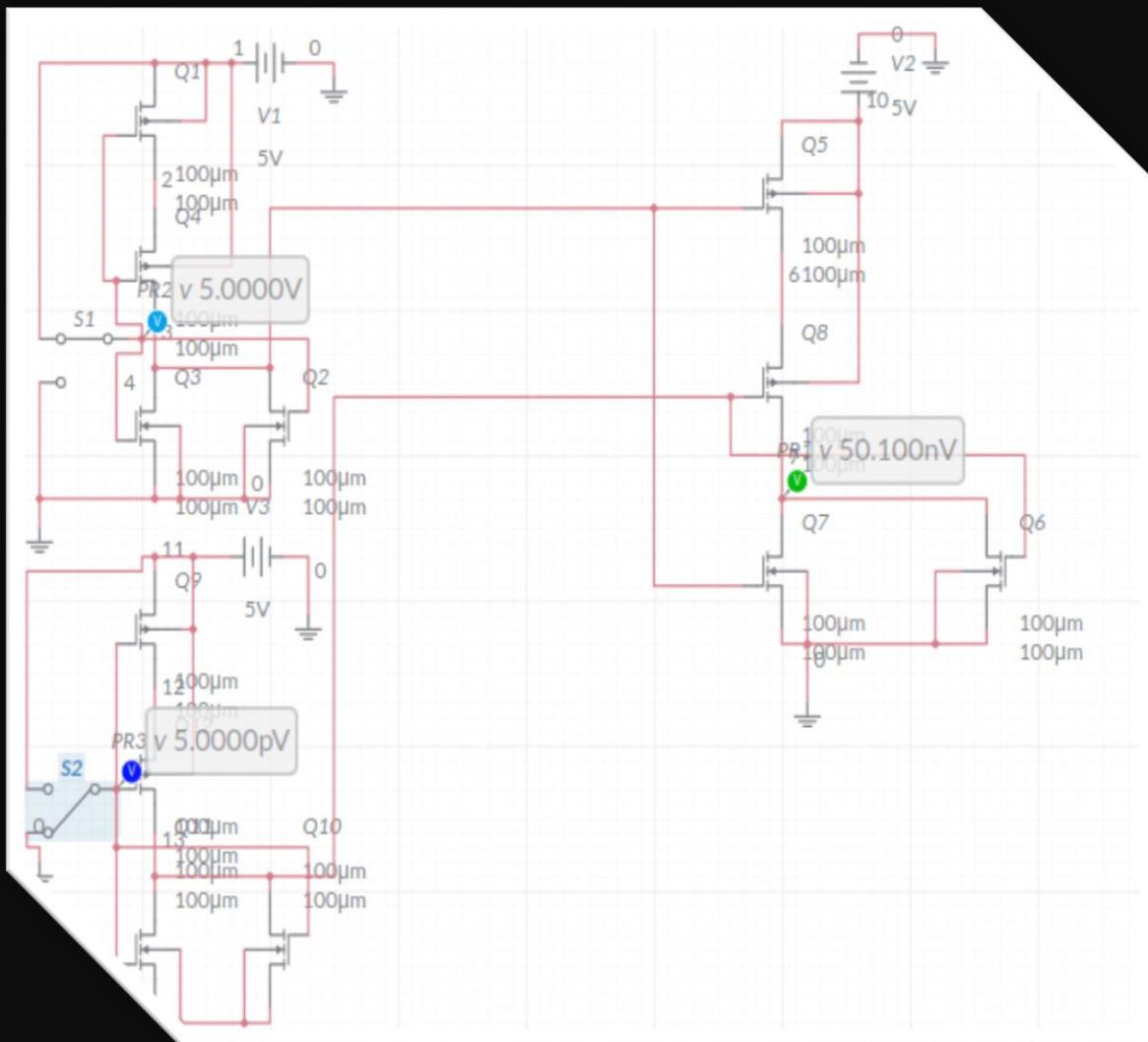
- In case input = 10



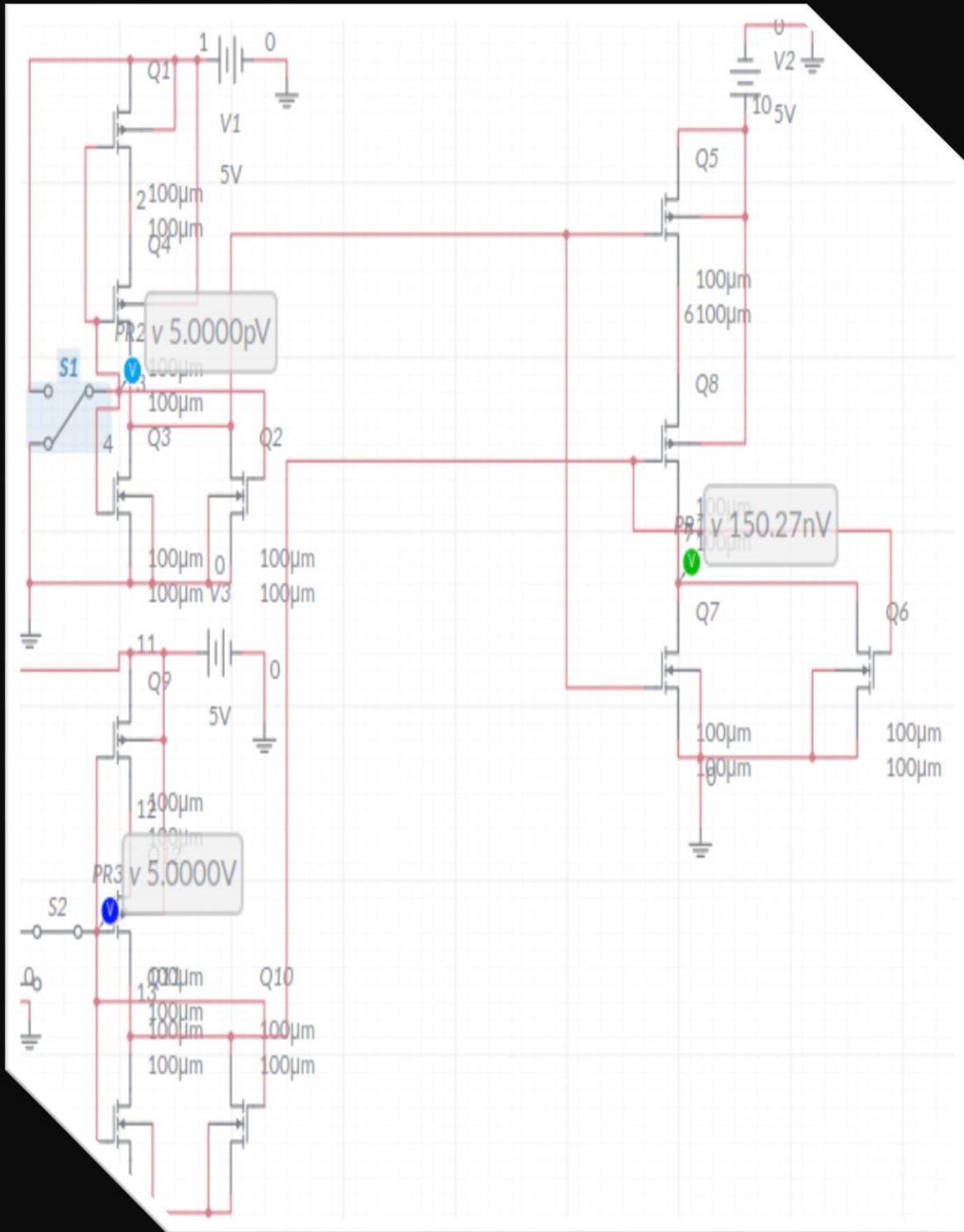
Using 3 NOR:



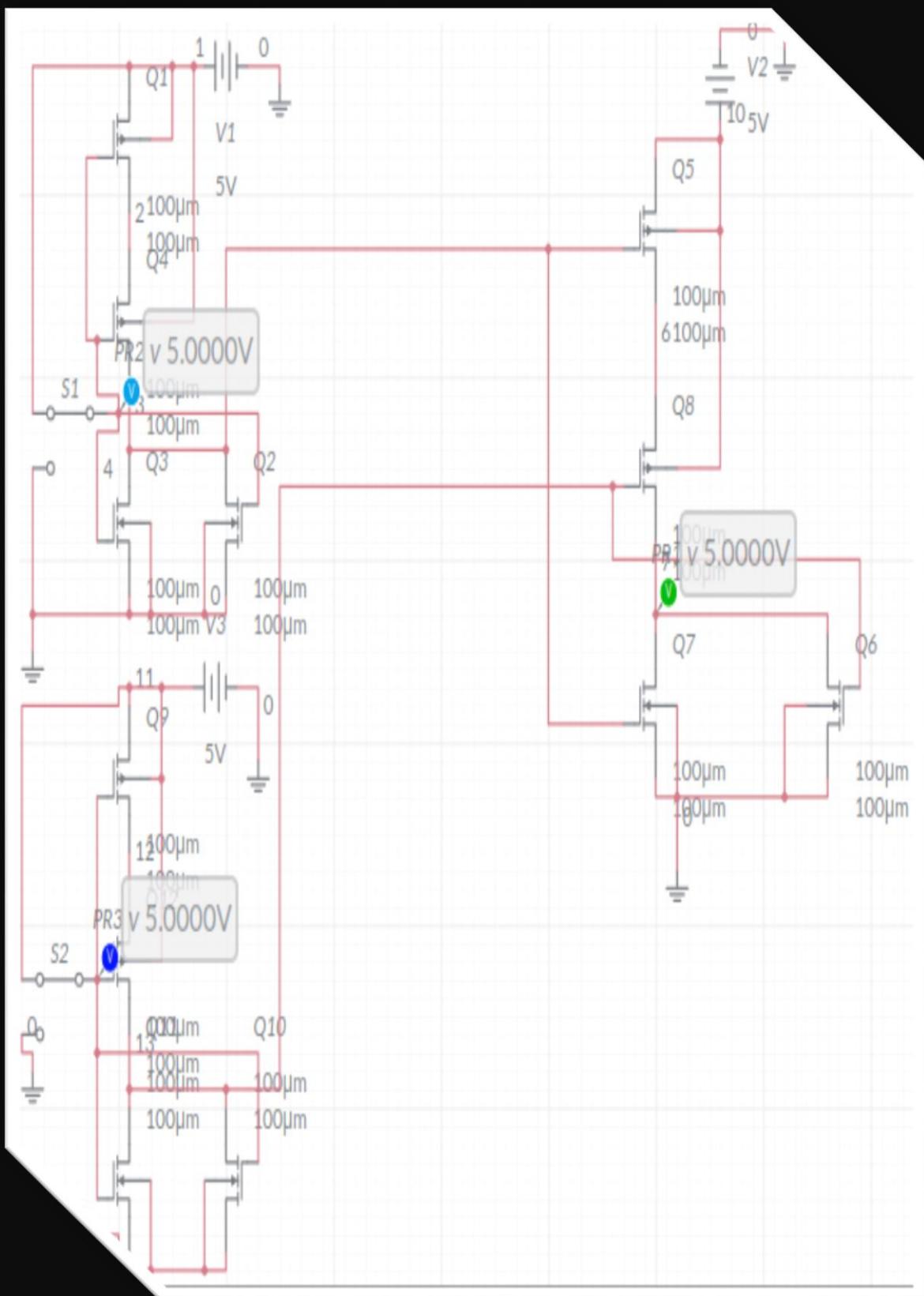
- In case input = 10



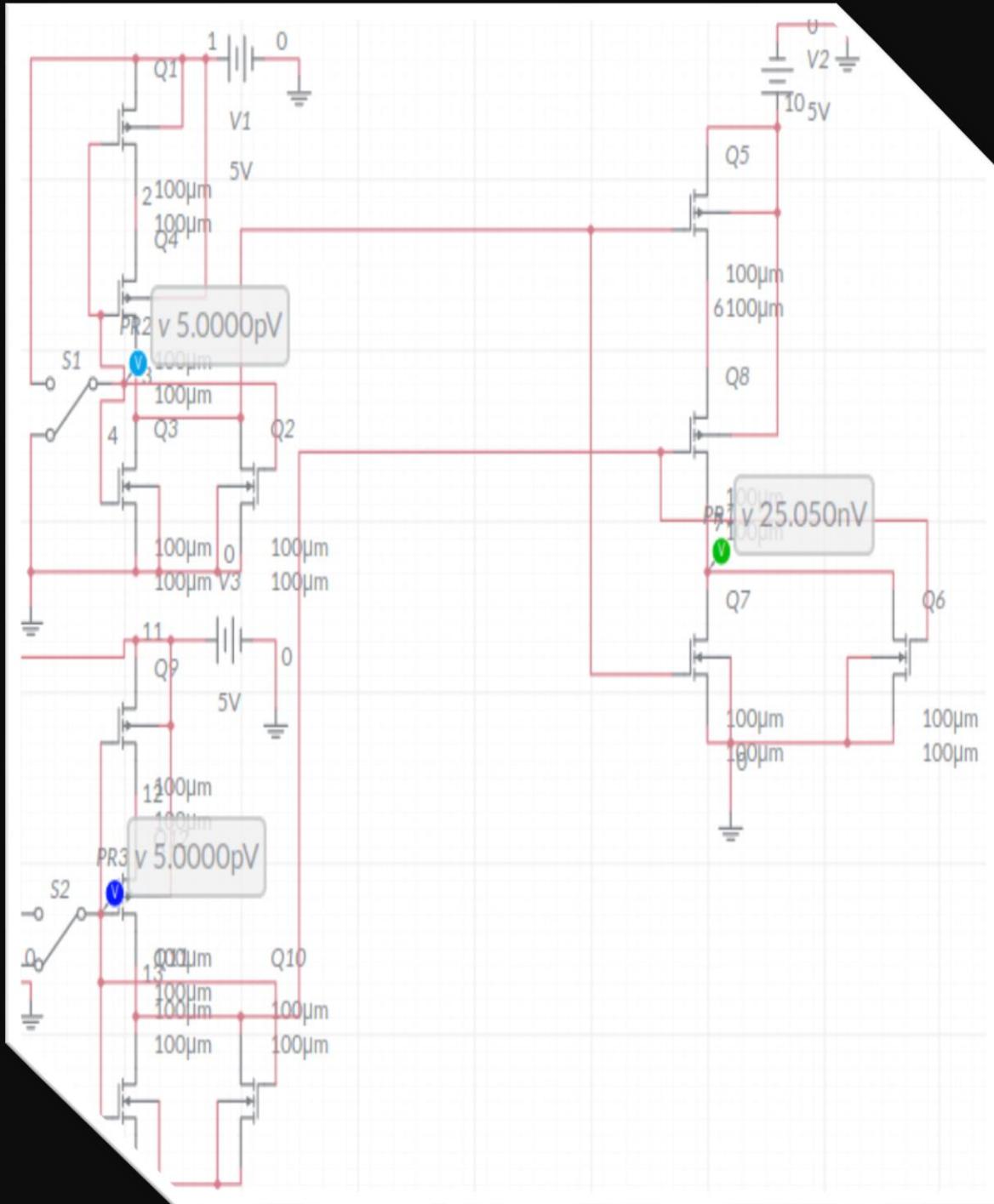
- In case input = 01



- In case input = 11



- In case input = 00



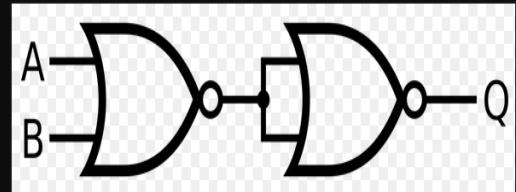
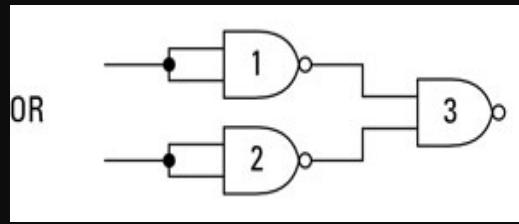
Comments:

The simulation results satisfy the truth table

OR Gate:

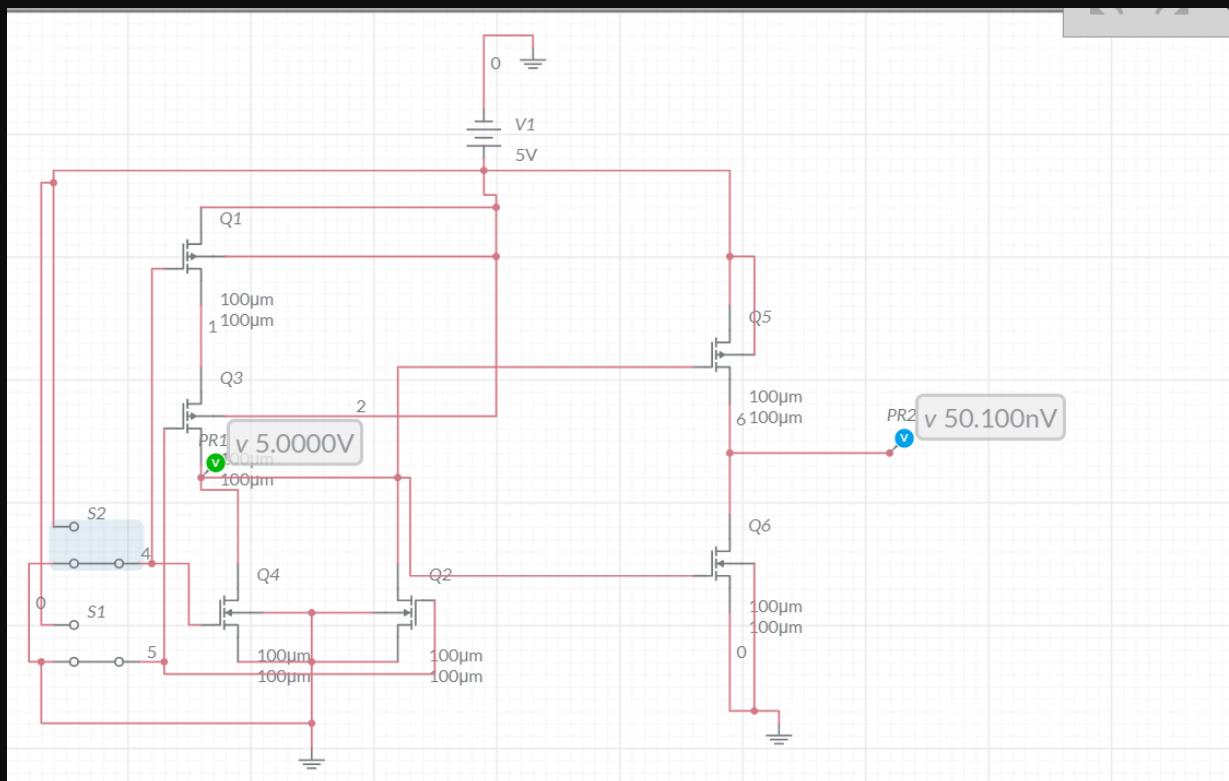
Options for creating OR:

- 3 NANDS
- 2 NOR
- NOR + NAND (one input)
- NOR + invertor (we used this method)

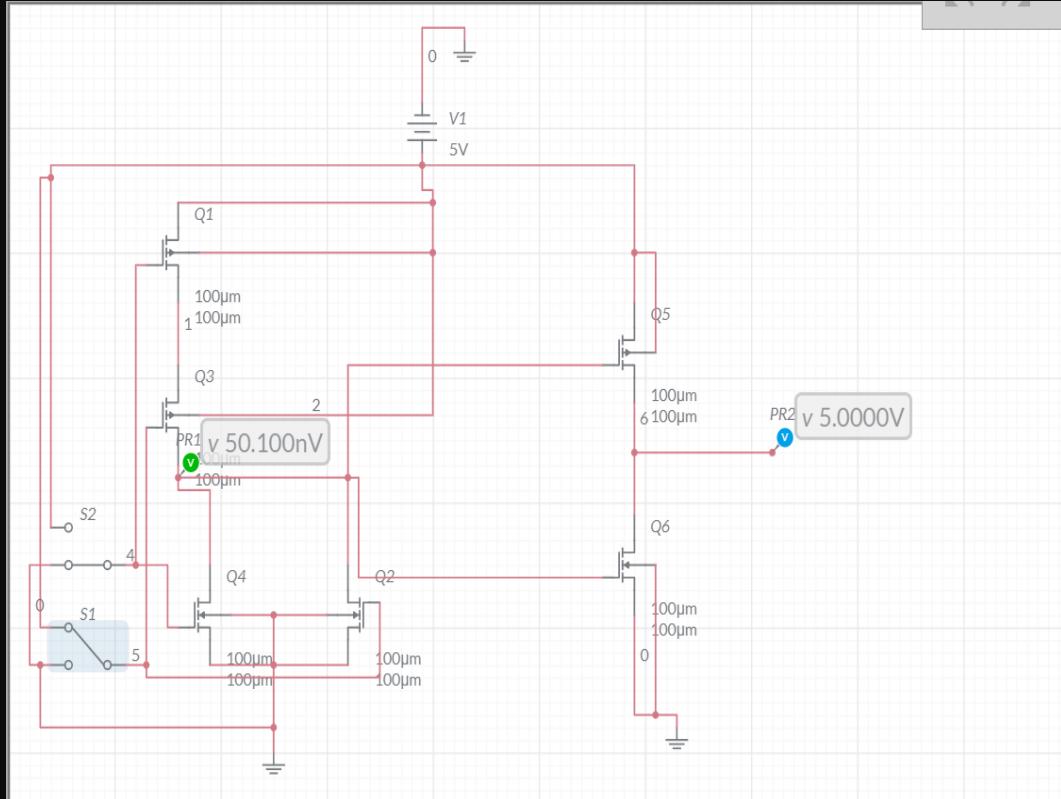


Simulation

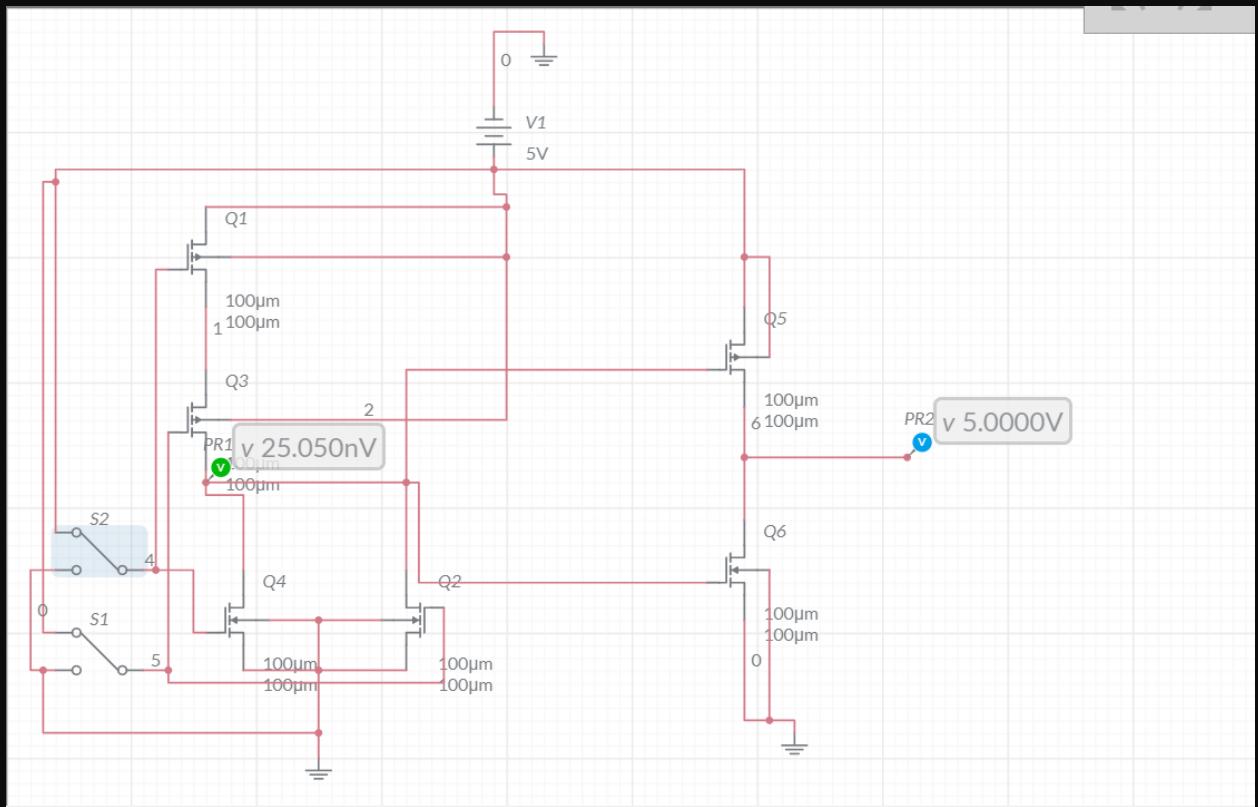
1) Case of input1=0, input2=0



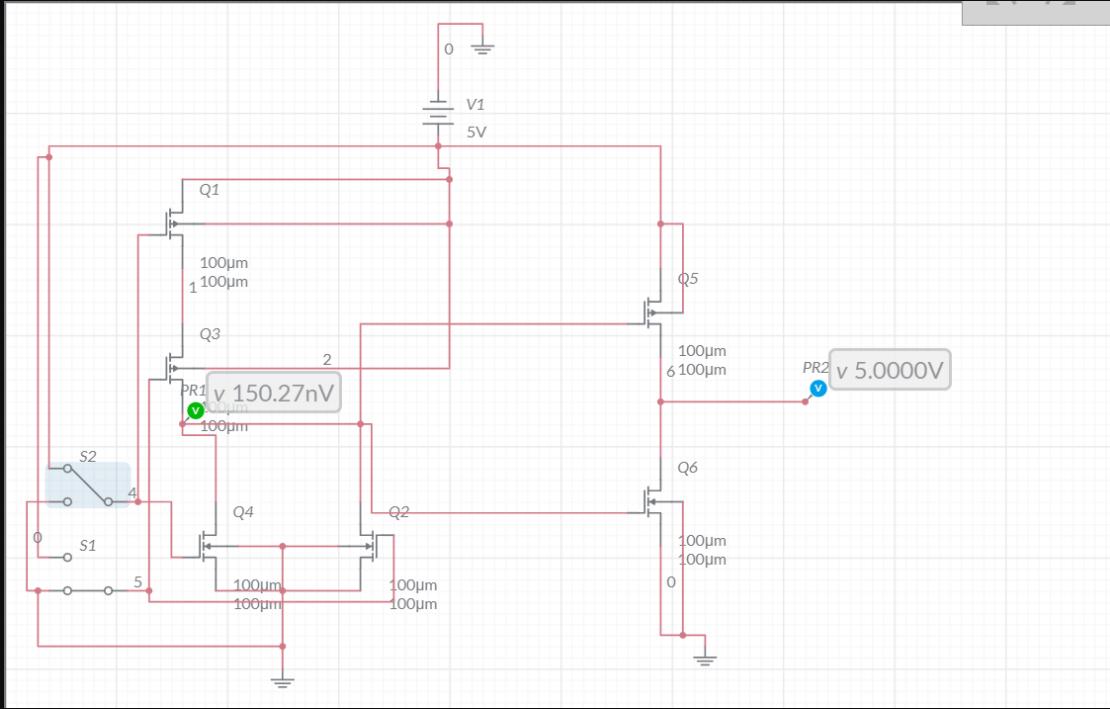
2) Case of input1 =0, input2= 1



3) case of input1 =1, input2=1



4) Case of input1 =1, input2=0



Comments:

The simulation results satisfy the truth table

Conclusion:

We were able to design an audio amplifier analytically and by trial and error on the simulation. However, in real life, we may not find the values of resistors industrially, so some changes will happen in real circuits. We were also able of using the OpAmp for differentiating or integrating signals. Also, we designed logic gates using CMOS transistors in different ways of designing the same gates.