Technology of IT Devices - Lab 1.

Introduction

During this lab practice we will use the Mentor Graphics's Hyperlynx analog circuit simulator tool. After unzipping the file downloaded from the website, open the **cmos.dxp** project file. Let's select the required schematic in Navigator window (Task 1 & 2: inverter, Task 3: CmpxOA21.)

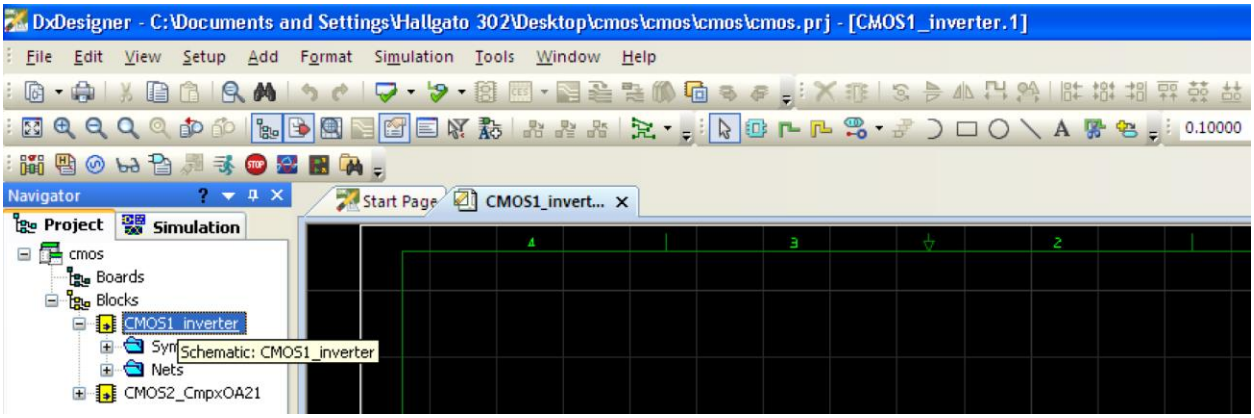


Figure 1. CMOS inverter is selected in Navigator window

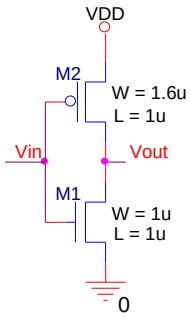
Now we have to create the netlist using **Simulation/Netlist** command, and click on OK. We will get some warnings, it's normal ☺.

Task 1

Simulate the threshold voltage of the inverter if the power supply is V_{DD}=3.3V.

Guide

Define the power supply voltage source between VDD and 0 nodes, and define another one and connect a 0V DC voltage source between the Vin and the ground using Simulation/Sources, and add a new source for power supply.



CMOS inverter

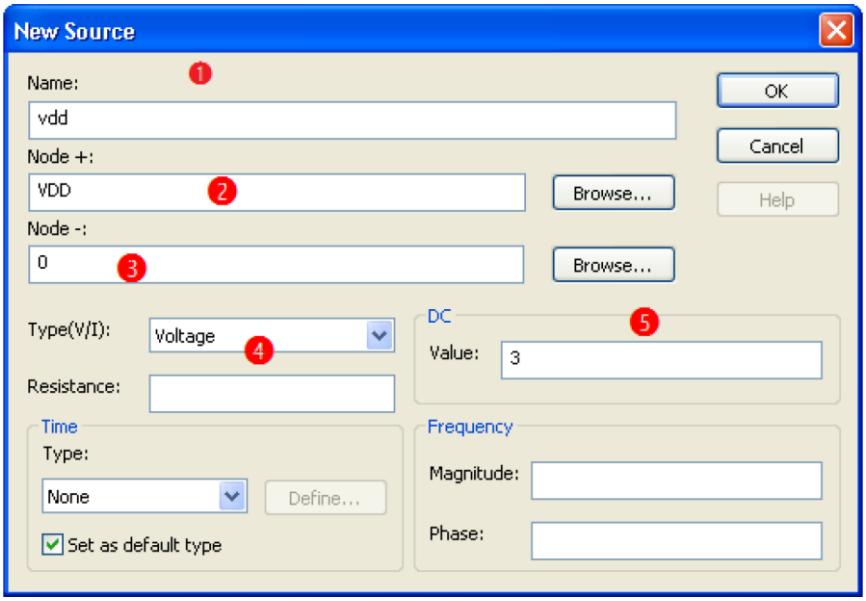
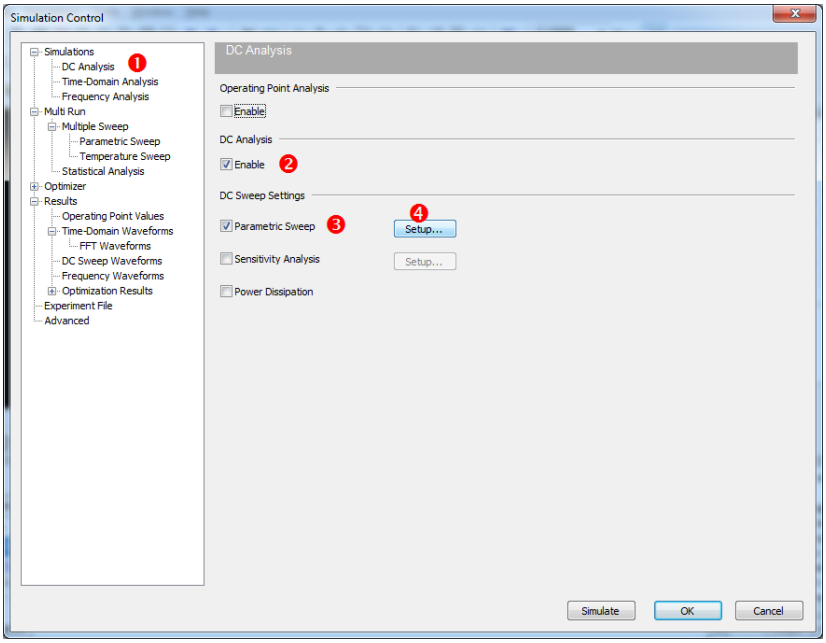


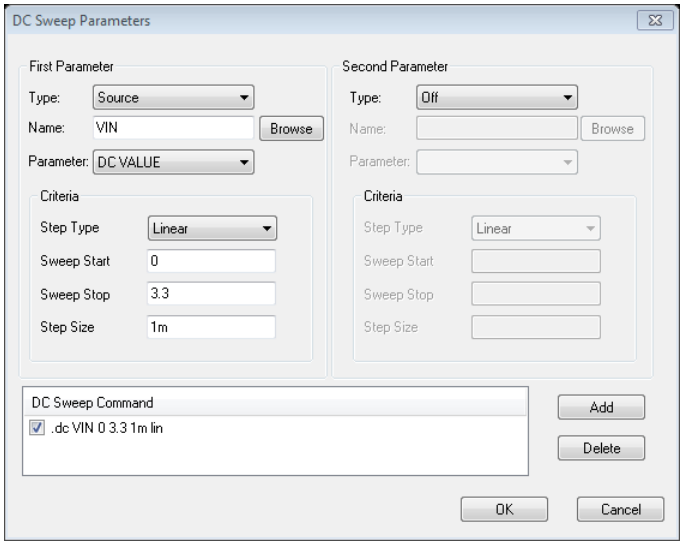
Figure 2. New source for PS

Perform a DC analysis using the following settings.



Set the simulation

Press „Simulate” then „Simulation Control” choose DC analysis (1), check enable (2), check „Parametric Sweep”(3) an set it up (4)! After the setting press „Add” button to set the simulation.



Setting of DC sweep

Use cursor (F5) to read the threshold voltage.

Task 2.

Simulate the delay of the inverter if a 0.1pF load capacitance is connected to the output.

Guide

Set the input voltage source. Define as pulse and here you can see the settings.

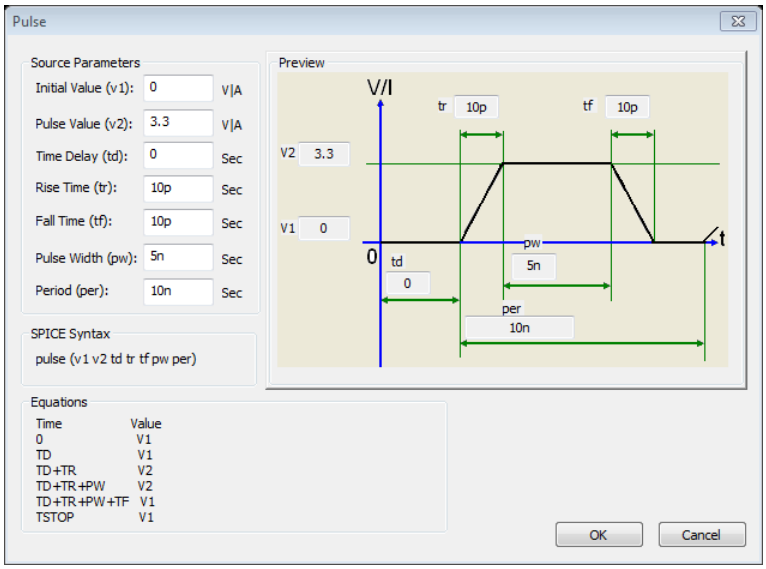


Figure 3. Set the parameters for source pulse

Switch the DC sweep of then set the time domain simulation. Tmax must be set of 1p.

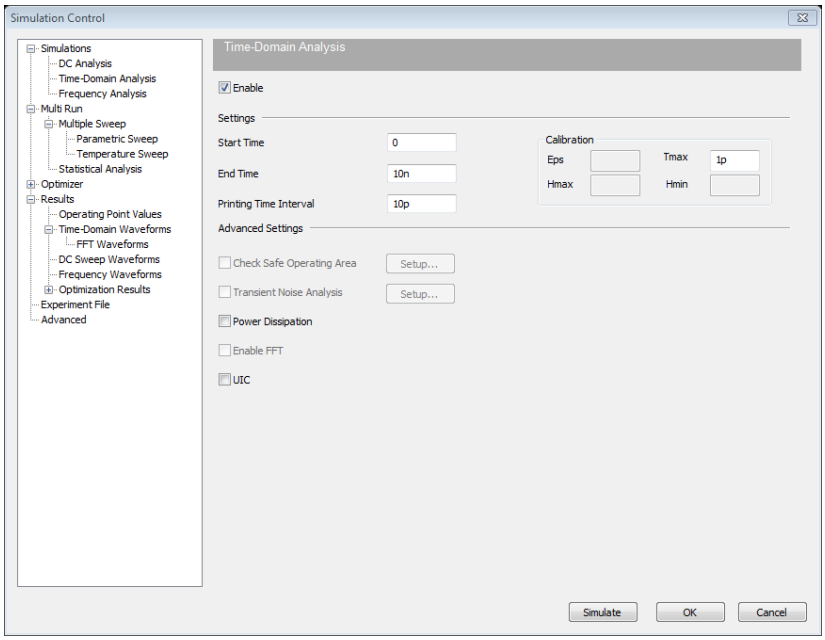
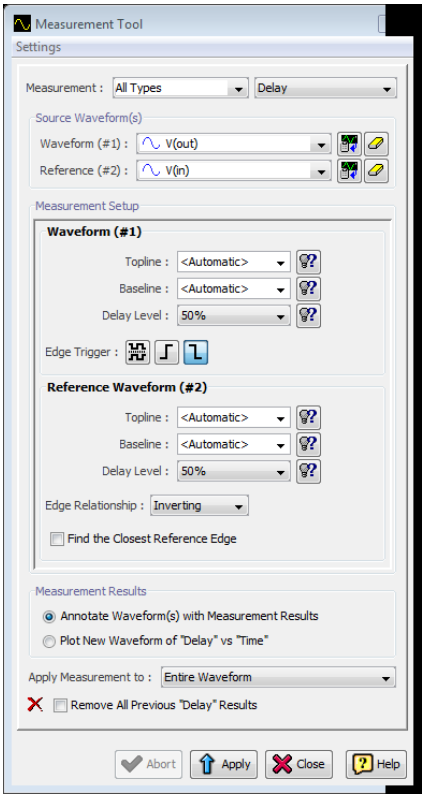


Figure 4. Set the parameters of time-domain analysis

The delay can be measured using EZWave „Measurement Tool”, choose „Delay” function. Drag and drop the voltage graph from the „Wave window”.



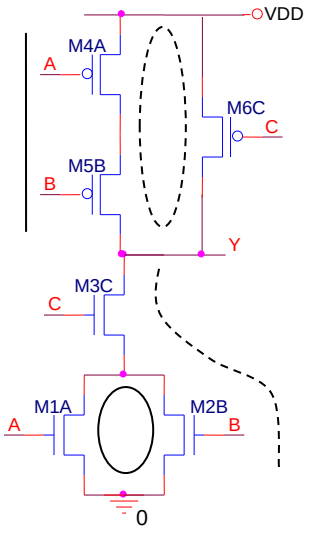
Measuring the delay

Edge relationship must be inverted and change the triggering to measure the delay in both cases.

Increase the frequency of the input signal (3x, 10x), and check the output wave.

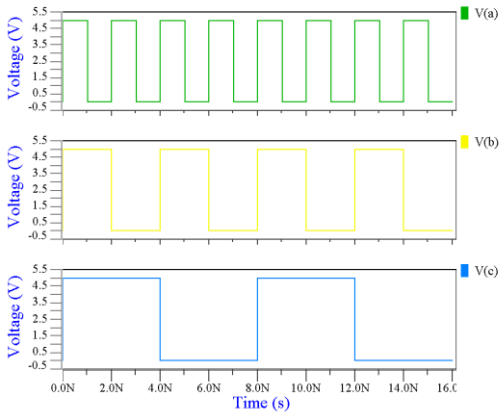
Task 3.

Simulate the CMOS digital complex gate which has a function of $Y = \overline{C(A+B)}$



Guide

Perform time domain simulation. Create all the input combinations. A signal has 2 ns periodic time and 1 ns long impulse, B has 4 ns periodic time and 2 length and C has 8ns periodic time and 4ns length as you can see in the figure below. Do not forget about the power supply source.



Input signals for the logic gate