Budapest University of Technology and Economics
Department of Electron Devices

Technology of IT Devices

Lecture 3

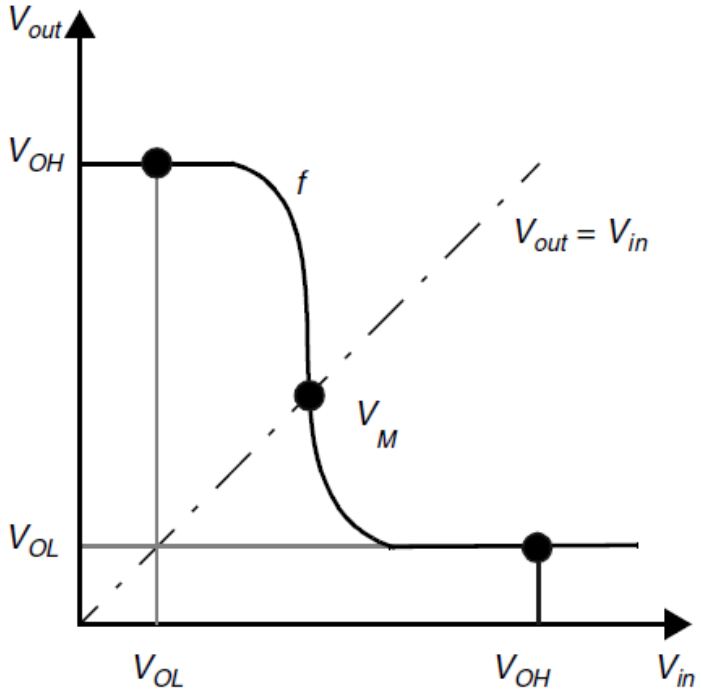
- Circuits of Boolean algebra
- Basic properties of digital logic

Circuits of Boolean algebra

- Boolean algebra
  - Boolean algebra is the branch of algebra in which the values of the variables are the truth values true and false, usually denoted 1 and 0 respectively.
    - Set of values $x \in \{0,1\}$
    - Basic operations $\neg \wedge \vee$ (NOT (negation), AND (conjunction), OR (disjunction))
- Physical quantities are assigned to the elements of the set of values, usually the voltage level.
  - (It can be current or voltage difference – in high speed logic circuits)
  - Generally, V_H is assigned to logical 1, and V_L is assigned to logical 0
  - Mostly V_H is equal to the positive supply voltage, and V_L is the ground
  - The voltage difference between V_H-V_L is the so-called swing
  - The difference between the positive power supply (VDD) and the ground (0V) is called RAIL
    - (The positive power supply and the ground have the widest wires in a circuit, and they seem like a rail - hence the name)

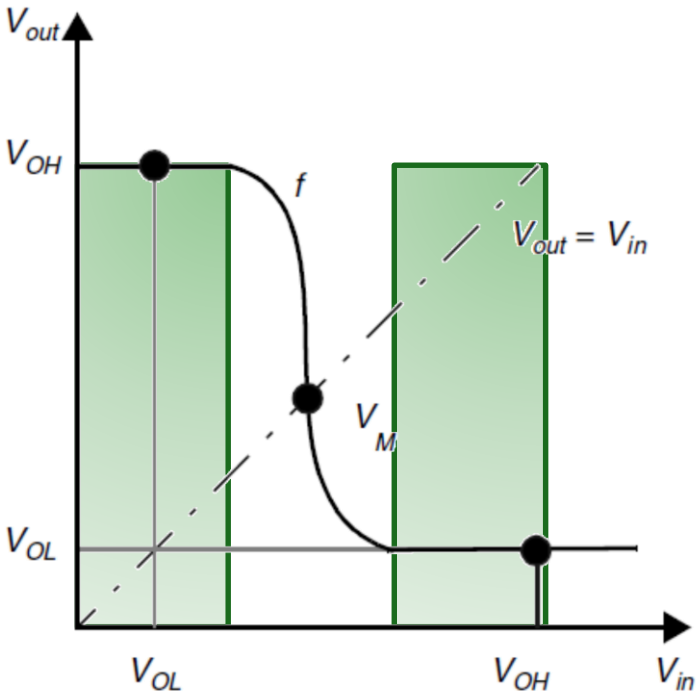
Transfer characteristic

- The relationship between the input and output of an electronic system, especially as depicted graphically
- The transfer characteristic of an inverter is shown on the right
- The output is the negated value of the input. $V_L=f(V_H)$ and $V_H=f(V_L)$
- The proximity of the supply voltage (VCC) is logic 1 or HIGH,
- and the proximity of the ground potential is logic 0 or LOW.
- The switching threshold, V_M, is defined as the point where $V_{in} = V_{out}$.



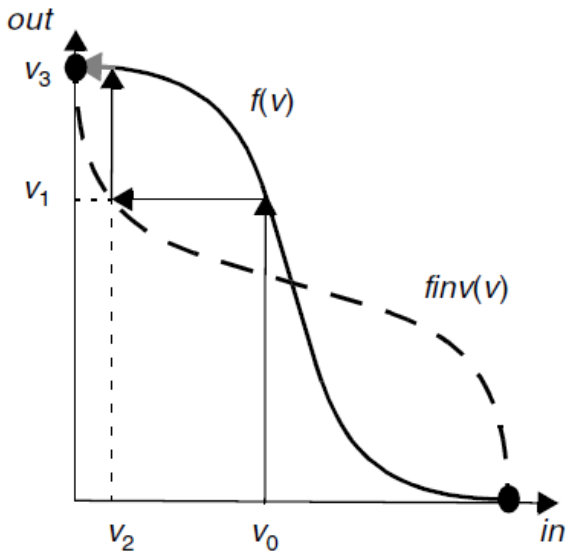
Noise immunity

- The same logic level is assigned to a wide range of input voltage.
  - When the noise level is lower than the limit it cannot appear on the output (the circuit can reject it)
- The characteristic has 3 regions
  - the extremes are flat, so the changes of input voltage cause only small changes on the output.
    - safe logic-level tolerances can be defined
  - In the central region the characteristic is steep.
    - (The amplification is high, so $A = \frac{dV_{OUT}}{dV_{IN}}$ high)
    - small changes of input voltage cause high changes on the output



Signal regeneration

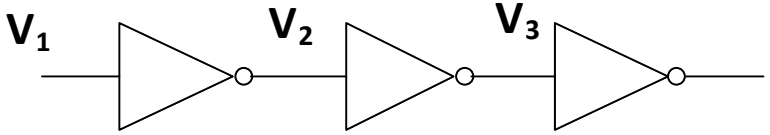
- During digital signal processing, digital signals regenerate



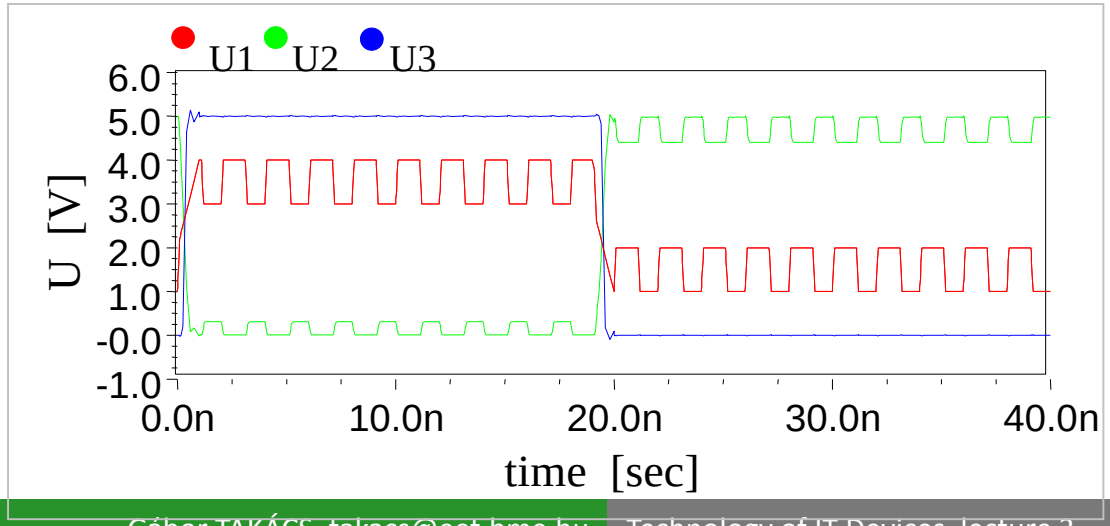
- In the figure above the transfer function of f(V) and its inverse function finv(V) can be seen
- The digital circuit converts the „weak” V_0 signal to V_1, V_2, V_3 voltages

Example: signal regeneration (circuit simulation)

- This is just a textbook example, the situation is even better in the real world!
  - A weak signal (lower than the nominal value by 1.5V) is applied on the input of the first inverter, and a $1V_{pp}$ noise signal is superimposed
  - On the output of the first inverter the voltage is lower than the nominal value by 0.5V, and the noise level is reduced by the factor of ~3.
  - The output of the second inverter is almost perfect.
  - The level and the shape of the signal is completely regenerated



V_L=0V, V_H=5V



Example for signal levels

- Fairchild, 74HC00

DC Electrical Characteristics (Note 4)

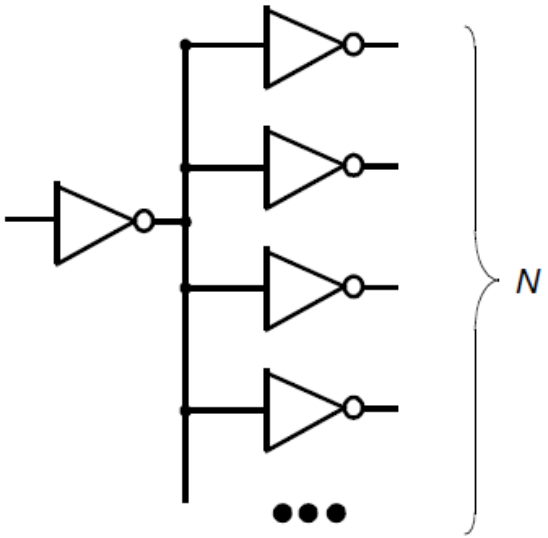
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\ \mu A$	6.0V		2.0	20	40	µA

Robustness

- Digital logic circuits are ROBUST
- Within given limits, they are not sensitive to
  - Changes in the power supply
  - Changes in the ambient temperature
  - Mismatches of component parameters
  - etc.

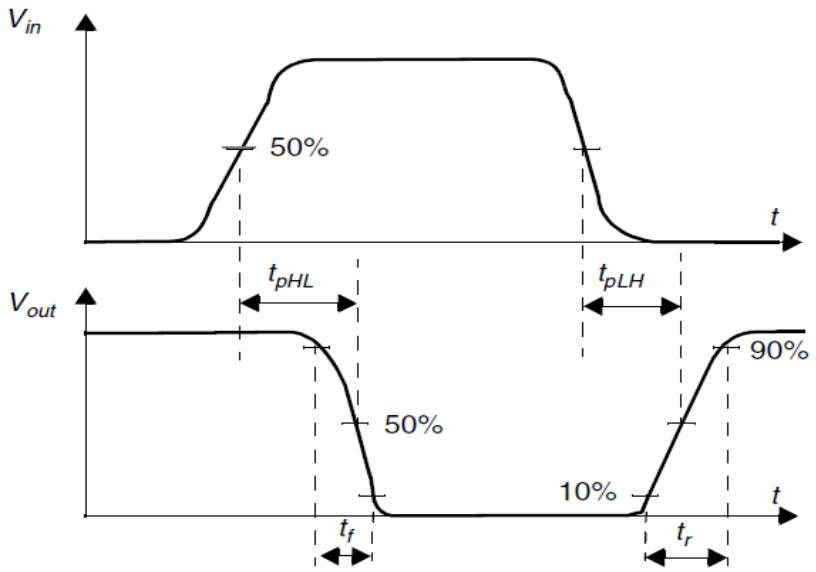
Fan-out

- Fan-out is a term that defines the maximum number (N) of digital inputs that the output of a single logic gate (of the same type) can feed.
- Eg. FO4 – 4 logic gates can be connected to the output



Propagation delay

- When an input signal of a logic gate is changed, there is a propagation delay before the output of the logic gate changes.
  - This is due to capacitive loading at the output.
  - The propagation delay (t_p) is measured between the 50% transition points of the input and output signals.
  - Rise time (t_r) and fall time (t_f) are measured between the 10% and 90% transition points

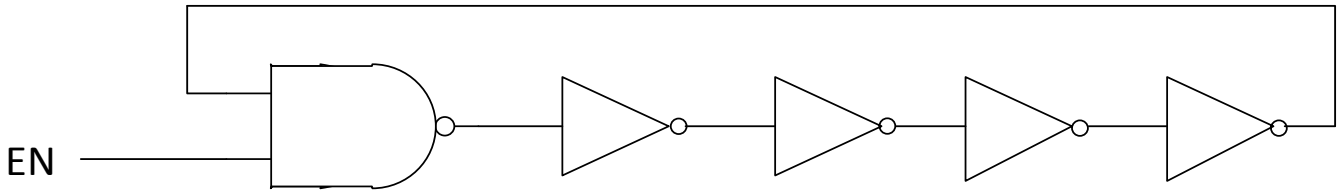


Propagation delay

- The length of the positive and negative edge can be different.
  - t_{pHL} – delay of high to low transition
  - t_{pLH} – delay of low to high transition
- The delay is the average value of these two values
  - $t_{pd} = \frac{t_{pLH}+t_{pHL}}{2}$
- The critical path is defined as the path between an input and an output with the maximum delay.
- The critical path determines the speed of the whole digital circuit

Ring oscillator

- Ring oscillator: an odd number (N) of inverters connected in series with the output connected to the input.
- The figure below depicts a practically used version.
  - The first inverter is replaced by a NAND gate.
  - If EN input is high, the NAND gate acts like an inverter
  - This circuit has no stable states, it oscillates
  - The frequency of the oscillation is a function of the propagation delay: $T = 2Nt_{pd}$
    - The pair delay can be measured with a ring oscillator



Power and energy

- Power = It is the amount of energy consumed per unit time.
  - SI unit: Watt (J/s)
  - Two important parameters
    - Average power: $P_{av} = \frac{V_{DD}}{T}\int_0^T I(t)dt$
    - Peak power: $P_{peak} = V_{DD}I_{peak} = V_{DD}\max(I(t))$
    - were V_{DD} is the supply voltage of the gate, I is the current
- The power consumption can be divided into two parts
  - Static consumption – It is always present
  - Dynamic consumption – at every switching event. It depends on the frequency and the switching probability.
- Energy
  - $E = \int P(t)dt$
  - SI unit: Joule (kWh)

Power–delay product (PDP)

- The power–delay product is correlated with the energy efficiency of a logic gate or logic family
  - In current technologies capacitive dissipation is by far dominant
- The power-delay-product (PDP) is a measure of energy and is defined by the product of the average power (P_{ave}) and the gate delay t_p
  - PDP is $C_L V_{DD}^2 f_{max} t_p$ which is equivalent to $C_L V_{DD}^2/2$.
  - This expresses the average energy consumed per switching event.
  - This is a metric for digital designs

Example

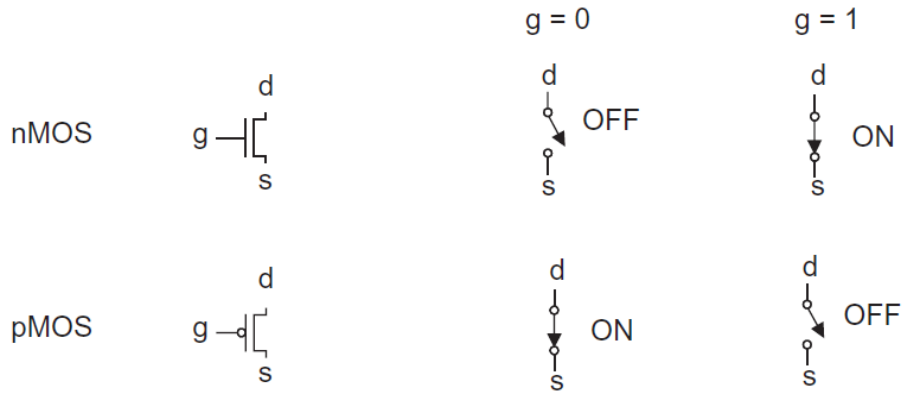
- Lets assume that we have a microprocessor, where the dominant factor is the dynamic power consumption. Lets decrease the frequency by the factor of 2. Can we extend the battery lifetime in this way?
- Solution:
  - The power at the half frequency is: $P' = \frac{P}{2}$
  - The runtime of the same program is double: $\Delta t' = 2\Delta t$
  - Energy consumption: $E' = P'\Delta \mathrm{t}' = 0.5\mathrm{P} \cdot 2\Delta t = E$
  - So the energy consumption is the same, but we have to wait twice as much time for the result

CMOS circuits

- Complementary MOS
  - The words "complementary" refer to the fact that the typical design style with CMOS uses complementary pairs of p-type and n-type MOS transistors for logic functions.
  - rail-to-rail levels: the logic levels are exactly equal to the supply levels
    - $V_H = V_{DD}$, $V_L = 0V$
  - Static (steady-state) current consumption is very low (almost zero).
  - Propagation delay of positive and negative edges are equal
  - Very low sensitivity to supply voltage ripple.
  - Area occupied by the logic gates is much smaller than other types
    - We can integrate more components on a unit surface

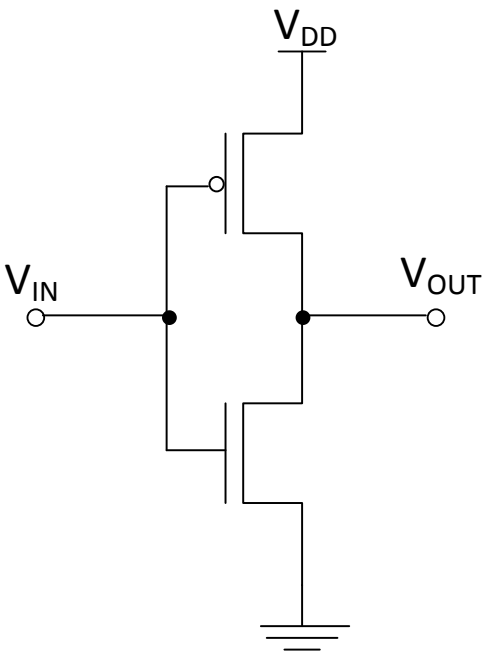
nMOS and pMOS transistors as switches

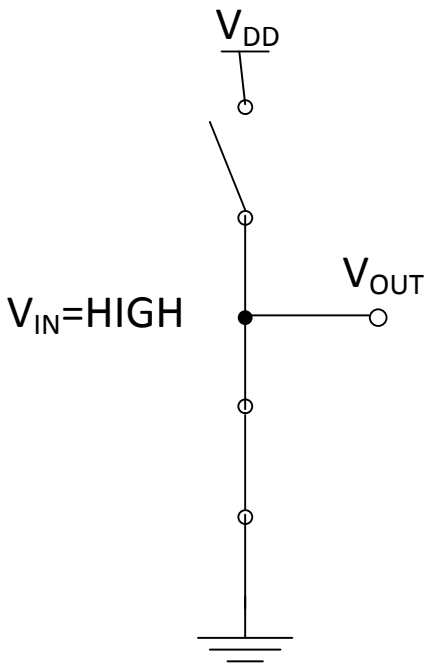
- nMOS
  - In case of logical 0: open switch (does not conduct current)
  - In case of logical 1: closed switch (conducts current)
- pMOS
  - logical 0: conducts current,
  - logical 1: does not conduct current
- The symbol of pMOS transistor has a circle at the gate terminal

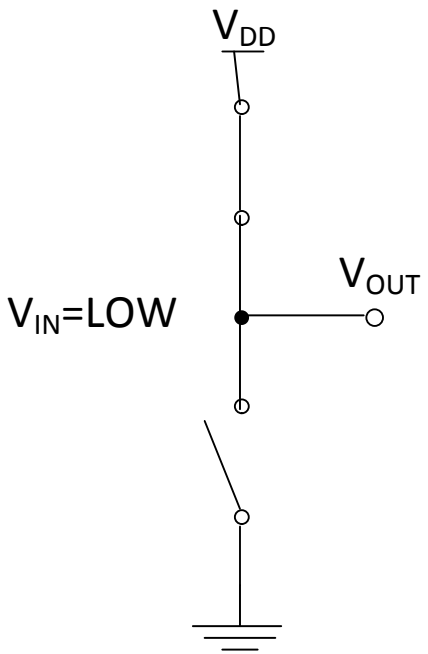


Schematic of CMOS inverter

- CMOS inverter: an n-MOS and a p-MOS
  - At any time only one of them is open

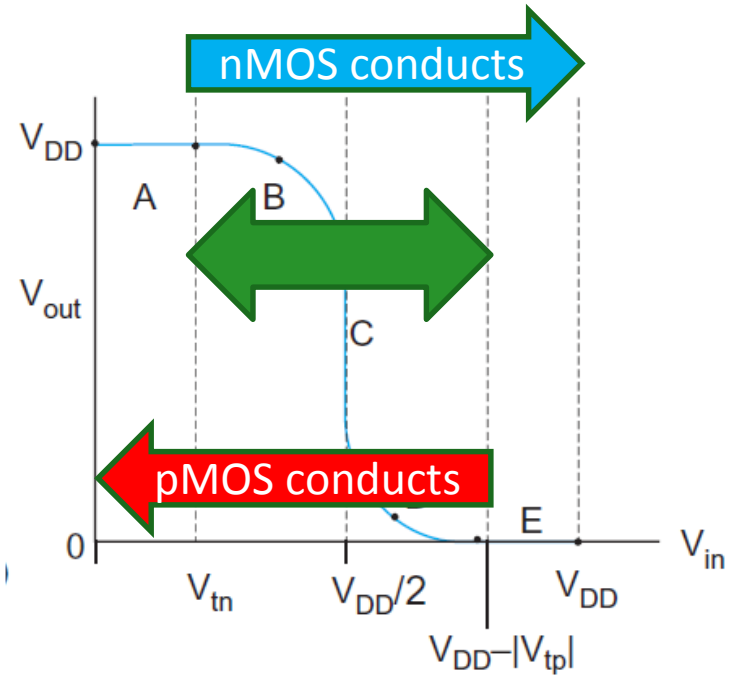




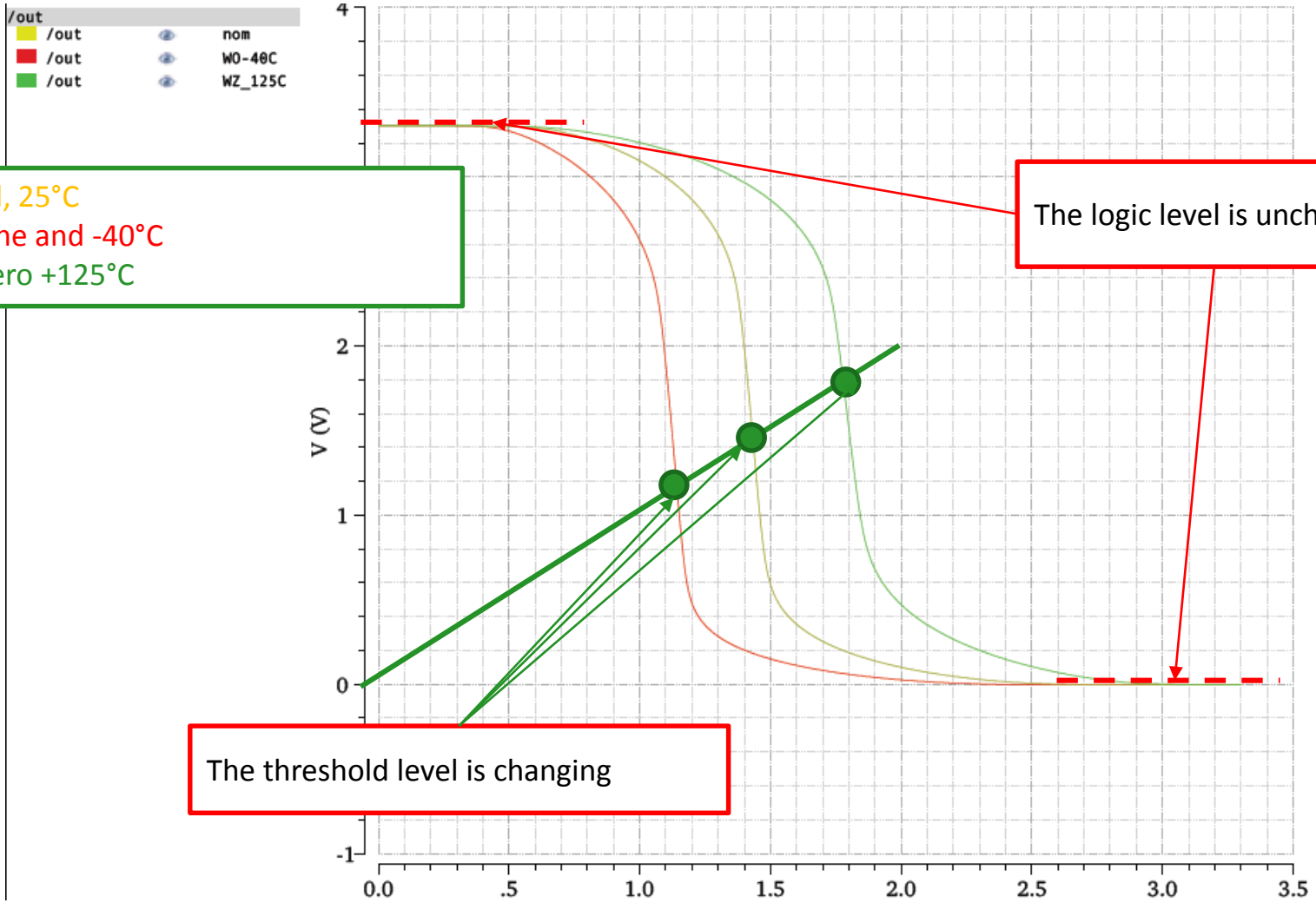


Transfer characteristic curve of the inverter

- The nMOS transistor conducts current when the input voltage is higher than the threshold voltage.
- The pMOS conducts current when the input voltage is lower than V_{DD}-V_T
- There is a region (in case of high supply voltage) where both transistors conduct current, $V_T \leq V_{IN} \leq V_{DD} - V_T$

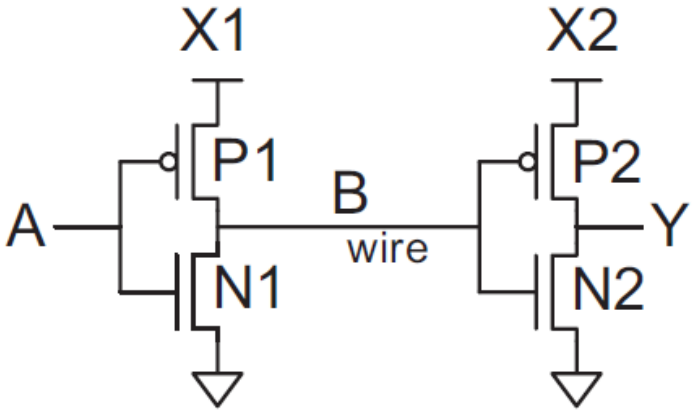


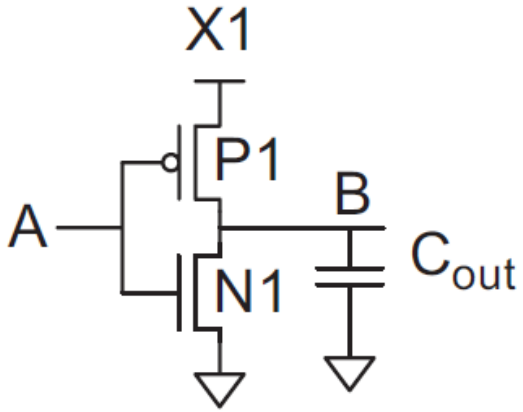
Simulated transfer characteristic of CMOS inverter



Load of CMOS inverter (gate)

- The load is capacitive
  - Transistors have internal parasitic capacitances (intrinsic capacitances)
  - Capacitances of interconnect wires – This is dominant in a modern technology



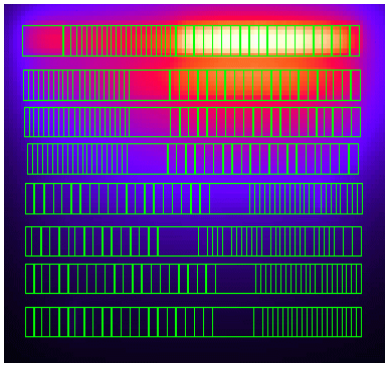


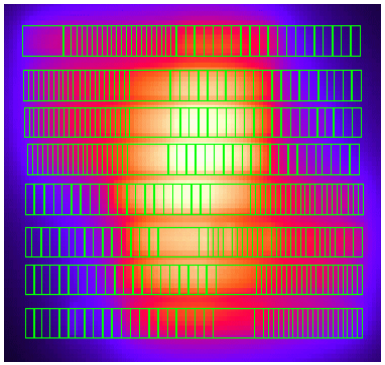
Propagation delay

- The propagation delay is determined by the charge and discharge of the (parasitic) capacitances
- The higher the capacitances, the higher the delay
- It the power supply voltage is higher, the delay is lower (due to the higher charging and discharging.
  - (To be more precise: $Q = CV_{DD}$, but $I \sim V_{DD}^2$)
  - How does the overvolting help us to overclock?
    - To improve a computer performance we can increase the clock frequency
    - It is necessary to increase the core voltage as well to maintain the signal levels

Power

- Static power consumption.
  - It is important in modern circuits
    - Sub-threshold currents,
    - Leakage currents of the pn-junctions,
    - Tunnel current through the gates
- Dynamic consumption – at every switching event:
  - The current that flows during transitions
  - It is proportional to the clock frequency and the activity of the circuit.

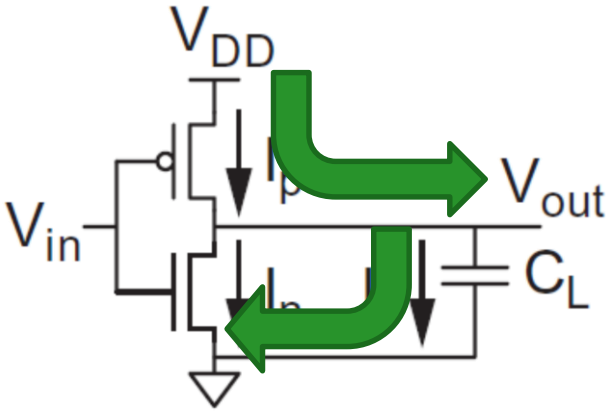




Dynamic current consumption

- The dynamic current consumption is the sum of two factors:
  - Transition current: both transistors are open during the transition between logic states
  - Charge pumping: during a positive edge the load capacitance is charged to logic 1 by the pMOS, during a negative edge the load capacitor is discharged through the nMOS.
- The dominant factor is the charge pumping.

Charge pumping



- The output capacitance is loading:
  - The stored energy in the capacitor:

$$E_C = \frac{1}{2} C_L V_{DD}^2$$

  - The energy needed from the power supply:

$$E = \int_0^\infty I(t) V_{DD} dt = \int_0^\infty C \frac{dV}{dt} V_{DD} dt = C V_{DD} \int_0^{V_{DD}} dV = C V_{DD}^2$$

Half of the energy is stored in the capictor, the other half is lost (dissipated by the pMOS transistor).

  - During the discharge event the charge is removed by the nMOS transistor (no energy is needed from the power supply).

Charge pumping

- During transitions charge is pumped into and out of the load capacitor, i.e. charge is pumped from the supply to the ground
- If the circuit switches at frequency (f_{sw}) per unit time (T), the number of switch transitions is

$$T f_{sw}$$

- The required power:

$$P = \frac{E}{T} = f C V_{DD}^2$$

The power consumption of a CMOS digital circuit is proportional to f and V_{DD}^2

$$P \sim f V_{DD}^2$$

Dynamic Voltage Frequency Scaling

- The frequency of a microprocessor can be automatically adjusted "on the fly" by the OS.
  - Higher clock frequency requires higher core voltage
  - At lower frequencies less voltage is enough
  - The power consumption is a square function of voltage
- Calculate the power ratio of the P0 (1.6GHz@1.484V) and the P5 (600MHz@0.956V) states of a Pentium M processor

$$\frac{P_0}{P_5} = \frac{1.6}{0.6}\left(\frac{1.484}{0.956}\right)^2 = 6.4$$

  - According to the Intel datasheet, the ratio is 4.2. The difference is due to other power consumption factors