Budapest University of Technology and Economics
Department of Electron Devices

Technology of IT Devices

Lecture 10

I/O, clock, data bus

Contents

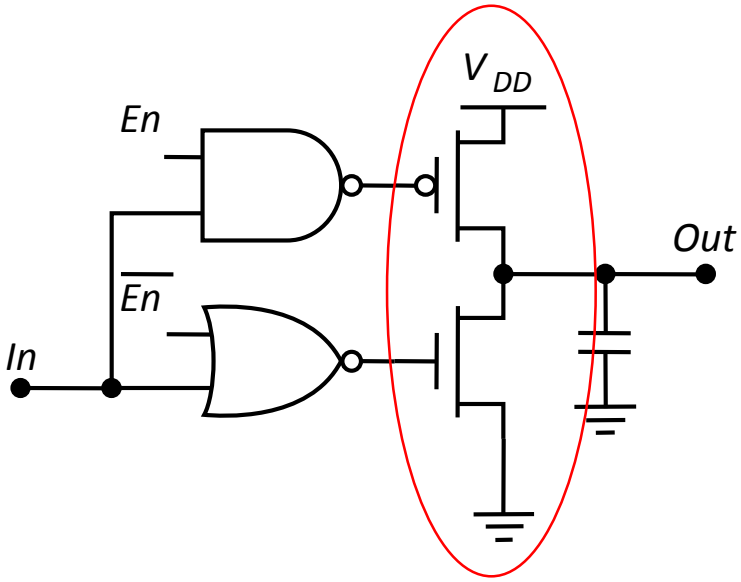
- I/O, realization of input and output
  - Architecture and operation of I/O pads
  - ESD protection
  - Settings of GPIO
- Clock signals
  - Generalization of clock signals
  - Clock signal distribution
- Data bus

I/O circuits

- Responsible for communication with external devices
- Protect chip against overvoltage and electrostatic discharge (ESD protection)
  - If a human touches an IC, the charge/discharge voltage can be a few kV, and the current is a few µA
  - Shock delivered to a chip can fry thin gates of input transistors.
- Drive large off-chip capacitance
  - High current required
  - Usually tri-state buffers with registers
- Power supply and ground pins
  - They provide the required power supply voltage and current
  - In a modern digital circuit there many VDD/GND pins
    - The sum of the switching currents is very high (up to 100A)

Tristate-buffers

- En=0
  - PMOS gate 1, NMOS gate 0
  - Both transistors are closed, so the output is “floating”
  - High impedance
- En=1
  - The input controls the gates.
  - E.g. In=1, the output of the NAND gate is 0, the output of the NOR gate 0.
  - Hence, the PMOS conducts current, and the output is logic 1
- This is called the PUSH-PULL stage



ESD protection

- ESD – Electrostatic Discharge
  - It is the sudden flow of electricity between two electrically charged objects
  - Caused by:
    - Contact
    - An electrical short
    - Dielectric breakdown
  - A few kV, but it has low energy.
- If an input voltage exceeds the breakdown voltage of the transistor's gate oxide, the transistor can be damaged
  - Usually the whole circuit is damaged
  - The breakdown voltage is ~40V, but in the case of low voltage circuits it can even be 5V.

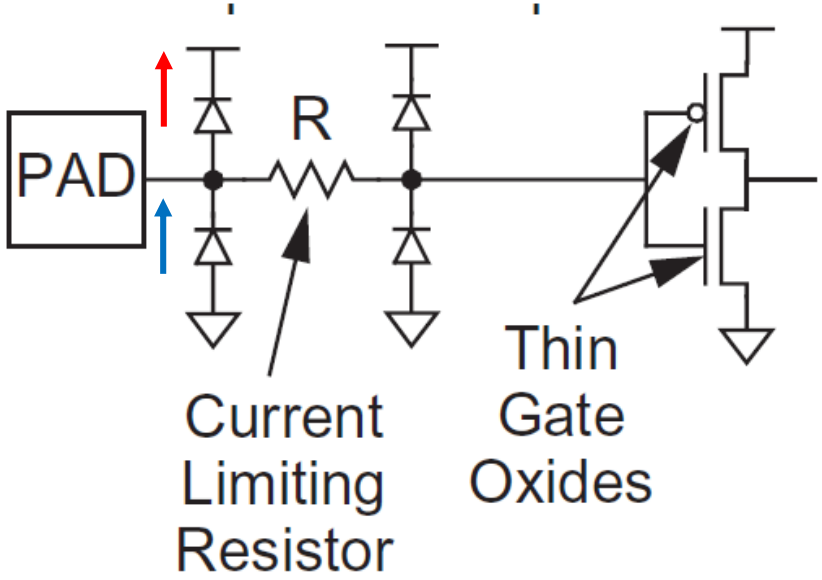
ESD protection

- High voltage on the output can cause a short circuit
  - Overheating
  - Total damage of the circuit

- The inputs and outputs are protected against overvoltage and ESD
  - Inside the IC package
  - On the PCB

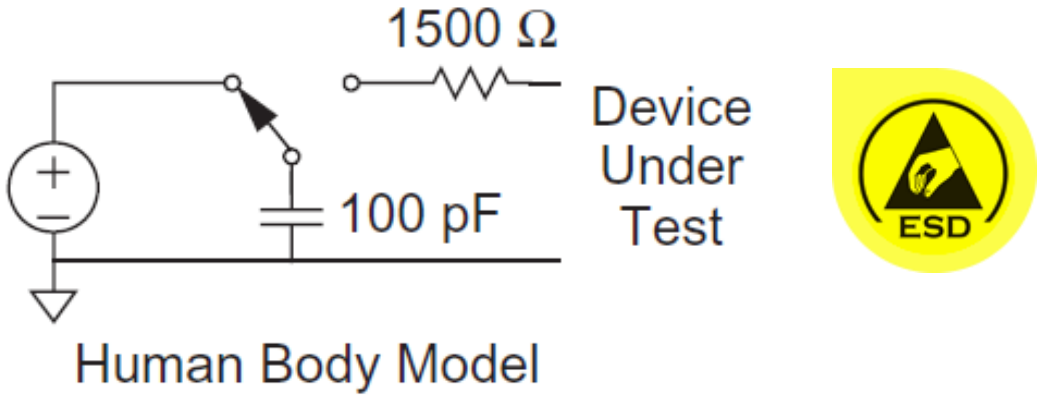
ESD protection

- Reminder
  - If the anode of a diode is at a higher potential than the cathode, the diode conducts large current
  - Otherwise, it doesn't conduct



- The diodes conduct when the input voltage is higher than the power supply voltage, or lower than the gnd voltage
  - The red arrow shows the current if the input voltage is positive
  - The blue arrow shows the current in the case of negative input voltage
    - The diode has ~1Ω series resistance, so the current can be a few 10s of Amps
    - The current is limited by a resistor, and another diode stage is inserted

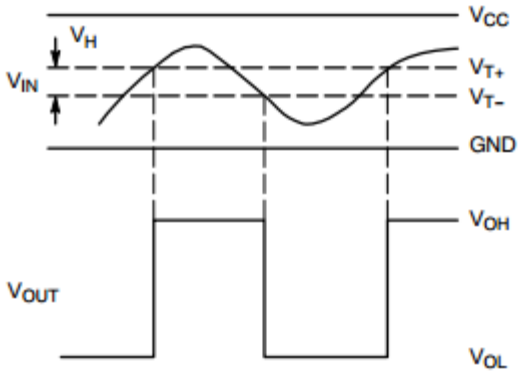
Human body model



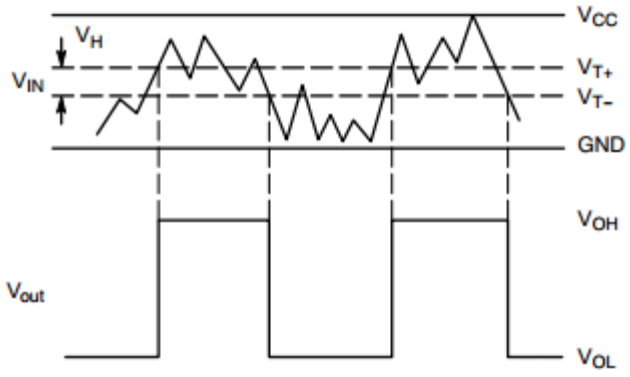
- A capacitor of 100pF is charged to certain voltage, and it is connected to the DUT through a 1,5kΩ resistor.
- The rating depends on the maximum survived voltage
  - E.g. ESD 2 – between 2kV and 4kV
- ESD protection (external)
  - Antistatic garments (antistatic clothing, shoes etc.)
  - Antistatic floor

Inputs

- Inputs are generally connected to Schmitt-trigger circuits
  - A Schmitt-trigger is a comparator circuit with hysteresis
  - It has two threshold levels
  - They are typically used in signal conditioning applications to remove noise from signals used in digital circuits
  - The hysteresis is usually ~100-200mV



(a) A Schmitt–Trigger Squares Up Inputs With Slow Rise and Fall Times

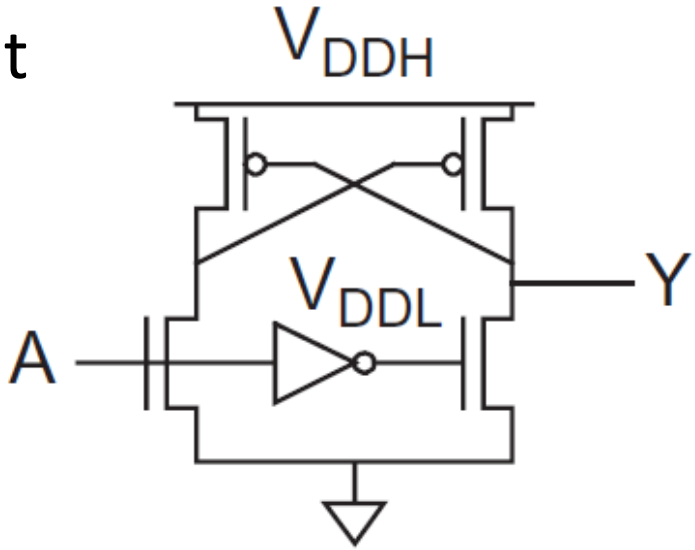


(b) A Schmitt–Trigger Offers Maximum Noise Immunity

Voltage of logic levels

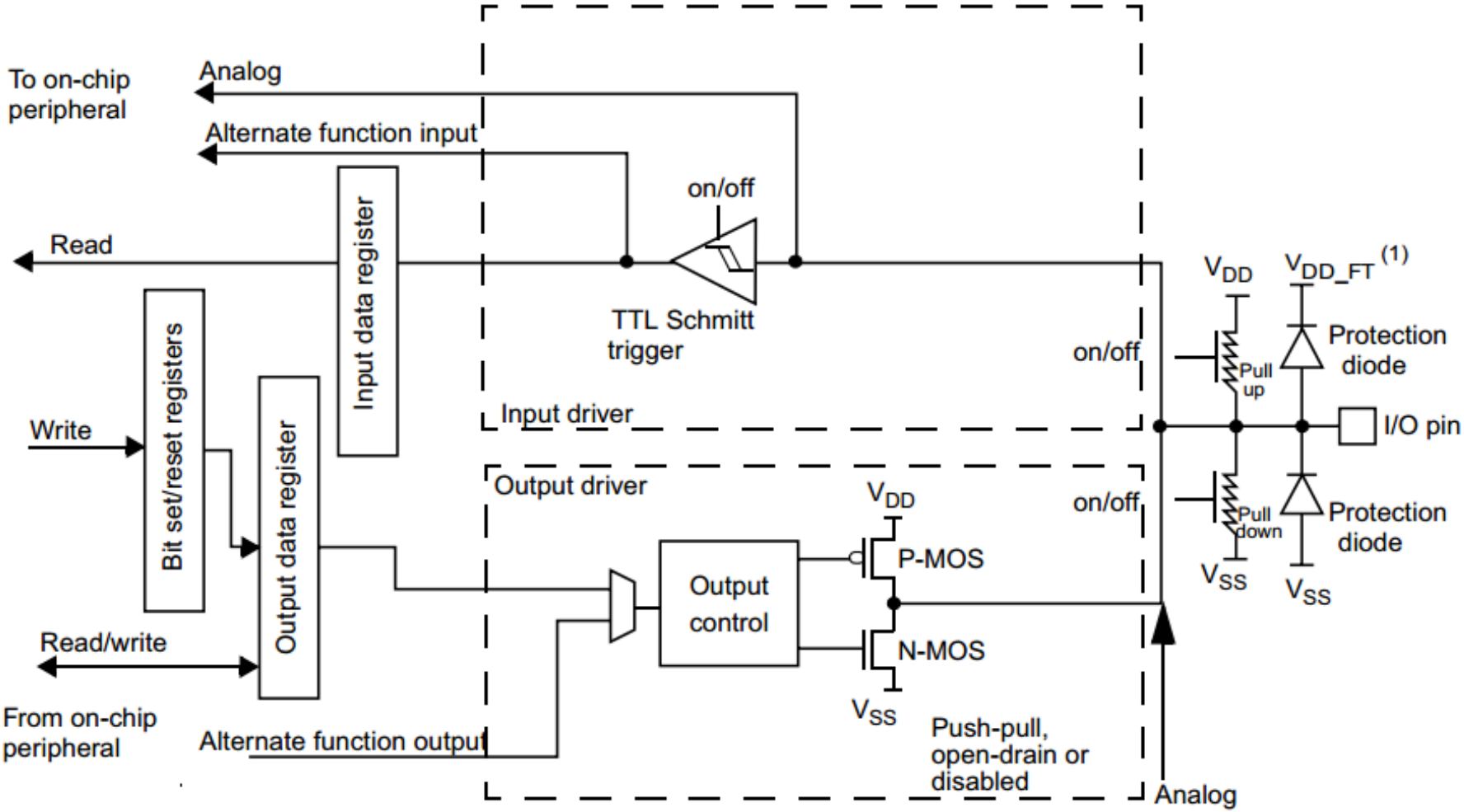
- The voltage of the core and the voltage of the I/O pins can be different
  - There are core power supply pins and I/O power supply pins
- In the case of I/O pins there are standard voltage levels
  - 5V (TTL) 3.3V, 2.5V, 1.8V, 1.5V, 1.2V
  - The core voltage is lower…
    - … and usually it changes dynamically (depending on the computational load)
- The oxide thickness and the threshold voltage of the I/O transistors are different
- The logic voltage conversion has to be solved
  - Level shifter circuits
  - They are the bridges between the two voltage domains

Level shifter circuit



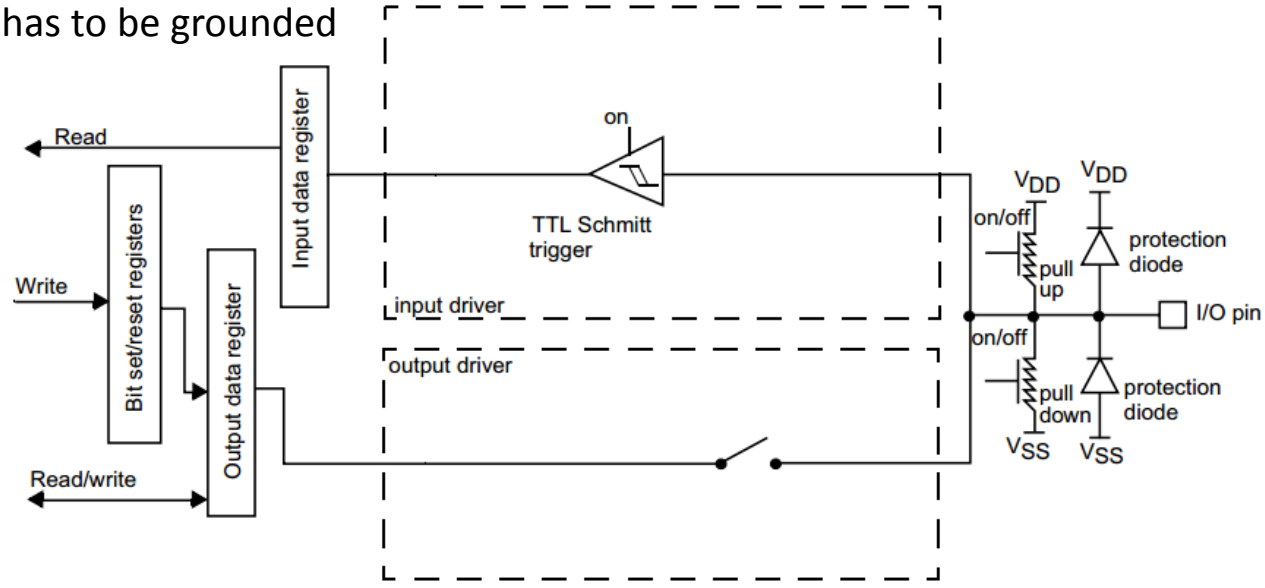
- It converts a lower logic voltage to a higher one
  - The schematic is similar to a latch / SRAM cell
  - If A = 0 then the inverter inverts, the NMOS transistor on the right conducts (output = 0)
  - If A = 0 then the NMOS on the left conducts, and the upper right PMOS conducts as well (output = 1)

Example – a practical GPIO. (STM32F407)



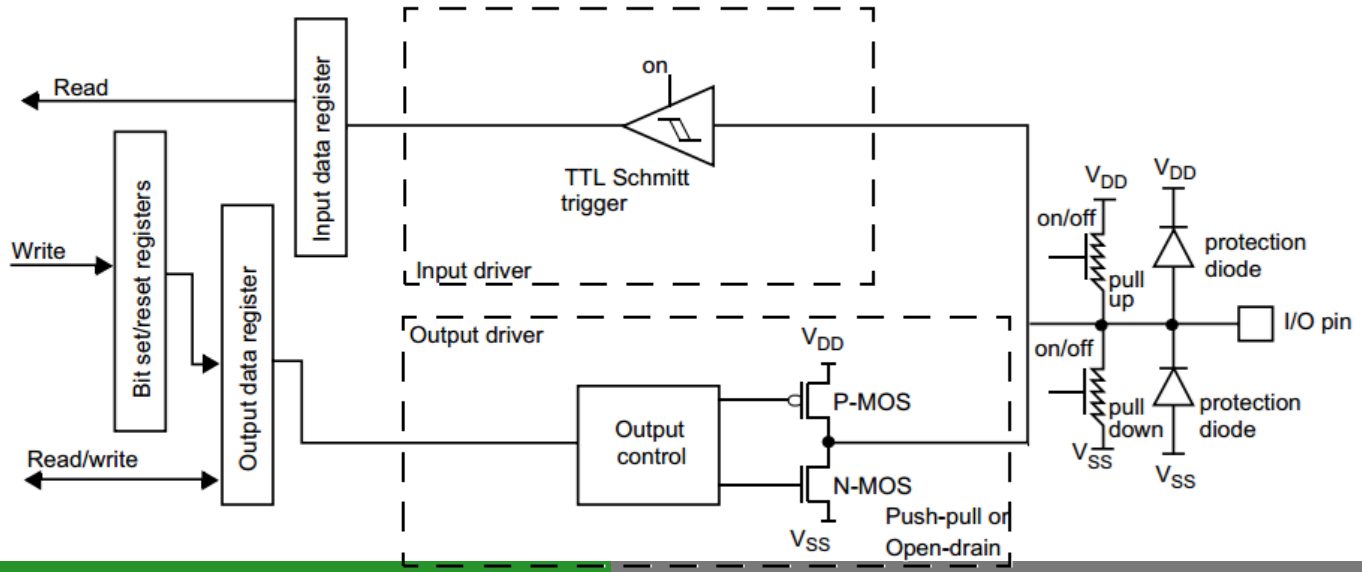
The input settings

- VDD_FT, 5V tolerant input,
  - It means that the pins can be driven up to a 5V logic level without damage or sinking current through protection diodes
  - The VDD voltage of the diode is connected to a higher potential (V_{DD_FT})
- The input is connected to a Schmitt trigger circuit which has a hysteresis of 5% or 100mV minimum.
- There are configurable pull-up and pull down resistors with values of ~40kΩ
  - We can fix the logic level (e.g in the case of interrupt request pin)
  - The unused pin has to be grounded



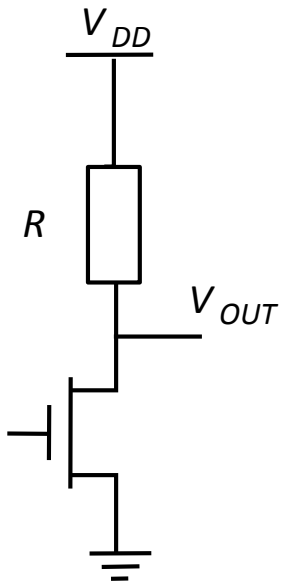
The output settings

- The output can be a push-pull stage
  - Either the NMOS or the PMOS conducts
  - It connects the output to the power supply or to the ground
- Open drain (or open collector – in TTL cases)
  - Only the NMOS is driven
    - It can only sink current (force 0)
    - More than one output pin can be connected to one input pin ($\overline{IRQ}$)



Open-drain output

- A single NMOS transistor is controlled
  - If the transistor is open-circuit, there is no current, the output is connected to VDD through the resistor
  - If the transistor conducts current, this circuit becomes a voltage divider
  - If the resistance of R is high enough, and the channel resistance of the transistor is low, the output voltage is around 0V (but not exactly 0)
  - If the output is low, current flows between VDD and the ground
    - This causes static power consumption!



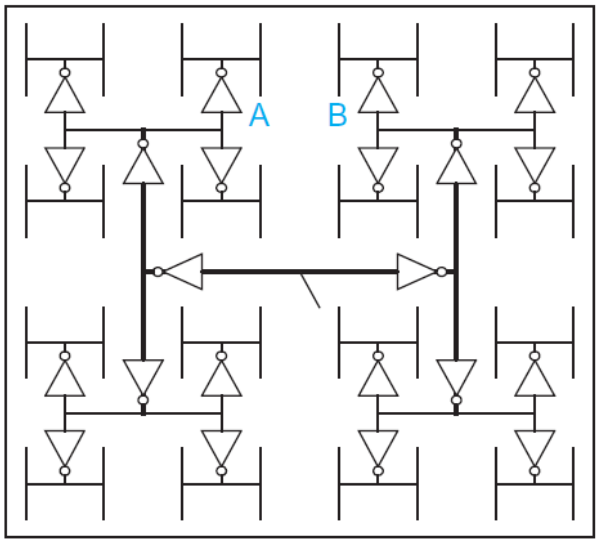
Further I/O settings

- Maximum output current (fanout)
  - Power saving: use the minimum sufficient current setting.
  - E.g. 10mA, 5mA or simply low/high strength
- Slope of the output (speed)
  - Slew rate.
  - $SR = \frac{dV}{dt}\Big|_{MAX}$
  - V/µs is the usual dimension
  - The faster the output the higher the noise
  - To decrease the noise the lowest acceptable SR has to be set

Clock signals

- Today's digital circuits have synchronous operation
  - The asynchronous circuits are more efficient and faster, but there are a lot of design challenges (like race conditions). And there are no logic synthesizers…
- Increasing the size of a chip results in longer clock signal paths on the surface of the integrated circuit
- The clock signal:
  - Switching probability = 1 (it always works)
  - It operates at the highest frequency
  - It is connected to almost all the cells in the case of ASIC and FPGA too
  - It causes ~40% of the power consumption
    - Power saving: clock gating, dynamic frequency scaling

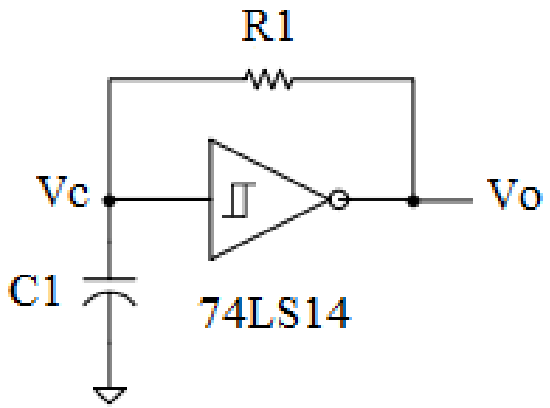
- Clock signal distribution
  - Clock distribution networks synchronize the flow of data signals among synchronous data paths
  - It distributes the clock signal(s) from a common point to all the elements that need it
  - Uncertainty in the arrival times of the clock signals can limit the maximum performance of the entire system
  - The most effective way to get the clock signal to every part of a chip that needs it, with the lowest skew, is a metal grid.
  - It can be a symmetrical, tree-topology network
  - Clock skew: a phenomenon in synchronous circuits in which the same clock source signal arrives at different components at different times.
  - The clock skew has to be lower than 5%
    - @3GHz it is 16ps!

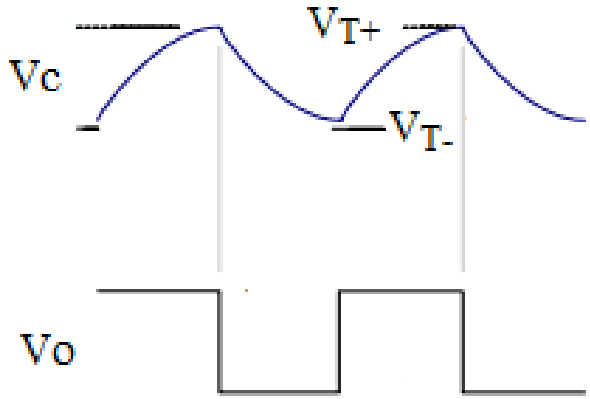


Clock signal generation

- Oscillators
  - It is an electronic circuit that produces a periodic, oscillating electronic signal
  - (e.g. a ring-oscillator (Lecture 3))
- RC oscillator
  - The oscillating frequency depend on the resistor and capacitor (f=1/(2*Pi*R*C)
  - In the case of integrated circuits it is not so precise (due to the variation of the resistance)
    - It requires calibration (after production or during operation)
  - The precision: 0.01%-1% (again it is not enough, and the frequency is temperature-dependent)
  - Fast startup
  - In the case of an external oscillator the chip starts using the internal oscillator, and after a while the chip switches to external one

A simple RC oscillator





- A Schmitt trigger based circuit
  - Assume that the voltage of C1 is 0V
  - The output of the inverter is VDD, the capacitor is charging through the resistor R1
  - If the voltage of C1 reaches the threshold level, the inverter switches, and C1 discharges through R1
  - Until the lower threshold level, when the output of the inverter becomes logic one again

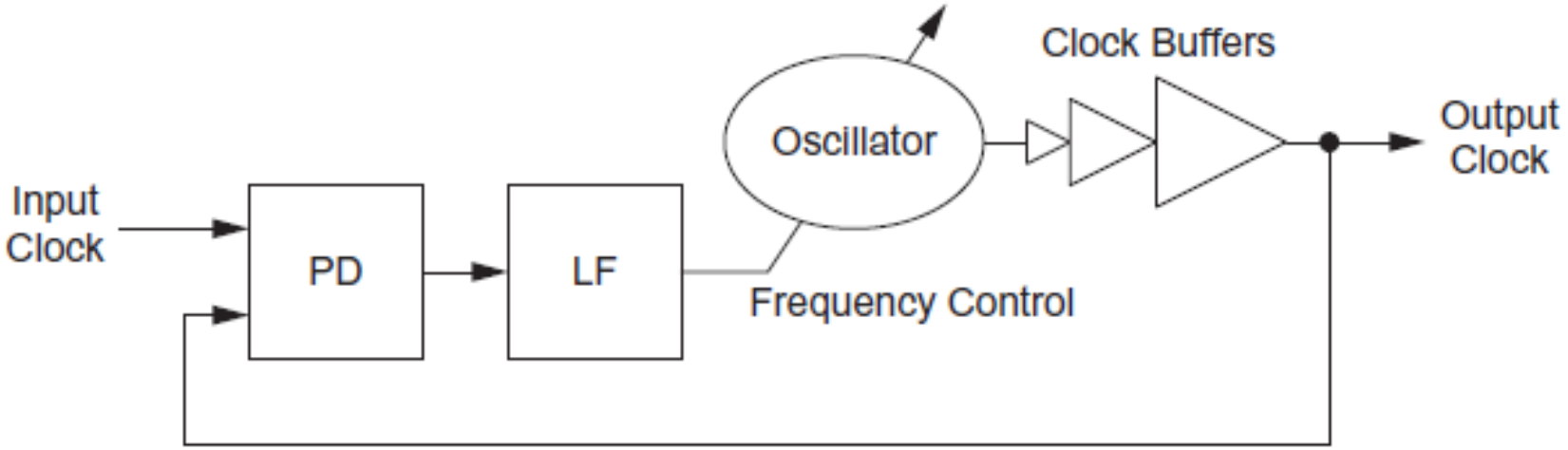
Resonators

- Crystal (quartz) or ceramic resonator
- It has piezoelectric effect
  - The electric charge that accumulates in certain solid materials in response to applied mechanical stress.
  - The quartz crystal has a precisely defined natural frequency (caused by its shape and size) at which it prefers to oscillate.
- The natural frequency can be set by the shape and size of the quartz crystal
  - Precision: ±10-100 ppm (parts per million)
  - E.g. a quartz of 4MHz with the precision of 10ppm: the output frequency is between 3 999 960 and 4 000 040Hz
  - The temperature dependency is low: 1-10ppm /°C
  - (sometimes this precision is not enough, so there are temperature controlled oscillators – OCXO)

Commonly used crystal frequencies

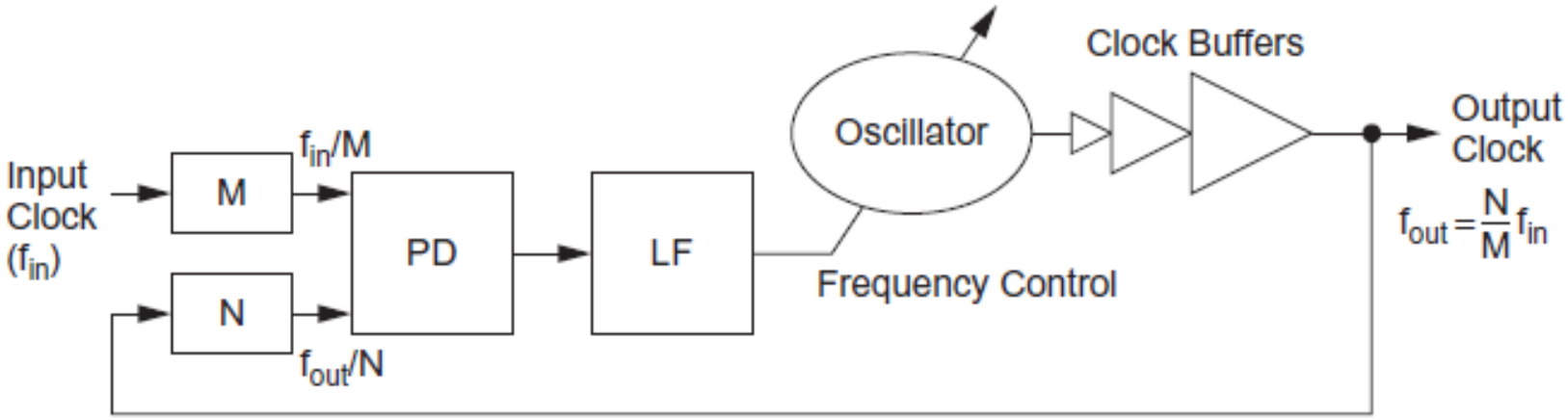
- Most important frequencies:
  - 32,768kHz – for all RTC (real time clock)
  - 8MHz, 10MHz, 20MHz, 25MHz – for general purposes
  - 11.0592MHz – UART
  - 12MHz – USB, CAN
  - 27MHz – PAL, NTSC television techniques…
  - Etc.

Phase-locked loops (PLL)



- It generates an output signal whose phase is related to the phase of an input signal
- It can generate a frequency that is a multiple of the input frequency
- Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications.

PLL – frequency synthesis

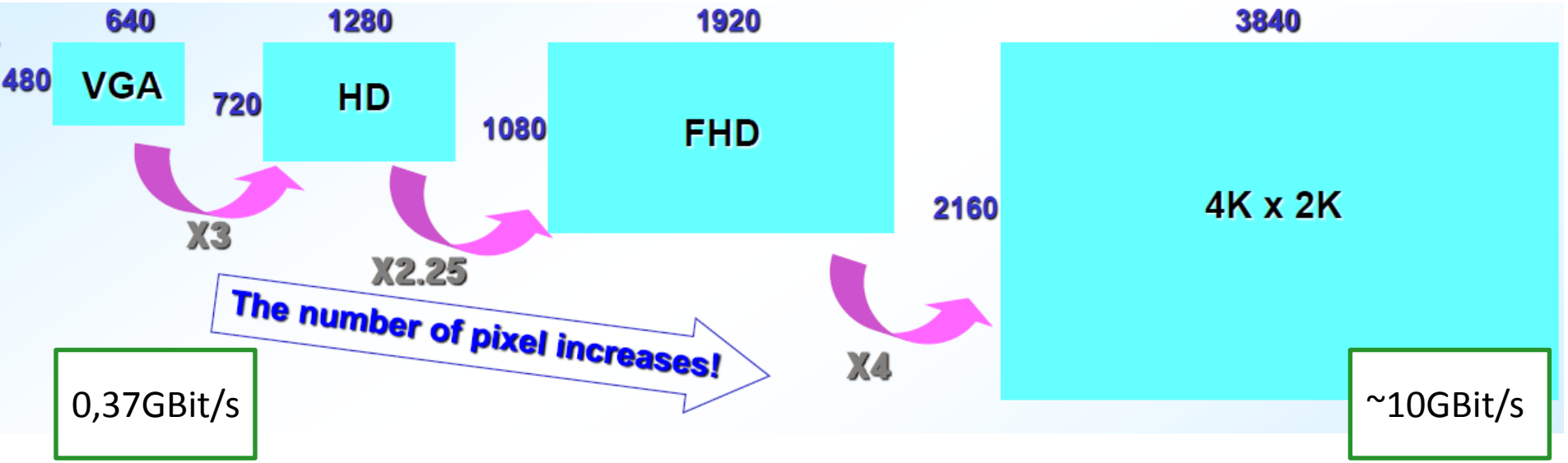


- Basic elements:
  - Frequency dividers (M and N)
  - Phase detector (PD): generates a voltage signal which represents the difference in phase between two input signals
  - Low pass filter (LF)
  - Variable-frequency oscillator (mostly voltage controlled oscillator)
- It generates a frequency that is a multiple of the input frequency

Digital communications

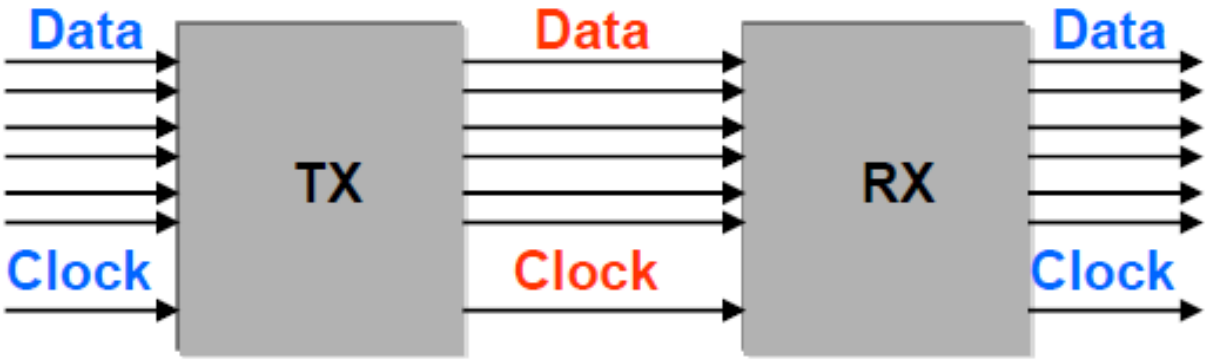
- Communication on a single chip is not so complicated and challenging
  - The real bottleneck can be found out of ICs
- The most problematic fields
  - Communication between ICs
  - Communication between PCBs
  - Communication between devices
- High bandwidth is required
  - But the power consumption has to be low
  - With low electromagnetic interference (EMI).
  - And with simple cabling or wireless

Example: displays



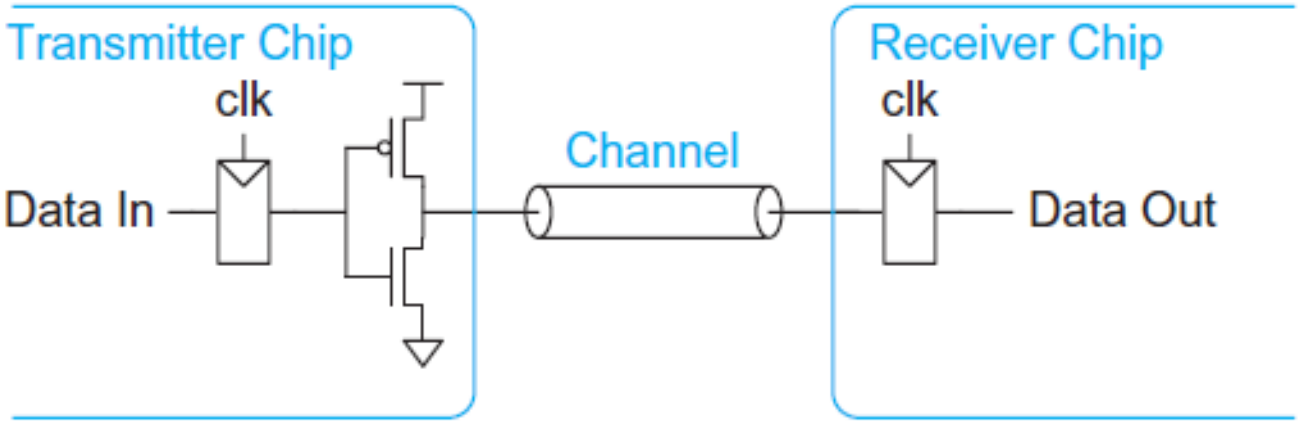
- The bandwidth requirement is 27×
  - From the VGA monitor to a 4K display

Parallel data bus.



- Direct connection (there is no data link layer, packet etc.)
- Easy to implement
- It requires a clock signal
- It occupies a huge chip area and lots of wires are required

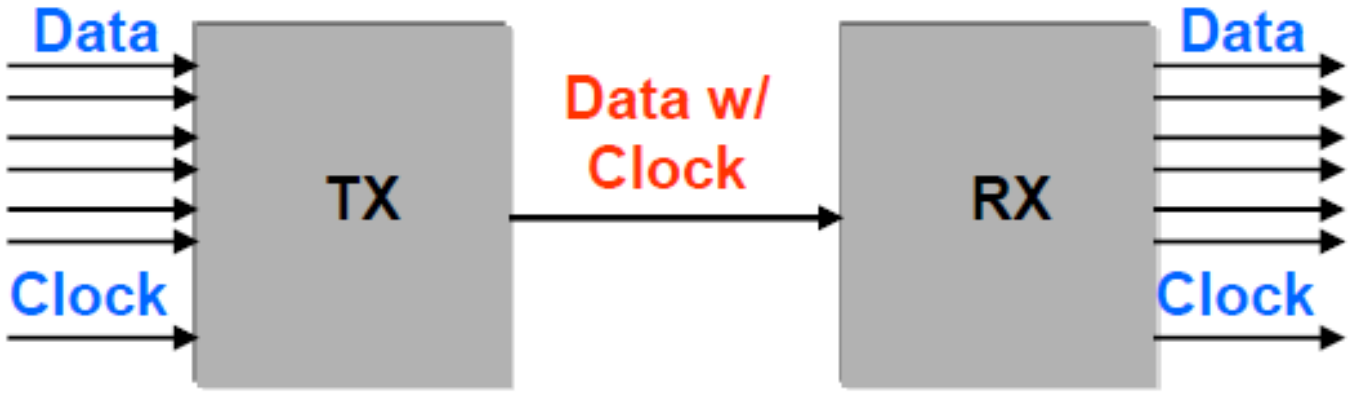
Logic signal transfer



- At low frequencies it is easy to transmit the usual logic levels (0 and VDD)
  - This is called single ended data transfer (as you can see in the picture above)
- It can be problematic when the periodic time is close to the propagation delay
  - The speed of the signal is exactly equal to the speed of light
  - $v = c/\sqrt{\varepsilon_r \mu_r}$

- Example: 10cm long wire on a PCB
  - $v = 3 \cdot \frac{10^8}{\sqrt{4{,}35}} = \frac{14{,}4cm}{ns}$
  - It takes 700ps to go 10cm.
  - If we suppose that the rising edge and the falling edge of the signal is the quarter of the periodic time, we got a signal with periodic time of 2.8ns.
  - It means the maximum frequency is 350MHz.
- In the case of parallel buses the length of the wires has to be perfectly equal!
- Anyway, they arrive at different time at the receiver
- It is difficult to maintain the signal integrity due to the inductance and capacitance of the wires
  - Furthermore, cross coupling occurs.
- This is the main drawback of the parallel communication

Serial data transfer



- Simple electronic connection (less wiring)
- The clock signal is embedded into the data
- Longer cables are possible because there is no data or clock skew.
- But the communication protocol is more complicated

- Based on its advantages, serial communication became the dominant data transfer solution
  - If the bandwidth is not enough, more serial channels can be used
  - Differential signal transfer (noise immunity)
  - The clock signal originates from the transferred data, or clock recovery packets are used
- For example: PCI Express, SATA, USB, HDMI etc.
- Practically, you can find serial data buses everywhere (except the memory bus)
- Physical layers:
  - LVDS (Low voltage differential signaling)
  - CML (Current mode logic)

LVDS and CML signal levels