Budapest University of Technology and Economics
Department of Electron Devices

Technology of IT Devices

Lecture 9

ASIC circuits

ASIC circuits

- Classification of integrated circuits
- ASIC categories
  - Standard cell ASIC
  - Gate array
  - PLDs
  - CPLD
  - FPGA

Classification of integrated circuits

- Catalog circuits
- Commercial off-the-shelf integrated circuits (COTS)
  - Wide range of applications (e.g. 555)
  - The designer of the IC and the engineer who uses it in a system do not cooperate
  - The IC designer helps users by writing data sheets and application notes.
  - These circuits are fabricated in large volumes – thus their price can be relatively low.
    - The 555 timer IC is still in widespread use
    - Introduced in 1971 by American company Signetics, 1 billion units are manufactured every year
- Systems made of catalog (integrated) circuits
  - Not an optimal solution (delay, power consumption)
  - Large-scale, easily reproducible

ASIC / SoC

- Application specific integrated circuit
  - Designed for one specific application.
  - The user designs it
  - The performance is better / simpler than with COTS circuits
  - Sometimes the reason for designing an ASIC is to make copying harder
  - The volumes of the production might differ substantially depending on the application
- The number of devices manufactured can differ from 1 to millions
- When the number needed is small, it is vital to minimalize the unique design and fabrication steps to minimize costs
- In IC design
  - Some components are prefabricated,
  - Some components are predesigned

  in order to save design and fabrication costs.

System on a chip (SoC)

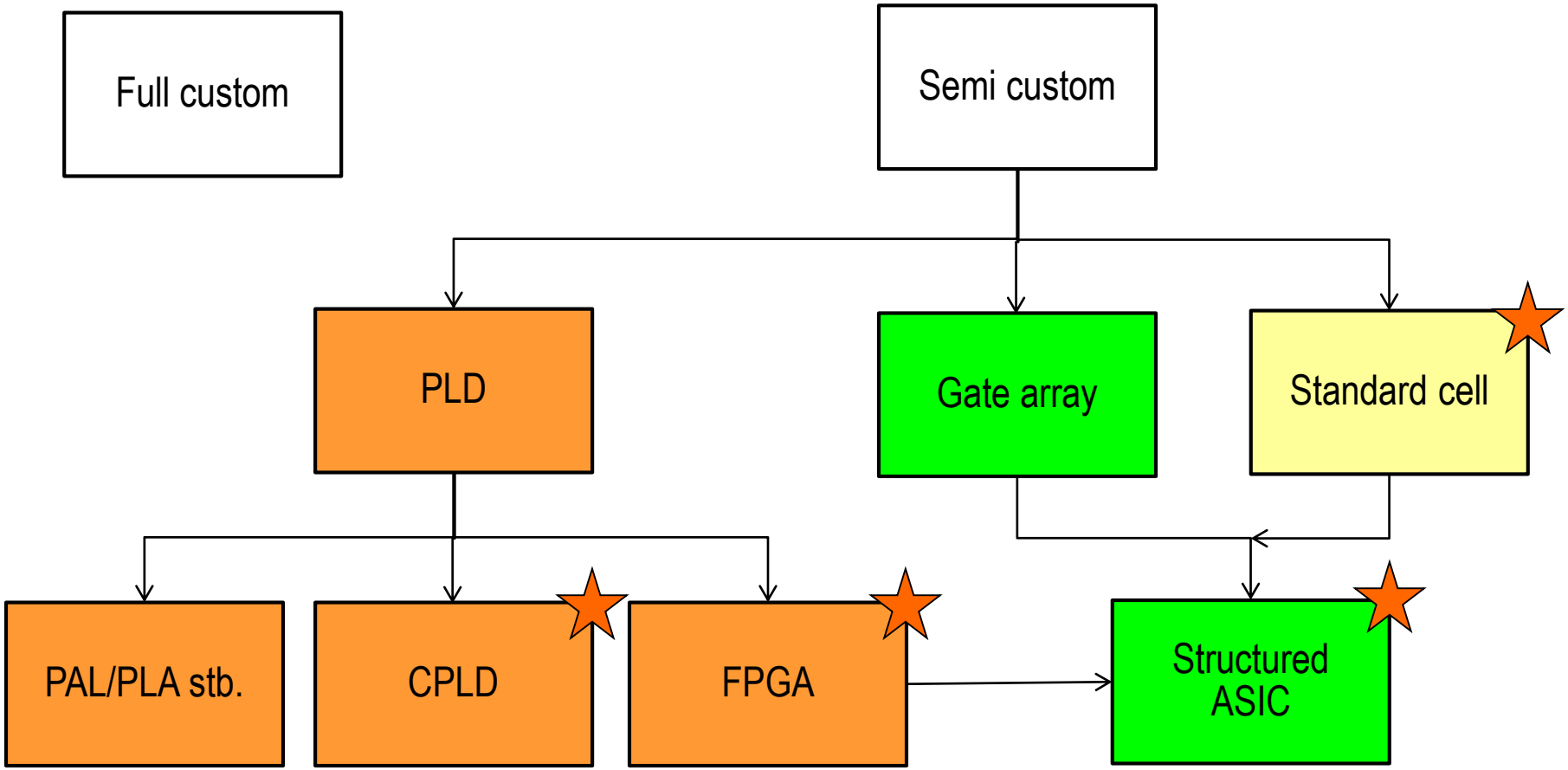
- A whole system on a chip
  - Digital circuits (processors, graphic accelerators, memory etc.)
  - Analog (and RF) parts.
  - Power supply etc.
- Advantages of the integration:
  - Lower delay, higher operating frequency, lower power consumption
  - Smaller physical size.
  - Cheaper (lower assembly costs)
- Drawbacks
  - The process yield of a complicated integrated circuit can be low
  - Sometimes the power supply voltages of integrated chips are different
    - E.g.: a digital circuit with memory: 1.2V core voltage, 0.3V threshold voltage, 2.5V supply voltage of DRAM, 0.7V threshold voltage, USB with 5V power supply…
  - A widely used solution
  - Package on package: EEPROM/DRAM chips are assembled onto SoC devices.

ASIC categories

- Custom ASIC (full custom)
  - Every mask of a custom ASIC needs to be designed and manufactured
  - Great expertise and expensive tools are needed
  - The price of a mask is $10,000–$100,000 at 14 nm
  - This is only worth doing when large volumes are needed
- Semi-custom ASICs
  - Partially or entirely prefabricated,
  - If they are prefabricated
    - The mask of the metal wiring is designed by the user,
    - Customization is done entirely by software means
  - If they are predesigned
    - The circuit is structured, most masks are predesigned and tested.

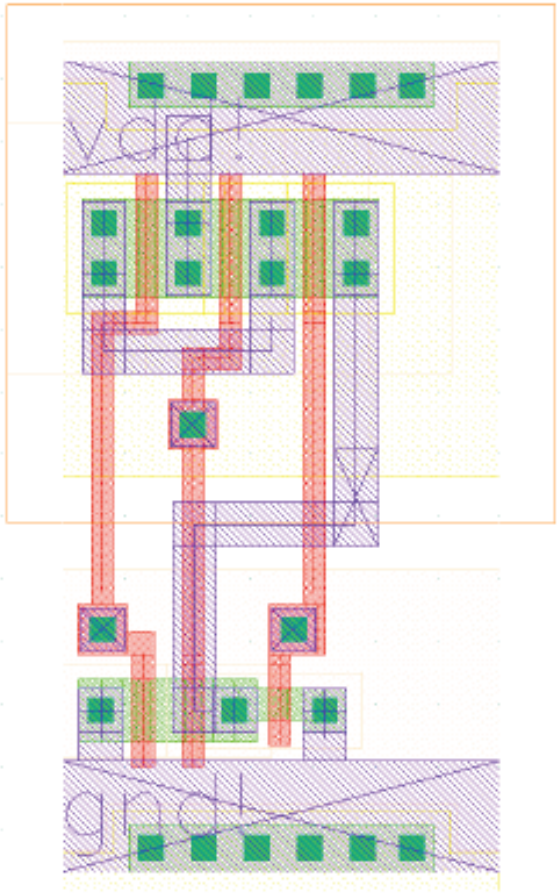
ASIC categories

- Predesigned
- Partially pre-manufactured
- Pre-manufactured, electrically programmable



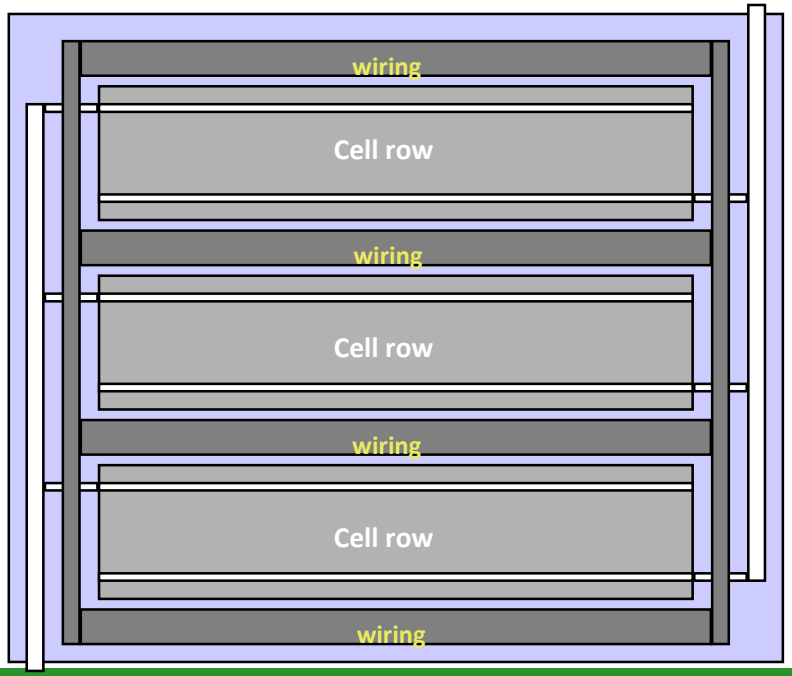
Standard cells ASIC

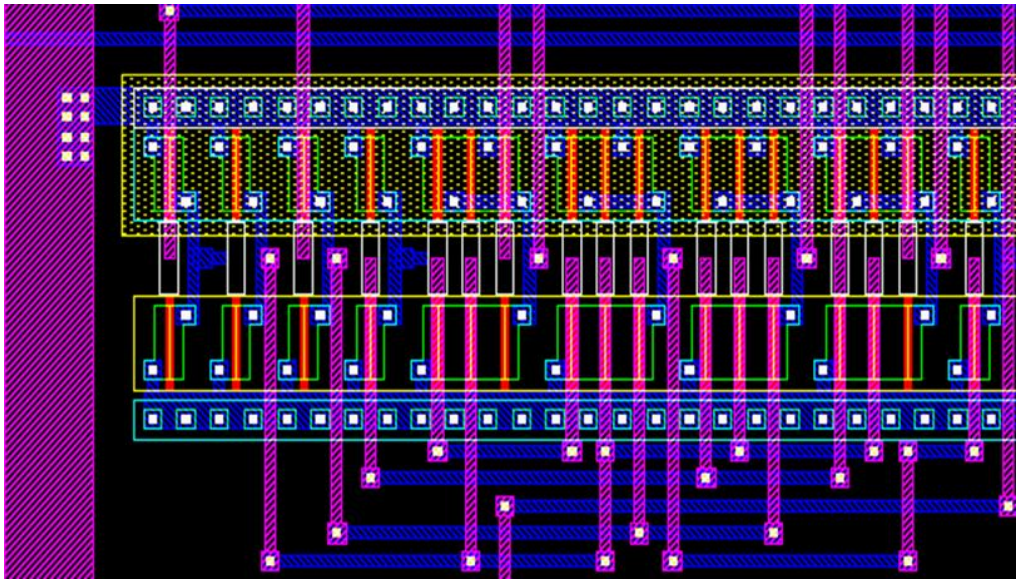
- The masks are predesigned – these are the cells.
- The application specific circuit is designed by instantiating and connecting standard cells.
- The heights of the cells are identical, the widths depend on the complexity of the function realized by the cell.
- The positions of the connections to the ground and supply voltage, and that of the inputs and outputs are fixed.
- The cell library is developed by the semiconductor company



Standard cell ASICs

- The custom function is realized by the unique placement and connection of standard cells
  - This task can be automated entirely.
  - Memory can be realized using generated megacell blocks
  - Cells are placed in rows, wires run between the cell rows.
  - Every mask needs to be manufactured which is expensive
  - When prototypes are created, multiple projects are gathered on the same chip to share costs – these are called multi project wafers – MPW.)





Standard cell ASIC

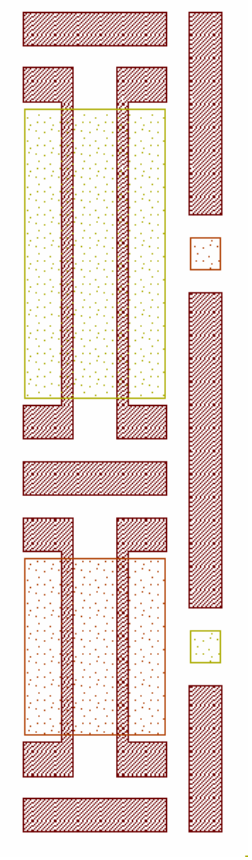
- The design is performed as if it was done by the manufacturer.
- The manufacturer provides the customer with:
  1. A limited view of the physical design including the positioning of the I/Os.
  2. Timing and power-consumption characteristics for post-layout simulations.
  3. Physical and electrical design rules for placement and routing.
  4. Parasitic extraction rules for LVS.
  5. Functional models for logic simulation.
- The design is done with this data set as shown in Lecture 6.
  - Mainly with pre-designed hard/soft IPs.
  - E.g. Apple's A9 processor
- In the case of standard cell design
  - Every mask must be manufactured, so there is no cost saving here.
  - The cells are pre-designed, tested, and characterized.

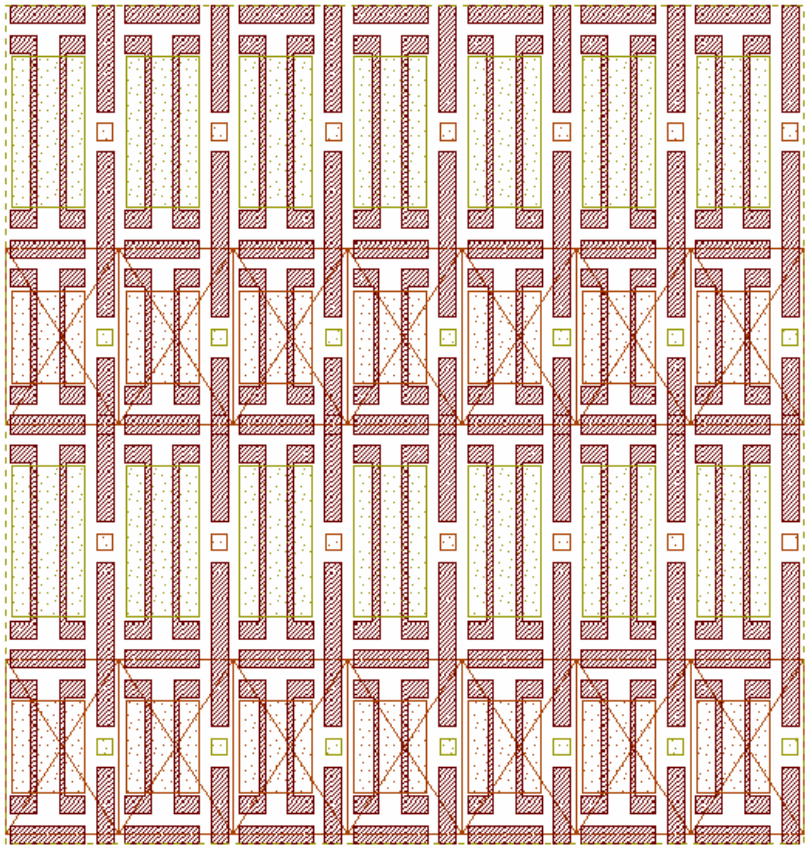
Gate array

- Everything is ready made except for the wiring.
  - “Sea of gates”: n and p type transistors are fabricated in a certain pattern.
- Circuits are realized by designing the multi-level connections:
  - Transistors are connected to form logic gates
  - Complex circuits are built of gates
  - Logic gates are created automatically – most of the design process steps are automated.
  - The internal connections in logic gates are pre-designed.
  - The design process is automated

- A cheaper solution
  - The number of the required masks is lower
  - This technology is cheap
  - Only four masks are needed (for an IC with 2 metal layers).
    - 1) Contacts between the components and metal 1 layer
    - 2) Metal 1 layer (wiring)
    - 3) Vias between metal 1 and metal 2
    - 4) Metal 2 layer
  - Gate array master slices are usually prefabricated and stockpiled in large quantities regardless of customer orders
- Compromise
  - The entire chip area is never fully utilized
  - The gates are not optimal
  - The wiring is not optimal, the propagation delay is higher than in the case of standard cells

Example





- In the gate array above a basic cell contains two n-type and two p-type transistors.
- A 2×7 part can be seen in the picture.

Programmable logic devices

- Programmable logic devices are entirely prefabricated
  - Both the logic components and the connections are programmable
- Electrically configurable
  - Programming is made possible by the same techniques as in memory circuits.
  - Volatile
    - The configuration is done by a static RAM
    - The configuration bits are loaded from an EEPROM at startup. The EEPROM is sometimes placed on the board with the device.
    - It can be reconfigured during operation.
  - Non-volatile
    - Mask programmed ROM
    - Flash EEPROM transistor
    - Antifuse (PLICE or ViaLink)

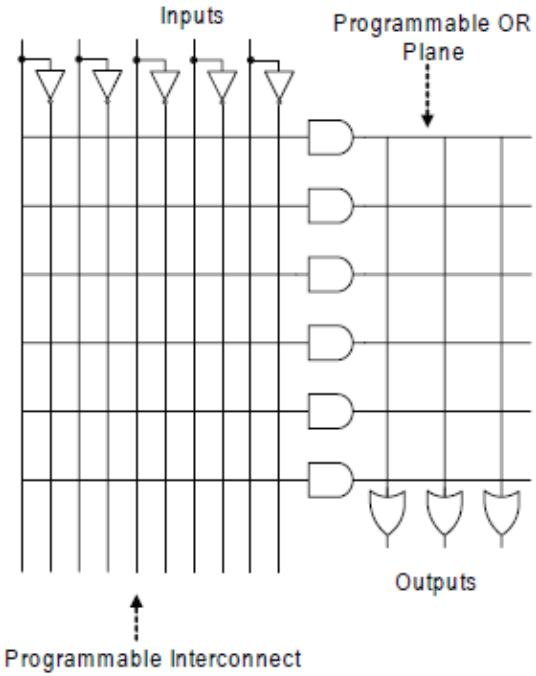
Comparison of programming methods

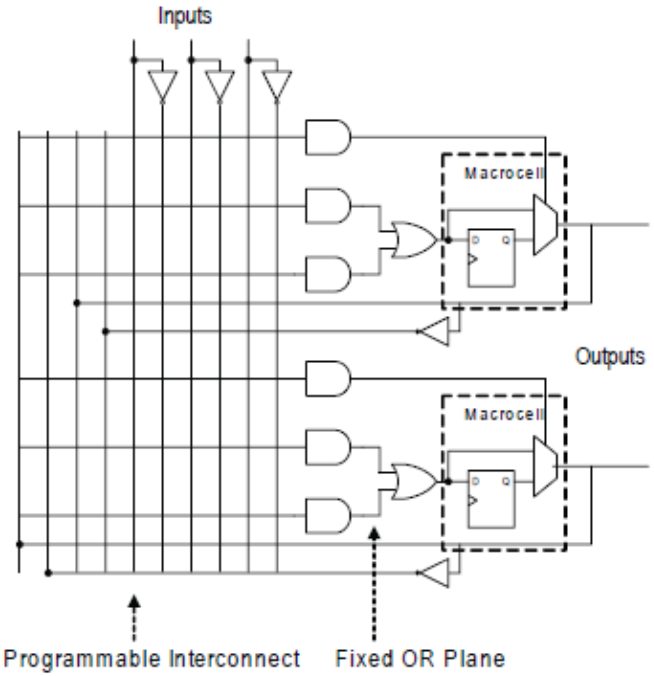
	SRAM	FLASH	Anti-fuse
Vulnerable	Yes	Not	Not
Can be reprogrammed	∞	limited	Not
Occupied area	6-transistor	1-transistor	1 contact
Technology	Standard CMOS	Spec. flash	Spec. ViaLink
ISP	Yes	Yes	not
Switching resistance(Ω)	500-1000	500-1000	20-100
Switching capacitance (fF)	1-2	1-2	<1
Reverse engineering	possible	hard	hard

- The lowest propagation delay can be achieved with Antifuse technology (**sacrificing the possibility of reconfiguration**)

PLA/PAL

- Programmable logic array (PLA)
  - Programming was performed using fuses
  - PLAs were used to realize logic functions as they have a programmable AND and an OR field connected.
    - One PLA could substitute several TTL gates.
  - PALs (Programmable Array Logic) contained registers as well.
  - First HDLs were created to program these devices (e.g. ABEL)

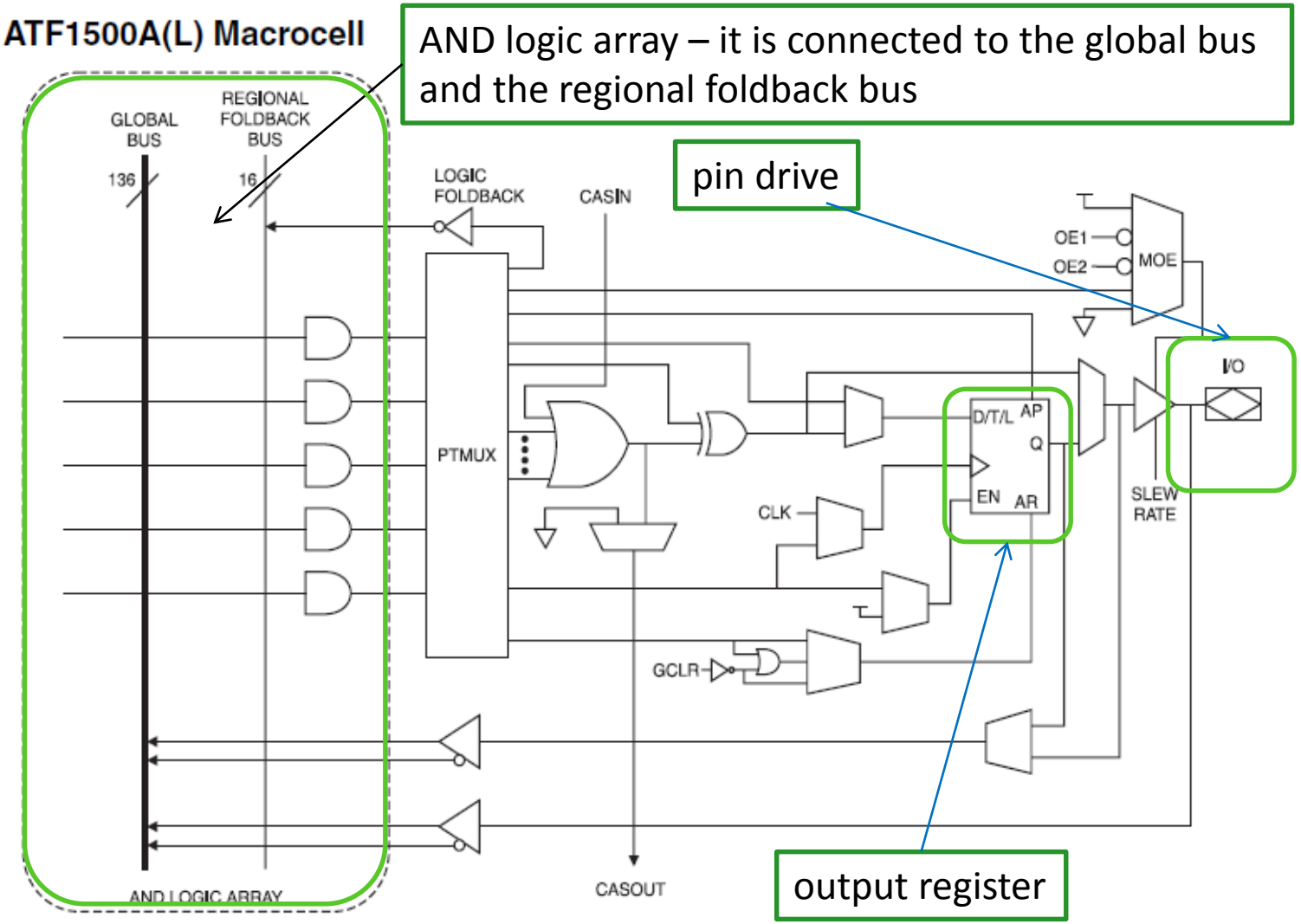




CPLD – Complex Programmable Logic Device

- Descendant of PLA/PAL
- Usually glue logics are realized with them (e.g. interface to a data bus).
  - This is often achieved using ordinary (cheap) 7400- or 4000-series components…
- They contain macrocells
  - Every macrocell contains.:
    - a programmable AND matrix for logic functions
    - a programmable flip-flop (J-K or D type),
    - a macrocell can usually drive output pins as well.
  - They can be programmed using EEPROMs.

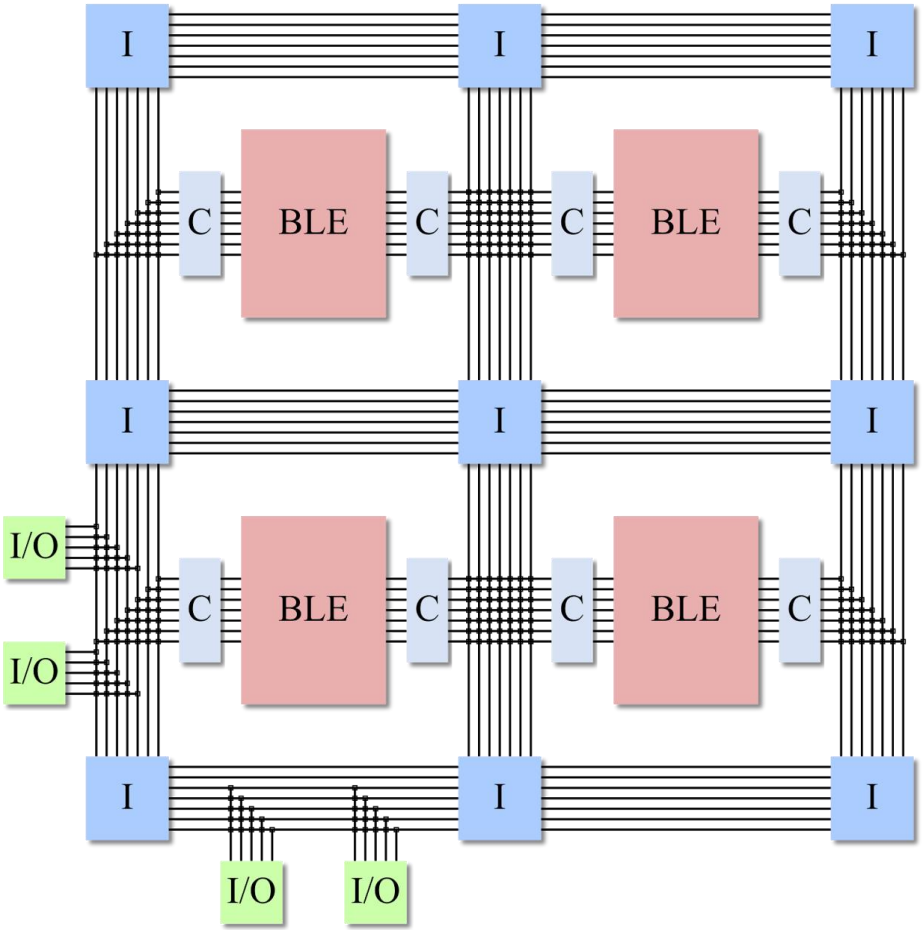
Example: ATMEL CPLD macrocell



Field Programmable Gate Array

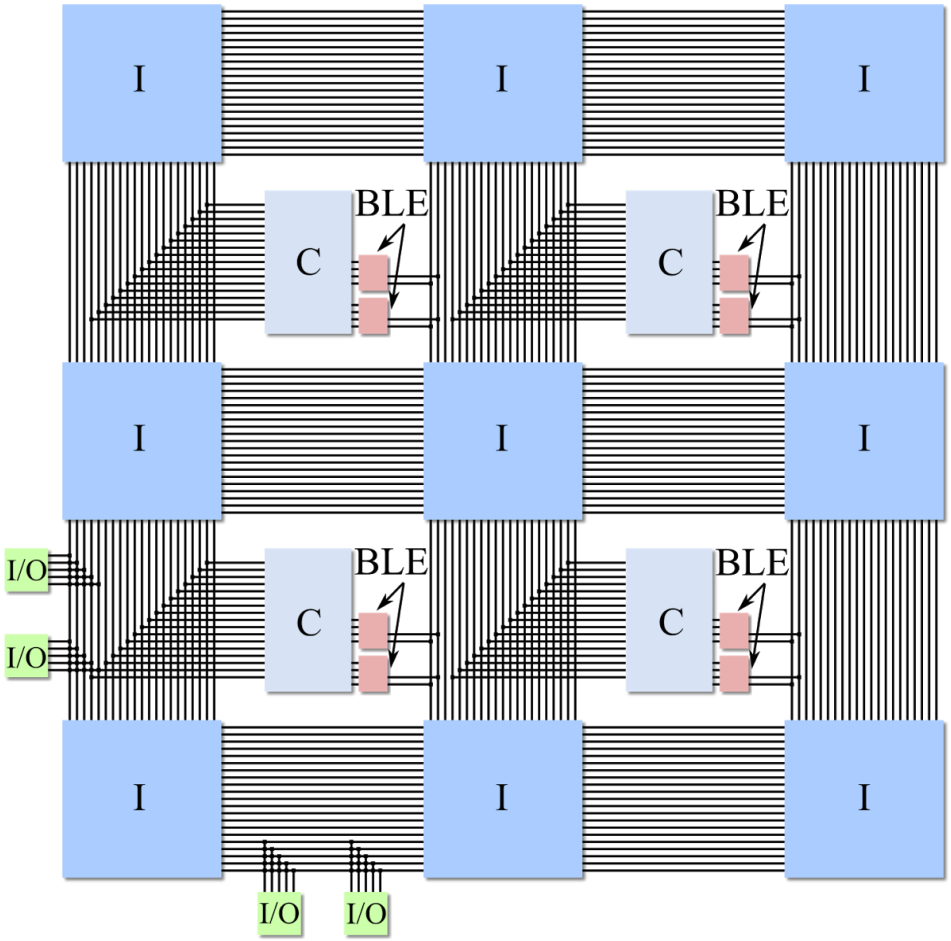
- General purpose, reconfigurable device
- Logic blocks can be configured to perform complex combinational functions, or simple logic gates like AND and XOR.
- Resources:
  - Configurable logic blocks
    - (Basic Logic Element, BLE – it has a lot of different names)
  - Configurable I/O blocks
    - Special blocks at periphery for external connections
  - Configurable connection resources
    - They connect logic blocks and I/O blocks
  - Configuration memory
    - Stores the states of aforementioned resources
    - Generally SRAM, but it can be EEPROM, FLASH, Anti-fuse etc…
  - Special purpose resources

Architecture



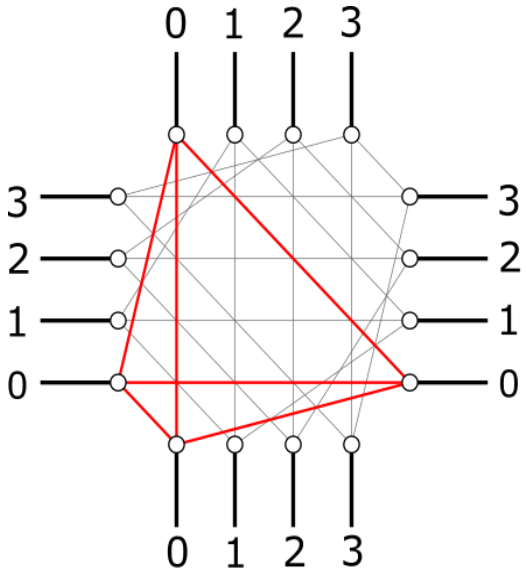
- I (interconnect block): realize the interconnections of wiring channels
- C (connection blocks): they connect the logic blocks to the routing network.

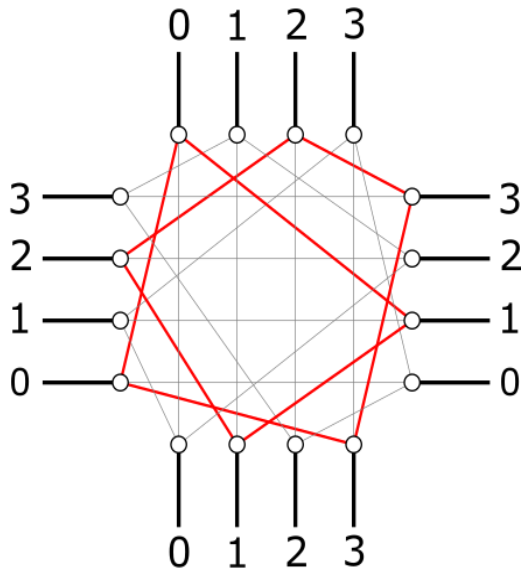
FPGA



- Wiring: the size of occupied area can be seen in the picture above
- The routing fabric occupies 80-90% of chip area

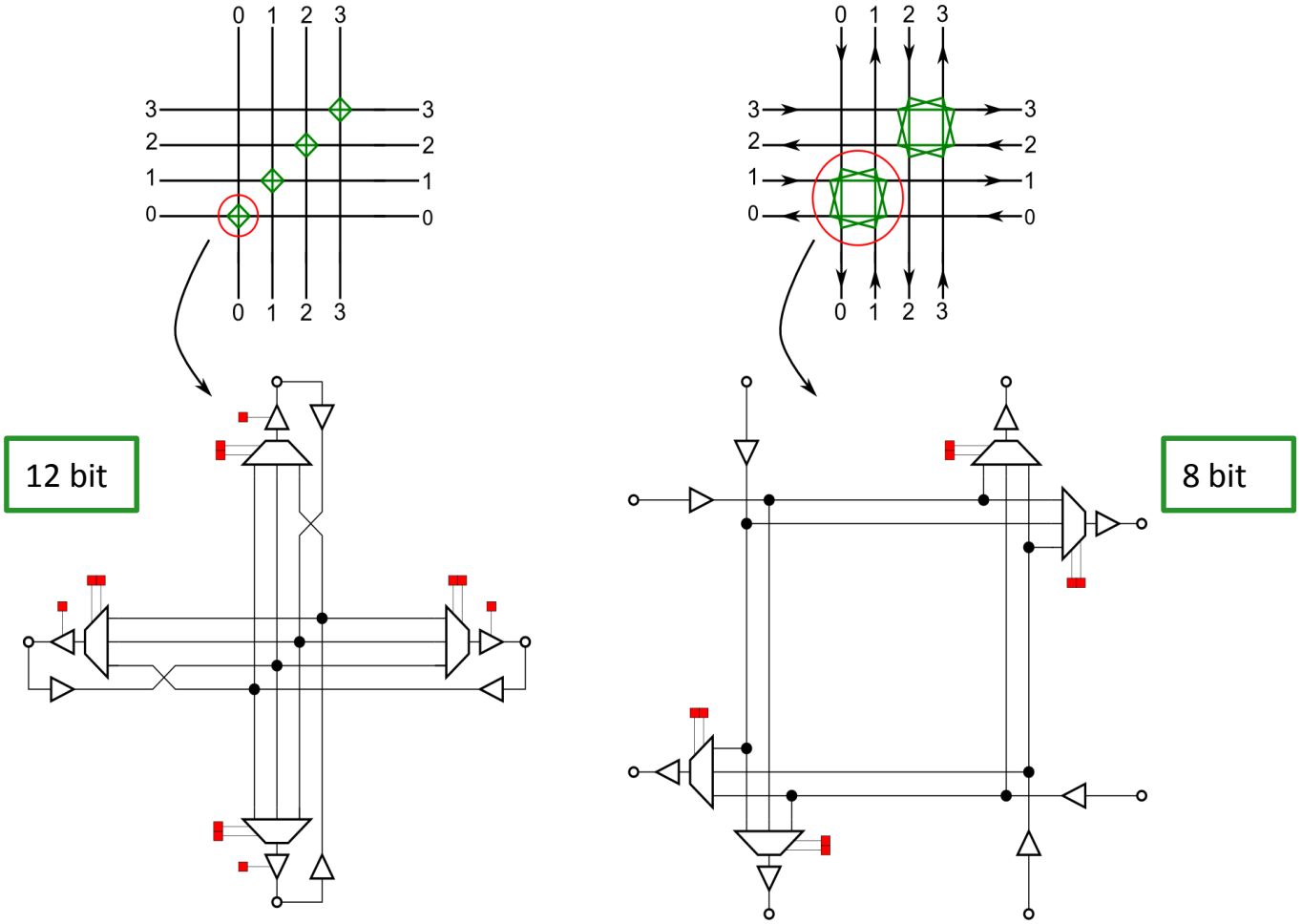
Programmable Interconnects





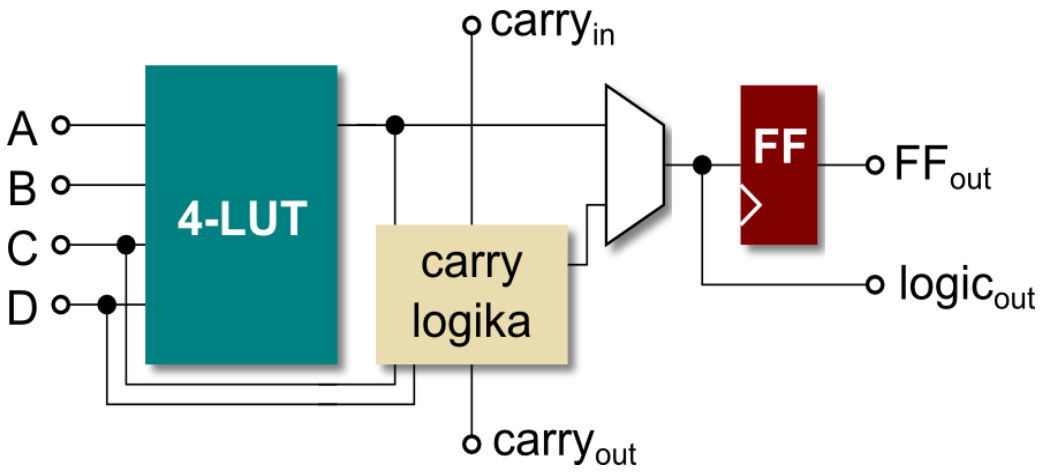
- Not all the connections are realized.
  - It would be too complicated and unnecessary
  - Disjoin-type matrix– change direction or go straight on
  - Wilton-type matrix – change direction or switches to another channel

Realizations of switching matrixes - Example

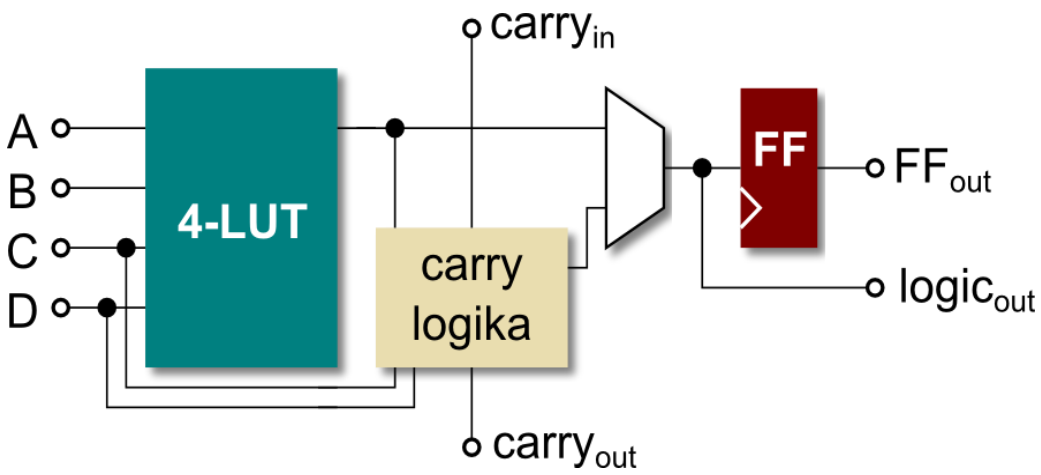


Basic Logic Element (BLE)

- Granularity
  - Describes the complexity of the basic logic element (thus the number of them)
- Modern FPGA – fine granularity
  - Simple function, but lots of BLEs.
  - A simplified BLE:

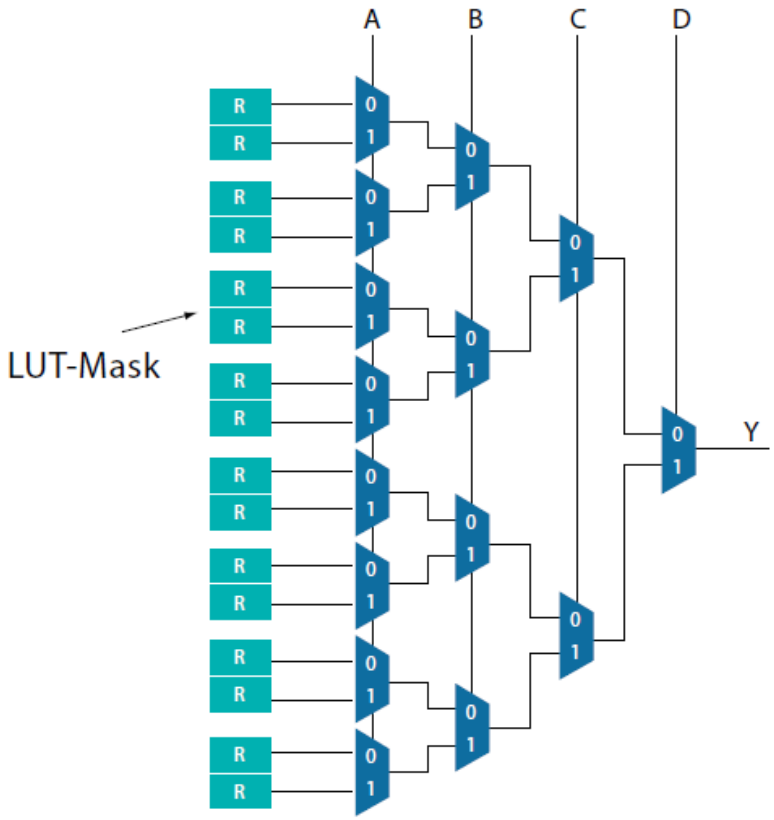


FPGA – configurable logic block– simplified



- Basic logic and storing functionality
- BLEs consist of a Look Up Table (LUT) implementing an arbitrary logic function, carry logic and a flip-flop.
  - Any 4-input, 1-output logic function can be realized.
- The carry logic increases the design efficiency of an adder.
  - Adding is a common function
- Configurable flip-flop/register storing the output of the LUT or the carry logic.

Realizing LUT

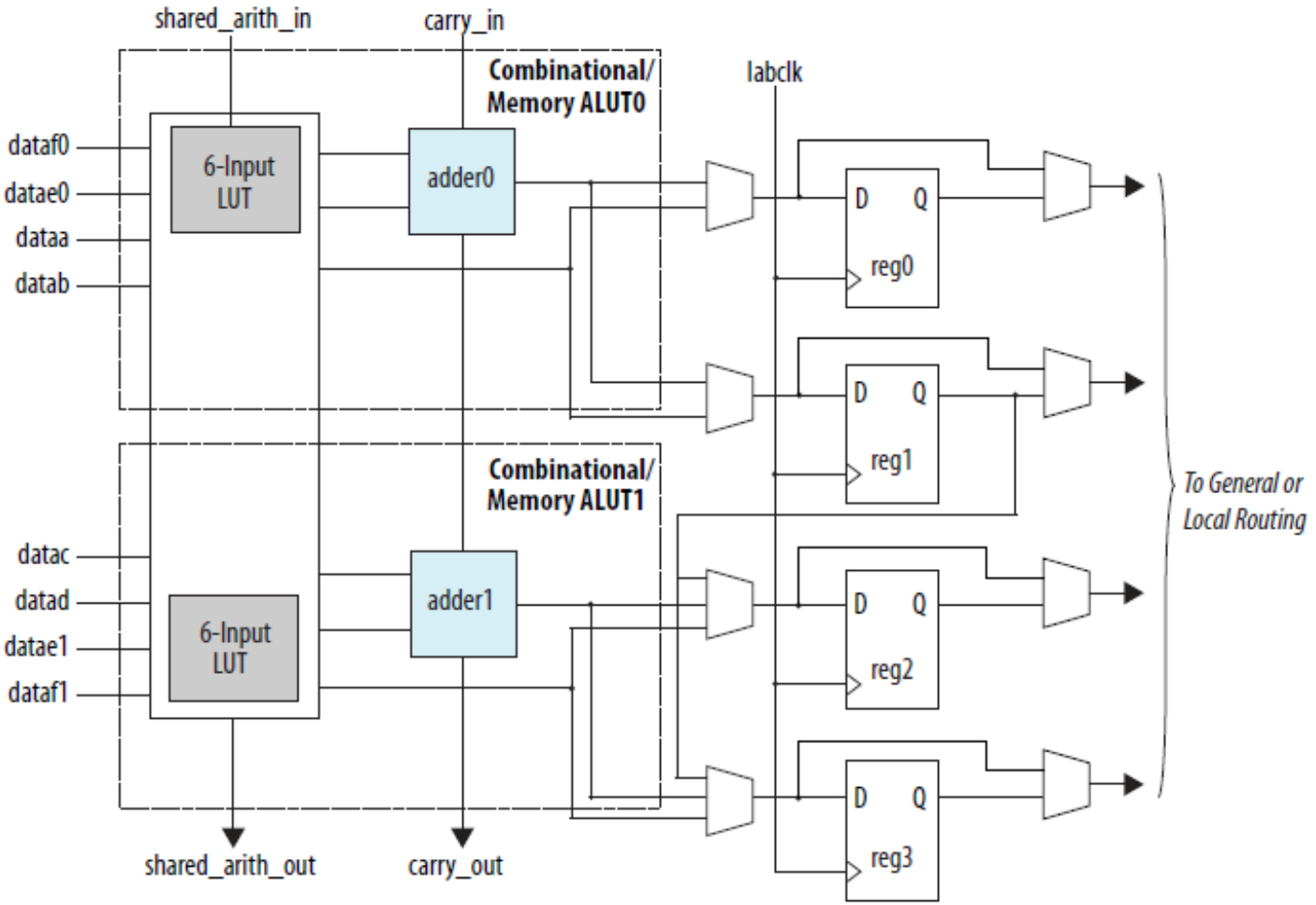


- The LUT mask is stored by the configuration memory.
- The output logic value is selected by 4 inputs (A, B, C, and D)
- The multiplexers can be realized using transmission gates

Example: Altera Cyclone V.

- The smallest logic element is the ALM
  - Adaptive Logic Module
- A logic block contains 10 ALMs
  - Logic Array Block (LAB) = 10 ALM + 1 control block
- MLAB – The LUTs may be used as dual-port SRAMs.
- 32 x 20-bit memory modules may be formed.
  - A single ALM may be used as a 32x2-bit dual-port SRAM.

FPGA – Example



- 4 registers, synchronous and asynchronous clear, synchronous load
- 2 x 6 inputs LUT (the 6th is the register feedback)
- 2 full adders

Special purpose resources

- Every logic function can be realized using general purpose resources
  - But depending on the required function, the efficiency may be poor.
- In modern FPGAs there are other special resources
- Block RAM
  - It contains a large amount of static RAM (on the order of a Mbit)
  - Single or dual port RAM, the capacitance and the worldlength can be easily configured on a wide range

- DSP slice
  - Implementing the multiplication operation is difficult using only simple logic elements
  - Generally, FPGAs contain multiplier circuits
  - Usually they are multiplier + accumulator circuits (A+=BC)
  - Shifter circuits (by more bits)
- SoPC – System on a Programmable Chip
  - One or more microprocessor cores, hard IP
  - Some additional logic for microprocessor-based systems
    - E.g. DRAM controller
  - External, high-speed communication
    - Gigabit Ethernet, PCI Express etc.
  - Generally, these functions are hard IPs.

Structured ASIC

- Incorporates the properties of FPGAs and standard cell ICs.
  - Not really widespread
- Similar to a modern FPGA, there are hard IP blocks, mask programmed logic blocks, and interconnections.
  - No configuration RAM
  - No configurable interconnections
  - Due to the lack of switching transistors, the connections are much faster than in FPGAs.
- Structured ASIC services are provided by the biggest FPGA companies
  - They produce ASIC ICs based on FPGA designs
  - Altera – HardCopy
  - Xilinx - EasyPath

Comparisons

	Std. Cell	FPGA	Structured ASIC
Maximum clock frequency (%)	100	**15**	75
Power (%)	100	**1200!**	300
Gates per area unit (%)	100	**1**	33

Table 7.1 The FPGA:ASIC gap from [120].

Metric	Soft logic only	Soft logic & DSP	Soft logic & memory	Soft logic, DSP & memory
Area	35	25	33	18
Delay	3.4	3.5	3.5	3.0
Dynamic power	14	12	14	7.1

- True only for the same technology
- In the case of FPGAs modern technologies is available
- In the case of ASICs, the modern technology is too expensive

Hardware acceleration

- FPGA
  - Parallel resources, pipelined
  - Reconfigurable.
- OpenCL support
  - Instead of CPU or GPU core FPGA can be used.