DIGITAL DESIGN I. - RTL MODELING AND SIMULATION

During this laboratory work we will use *Mentor Graphics QuestaSim* simulation tool. We will perform the functional verification of a RTL model of simple functional entity. A VHDL-based testbench is created for simulation.

After starting the program (use the desktop icon) we have to create a new project (***File*** menu ***New*** -> ***Project…****)*

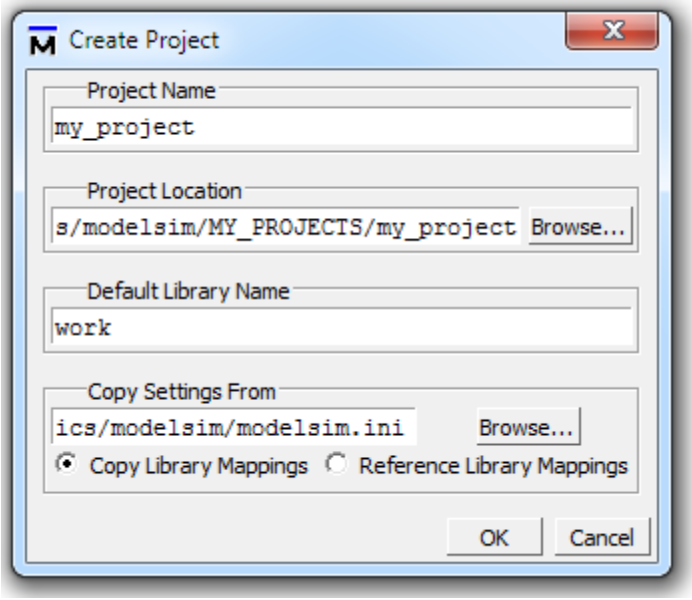

Figure 1. Creating a new project

Type a name into the ***Project Name*** field, the location has to be *home or Desktop, and click on OK.*!

A new window will appear ***(Add items to the project)***, where you can add source files to your project (see Figure 2).

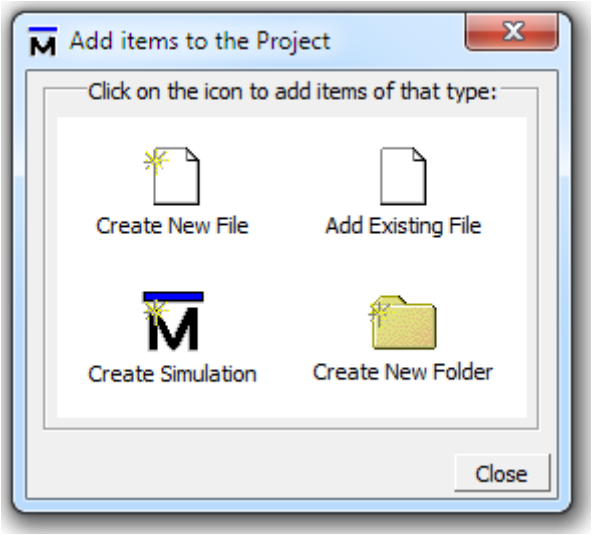

Figure 2. Creating/adding source files

Click on ***Add Existing File*** and browse for **COUNTER** and **TESTBENCH_COUNTER** files, select both and open them.

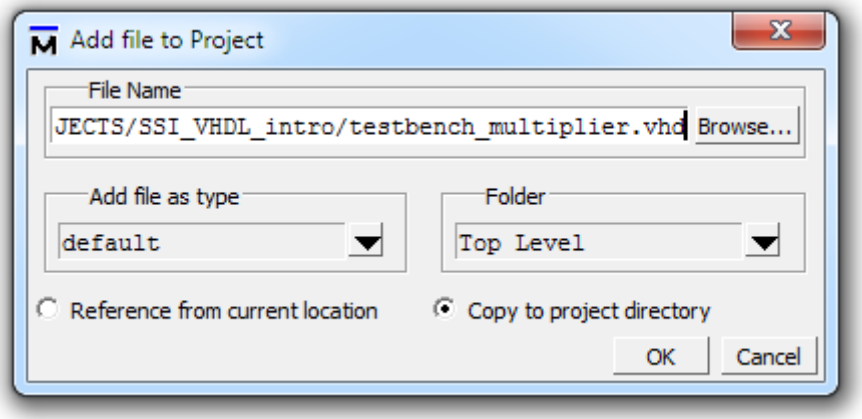

*Figure 3. Adding existing file. Please open the **COUNTER** and **TESTBECH_COUNTER***

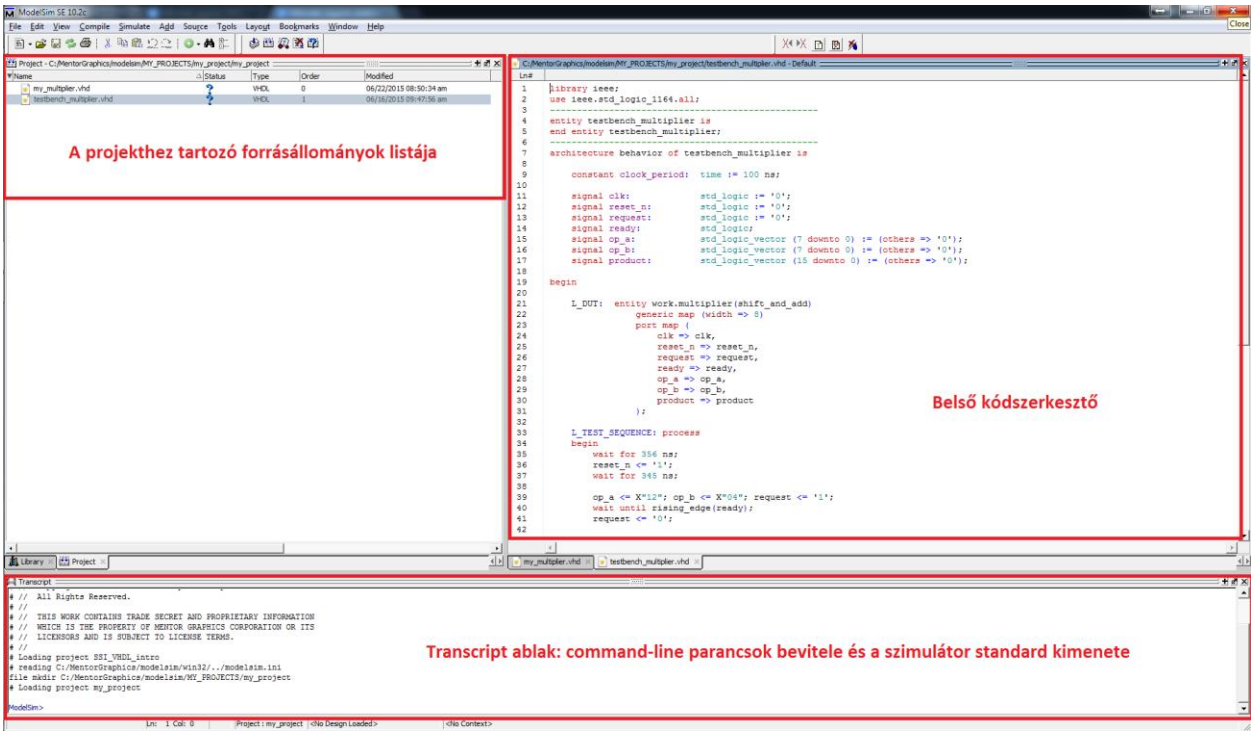

Figure 4. Internal code editor

Select ***Compile*** menu ***Compile All*** command. If it is successful you will see something similar than in Figure 5.

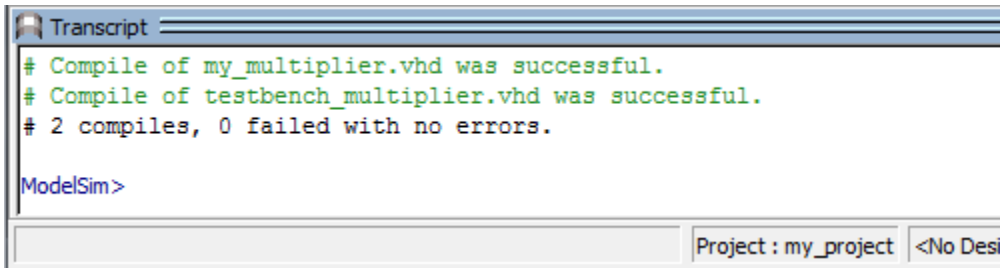

Figure 5. Successful compilation

In any error occurs, please double click on the red text line and read the message (see Figure 6).

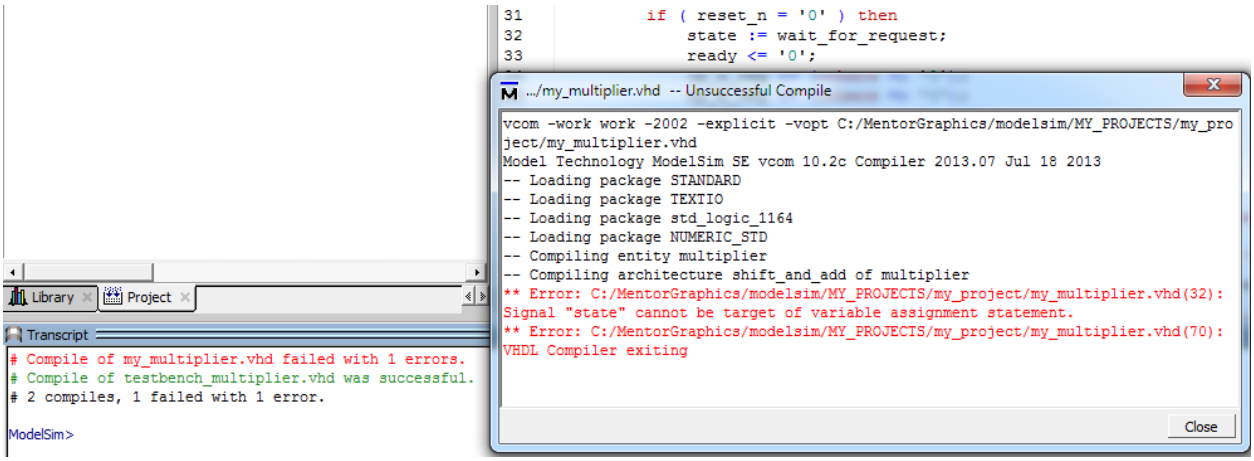

Figure 6. Compile error

After successful compilation we can start the simulation using ***Simulate*** menu ***Start Simulation…*** command.

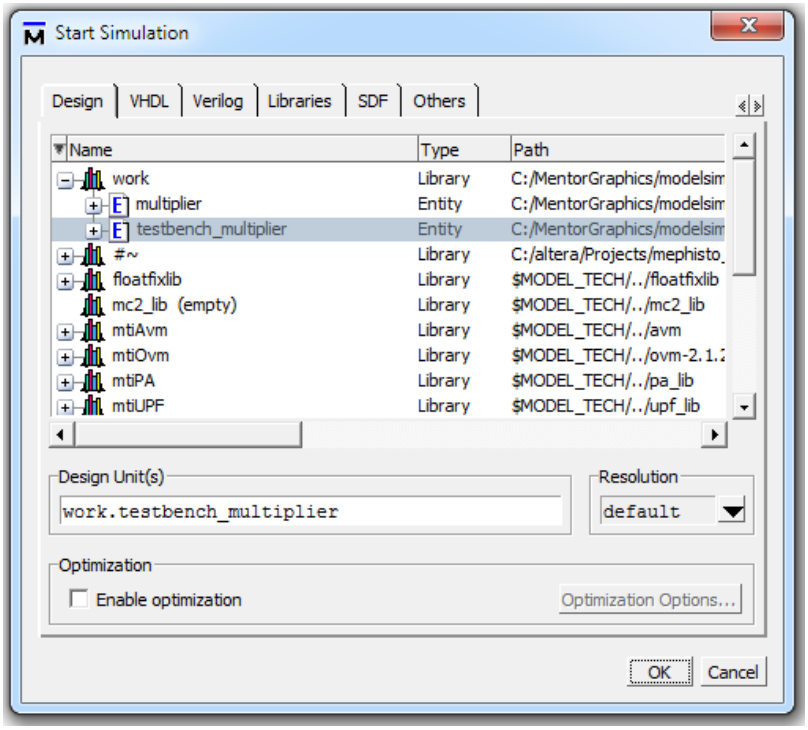

Figure 7. Start simulation window

Before starting the simulation please select the TESTBENCH_COUNTER module. Please **disable** the ***Optimization)*** and press ***OK*** *to start the simulation*.

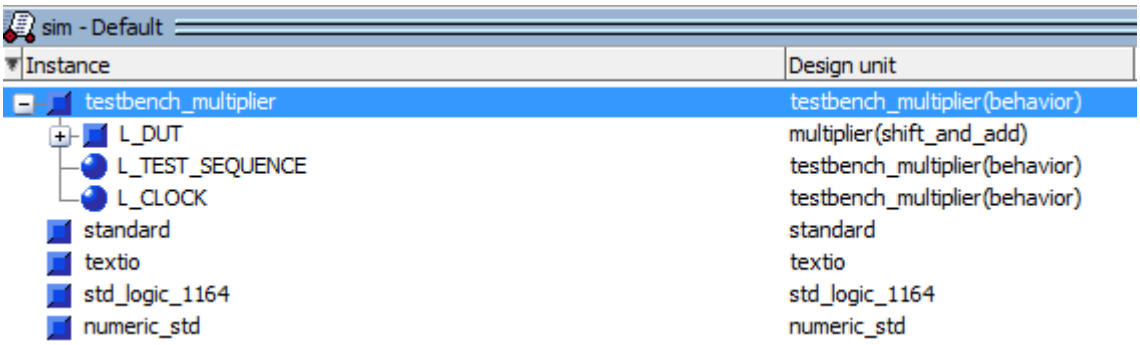

Figure 8. Hierarchy of DUT

Actually, the simulation doesn't start yet. We have to select the waves using ***Add to*** menu ***Wave*** submenu, and ***All items in design***. The program opens the waveform window (Figure 9).

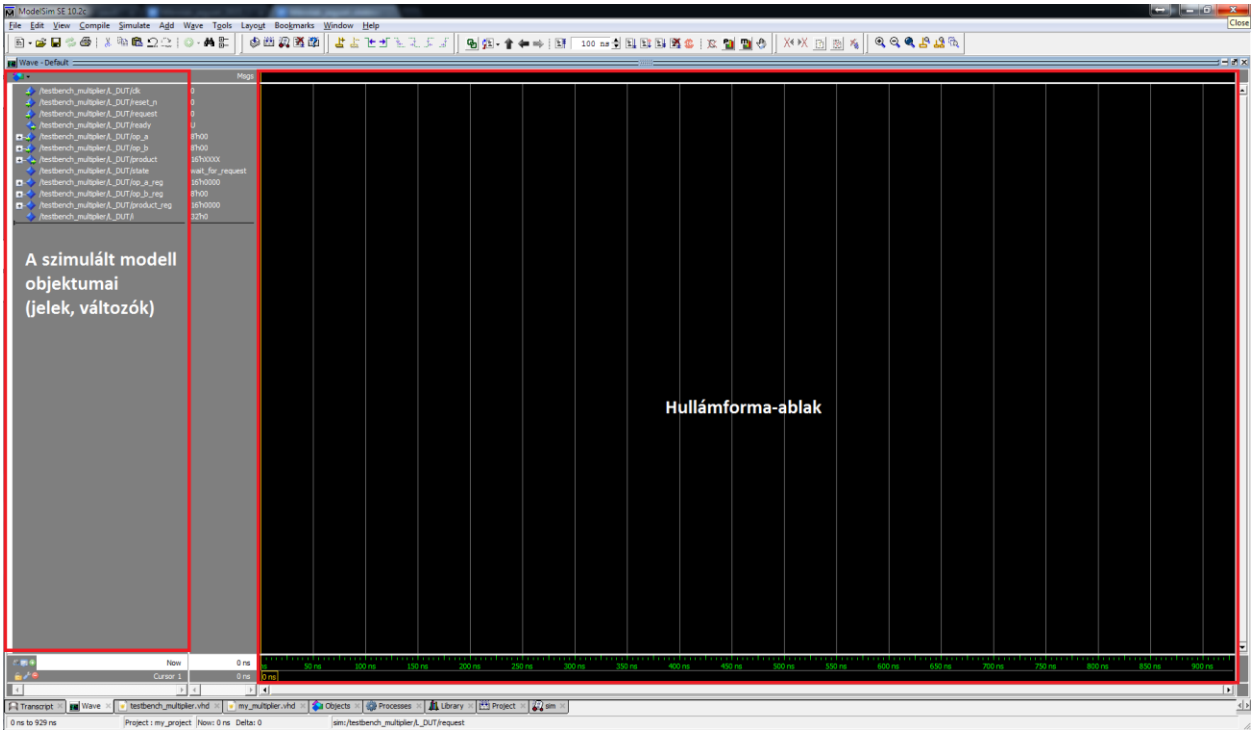

Figure 9. Waveform window

Before running the simulation we have to set the simulation time (10 us) (see Figure 10).

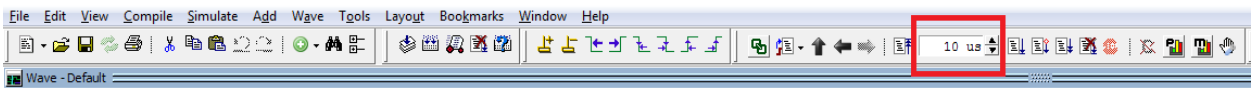

Figure 10. Setting the simulation time

The simulation can be started by the button on the right side of simulation time input field. You can use ***Zoom*** and the other elements of ***Wave Cursor*** toolbar.

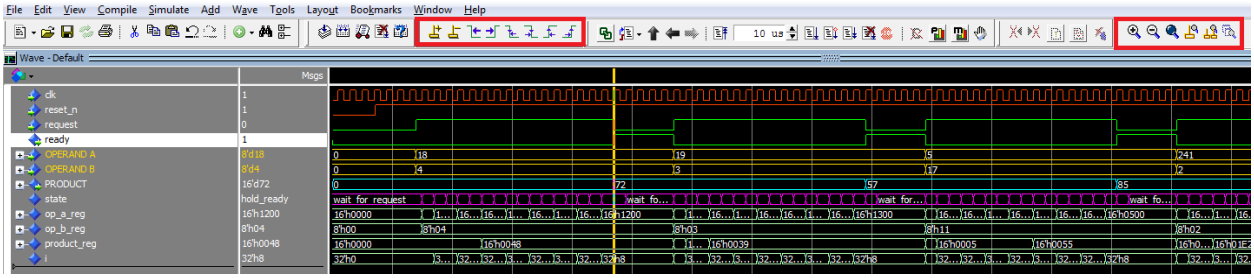

Figure 11. Zoom and Wave Cursor tools

You can stop the simulation using ***Simulate*** menu ***End Simulation*** command. If you modify the VHDL code, please make sure it is saved (ctrl+s), and use ***Compile*** menu: ***Compile All*** command. You have to clear the waveform windows using ***Restart*** button (left side of the simulation time).

TASKS

- In the testbench the instantiated entity (so the DUT) is the ring counter. Please modify the testbench code to simulate the normal counter.
    - HINT: delete the VHDL code of the ring counter in counters.vhd
    - HINT: the ports in testbench have to be in matching the ports of the counter entity
- Increase the bit number of the counter from 4 to 5 bits.
- Create a flag output which is activated when the counter reaches the maximum value („11111”)