UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, Fall 1398
Computer Assignment 3
Combinational packages and their gate-level equivalent
Week 7

Name:
Date:

Serial data have been collected in two 16-bit registers and their outputs are available to you. You are to build a multi-function comparator (MFC) that compares there two 16-bit data inputs. The data you are dealing with are 2's complement signed numbers. We refer to the inputs as *A[15:0]* and *B[15:0]*. The comparator you are building has four outputs, *eq*, *gt*, *ae*, and *d[3:0]*. The *eq* output becomes 1 when *A* and *B* are equal. The *gt* output becomes 1 when *A* is greater than *B*. The *ae* output becomes 1 when the absolute value of *A* and *B* are equal. The 4-bit output, *d[3:0]*, indicates how different the magnitude of the two inputs are, i.e., 0000 for no difference and 1111 for most difference.

1. Using primitive gates of SystemVerilog, build *eq*, *ae*, and *d[3:0]* outputs of the comparator. Assume the primitives are built using transistors of Computer Assignment 1, and use appropriate gate delays based on the delay values given for the transistors.
2. Assume that you have a 16-bit magnitude comparator available to you that is built by iteration of 16 one-bit comparators, each of which is built of two-level logic circuits. Write an **assign** statement describing this comparator and use delay values according to the transistor delays of Computer Assignment 1.
3. Put the circuits of Part 1 and Part 2 together to build your MFC. This is your gate-level MFC.
4. Redo your MFC, this time using **assign**, and **always** statements. Use procedural statements in your always statement such as, **if-else**, **while**, and **for** statements. This is your behavioral MFC.
5. Generate a testbench to test the two MFC circuits of Part 3 and Part 4 alongside each other. By running simulations, use worst-case delay values from the gate-level MFC to back-annotate into the behavioral MFC
6. Run simulations on the two circuits of Part 5 and compare the timings and explain the discrepancies.