```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                        2 ************************************************************************
                                                        3 *
                                                        4 *        Zvector E6 instruction tests for VRS-d encoded:
                                                        5 *
                                                        6 *        E63F VECTOR STORE RIGHTMOST WITH LENGTH  (reg)
                                                        7 *
                                                        8 *        also tests
                                                        9 *        E637 VLRLR  - VECTOR LOAD RIGHTMOST WITH LENGTH (reg)
                                                       10 *
                                                       11 *        James Wekel June 2024
                                                       12 ************************************************************************
                                                       13
                                                       14 ************************************************************************
                                                       15 *
                                                       16 *        basic instruction tests
                                                       17 *
                                                       18 ************************************************************************
                                                       19 *  This program tests proper functioning of the z/arch E6 VRS-d vector
                                                       20 *  store rightmost with length (reg). Exceptions are not tested.
                                                       21 *
                                                       22 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                       23 *  obvious coding errors.  None of the tests are thorough.  They are
                                                       24 *  NOT designed to test all aspects of any of the instructions.
                                                       25 *
                                                       26 ************************************************************************
                                                       27 *
                                                       28 *   *Testcase zvector-e6-09-VSTRLR: VECTOR E6 VRS-d VSTRLR instruction
                                                       29 *   *
                                                       30 *   *   Zvector E6 tests for VRS-d encoded instructions:
                                                       31 *   *
                                                       32 *   *   E63F VECTOR STORE RIGHTMOST WITH LENGTH  (reg)
                                                       33 *   *
                                                       34 *   *   # ---------------------------------------------------------
                                                       35 *   *   #  This tests only the basic function of the instruction.
                                                       36 *   *   #  Exceptions are NOT tested.
                                                       37 *   *   # ---------------------------------------------------------
                                                       38 *   *
                                                       39 *   mainsize    2
                                                       40 *   numcpu      1
                                                       41 *   sysclear
                                                       42 *   archlvl     z/Arch
                                                       43 *
                                                       44 *   diag8cmd    enable    # (needed for messages to Hercules console)
                                                       45 *   loadcore    "$(testpath)/zvector-e6-09-VSTRLR.core" 0x0
                                                       46 *   diag8cmd    disable   # (reset back to default)
                                                       47 *
                                                       48 *   *Done
                                                       49 ************************************************************************


                          00000000  000013DF     51 ZVE6TST  START 0
00000000                  00000000                 52          USING ZVE6TST,R0            Low core addressability
                                                   53
                          00000140  00000000     54 SVOLDPSW EQU   ZVE6TST+X'140'        z/Arch Supervisor call old PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00000000                     00000000  000001A0    56          ORG   ZVE6TST+X'1A0'        z/Architecure RESTART PSW
000001A0  00000001 80000000                         57          DC    X'0000000180000000'
000001A8  00000000 00000200                         58          DC    AD(BEGIN)

000001B0                     000001B0  000001D0    60          ORG   ZVE6TST+X'1D0'        z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                         61          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                         62          DC    AD(X'DEAD')

000001E0                     000001E0  00000200    64          ORG   ZVE6TST+X'200'        Start of actual test program...
                                                    65
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     67 ************************************************************************
                                                     68 *               The actual "ZVE6TST" program itself...
                                                     69 ************************************************************************
                                                     70 *
                                                     71 *  Architecture Mode: z/Arch
                                                     72 *  Register Usage:
                                                     73 *
                                                     74 *   R0       (work)
                                                     75 *   R1-4     (work)
                                                     76 *   R5       Testing control table - current test base
                                                     77 *   R6-R7    (work)
                                                     78 *   R8       First base register
                                                     79 *   R9       Second base register
                                                     80 *   R10      Third base register
                                                     81 *   R11      E6TEST call return
                                                     82 *   R12      E6TESTS register
                                                     83 *   R13      (work)
                                                     84 *   R14      Subroutine call
                                                     85 *   R15      Secondary Subroutine call or work
                                                     86 *
                                                     87 ************************************************************************

00000200                        00000200             89          USING  BEGIN,R8        FIRST Base Register
00000200                        00001200             90          USING  BEGIN+4096,R9   SECOND Base Register

00000200  0580                                       92 BEGIN    BALR  R8,0             Initalize FIRST base register
00000202  0680                                       93          BCTR  R8,0             Initalize FIRST base register
00000204  0680                                       94          BCTR  R8,0             Initalize FIRST base register

00000206  4190 8800                  00000800        96          LA    R9,2048(,R8)     Initalize SECOND base register
0000020A  4190 9800                  00000800        97          LA    R9,2048(,R9)     Initalize SECOND base register

0000020E  41A0 9800                  00000800        99          LA    R10,2048(,R9)    Initalize THIRD base register
00000212  41A0 A800                  00000800       100          LA    R10,2048(,R10)   Initalize THIRD base register
                                                    101
00000216  B600 81EC                  000003EC       102          STCTL R0,R0,CTLR0      Store CR0 to enable AFP
0000021A  9604 81ED                  000003ED       103          OI    CTLR0+1,X'04'    Turn on AFP bit
0000021E  9602 81ED                  000003ED       104          OI    CTLR0+1,X'02'    Turn on Vector bit
00000222  B700 81EC                  000003EC       105          LCTL  R0,R0,CTLR0      Reload updated CR0
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    107 ************************************************************************
                                                    108 *               Do tests in the E6TESTS table
                                                    109 ************************************************************************
                                                    110
00000226  58C0 81F4                       000003F4 111           L     R12,E6TADR       get table of test addresses
                                                    112
                                0000022A  00000001 113 NEXTE6    EQU   *
0000022A  5850 C000                       00000000 114           L     R5,0(0,R12)       get test address
0000022E  1255                                     115           LTR   R5,R5                have a test?
00000230  4780 80BE                       000002BE 116           BZ    ENDTEST                 done?
                                                    117
00000234                        00000000           118           USING E6TEST,R5
00000234  E710 8ED0 0006                  000010D0 119           VL    V1,V1FUDGEB       fudge output
0000023A  E710 8EA0 000E                  000010A0 120           VST   v1,V1OUTPUT
00000240  E710 8EC0 0006                  000010C0 121           VL    V1,V1FUDGE        fudge input
                                                    122
00000246  58B0 5000                       00000000 123           L     R11,TSUB          get address of test routine
0000024A  05BB                                     124           BALR  R11,R11           do test
                                                    125
                                0000024C  00000001 126 TESTREST  EQU   *
0000024C  E310 501C 0014                  0000001C 127           LGF   R1,READDR         get address of expected result
00000252  D50F 8EA0 1000        000010A0  00000000 128           CLC   V1OUTPUT,0(R1)    valid?
00000258  4770 8064                       00000264 129           BNE   FAILMSG              no, issue failed message
                                                    130
0000025C  41C0 C004                       00000004 131           LA    R12,4(0,R12)      next test address
00000260  47F0 802A                       0000022A 132           B     NEXTE6
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    134 ************************************************************************
                                                    135 * result not as expected:
                                                    136 *        issue message with test number, instruction under test
                                                    137 *              and instruction l2
                                                    138 ************************************************************************
                                 00000264  00000001 139 FAILMSG  EQU   *
00000264  4820 5004                        00000004 140           LH    R2,TNUM              get test number and convert
00000268  4E20 8E70                        00001070 141           CVD   R2,DECNUM
0000026C  D211 8E5A 8E44       0000105A  00001044 142           MVC   PRT3,EDIT
00000272  DE11 8E5A 8E70       0000105A  00001070 143           ED    PRT3,DECNUM
00000278  D202 8E14 8E67       00001014  00001067 144           MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                    145
0000027E  D207 8E2F 5010       0000102F  00000010 146           MVC   PRTNAME,OPNAME       fill in message with instruction
                                                    147
00000284  B982 0022                                148           XGR   R2,R2                get l2 as U32
00000288  5820 5008                        00000008 149           L     R2,L2
0000028C  4E20 8E70                        00001070 150           CVD   R2,DECNUM            and convert
00000290  D211 8E5A 8E44       0000105A  00001044 151           MVC   PRT3,EDIT
00000296  DE11 8E5A 8E70       0000105A  00001070 152           ED    PRT3,DECNUM
0000029C  D202 8E40 8E67       00001040  00001067 153           MVC   PRTL2(3),PRT3+13     fill in message with l2 field
                                                    154
000002A2  4100 0040                        00000040 155           LA    R0,PRTLNG            message length
000002A6  4110 8E04                        00001004 156           LA    R1,PRTLINE           messagfe address
000002AA  45F0 80CC                        000002CC 157           BAL   R15,RPTERROR
```

```
                                                    159 ************************************************************************
                                                    160 * continue after a failed test
                                                    161 ************************************************************************
                                 000002AE  00000001 162 FAILCONT EQU   *
000002AE  5800 81F8                        000003F8 163           L     R0,=F'1'             set GLOBAL failed test indicator
000002B2  5000 8E00                        00001000 164           ST    R0,FAILED
                                                    165
000002B6  41C0 C004                        00000004 166           LA    R12,4(0,R12)         next test address
000002BA  47F0 802A                        0000022A 167           B     NEXTE6
```

```
                                                    169 ************************************************************************
                                                    170 * end of testing; set ending psw
                                                    171 ************************************************************************
                                 000002BE  00000001 172 ENDTEST  EQU   *
000002BE  5810 8E00                        00001000 173           L     R1,FAILED            did a test fail?
000002C2  1211                                     174           LTR   R1,R1
000002C4  4780 81D0                        000003D0 175           BZ    EOJ                     No, exit
000002C8  47F0 81E8                        000003E8 176           B     FAILTEST                Yes, exit with BAD PSW
                                                    177
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    179 ************************************************************************
                                                    180 *        RPTERROR          Report instruction test in error
                                                    181 *                             R0 = MESSGAE LENGTH
                                                    182 *                             R1 = ADDRESS OF MESSAGE
                                                    183 ************************************************************************

000002CC  50F0 80EC                 000002EC    185 RPTERROR ST    R15,RPTSAVE          Save return address
000002D0  5050 80F0                 000002F0    186          ST    R5,RPTSVR5           Save R5
                                                    187 *
                                                    188 *        Use Hercules Diagnose for Message to console
                                                    189 *
000002D4  9002 80F8                 000002F8    190          STM   R0,R2,RPTDWSAV       save regs used by MSG
000002D8  4520 8108                 00000308    191          BAL   R2,MSG               call Hercules console MSG display
000002DC  9802 80F8                 000002F8    192          LM    R0,R2,RPTDWSAV       restore regs


000002E0  5850 80F0                 000002F0    194          L     R5,RPTSVR5           Restore R5
000002E4  58F0 80EC                 000002EC    195          L     R15,RPTSAVE          Restore return address
000002E8  07FF                                  196          BR    R15                  Return to caller

000002EC  00000000                              198 RPTSAVE  DC    F'0'                 R15 save area
000002F0  00000000                              199 RPTSVR5  DC    F'0'                 R5 save area

000002F8  00000000 00000000                     201 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    203 ************************************************************************
                                                    204 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    205 *              R2 = return address
                                                    206 ************************************************************************
                                                    207
00000308  4900 81FC                 000003FC       208 MSG      CH    R0,=H'0'                Do we even HAVE a message?
0000030C  07D2                                     209          BNHR  R2                      No, ignore
                                                    210
0000030E  9002 8140                 00000340       211          STM   R0,R2,MSGSAVE           Save registers
                                                    212
00000312  4900 81FE                 000003FE       213          CH    R0,=AL2(L'MSGMSG)       Message length within limits?
00000316  47D0 811E                 0000031E       214          BNH   MSGOK                   Yes, continue
0000031A  4100 005F                 0000005F       215          LA    R0,L'MSGMSG             No, set to maximum
                                                    216
0000031E  1820                                     217 MSGOK    LR    R2,R0                   Copy length to work register
00000320  0620                                     218          BCTR  R2,0                    Minus-1 for execute
00000322  4420 814C                 0000034C       219          EX    R2,MSGMVC               Copy message to O/P buffer
                                                    220
00000326  4120 200A                 0000000A       221          LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
0000032A  4110 8152                 00000352       222          LA    R1,MSGCMD               Point to true command
                                                    223
0000032E  83120008                                 224          DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
00000332  4780 8138                 00000338       225          BZ    MSGRET                  Return if successful
00000336  0000                                     226          DC    H'0'                    CRASH for debugging purposes
                                                    227
00000338  9802 8140                 00000340       228 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
0000033C  07F2                                     229          BR    R2                      Return to caller


00000340  00000000 00000000                        231 MSGSAVE  DC    3F'0'                   Registers save area
0000034C  D200 815B 1000      0000035B  00000000   232 MSGMVC   MVC   MSGMSG(0),0(R1)         Executed instruction


00000352  D4E2C7D5 D6C8405C                        234 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
0000035B  40404040 40404040                        235 MSGMSG   DC    CL95' '                 The message text to be displayed
                                                    236
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      238 ************************************************************************
                                                      239 *        Normal completion or Abnormal termination PSWs
                                                      240 ************************************************************************


000003C0  00020001 80000000                           242 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

000003D0  B2B2 81C0                   000003C0        244 EOJ      LPSWE EOJPSW               Normal completion


000003D8  00020001 80000000                           246 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

000003E8  B2B2 81D8                   000003D8        248 FAILTEST LPSWE FAILPSW              Abnormal termination


                                                      250 ************************************************************************
                                                      251 *        Working Storage
                                                      252 ************************************************************************

000003EC  00000000                                    254 CTLR0    DS    F                    CR0
000003F0  00000000                                    255         DS    F
                                                      256
000003F4  000013B4                                    257 E6TADR   DC    A(E6TESTS)           address of E6 test table


000003F8                                              259         LTORG ,                    Literals pool
000003F8  00000001                                    260               =F'1'
000003FC  0000                                        261               =H'0'
000003FE  005F                                        262               =AL2(L'MSGMSG)
                                                      263
                                                      264 *        some constants
                                                      265
                          00000400  00000001          266 K        EQU   1024               One KB
                          00001000  00000001          267 PAGE     EQU   (4*K)              Size of one page
                          00010000  00000001          268 K64      EQU   (64*K)             64 KB
                          00100000  00000001          269 MB       EQU   (K*K)               1 MB
                                                      270
                          AABBCCDD  00000001          271 REG2PATT EQU   X'AABBCCDD'      Polluted Register pattern
                          000000DD  00000001          272 REG2LOW  EQU         X'DD'      (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     274 *=====================================================================
                                                     275 *
                                                     276 *  NOTE: start data on an address that is easy to display
                                                     277 *        within Hercules
                                                     278 *
                                                     279 *=====================================================================
                                                     280
00000400                          00000400  00001000   281          ORG   ZVE6TST+X'1000'
00001000  00000000                                   282 FAILED   DC    F'0'                      some test failed?


                                                     284 ************************************************************************
                                                     285 *        TEST failed : result messgae
                                                     286 ************************************************************************
                                                     287 *
                                                     288 *        failed message and associated editting
                                                     289 *
00001004  40404040 40404040                          290 PRTLINE  DC    C'         Test # '
00001014  A7A7A7                                     291 PRTNUM   DC    C'xxx'
00001017  40868189 93858440                          292          DC    C' failed for instruction '
0000102F  A7A7A7A7 A7A7A7A7                          293 PRTNAME  DC    CL8'xxxxxxxx'
00001037  40A689A3 884093F2                          294          DC    C' with l2='
00001040  A7A7A7                                     295 PRTL2    DC    C'xxx'
00001043  4B                                         296          DC    C'.'
                                00000040  00000001   297 PRTLNG   EQU   *-PRTLINE
                                                     298
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    300 ************************************************************************
                                                    301 *        TEST failed : message working storge
                                                    302 ************************************************************************
00001044  40212020 20202020                         303 EDIT     DC    XL18'4021202020202020202020202020202020'
                                                    304
00001056  7E7E7E6E                                  305          DC    C'===>'
0000105A  40404040 40404040                         306 PRT3     DC    CL18' '
0000106C  4C7E7E7E                                  307          DC    C'<==='
00001070  00000000 00000000                         308 DECNUM   DS    CL16
                                                    309 *
                                                    310 *        CC extrtaction
                                                    311 *
00001080  00000000 00000000                         312 CCPSW    DS    2F          extract PSW after test (has CC)
00001088  00                                        313 CCFOUND  DS    X           extracted cc

                                                    315 ************************************************************************
                                                    316 *        Vector instruction results, pollution and input
                                                    317 ************************************************************************
00001090                                            318          DS    0FD
00001090  00000000 00000000                         319          DS    XL16                                        gap
000010A0  00000000 00000000                         320 V1OUTPUT DS    XL16                                     V1 OUTPUT
000010B0  00000000 00000000                         321          DS    XL16                                        gap
000010C0  FFFFFFFF FFFFFFFF                         322 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   V1 FUDGE
000010D0  BBBBBBBB BBBBBBBB                         323 V1FUDGEB DC    XL16'BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB'   V1 FUDGE b
000010E0  F1F2F3F4 F5F6F7F8                         324 V1INPUT  DC    CL16'1234567890123456'                   V1 input
000010F0  F7F8F9F0 F1F2F3F4                         325          DC    CL14'78901234567890'
000010FE  D9                                        326          DC    X'D9'
                                                    327
000010FF  00000000 00000000                         328          DS    XL16                                        gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     330 ********************************************************************************
                                                     331 *        E6TEST DSECT
                                                     332 ********************************************************************************


                                                     334 E6TEST   DSECT ,
00000000  00000000                                   335 TSUB     DC    A(0)           pointer  to test
00000004  0000                                       336 TNUM     DC    H'00'          Test Number
00000006  00                                         337          DC    X'00'
00000007  00                                         338          DC    X'00'
00000008  00000000                                   339 L2       DC    F'00'          L2 used
0000000C  00000000                                   340 EADDR    DC    A(0)           address of source
                                                     341
00000010  40404040 40404040                         342 OPNAME   DC    CL8' '         E6 name
                                                     343
00000018  00000000                                   344 RELEN    DC    A(0)           RESULT LENGTH
0000001C  00000000                                   345 READDR   DC    A(0)           expected result address
                                                     346
                                                     347 **
                                                     348 *        test routine will be here (from VRS_D macro)
                                                     349 * followed by
                                                     350 *        16-byte EXPECTED RESULT
                                                     351 *        16-byte source
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   353 ********************************************************************************
                                                   354 *     Macros to help build test tables
                                                   355 *------------------------------------------------------------------------------
                                                   356 *     VRS_D Macro to help build test tables
                                                   357 ********************************************************************************
                                                   358          MACRO
                                                   359          VRS_D &INST,&L2
                                                   360 .*                                  &INST  - VRS-d instruction under test
                                                   361 .*                                  &L2    - length (loaded into reg)
                                                   362 .*
                                                   363          LCLA  &XCC(4)  &CC has mask values for FAILED condition codes
                                                   364 &XCC(1)  SETA  7                    CC != 0
                                                   365 &XCC(2)  SETA  11                   CC != 1
                                                   366 &XCC(3)  SETA  13                   CC != 2
                                                   367 &XCC(4)  SETA  14                   CC != 3
                                                   368
                                                   369          GBLA  &TNUM
                                                   370 &TNUM    SETA  &TNUM+1
                                                   371
                                                   372          DS    0FD
                                                   373          USING *,R5                base for test data and test routine
                                                   374
                                                   375 T&TNUM   DC    A(X&TNUM)           address of test routine
                                                   376          DC    H'&TNUM'            test number
                                                   377          DC    X'00'
                                                   378          DC    X'00'
                                                   379          DC    F'&L2'              l2
                                                   380 EA2_&TNUM DC    A(RE&TNUM+16)       addr of 16-byte source
                                                   381          DC    CL8'&INST'          instruction name
                                                   382          DC    A(16)               result length
                                                   383 REA&TNUM DC    A(RE&TNUM)          result address
                                                   384 .*
                                                   385 *                                  INSTRUCTION UNDER TEST ROUTINE
                                                   386 X&TNUM   DS    0F
                                                   387          L     R1,L2               get number of bytes to load / store
                                                   388          L     R2,EADDR            get address of source
                                                   389          VLRLR V1,R1,0(R2)         load some bytes
                                                   390
                                                   391          L     R1,L2               get number of bytes to store
                                                   392          &INST V1,R1,V1OUTPUT      test instruction
                                                   393
                                                   394          BR    R11                 return
                                                   395
                                                   396 RE&TNUM  DC    0F
                                                   397          DROP  R5
                                                   398
                                                   399          MEND
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      401 ************************************************************************
                                                      402 *     PTTABLE Macro to generate table of pointers to individual tests
                                                      403 ************************************************************************
                                                      404
                                                      405          MACRO
                                                      406          PTTABLE
                                                      407          GBLA  &TNUM
                                                      408          LCLA  &CUR
                                                      409 &CUR     SETA  1
                                                      410 .*
                                                      411 TTABLE   DS    0F
                                                      412 .LOOP    ANOP
                                                      413 .*
                                                      414          DC    A(T&CUR)           address of test
                                                      415 .*
                                                      416 &CUR     SETA  &CUR+1
                                                      417          AIF   (&CUR LE &TNUM).LOOP
                                                      418 *
                                                      419          DC    A(0)               END OF TABLE
                                                      420          DC    A(0)
                                                      421 .*
                                                      422          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     424 ********************************************************************************
                                                     425 *        E6 VRS_D tests
                                                     426 ********************************************************************************
                             00000000  000013DF      427 ZVE6TST  CSECT ,
00001110                                             428          DS    0F


                                                     430          PRINT DATA
                                                     431 *
                                                     432 *        E63F VECTOR STORE RIGHTMOST WITH LENGTH  (reg)
                                                     433 *
                                                     434 *        VRS_D instr,l2
                                                     435 *             followed by
                                                     436 *             v1     - 16 byte expected result
                                                     437 *             source - 16 byte source from which to get
                                                     438 *                      L2+1 (up to 16) bytes
                                                     439
                                                     440 *-------------------------------------------------------------------
                                                     441 *VSTRLR  - VECTOR STORE RIGHTMOST WITH LENGTH  (reg)
                                                     442 *-------------------------------------------------------------------
                                                     443 * VSTRLR simple
                                                     444
                                                     445          VRS_D VSTRLR,0                                  1-byte
00001110                                             446+         DS    0FD
00001110                             00001110        447+         USING *,R5              base for test data and test routine
00001110  00001130                                   448+T1       DC    A(X1)             address of test routine
00001114  0001                                       449+         DC    H'1'              test number
00001116  00                                         450+         DC    X'00'
00001117  00                                         451+         DC    X'00'
00001118  00000000                                   452+         DC    F'0'              l2
0000111C  0000115C                                   453+EA2_1    DC    A(RE1+16)         addr of 16-byte source
00001120  E5E2E3D9 D3D94040                          454+         DC    CL8'VSTRLR'       instruction name
00001128  00000010                                   455+         DC    A(16)             result length
0000112C  0000114C                                   456+REA1     DC    A(RE1)            result address
                                                     457+*                                  INSTRUCTION UNDER TEST ROUTINE
00001130                                             458+X1       DS    0F
00001130  5810 5008                  00000008        459+         L     R1,L2             get number of bytes to load / store
00001134  5820 500C                  0000000C        460+         L     R2,EADDR          get address of source
00001138  E601 2000 1037             00000000        461+         VLRLR V1,R1,0(R2)       load some bytes
0000113E  5810 5008                  00000008        462+         L     R1,L2             get number of bytes to store
00001142  E601 8EA0 103F             000010A0        463+         VSTRLR V1,R1,V1OUTPUT   test instruction
00001148  07FB                                       464+         BR    R11               return
0000114C                                             465+RE1      DC    0F
0000114C                                             466+         DROP  R5
0000114C  22BBBBBB BBBBBBBB                          467          DC    XL16'22BBBBBBBBBBBBBBBBBBBBBBBBBBBBBB'   V1
00001154  BBBBBBBB BBBBBBBB
0000115C  22000000 00000000                          468          DC    XL16'2200000000000000000000000000023C'   source
00001164  00000000 0000023C
                                                     469
                                                     470          VRS_D VSTRLR,1
00001170                                             471+         DS    0FD
00001170                             00001170        472+         USING *,R5              base for test data and test routine
00001170  00001190                                   473+T2       DC    A(X2)             address of test routine
00001174  0002                                       474+         DC    H'2'              test number
00001176  00                                         475+         DC    X'00'
00001177  00                                         476+         DC    X'00'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001178  00000001                                477+          DC    F'1'                l2
0000117C  000011BC                                478+EA2_2     DC    A(RE2+16)           addr of 16-byte source
00001180  E5E2E3D9 D3D94040                       479+          DC    CL8'VSTRLR'         instruction name
00001188  00000010                                480+          DC    A(16)               result length
0000118C  000011AC                                481+REA2      DC    A(RE2)              result address
                                                  482+*                                   INSTRUCTION UNDER TEST ROUTINE
00001190                                          483+X2        DS    0F
00001190  5810 5008                     00000008  484+          L     R1,L2               get number of bytes to load / store
00001194  5820 500C                     0000000C  485+          L     R2,EADDR            get address of source
00001198  E601 2000 1037                00000000  486+          VLRLR V1,R1,0(R2)         load some bytes
0000119E  5810 5008                     00000008  487+          L     R1,L2               get number of bytes to store
000011A2  E601 8EA0 103F                000010A0  488+          VSTRLR V1,R1,V1OUTPUT     test instruction
000011A8  07FB                                    489+          BR    R11                 return
000011AC                                          490+RE2       DC    0F
000011AC                                          491+          DROP  R5
000011AC  2233BBBB BBBBBBBB                       492           DC    XL16'2233BBBBBBBBBBBBBBBBBBBBBBBB'    V1
000011B4  BBBBBBBB BBBBBBBB
000011BC  22330000 00000000                       493           DC    XL16'223300000000000000000000000023C'   source
000011C4  00000000 0000023C
                                                  494
                                                  495           VRS_D VSTRLR,5
000011D0                                          496+          DS    0FD
000011D0                  000011D0                497+          USING *,R5                base for test data and test routine
000011D0  000011F0                                498+T3        DC    A(X3)               address of test routine
000011D4  0003                                    499+          DC    H'3'                test number
000011D6  00                                      500+          DC    X'00'
000011D7  00                                      501+          DC    X'00'
000011D8  00000005                                502+          DC    F'5'                l2
000011DC  0000121C                                503+EA2_3     DC    A(RE3+16)           addr of 16-byte source
000011E0  E5E2E3D9 D3D94040                       504+          DC    CL8'VSTRLR'         instruction name
000011E8  00000010                                505+          DC    A(16)               result length
000011EC  0000120C                                506+REA3      DC    A(RE3)              result address
                                                  507+*                                   INSTRUCTION UNDER TEST ROUTINE
000011F0                                          508+X3        DS    0F
000011F0  5810 5008                     00000008  509+          L     R1,L2               get number of bytes to load / store
000011F4  5820 500C                     0000000C  510+          L     R2,EADDR            get address of source
000011F8  E601 2000 1037                00000000  511+          VLRLR V1,R1,0(R2)         load some bytes
000011FE  5810 5008                     00000008  512+          L     R1,L2               get number of bytes to store
00001202  E601 8EA0 103F                000010A0  513+          VSTRLR V1,R1,V1OUTPUT     test instruction
00001208  07FB                                    514+          BR    R11                 return
0000120C                                          515+RE3       DC    0F
0000120C                                          516+          DROP  R5
0000120C  22334455 6677BBBB                       517           DC    XL16'223344556677BBBBBBBBBBBBBBBBBBBB'    V1
00001214  BBBBBBBB BBBBBBBB
0000121C  22334455 66778800                       518           DC    XL16'2233445566778800000000000000023C'   source
00001224  00000000 0000023C
                                                  519
                                                  520           VRS_D VSTRLR,14
00001230                                          521+          DS    0FD
00001230                  00001230                522+          USING *,R5                base for test data and test routine
00001230  00001250                                523+T4        DC    A(X4)               address of test routine
00001234  0004                                    524+          DC    H'4'                test number
00001236  00                                      525+          DC    X'00'
00001237  00                                      526+          DC    X'00'
00001238  0000000E                                527+          DC    F'14'               l2
0000123C  0000127C                                528+EA2_4     DC    A(RE4+16)           addr of 16-byte source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001240  E5E2E3D9 D3D94040                        529+          DC    CL8'VSTRLR'       instruction name
00001248  00000010                                 530+          DC    A(16)             result length
0000124C  0000126C                                 531+REA4      DC    A(RE4)            result address
                                                   532+*                                 INSTRUCTION UNDER TEST ROUTINE
00001250                                           533+X4        DS    0F
00001250  5810 5008                      00000008  534+          L     R1,L2             get number of bytes to load / store
00001254  5820 500C                      0000000C  535+          L     R2,EADDR          get address of source
00001258  E601 2000 1037                 00000000  536+          VLRLR V1,R1,0(R2)       load some bytes
0000125E  5810 5008                      00000008  537+          L     R1,L2             get number of bytes to store
00001262  E601 8EA0 103F                 000010A0  538+          VSTRLR V1,R1,V1OUTPUT   test instruction
00001268  07FB                                     539+          BR    R11               return
0000126C                                           540+RE4       DC    0F
0000126C                                           541+          DROP  R5
0000126C  22334455 66778800                        542           DC    XL16'223344556677880000000000000002BB'    V1
00001274  00000000 000002BB
0000127C  22334455 66778800                        543           DC    XL16'223344556677880000000000000023C'   source
00001284  00000000 0000023C
                                                   544
                                                   545           VRS_D VSTRLR,15
00001290                                           546+          DS    0FD
00001290                           00001290        547+          USING *,R5              base for test data and test routine
00001290  000012B0                                 548+T5        DC    A(X5)             address of test routine
00001294  0005                                     549+          DC    H'5'              test number
00001296  00                                       550+          DC    X'00'
00001297  00                                       551+          DC    X'00'
00001298  0000000F                                 552+          DC    F'15'             l2
0000129C  000012DC                                 553+EA2_5     DC    A(RE5+16)         addr of 16-byte source
000012A0  E5E2E3D9 D3D94040                        554+          DC    CL8'VSTRLR'       instruction name
000012A8  00000010                                 555+          DC    A(16)             result length
000012AC  000012CC                                 556+REA5      DC    A(RE5)            result address
                                                   557+*                                 INSTRUCTION UNDER TEST ROUTINE
000012B0                                           558+X5        DS    0F
000012B0  5810 5008                      00000008  559+          L     R1,L2             get number of bytes to load / store
000012B4  5820 500C                      0000000C  560+          L     R2,EADDR          get address of source
000012B8  E601 2000 1037                 00000000  561+          VLRLR V1,R1,0(R2)       load some bytes
000012BE  5810 5008                      00000008  562+          L     R1,L2             get number of bytes to store
000012C2  E601 8EA0 103F                 000010A0  563+          VSTRLR V1,R1,V1OUTPUT   test instruction
000012C8  07FB                                     564+          BR    R11               return
000012CC                                           565+RE5       DC    0F
000012CC                                           566+          DROP  R5
000012CC  22334455 66778800                        567           DC    XL16'223344556677880000000000000023C'    V1
000012D4  00000000 0000023C
000012DC  22334455 66778800                        568           DC    XL16'223344556677880000000000000023C'   source
000012E4  00000000 0000023C
                                                   569
                                                   570           VRS_D VSTRLR,32                      check r3>15
000012F0                                           571+          DS    0FD
000012F0                           000012F0        572+          USING *,R5              base for test data and test routine
000012F0  00001310                                 573+T6        DC    A(X6)             address of test routine
000012F4  0006                                     574+          DC    H'6'              test number
000012F6  00                                       575+          DC    X'00'
000012F7  00                                       576+          DC    X'00'
000012F8  00000020                                 577+          DC    F'32'             l2
000012FC  0000133C                                 578+EA2_6     DC    A(RE6+16)         addr of 16-byte source
00001300  E5E2E3D9 D3D94040                        579+          DC    CL8'VSTRLR'       instruction name
00001308  00000010                                 580+          DC    A(16)             result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000130C  0000132C                                581+REA6     DC    A(RE6)            result address
                                                  582+*                                INSTRUCTION UNDER TEST ROUTINE
00001310                                          583+X6       DS    0F
00001310  5810 5008                     00000008  584+         L     R1,L2             get number of bytes to load / store
00001314  5820 500C                     0000000C  585+         L     R2,EADDR          get address of source
00001318  E601 2000 1037                00000000  586+         VLRLR V1,R1,0(R2)       load some bytes
0000131E  5810 5008                     00000008  587+         L     R1,L2             get number of bytes to store
00001322  E601 8EA0 103F                000010A0  588+         VSTRLR V1,R1,V1OUTPUT   test instruction
00001328  07FB                                    589+         BR    R11               return
0000132C                                          590+RE6      DC    0F
0000132C                                          591+         DROP  R5
0000132C  22334455 66778800                       592          DC    XL16'223344556677880000000000000023C'    V1
00001334  00000000 0000023C
0000133C  22334455 66778800                       593          DC    XL16'223344556677880000000000000023C'   source
00001344  00000000 0000023C
                                                  594
                                                  595          VRS_D VSTRLR,999                      check r3>15
00001350                                          596+         DS    0FD
00001350                  00001350                597+         USING *,R5              base for test data and test routine
00001350  00001370                                598+T7       DC    A(X7)             address of test routine
00001354  0007                                    599+         DC    H'7'              test number
00001356  00                                      600+         DC    X'00'
00001357  00                                      601+         DC    X'00'
00001358  000003E7                                602+         DC    F'999'            l2
0000135C  0000139C                                603+EA2_7    DC    A(RE7+16)         addr of 16-byte source
00001360  E5E2E3D9 D3D94040                       604+         DC    CL8'VSTRLR'       instruction name
00001368  00000010                                605+         DC    A(16)             result length
0000136C  0000138C                                606+REA7     DC    A(RE7)            result address
                                                  607+*                                INSTRUCTION UNDER TEST ROUTINE
00001370                                          608+X7       DS    0F
00001370  5810 5008                     00000008  609+         L     R1,L2             get number of bytes to load / store
00001374  5820 500C                     0000000C  610+         L     R2,EADDR          get address of source
00001378  E601 2000 1037                00000000  611+         VLRLR V1,R1,0(R2)       load some bytes
0000137E  5810 5008                     00000008  612+         L     R1,L2             get number of bytes to store
00001382  E601 8EA0 103F                000010A0  613+         VSTRLR V1,R1,V1OUTPUT   test instruction
00001388  07FB                                    614+         BR    R11               return
0000138C                                          615+RE7      DC    0F
0000138C                                          616+         DROP  R5
0000138C  99334455 66778800                       617          DC    XL16'993344556677880000000000009023C'    V1
00001394  00000000 0009023C
0000139C  99334455 66778800                       618          DC    XL16'993344556677880000000000009023C'   source
000013A4  00000000 0009023C
                                                  619
000013AC  00000000                                620          DC    F'0'     END OF TABLE
000013B0  00000000                                621          DC    F'0'
                                                  622 *
                                                  623 * table of pointers to individual load test
                                                  624 *
000013B4                                          625 E6TESTS  DS    0F
                                                  626          PTTABLE
000013B4                                          627+TTABLE   DS    0F
000013B4  00001110                                628+         DC    A(T1)             address of test
000013B8  00001170                                629+         DC    A(T2)             address of test
000013BC  000011D0                                630+         DC    A(T3)             address of test
000013C0  00001230                                631+         DC    A(T4)             address of test
000013C4  00001290                                632+         DC    A(T5)             address of test
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000013C8  000012F0                            633+          DC    A(T6)             address of test
000013CC  00001350                            634+          DC    A(T7)             address of test
                                              635+*
000013D0  00000000                            636+          DC    A(0)              END OF TABLE
000013D4  00000000                            637+          DC    A(0)
                                              638
000013D8  00000000                            639           DC    F'0'     END OF TABLE
000013DC  00000000                            640           DC    F'0'
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   642 ********************************************************************************
                                                   643 *        Register equates
                                                   644 ********************************************************************************

                                00000000  00000001   646 R0       EQU   0
                                00000001  00000001   647 R1       EQU   1
                                00000002  00000001   648 R2       EQU   2
                                00000003  00000001   649 R3       EQU   3
                                00000004  00000001   650 R4       EQU   4
                                00000005  00000001   651 R5       EQU   5
                                00000006  00000001   652 R6       EQU   6
                                00000007  00000001   653 R7       EQU   7
                                00000008  00000001   654 R8       EQU   8
                                00000009  00000001   655 R9       EQU   9
                                0000000A  00000001   656 R10      EQU   10
                                0000000B  00000001   657 R11      EQU   11
                                0000000C  00000001   658 R12      EQU   12
                                0000000D  00000001   659 R13      EQU   13
                                0000000E  00000001   660 R14      EQU   14
                                0000000F  00000001   661 R15      EQU   15


                                                   663 ********************************************************************************
                                                   664 *        Register equates
                                                   665 ********************************************************************************

                              00000000  00000001   667 V0       EQU   0
                              00000001  00000001   668 V1       EQU   1
                              00000002  00000001   669 V2       EQU   2
                              00000003  00000001   670 V3       EQU   3
                              00000004  00000001   671 V4       EQU   4
                              00000005  00000001   672 V5       EQU   5
                              00000006  00000001   673 V6       EQU   6
                              00000007  00000001   674 V7       EQU   7
                              00000008  00000001   675 V8       EQU   8
                              00000009  00000001   676 V9       EQU   9
                              0000000A  00000001   677 V10      EQU   10
                              0000000B  00000001   678 V11      EQU   11
                              0000000C  00000001   679 V12      EQU   12
                              0000000D  00000001   680 V13      EQU   13
                              0000000E  00000001   681 V14      EQU   14
                              0000000F  00000001   682 V15      EQU   15
                              00000010  00000001   683 V16      EQU   16
                              00000011  00000001   684 V17      EQU   17
                              00000012  00000001   685 V18      EQU   18
                              00000013  00000001   686 V19      EQU   19
                              00000014  00000001   687 V20      EQU   20
                              00000015  00000001   688 V21      EQU   21
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                00000016  00000001   689 V22      EQU   22
                                00000017  00000001   690 V23      EQU   23
                                00000018  00000001   691 V24      EQU   24
                                00000019  00000001   692 V25      EQU   25
                                0000001A  00000001   693 V26      EQU   26
                                0000001B  00000001   694 V27      EQU   27
                                0000001C  00000001   695 V28      EQU   28
                                0000001D  00000001   696 V29      EQU   29
                                0000001E  00000001   697 V30      EQU   30
                                0000001F  00000001   698 V31      EQU   31
                                                     699
                                                     700          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	92	58 89 90
CCFOUND	X	00001088	1	313	
CCPSW	F	00001080	4	312	
CTLR0	F	000003EC	4	254	102 103 104 105
DECNUM	C	00001070	16	308	141 143 150 152
E6TADR	A	000003F4	4	257	111
E6TEST	4	00000000	32	334	118
E6TESTS	F	000013B4	4	625	257
EA2_1	A	0000111C	4	453	
EA2_2	A	0000117C	4	478	
EA2_3	A	000011DC	4	503	
EA2_4	A	0000123C	4	528	
EA2_5	A	0000129C	4	553	
EA2_6	A	000012FC	4	578	
EA2_7	A	0000135C	4	603	
EADDR	A	0000000C	4	340	460 485 510 535 560 585 610
EDIT	X	00001044	18	303	142 151
ENDTEST	U	000002BE	1	172	116
EOJ	I	000003D0	4	244	175
EOJPSW	D	000003C0	8	242	244
FAILCONT	U	000002AE	1	162	
FAILED	F	00001000	4	282	164 173
FAILMSG	U	00000264	1	139	129
FAILPSW	D	000003D8	8	246	248
FAILTEST	I	000003E8	4	248	176
IMAGE	1	00000000	5088	0	
K	U	00000400	1	266	267 268 269
K64	U	00010000	1	268	
L2	F	00000008	4	339	149 459 462 484 487 509 512 534 537 559 562 584 587 609 612
MB	U	00100000	1	269	
MSG	I	00000308	4	208	191
MSGCMD	C	00000352	9	234	221 222
MSGMSG	C	0000035B	95	235	215 232 213
MSGMVC	I	0000034C	6	232	219
MSGOK	I	0000031E	2	217	214
MSGRET	I	00000338	4	228	225
MSGSAVE	F	00000340	4	231	211 228
NEXTE6	U	0000022A	1	113	132 167
OPNAME	C	00000010	8	342	146
PAGE	U	00001000	1	267	
PRT3	C	0000105A	18	306	142 143 144 151 152 153
PRTL2	C	00001040	3	295	153
PRTLINE	C	00001004	16	290	297 156
PRTLNG	U	00000040	1	297	155
PRTNAME	C	0000102F	8	293	146
PRTNUM	C	00001014	3	291	144
R0	U	00000000	1	646	52 102 105 155 163 164 190 192 208 211 213 215 217 228
R1	U	00000001	1	647	127 128 156 173 174 222 232 459 461 462 463 484 486 487 488 509 511 512 513 534 536 537 538 559 561 562 563 584 586 587 588 609 611 612 613
R10	U	0000000A	1	656	99 100
R11	U	0000000B	1	657	123 124 464 489 514 539 564 589 614
R12	U	0000000C	1	658	111 114 131 166
R13	U	0000000D	1	659	
R14	U	0000000E	1	660	
R15	U	0000000F	1	661	157 185 195 196

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
R2	U	00000002	1	648	140 141 148 149 150 190 191 192 209 211 217 218 219 221 228 229 460 461 485 486 510 511 535 536 560 561 585 586 610 611
R3	U	00000003	1	649	
R4	U	00000004	1	650	
R5	U	00000005	1	651	114 115 118 186 194 447 466 472 491 497 516 522 541 547 566 572 591 597 616
R6	U	00000006	1	652	
R7	U	00000007	1	653	
R8	U	00000008	1	654	89 92 93 94 96
R9	U	00000009	1	655	90 96 97 99
RE1	F	0000114C	4	465	453 456
RE2	F	000011AC	4	490	478 481
RE3	F	0000120C	4	515	503 506
RE4	F	0000126C	4	540	528 531
RE5	F	000012CC	4	565	553 556
RE6	F	0000132C	4	590	578 581
RE7	F	0000138C	4	615	603 606
REA1	A	0000112C	4	456	
REA2	A	0000118C	4	481	
REA3	A	000011EC	4	506	
REA4	A	0000124C	4	531	
REA5	A	000012AC	4	556	
REA6	A	0000130C	4	581	
REA7	A	0000136C	4	606	
READDR	A	0000001C	4	345	127
REG2LOW	U	000000DD	1	272	
REG2PATT	U	AABBCCDD	1	271	
RELEN	A	00000018	4	344	
RPTDWSAV	D	000002F8	8	201	190 192
RPTERROR	I	000002CC	4	185	157
RPTSAVE	F	000002EC	4	198	185 195
RPTSVR5	F	000002F0	4	199	186 194
SVOLDPSW	U	00000140	0	54	
T1	A	00001110	4	448	628
T2	A	00001170	4	473	629
T3	A	000011D0	4	498	630
T4	A	00001230	4	523	631
T5	A	00001290	4	548	632
T6	A	000012F0	4	573	633
T7	A	00001350	4	598	634
TESTREST	U	0000024C	1	126	
TNUM	H	00000004	2	336	140
TSUB	A	00000000	4	335	123
TTABLE	F	000013B4	4	627	
V0	U	00000000	1	667	
V1	U	00000001	1	668	119 120 121 461 463 486 488 511 513 536 538 561 563 586 588 611 613
V10	U	0000000A	1	677	
V11	U	0000000B	1	678	
V12	U	0000000C	1	679	
V13	U	0000000D	1	680	
V14	U	0000000E	1	681	
V15	U	0000000F	1	682	
V16	U	00000010	1	683	
V17	U	00000011	1	684	
V18	U	00000012	1	685	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V19	U	00000013	1	686	
V1FUDGE	X	000010C0	16	322	121
V1FUDGEB	X	000010D0	16	323	119
V1INPUT	C	000010E0	16	324	
V1OUTPUT	X	000010A0	16	320	120 128 463 488 513 538 563 588 613
V2	U	00000002	1	669	
V20	U	00000014	1	687	
V21	U	00000015	1	688	
V22	U	00000016	1	689	
V23	U	00000017	1	690	
V24	U	00000018	1	691	
V25	U	00000019	1	692	
V26	U	0000001A	1	693	
V27	U	0000001B	1	694	
V28	U	0000001C	1	695	
V29	U	0000001D	1	696	
V3	U	00000003	1	670	
V30	U	0000001E	1	697	
V31	U	0000001F	1	698	
V4	U	00000004	1	671	
V5	U	00000005	1	672	
V6	U	00000006	1	673	
V7	U	00000007	1	674	
V8	U	00000008	1	675	
V9	U	00000009	1	676	
X1	F	00001130	4	458	448
X2	F	00001190	4	483	473
X3	F	000011F0	4	508	498
X4	F	00001250	4	533	523
X5	F	000012B0	4	558	548
X6	F	00001310	4	583	573
X7	F	00001370	4	608	598
ZVE6TST	J	00000000	5088	51	54 56 60 64 281 52
=AL2(L'MSGMSG)	R	000003FE	2	262	213
=F'1'	F	000003F8	4	260	163
=H'0'	H	000003FC	2	261	208

```
 MACRO    DEFN   REFERENCES

PTTABLE    406    626
VRS_D      359    445    470    495    520    545    570    595
```

```
   DESC      SYMBOL   SIZE     POS         ADDR

Entry: 0

Image       IMAGE    5088  0000-13DF  0000-13DF
  Region             5088  0000-13DF  0000-13DF
    CSECT   ZVE6TST  5088  0000-13DF  0000-13DF
```

```
   STMT                    FILE NAME
1     /devstor/dev/tests/zvector-e6-09-VSTRLR.asm

** NO ERRORS FOUND **
```