ASMA Ver.	0. 7. 0 zv	ector- e6- 13-	convertto	deci mal	(Zvect	or E6 VRR	?- g)		18 Jun 2024 18: 58: 17 Page	2
LOC	ОВЈЕСТ	CODE	ADDR1	ADDR2	STMT					
					49	*****	*****	*******	**********	
					50 51	*	FCHECK	Macro - Is a Facility	Bit set?	
					<b>52</b>	*			et, an message is issued and	
					53 54		the te	est is skipped.		
					55 56	*	Fcheck	uses RO, R1 and R2		
					<b>57</b>	* eg. ******	FCHECK	134, 'vector-packed-de	cimal'	
					58 59		MACRO	******	*********	
					60 61	*	FCHECK	X &BITNO, &NOTSETMSG &RITNO · fa	cility bit number to check	
					62	*	T CT A	&NOTSETMSG	: 'facility name'	
					63 64			&FBBYTE Faci &FBBIT Faci	lity bit in Byte lity bit within Byte	
					65 66		LCLA			
						&L(1)			bit positions within byte	
					69			&BITNO/8		
					70 71			&L((&BITNO-(&FBBYTE*8) 0, 'checking Bit=&BITNO	)+1) : FBBYTE=&FBBYTE, FBBIT=&FBBIT'	
					72 73			X&SYSNDX		
					<b>74</b>		_	140 1511211	Fcheck data area	
						SKT&SYSNI			skip messgae ests: '	
					77 78			C&NOTSETMSG C' facility (bit &BITN	(0) is not installed.'	
					79 80	SKL&SYSNI *	X EQU	*-SKT&SYSNĎX	facility bits	
					81		DS	FD	gap	
					83		DS DS	4FD FD	gap	
					84 85	* X&SYSNDX	EQU *			
					86 87		LA	RO, ((X&SYSNDX-FB&SYSND FB&SYSNDX		
					88				get facility bits	
					89 90			RO, RO RO, FB&SYSNDX+&FBBYTE	get fbit byte	
					91 92		N	RO, =F' &FBBIT' XC&SYSNDX	get fbit byte is bit set?	
					93				1	
					95	*		not set, issue message		
					96 97		LA LA	RO, SKL&SYSNDX R1, SKT&SYSNDX	message length message address	
					98 99			R2, MSG		
					100	TICO CTICITE		ЕОЈ		
					101 102	XC&SYSNDX	X EQU * Mend			

ASMA Ver.	0. 7. 0 zvector-e6-1	3-convertt	odeci mal	(Zvector	E6 VRR-g)		18 Jun 2024 18: 58: 17 Page
LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				105 *	Low co	ore PSWs	************
00000000		00000000 00000000	000013BB	108 ZVI 109 110	E6TST START USING	0 ZVE6TST, R0	Low core addressability
		00000140	0000000		OLDPSW EQU	ZVE6TST+X' 140'	z/Arch Supervisor call old PSW
	00000001 80000000 0000000 00000200	0000000	000001A0	113 114 115	DC	ZVE6TST+X' 1A0' X' 0000000180000000' AD(BEGIN)	z/Architecure RESTART PSW
	00020001 80000000 0000000 0000DEAD	000001B0	000001D0	117 118 119	DC	ZVE6TST+X' 1D0' X' 0002000180000000' AD(X' DEAD')	z/Architecure PROGRAM CHECK PSW
000001E0		000001E0	00000200	121 122	ORG	ZVE6TST+X' 200'	Start of actual test program

ASMA Ver.	0. 7. 0 zvector-e6-1	3-convertt	odecimal (	Zvector E6 VR	R- g)		18 Jun 2024 18: 58: 17 Page	4
LOC	OBJECT CODE	ADDR1	ADDR2	STMI				
				124 ******	****	******	***********	
				125 *		The actual "ZVE	6TST" program itself	
				126 ******* 127 *	*****	******	*************	
				128 * Archi		e Mode: z/Arch		
				129 * Regis 130 *	ter Us	age:		
				131 * <b>R</b> 0		work)		
				132 * R1-4 133 * R5		work)	ble - current test base	
				134 * R6-R	7 (1	work)		
				135 * R8 136 * R9	Fi	irst base registe econd base registe	r or	
				137 * R10	T	hird base registe	r	
				138 * R11 139 * R12		6TEST call return 6TESTS register		
				140 * R13	()	work)		
				141 * R14 142 * R15		ubroutine call econdary Subrouti	ne call or work	
				143 *	50	econdary Subrouch	ne carr or work	
				144 ******	*****	******	************	
00000200		00000200		146		BEGIN, R8	FIRST Base Register	
00000200 00000200		00001200 00002200		147 148	USI NG USI NG		SECOND Base Register THIRD Base Register	
		00002200		149		·		
00000200 00000202	0580 0680			150 BEGIN 151	BALR BCTR	R8, 0	Initalize FIRST base register Initalize FIRST base register	
00000204	0680			152		R8, 0	Initalize FIRST base register	
00000206	4190 8800		00800000	153 154	LA	R9, 2048(, R8)	Initalize SECOND base register	
0000020A	4190 9800		00000800	155	LA	R9, 2048(, R9)	Initalize SECOND base register	
0000020E	41A0 9800		00800000	156 157	LA	R10, 2048(, R9)	Initalize THIRD base register	
00000212	41A0 A800		00000800	158	LA	R10, 2048(, R10)	Initalize THIRD base register	
00000216	B600 82C4		000004C4	159 160	STCTI.	RO, RO, CTLRO	Store CRO to enable AFP	
0000021A	9604 82C5		000004C5	161	<b>0I</b>	CTLR0+1, X' 04'	Turn on AFP bit	
0000021E 00000222	9602 82C5 B700 82C4		000004C5 000004C4	162 163	OI LCTL	CTLRO+1, X' 02' RO, RO, CTLRO	Turn on Vector bit Reload updated CRO	
	2.00 0.01			164			•	
				165 ******* 166 * Is Vec	tor pa	cked-decimal faci	**************************************	
				167 ******	****	******	************	
				168 169	FCHEC	K 134, 'vector-pac	ked-decimal'	
00000226	47F0 80B0		000002B0	170+	В	X0001		
				171+* 172+*			Fcheck data area skip messgae	
0000022A	40404040 40404040			173+SKT0001	DC		ping tests: '	
00000244 00000259	A58583A3 96996097 40868183 899389A3			174+ 175+	DC DC	C' vector-packed- C' facility (bit	decimal' 134) is not installed.'	
		00000054	0000001	176+SKL0001	EQU	*- SKT0001		
00000280	0000000 00000000			177+* 178+	DS	FD	facility bits gap	
00000288	00000000 00000000			179+FB0001	DS	4FD	0 1	

ASMA Ver.	0. 7. 0 zvector- e6-	13-convertt	odeci mal	(Zvector E6 VR	R- g)		18 Jun 2024 18: 58: 17 Page	8
LOC	OBJECT CODE	ADDR1	ADDR2	STMI				
00000386 0000038A 0000038E 00000392	5800 82D8 5000 8E00 41C0 C004 47F0 80DC	00000386	00000001 000004D8 00001000 00000004 000002DC	268 ******** 269 * contin 270 ******* 271 FAILCONT 272 273 274 275 276	*****	**************************************	**************************************	
				278 ******* 279 * end of 280 ******	***** <b>testi</b> ****	**************************************	**************************************	
00000396 0000039A 0000039C	5810 8E00 1211 4780 82A8	00000396	00000001 00001000 000004A8	281 ENDTEST 282 283 284	EQU L LTR BZ	* R1, FAILED R1, R1 EOJ	did a test fail? No, exit	
00003A0	47F0 82C0		000004C0	285 286	В	FAILTEST	Yes, exit with BAD PSW	

ASMA Ver.	0. 7. 0 zvector- e6- 1	3-convertto	odecimal (	Zvector E6 VR	R- g)		18 Jun 2024 18: 58: 17 Page	9
LOC	OBJECT CODE	ADDR1	ADDR2	STMF				
				288 ******* 289 * 290 *	* * * * * * <b>RPTER</b>		**************************************	
				291 * 292 ******	*****		= NESSGAE LENGTH = ADDRESS OF MESSAGE ************************************	
000003A4 000003A8	50F0 81C4 5050 81C8		000003C4 000003C8	294 RPTERROR 295 296 *	ST ST	R15, RPTSAVE R5, RPTSVR5	Save return address Save R5	
				297 * 298 *		G	r Message to console	
000003AC 000003B0 000003B4	9002 81D0 4520 81E0 9802 81D0		000003D0 000003E0 000003D0	299 300 301	STM BAL LM	RO, R2, RPTDWSAV R2, MSG R0, R2, RPTDWSAV	save regs used by MSG call Hercules console MSG display restore regs	
000003B8	5850 81C8		000003C8	303	L	R5, RPTSVR5	Restore R5	
000003BC 000003C0	58F0 81C4 07FF		000003C4	304 305	L BR	R15, RPTSAVE R15	Restore return address Return to caller	
000003C4 000003C8	00000000 00000000			307 RPTSAVE 308 RPTSVR5	DC DC	F' 0' F' 0'	R15 save area R5 save area	
000003D0	00000000 00000000			310 RPTDWSAV	DC	2D' 0'	RO-R2 save area for MSG call	

ASMA Ver.	0. 7. 0 zvector-e6-1	3-converttoded	cimal (	Zvector E6 VR	R- g)		18 Jun 2024 18: 58: 17 Page 10
LOC	OBJECT CODE	ADDR1 AI	DDR2	STMI			
				312 ******* 313 * 314 * 315 ******		HERCULES MESSAGE point R2 = return address	**************************************
000003E0 000003E4	4900 82DC 07D2	000	0004DC	317 MSG 318 319	CH BNHR	RO, =H' O' R2	Do we even HAVE a message? No, ignore
000003E6	9002 821C	000	00041C	320 321	STM	RO, R2, MSGSAVE	Save registers
000003EA	4900 82DE		0004DE	322	СН	RO, =AL2(L' MSGMSG)	Message length within limits?
000003EE 000003F2	47D0 81F6 4100 005F		0003F6 00005F	323 324 325	BNH LA	MSGOK RO, L' MSGMSG	Yes, continue No, set to maximum
000003F6 000003F8 000003FA	1820 0620 4420 8228	000	000428	326 MSGOK 327 328	LR BCTR EX	R2, R0 R2, 0 R2, MSGMVC	Copy length to work register Minus-1 for execute Copy message to 0/P buffer
000003FE 00000402	4120 200A 4110 822E		00000A 00042E	329 330 331	LA LA	R2, 1+L' MSGCMD(, R2) R1, MSGCMD	Calculate true command length Point to true command
00000406 0000040A		000	000416	332 333 334 335	DC BZ	X' 83' , X' 12' , X' 0008' MSGRET	Issue Hercules Diagnose X'008' Return if successful
0000040E 00000410	1222 4780 8216	000	000416	336 337	LTR BZ	R2, R2 MSGRET	Is Diag8 Ry (R2) 0? an error occurred but coninue
00000414	0000			338 339 340	DC	Н' О'	CRASH for debugging purposes
00000416 0000041A	9802 821C 07F2	000	00041C	341 MSGRET 342	LM BR	RO, R2, MSGSAVE R2	Restore registers Return to caller
0000041C 00000428		00000437 000	000000	344 MSGSAVE 345 MSGMVC	DC MVC	3F' 0' MSGMSG(0), 0(R1)	Registers save area Executed instruction
0000042E 00000437	D4E2C7D5 D6C8405C 40404040 40404040			347 MSGCMD 348 MSGMSG 349	DC DC	C' MSGNOH * ' CL95' '	*** HERCULES MESSAGE COMMAND *** The message text to be displayed

ASMA Ver.	0. 7. 0 zvector-e6-1	13-convertt	odeci mal	(Zvector E6	VRR-g)		18 Jun 2024 18: 58: 17 Page	11
LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				351 ****** 352 * 353 *****	**************************************	**************************************	**************************************	
0000498	00020001 80000000			355 EOJPSV	N DC	OD' O' , X' 00020	000180000000', AD(0)	
00004A8	B2B2 8298		00000498	357 E0J	LPSWE	EOJPSW	Normal completion	
0000 4 <b>D</b> O	0000001 0000000			050 54110	NII DO		00010000000	
	00020001 80000000			359 FAILPS			000180000000', AD(X'BAD')	
00004C0	B2B2 82B0		000004B0	361 FAILTI	EST LPSWE	FAILPSW	Abnormal termination	
				363 ***** 364 *	******** Worki	************* ng Storage	*************	
				365 *****	*****	******	**************	
	00000000 00000000			367 CTLR0 368	DS DS	F F	CRO	
00004CC	00000002			370 371	LTORG	, =F' 2'	Literals pool	
00004D0 00004D4	0000138C 00000003 00000001			372 373 374		=A(E6TESTS) =XL4'3' =F'1'		
00004DC	0000 005F			375 376 377		=H' 0' =AL2(L' MSGMSG	G)	
				378 * 379	some	constants		
		00000400		380 K 381 PAGE	EQU	1024	One KB	
		00001000 00010000 00100000	00000001 00000001 00000001	382 K64 383 MB	EQU EQU EQU	(4*K) (64*K) (K*K)	Size of one page 64 KB 1 MB	
			00000	384 385				
		AABBCCDD 00000DD	00000001 00000001	386 REG2PA 387 REG2L0		X' AABBCCDD' X' DD'	Polluted Register pattern (last byte above)	

SMA Ver.	0. 7. 0 zvector-e6-1	3-convertt	odeci mal	(Zvector E6 VI	RR-g)		18 Jun 2024 18: 58: 17 Page	e 14
LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				451 *	<b>E6TES</b> * * * * * * *	T DSECT *******	**************************************	
0000000 0000004 0000006				454 E6TEST 455 TSUB 456 TNUM 457	DU	, A(0) H' 00' XL1' 00'	pointer to test Test Number	
0000007	00			458 CC 459 CCMASK 460	DC	HL1' 00' HL1' 00'	cc not expected CC mask	
0000009	40404040 40404040			461 OPNAME 462	DC	CL8' '	E6 name	
	00000000 00000000			463 RELEN 464 READDR 465	DC DC	A(0) A(0)	RESULT LENGTH expected result address	
				466 ** 467 * 468 * follow	ved by		l be here (from VRR_G macro)	
				469 * 470 *		te EXPECTED e byte sou		

ASMA Ver.	0. 7. 0 zvector-e6-	13-convertte	odeci mal	(Zvector E6 VRF	(- g)		18 Jun 2024 18: 58: 17 Page	15
LOC	OBJECT CODE	ADDR1	ADDR2	STM				
							**************************************	
				473 * Mac 474 *	ros to	o help build test	tables	
					R_G Mac	cro to help build	test tables *************	
					MACRO			
				478 479 .*	VRR_G	&I NST, &CC	&INST - instruction under test	
				480 . *			&CC - expected CC	
				481 .*			•	
							mask values for FAILED condition codes	
				483 &XCC(1) 484 &XCC(2)	SETA SETA	7 11	CC != 0 CC != 1	
				485 &XCC(3)	SETA	13	CC != 2	
				486 &XCC(4)	<b>SETA</b>	14	CC != 3	
				487	CDI A	o TNIIM		
					GBLA SETA	&TNUM &TNUM+1		
				490	<b>JLI</b> II	arrowr r		
				491	DS	OFD		
				492	USING	*, <b>R</b> 5	base for test data and test routine	
				493 494 T&TNUM	DC	A(X&TNUM)	address of test routine	
					DC	H' &TNUM	test number	
				496	DC	XL1' 00'		
					DC DC	HL1' &CC'	cc cc failed mask	
				498 499	DC	HL1' &XCC(&CC+1)'	cc rarred mask	
				<b>500</b>	DC	CL8' &INST'	instruction name	
				501	D.C.	1 (10)	1. 1	
				502 503 REA&TNUM	DC DC	A(16) A(RE&TNUM)	result length result address	
				504 . *	ЪС	A(MEXINUM	resurt address	
				<b>505</b> *			INSTRUCTION UNDER TEST ROUTINE	
					DS	OF	got VI govern	
				507 508	VL	V1, RE&TNUM	get V1 source	
				<b>509</b>	&I NST	V1	test instruction	
				510				
				511 512		R2, R0	exptract psw	
				512 513	ST	R2, CCPSW	to save CC	
				514	BR	R11	return	
				515	D.C.			
					DC DROP	0F P5		
				517 518	DWOL	NJ		
					MEND			

ASMA Ver.	0. 7. 0 zvector-e6-1	3- convertt	odeci mal	(Zvector E6 VR	R-g)		18 Jun 2024 18: 58: 17 Page 17
LOC	OBJECT CODE	ADDR1	ADDR2	STMI			
					****	******	*********
				545 *	F6 VR	R C tosts	*********
		00000000	000013BB	546 ********* 547 ZVE6TST	CSECT		· · · · · · · · · · · · · · · · · · ·
00001148				548	DS	0F	
				550	DDI MT	DATTA	
				550 551 *	PRINT	DAIA	
				552 * 553 *	E65F VRR C	VTP	TEST DECIMAL
				<b>554</b> *	VMM_U	followed by	
				555 * 55 <b>6</b>		v1 - 16 byte	source
				557 * 558 * VTP	VE	CTOR TEST DECIMAL	
				559 *		DUCINIL	
				560 * VTP si 561	•		
				562 * digits 563	valid, VRR G	, sign valid VTP,0	
00001148		00001140		<b>564</b> +	DS	OFD	
00001148 00001148	00001164	00001148		565+ 566+T1	USI NG DC	*, K5 A(X1)	base for test data and test routine address of test routine
0000114C 0000114E	0001 00			567+ 568+	DC DC	H' 1' XL1' 00'	test number
0000114F	00			<b>569</b> +	DC	HL1' 0'	cc
00001150 00001151	07 E5E3D740 40404040			570+ 571+	DC DC	HL1' 7' CL8' VTP'	cc failed mask instruction name
0000115C 00001160	00000010 0000117C			572+ 573+REA1	DC DC	A(16) A(RE1)	result length result address
	00001170			<b>574</b> +*			INSTRUCTION UNDER TEST ROUTINE
$00001164 \\ 00001164$	E710 5034 0006		0000117C	575+X1 576+	DS VL	OF V1, RE1	get V1 source
	E601 0000 005F B98D 0020			577+ 578+	VTP	V1 R2, R0	test instruction exptract psw
00001174	5020 8E9C		0000109C	<b>579</b> +	ST	R2, CCPSW	to save CC
00001178 0000117C	07FB			580+ 581+RE1	BR DC	R11 OF	return
0000117C	0000000 00000000			582+ 583	DROP DC	R5	00000000000000000000C' V1 source
	0000000 0000000C				ЪС	ALIO 0000000000	VI Source
				584 585	VRR_G	VTP, 0	
00001190 00001190		00001190		586+ 587+	DS USING	OFD	base for test data and test routine
00001190		00001130		588+T2	DC	A(X2)	address of test routine
00001194 00001196				589+ 590+	DC DC	H' 2' XL1' 00'	test number
00001197 00001198	00			591+ 592+	DC DC	HL1' 0' HL1' 7'	cc cc failed mask
00001199	E5E3D740 40404040			<b>593</b> +	DC	CL8' VTP'	instruction name
000011A4 000011A8	00000010 000011C4			594+ 595+REA2	DC DC	A(16) A(RE2)	result length result address
				<b>596</b> +*			INSTRUCTION UNDER TEST ROUTINE
000011AC				597+X2	DS	0F	

ASMA Ver.	0. 7. 0 zv	ector- e6- 13	3- convertto	odeci mal	(Zvector E6	VRR-g)		18 Jun 2024	18: 58: 17	Page	18
LOC	ОВЈЕСТ	CODE	ADDR1	ADDR2	STMT						
000011AC 000011B2	E710 5034 E601 0000	005F		000011C4	598+ 599+	VL VTP	V1, RE2 V1	get V1 source test instruction			
000011B8 000011BC 000011C0	B98D 0020 5020 8E90 07FB			0000109C	600+ 601+ 602+	ST BR	R2, R0 R2, CCPSW R11	exptract psw to save CC return			
000011C4 000011C4 000011C4	00000000	00000000			603+RE2 604+ 605	DC DROP DC	OF R5 XL16' 0000000000000	0000001234500000000D'	V1 source		
000011CC	00123450	000000D			606 607 * digi	its valid	sign invalid				
00001100					608	VRR_G	VTP, 1				
000011D8 000011D8			000011D8		609+ 610+	DS USING	OFD *. R5	base for test data and	test routi	ne	
000011D8 000011DC	000011F4 0003				611+T3 612+	DC DC	A(X3) H' 3'	address of test routine test number			
000011DE 000011DF	00 01				613+ 614+	DC DC	XL1' 00' HL1' 1'	cc			
000011E1 000011E1	0B E5E3D740	40404040			615+ 616+	DC DC	HL1' 11' CL8' VTP'	cc failed mask instruction name			
000011EC 000011F0	00000010 0000120C				617+ 618+REA3 619+*	DC DC	A(16) A(RE3)	result length result address INSTRUCTION UNDER TEST	ROUTINE		
000011F4 000011F4 000011FA	E710 9000 E601 0000			0000120C	620+X3 621+ 622+	DS VL VTP	0F V1, RE3 V1	get V1 source test instruction			
00001200 00001204 00001208	B98D 0020 5020 8E90 07FB			0000109C	623+ 624+ 625+	EPSW ST BR	R2, R0 R2, CCPSW R11	exptract psw to save CC return			
0000120C 0000120C 0000120C	00000000	0000000			626+RE3 627+ 628	DC DROP DC	OF R5	000000000000000000000000000000000000000	V1 source		
00001200	00000000				629			000000000000000000000000000000000000000	VI Source		
00001220					630 631+	VRR_G DS	OFD				
00001220 00001220	0000123C		00001220		632+ 633+T4	USI NG DC	*, <b>R5</b> <b>A(X4)</b>	base for test data and address of test routine		ne	
$\begin{array}{c} 00001224 \\ 00001226 \\ 00001227 \end{array}$	0004 00 01				634+ 635+ 636+	DC DC DC	H' 4' XL1' 00' HL1' 1'	test number			
00001228 00001229	0B E5E3D740	40404040			637+ 638+	DC DC	HL1' 11' CL8' VTP'	cc failed mask instruction name			
00001234 00001238	00000010 00001254				639+ 640+REA4 641+*	DC DC	A(16) A(RE4)	result length result address INSTRUCTION UNDER TEST	ROUTINE		
0000123C 0000123C 00001242	E710 5034 E601 0000			00001254	642+X4 643+ 644+	DS VL VTP	0F V1, RE4 V1	get V1 source test instruction			
00001248 0000124C	B98D 0020 5020 8E90			0000109C	645+ 646+	EPSW ST	R2, R0 R2, CCPSW	exptract psw to save CC			
00001250 00001254 00001254	07FB				647+ 648+RE4 649+	BR DC DROP	R11 OF R5	return			
00001254	$\begin{array}{c} 00000000 \\ 00123450 \end{array}$				650	DC		00000012345000000000'	V1 source		

ASMA Ver.	0. 7. 0 zvector- e6-	13-convertt	odeci mal	(Zvector E6 V	RR-g)		18 Jun 2024 18: 58: 17 Page	19
LOC	OBJECT CODE	ADDR1	ADDR2	STMI				
				651				
				652 * a dig 653	git inva VDD C	lid, sign valid VTP,2		
00001268				65 <b>4</b> +	DS	OFD		
00001268		00001268		<b>655</b> +	USING	*, <b>R</b> 5	base for test data and test routine	
00001268	00001284			656+T5	DC	A(X5)	address of test routine	
0000126C 0000126E	0005 00			657+ 658+	DC DC	H' 5' XL1' 00'	test number	
000126F	02			<b>659</b> +	DC	HL1' 2'	cc	
00001270	OD ESEODE 40 40 40 40 40			660+	DC	HL1' 13'	cc failed mask	
0001271 000127C	E5E3D740 40404040 00000010			661+ 662+	DC DC	CL8' VTP' A(16)	instruction name result length	
0001270	0000010 0000129C			663+REA5	DC	A(RE5)	result address	
				664+*	The Co		INSTRUCTION UNDER TEST ROUTINE	
00001284 00001284	E710 5034 0006		0000129C	665+X5 666+	DS VL	0F V1, RE5	get V1 source	
000128A	E601 0000 005F		00001630	667+	VL VTP	VI, KES VI	test instruction	
00001290	B98D 0020			668+	<b>EPSW</b>	R2, RO	exptract psw	
00001294 00001298	5020 8E9C 07FB		0000109C	669+ 670+	ST BR	R2, CCPSW R11	to save CC	
00001298 0000129C	U/FD			671+RE5	DC	OF	return	
000129C				672+	DROP	<b>R5</b>		
000129C	00000000 0FF00000			673	DC	XL16' 000000000	FF0000000000000000000C' V1 source	
000012A4	00000000 0000000C			674				
				675		VTP, 2		
000012B0		00001000		676+	DS	OFD		
000012B0 000012B0	000012CC	000012B0		677+ 678+T6	USI NG DC	*, K5 A(X6)	base for test data and test routine address of test routine	
000012B4	0006			679+	DC	H' 6'	test number	
000012B6	00			680+	DC	XL1' 00'		
000012B7 000012B8	02 on			681+ 682+	DC DC	HL1' 2' HL1' 13'	cc cc failed mask	
	E5E3D740 40404040			683+	DC	CL8' VTP'	instruction name	
000012C4				684+	DC	A(16)	result length	
000012C8	000012E4			685+REA6 686+*	DC	A(RE6)	result address INSTRUCTION UNDER TEST ROUTINE	
00012CC				687+X6	DS	<b>0F</b>	INSTRUCTION UNDER TEST ROUTINE	
000012CC	E710 5034 0006		000012E4	688+	VL	V1, RE6	get V1 source	
000012D2 000012D8	E601 0000 005F B98D 0020			689+ 690+	VTP FDSW	V1 R2, R0	test instruction exptract psw	
000012DC	5020 8E9C		0000109C	691+	ST	R2, CCPSW	to save CC	
00012E0	07FB			692+	BR	R11	return	
000012E4 000012E4				693+RE6 694+	DC DROP	OF R5		
00012E4	F0F00000 00000000			695	DKOP		00000000123450000000F' V1 source	
000012EC								
				696 697 * a dig 698	git inva VRR G	lid, sign inva VTP, 3	lid	
00012F8		00001070		699+	DS	OFD		
00012F8 00012F8	00001314	000012F8		700+ 701+T7	USI NG DC	*, R5 A(X7)	base for test data and test routine address of test routine	
00012F6	0007			701+17 702+	DC DC	H' 7'	test number	
00012FE	00			703+	DC	XL1' 00'		
000012FF	03			704+	DC	HL1'3'	cc	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI						
00001300	0E			705+	DC	HL1' 14'	cc failed mask			
00001301	E5E3D740 40404040			<b>706</b> +	DC	CL8' VTP'	instruction name			
0000130C	00000010			707+	DC	A(16)	result length			
00001310	0000132C			708+REA7	DC	A(RE7)	result address			
00001014				709+*	D.C.	O.E.	INSTRUCTION UNDER TEST	ROUTINE		
00001314	E710 5004 0000		00001000	710+X7	DS	OF				
00001314	E710 5034 0006		0000132C	711+	VL VTD	V1, RE7	get V1 source			
0000131A 00001320	E601 0000 005F B98D 0020			712+ 713+	VTP EPSW	V1 R2, R0	test instruction			
00001320	5020 8E9C		0000109C	713+ 714+	EPSW ST	R2, CCPSW	exptract psw to save CC			
00001324	07FB		00001030	714+ 715+	BR	R11	return			
00001328 0000132C	0/IB			716+ <b>RE</b> 7	DC	OF	1 ecui ii			
0000132C				717+	DROP	R5				
0000132C	0000000 0FF00000			718	DC		00000FF0000000000000000000000000000000	V1 source		
00001334	0000000 00000009			710	DU	ALIO GOOG		VI Source		
00001001				719						
				720	VRR G	VTP, 3				
00001340				721+	DS	OFD				
00001340		00001340		722+	USING		base for test data and		ne	
00001340	0000135C			723+T8	DC	A(X8)	address of test routine	,		
00001344	0008			<b>724</b> +	DC	H' 8'	test number			
00001346	00			<b>725</b> +	DC	XL1' 00'				
00001347	03			<b>726</b> +	DC	HL1'3'	cc			
00001348	<u>OE</u>			727+	DC	HL1' 14'	cc failed mask			
00001349	E5E3D740 40404040			728+	DC	CL8' VTP'	instruction name			
00001354	00000010			729+	DC	A(16)	result length			
00001358	00001374			730+REA8	DC	A(RE8)	result address	DOUBLINE		
00001256				731+*	DC	OE	INSTRUCTION UNDER TEST	ROUIINE		
0000135C 0000135C	E710 5034 0006		00001374	732+X8 733+	DS VL	0F V1, RE8	got V1 source			
00001350	E601 0000 005F		00001374	733+ 734+	VL VTP	VI, REO V1	get V1 source test instruction			
00001362	B98D 0020			73 <del>4</del> + 735+	EPSW	R2, R0	exptract psw			
	5020 8E9C		0000109C	736+	ST	R2, CCPSW	to save CC			
00001370			00001000	737+	BR	R11	return			
00001374	3.12			738+RE8	DC	0F				
00001374				739+	DROP	<b>R5</b>				
	F0F00000 00000000			740	DC	XL16' F0F0	000000000000012345000000002'	V1 source		
0000137C	00123450 00000002									
				741						
00001384				742	DC		END OF TABLE			
00001388	0000000			743	DC	F' 0'				
				744 *						
					of poin	nters to i	ndividual load test			
00001000				746 *	DC	OE				
0000138C				747 E6TESTS	DS DTTAD	OF				
0000138C				748 749+TTABLE	PTTAB DS	LE OF				
0000138C	00001148			749+11ABLE 750+	DC DC	A(T1)	address of test			
00001380	00001148			750+ 751+	DC	A(T2)	address of test			
00001390	00001130 000011D8			751+ 752+	DC	A(T3)	address of test			
00001394	00001120			753+	DC	A(T4)	address of test			
0000139C	00001268			<b>754</b> +	DC	A(T5)	address of test			
000013A0	000012B0			755+	DC	A(T6)	address of test			
000013A4				<b>756</b> +	DC	A(T7)	address of test			
000013A8	00001340			<b>757</b> +	DC	<b>A(T8)</b>	address of test			
				<b>758</b> +*						

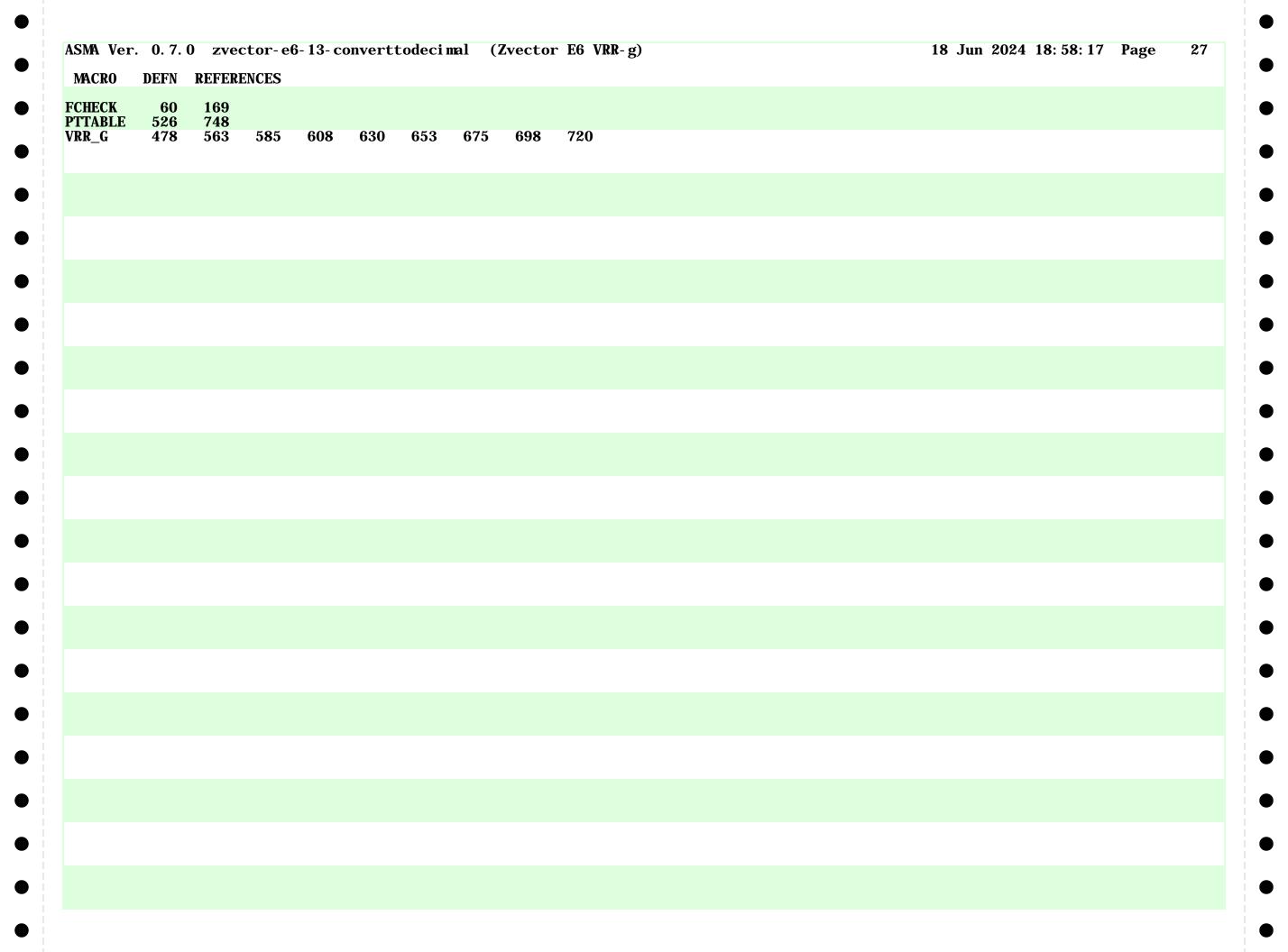
	0. 7. 0 zvector- e6				o vrr-g)			18 Jun 2024 18: 58: 17	Page	21
LOC	OBJECT CODE	ADDR1	ADDR2	STMI						
00013AC 00013B0	0000000 0000000			759+ 760+	DC DC	A(0) A(0)	END OF TABLE			
0013B4 0013B8	0000000 0000000			761 762 763	DC DC	F' 0' F' 0'	END OF TABLE			
001020				, 00	20	1 0				

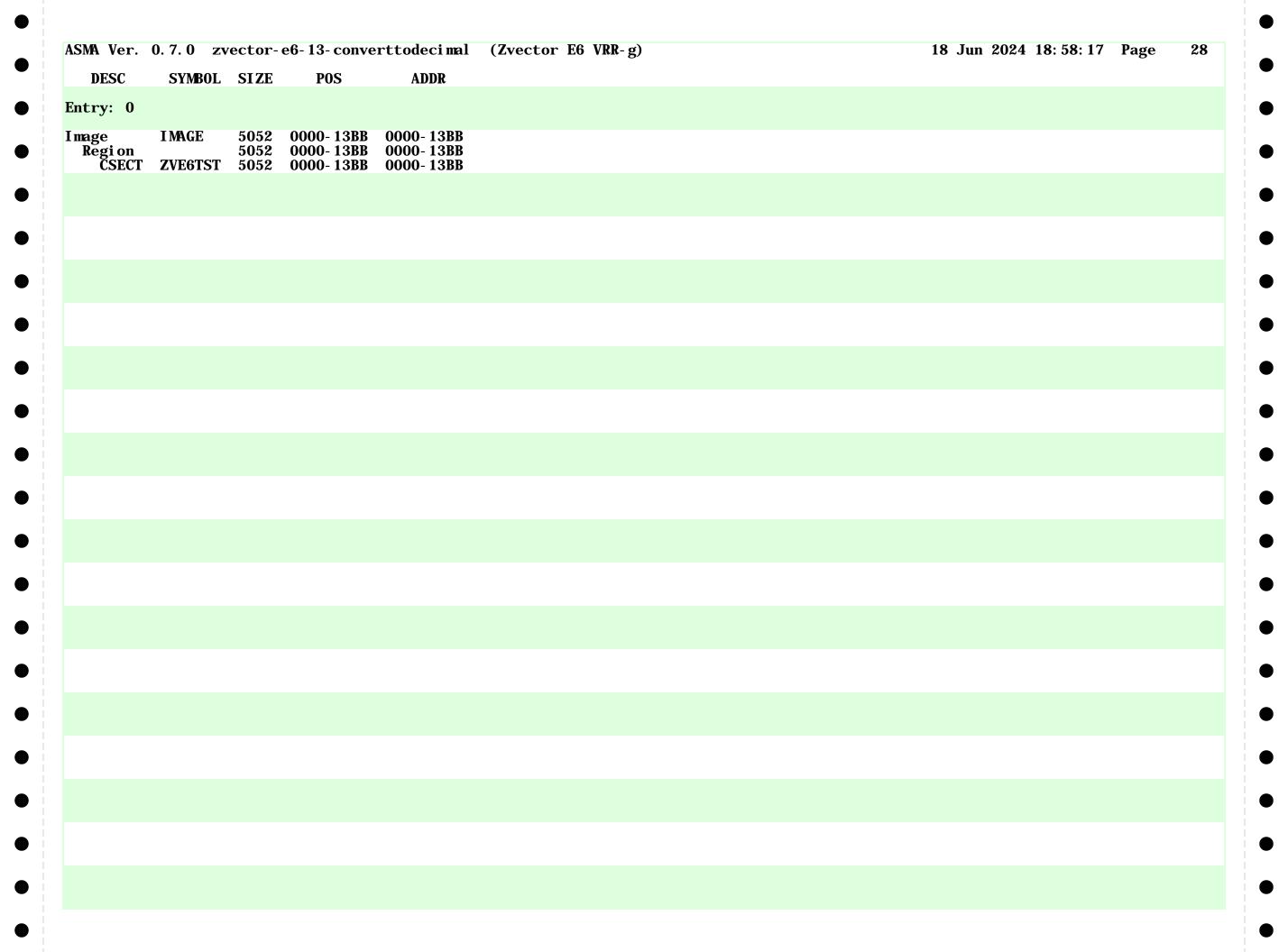
SMA Ver.	0. 7. 0 zvector-e6	3-13-convertt	odeci mal	(Zvector E6	VRR-g)	18 Jun 2024 18: 58: 17 Page	22
LOC	OBJECT CODE	ADDR1	ADDR2	STMI			
				765 *****	*****	**********************	•
				766 *	Regis	ster equates	
				767 *****	*****	****** <sup>*</sup> *****************************	•
		0000000	0000001	760 DO	EOU		
		0000000 0000001	00000001 00000001	769 RO 770 R1	EQU EQU	<b>0</b> 1	
		0000002	0000001	771 R2	EQU	2 3	
		$00000003 \\ 00000004$	00000001 00000001	772 R3 773 R4	EQU FOII	<b>3</b> <b>4</b>	
		0000005	0000001	774 R5	EQU	5	
		0000006 0000007	00000001 00000001	775 R6 776 R7	EQU	6 7	
		0000007	00000001	770 R7	EQU	8	
		00000009	00000001	778 R9	EQU	8 9	
		0000000A 0000000B	00000001 00000001	779 R10 780 R11	EQU EQU	10 11	
		000000C	0000001	781 R12	EQU EQU	10 11 12 13 14	
		0000000D 0000000E	00000001 00000001	782 R13 783 R14	EQU EQU	13 14	
		000000E	00000001	784 R15	EQU	15	
				786 *****		********************	•
				787 * 788 *****	<b>Regis</b>	ster equates ************************************	•
				700			
		0000000	00000001	790 VO	EOH		
		00000001			r.wu	0	
			00000001	791 V1	EQU EQU		
		0000002	0000001	792 V2	EQU EQU	1 2	
		0000002 0000003 0000004		792 V2 793 V3 794 V4	EQU EQU EQU EQU	1	
		00000002 00000003 00000004 00000005	00000001 00000001 00000001 00000001	792 V2 793 V3 794 V4 795 V5	EQU EQU EQU EQU EQU	1 2 3 4 5	
		0000002 0000003 0000004 0000005 0000006	00000001 00000001 00000001 00000001	792 V2 793 V3 794 V4 795 V5 796 V6	EQU EQU EQU EQU EQU EQU	1 2 3 4 5 6	
		0000002 0000003 00000004 00000005 00000006 00000007 00000008	00000001 00000001 00000001 00000001 000000	792 V2 793 V3 794 V4 795 V5 796 V6 797 V7 798 V8	EQU EQU EQU EQU EQU EQU EQU	1 2 3 4 5 6 7 8	
		0000002 0000003 0000004 0000005 0000006 0000007 0000008 0000009	0000001 00000001 00000001 00000001 000000	792 V2 793 V3 794 V4 795 V5 796 V6 797 V7 798 V8 799 V9	EQU EQU EQU EQU EQU EQU EQU EQU	1 2 3 4 5 6 7 8 9	
		0000002 0000003 0000004 0000005 0000006 0000007 0000008 0000009 0000000A	0000001 0000001 0000001 0000001 0000001 000000	792 V2 793 V3 794 V4 795 V5 796 V6 797 V7 798 V8 799 V9 800 V10 801 V11	EQU EQU EQU EQU EQU EQU EQU EQU EQU	1 2 3 4 5 6 7 8 9 10	
		0000002 0000003 0000004 0000005 0000006 0000007 0000008 0000009 0000000A 0000000B	0000001 0000001 0000001 0000001 0000001 000000	792 V2 793 V3 794 V4 795 V5 796 V6 797 V7 798 V8 799 V9 800 V10 801 V11 802 V12	EQU	1 2 3 4 5 6 7 8 9 10 11	
		0000002 0000003 0000004 0000005 0000006 0000007 0000008 0000009 0000000A	0000001 0000001 0000001 0000001 0000001 000000	792 V2 793 V3 794 V4 795 V5 796 V6 797 V7 798 V8 799 V9 800 V10 801 V11	EQU	1 2 3 4 5 6 7 8 9 10 11 12	
		0000002 0000003 0000004 0000005 0000006 0000008 0000009 000000A 000000B 000000C 000000D 000000E	00000001 00000001 00000001 00000001 000000	792 V2 793 V3 794 V4 795 V5 796 V6 797 V7 798 V8 799 V9 800 V10 801 V11 802 V12 803 V13 804 V14 805 V15	EQU	1 2 3 4 5 6 7 8 9 10 11 12 13 14	
		0000002 0000003 0000004 0000005 00000006 00000008 00000009 0000000A 0000000B 0000000C 0000000D 0000000E 0000000F	0000001 0000001 0000001 0000001 0000001 000000	792 V2 793 V3 794 V4 795 V5 796 V6 797 V7 798 V8 799 V9 800 V10 801 V11 802 V12 803 V13 804 V14 805 V15 806 V16	EQU	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
		0000002 0000003 0000004 0000005 0000006 0000007 0000008 0000009 0000000B 0000000C 0000000D 000000D 000000F 00000011 00000012	0000001 0000001 0000001 0000001 0000001 000000	792 V2 793 V3 794 V4 795 V5 796 V6 797 V7 798 V8 799 V9 800 V10 801 V11 802 V12 803 V13 804 V14 805 V15 806 V16 807 V17 808 V18	EQU	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17	
		0000002 0000003 0000004 0000005 0000006 0000007 0000008 0000009 0000000A 0000000B 0000000C 0000000D 0000000E 0000000F 00000010 00000011	0000001 0000001 0000001 0000001 0000001 000000	792 V2 793 V3 794 V4 795 V5 796 V6 797 V7 798 V8 799 V9 800 V10 801 V11 802 V12 803 V13 804 V14 805 V15 806 V16 807 V17	EQU	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	

	0. 7. 0 zvector- e6				vkk-g)			18 Jun 2024	16: 58: 17	rage	23
LOC	OBJECT CODE	ADDR1	ADDR2	STMT							
		00000016 00000017	00000001 00000001	812 V22 813 V23	EQU	22 23					
		00000018	00000001	814 V24	EQU	24					
		00000019 0000001A	00000001 00000001	816 V26	EQU EQU	25 26					
		0000001B	00000001 00000001	817 V27 818 V28	EQU FOU	27 28					
		0000001D 0000001E	00000001	819 V29	EQU EQU EQU EQU EQU EQU EQU EQU	22 23 24 25 26 27 28 29 30 31					
		0000001E	00000001	821 V31	EQU	31					
				822 823	END						

SYMBOL	ТҮРЕ	VALUE	LENGTH	DEFN	REFE	RENCE	S													
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EGI N	I	00000200	2		115	146	147	148												
CECHNIA	U	00000007	1	458	249	050														
CFOUND	X	000010A4	1	431	236	<b>256</b>														
CCMASK	U	00000008	1	459	216															
CCMSG	U	0000030A	1	229	223															
CCPRTEXP	C	0000104B	1	411	253															
CCPRTGOT	C	0000105B	1	414	260															
CCPRTLINE	<u>C</u>	00001008	16	406	416	<b>263</b>														
CCPRTLNG	U	00000055	1	416	262															
CCPRTNAME	C	00001035	8	409	246															
CCPRTNUM	C	00001018	3	407	<b>244</b>															
CCPSW	F	0000109C	4	430	233	<b>579</b>	601	<b>624</b>	646	669	691	714	<b>736</b>							
CTLRO	F	000004C4	4	367	160	161	162	163												
DECNUM	C	00001089	16	426	<b>241</b>	<b>243</b>	<b>250</b>	<b>252</b>	257	259										
E6TEST	4	00000000	28	<b>454</b>	211															
E6TESTS	F	0000138C	4	747	202															
E <b>DIT</b>	X	0000105D	18	421	242	251	258													
ENDTEST	U	00000396	1	281	207															
E <b>OJ</b>	I	000004A8	4	357	195	284														
EOJPSW	D	00000498	8	355	357															
FAI LCONT	U	00000386	1	271	266															
FAI LED	F	00001000	4	397	273	282														
FAILPSW	$\overline{\mathbf{D}}$	000004B0	8	359	361															
FAILTEST	Ī	000004C0	4	361	285															
FB0001	F	00000288	8	179	183	184	186													
MAGE	1	00000000	5052	0																
K	Ū	00000400	1	380	381	382	383													
K64	Ü	00010000	<u>-</u>	382		002														
MB	Ŭ	00100000	1	383																
MSG	Ĭ	000003E0	4	317	194	300														
MSGCMD	Ĉ	0000042E	9	347	330	331														
MSGMSG	č	00000422	95	348	324	345	322													
MSGMVC	Ĭ	00000428	6	345	328	010	0~~													
MSGOK	Ť	00000428 000003F6	2	326	323															
MSGRET	Ť	00000310	$\tilde{\tilde{4}}$	341	334	337														
MSGSAVE	F	00000410 0000041C	4	344	320	341														
NEXTE6	II.	0000041C 000002DC	1	204	221	276														
OPNAME	Č	00000200	8	461	246	210														
PAGE	Ü	0000009	4	381	<b>~40</b>															
PRT3	C	00001000	1 18	381 424	242	243	244	951	252	253	258	259	260							
	U	00001073		769	242 109	243 160		251		253 186		259 192	200 209	969	979	979	200	301	317	
RO	U	0000000	1	709			163	183	185		187	623	645	262	272	273		<b>301</b>	317	
D1	TT	0000001	1	770	320	322	324	326	341	578 224	600			668	690	713	735			
R1	U	00000001	1	770	193	216	217	218	233	234	235	236	263	282	283	331	345			
R10	U	0000000A	1	779	148	157	158	gno	COF	647	670	COO	715	707						
R11	U	0000000B	1	780 781	213	214	580	602	625	647	670	692	715	737						
R12	U	000000C	I ·	781	202	205	220	275												
R13	U	000000D	I 1	782																
	U	000000E	1	783	004	004	004	005												
R14	U	000000F	1	784	<b>264</b>	294	304	<b>305</b>												
R14 R15	<b>T7</b>	$\alpha \alpha $	0	437																
R14 R15 R1FUDGE	X	000010A8	8	4 4 4																
R14 R15 R1FUDGE R1OUTPUT	F	000010E0	8	441	40:	0.40	0 4 4	0.40	0.40	0	0	0	~~~	000	000	001	0.1.0	000	000	
R14 R15 R1FUDGE R1OUTPUT				441 771	194	240	241	248	249	250	255	256	257	299	300	301		320	326	
R14 R15 R1FUDGE	F	000010E0	8		327	328	330	336	341	342	<b>578</b>	256 579	257 600	299 601	300 623	301 624		320 646	326 668	
R14 R15 R1FUDGE R1OUTPUT R2	F U	000010E0 00000002	8	771																
R14 R15 R1FUDGE R1OUTPUT	F	000010E0	8		327	328	330	336	341	342	<b>578</b>									

SYMB0L	TYPE	VALUE	LENGTH	DEFN	REFE	RENCE	S													
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6	U	0000006	1	775	077	001	700	, , ,	<i>  ~~</i>	733										
7	Ū	0000007	$\bar{1}$	776																
8	U	8000000	1	777	146	150	151		154											
9	U	00000009	1	778	147	154	155	157												
E1	<u>F</u>	0000117C	4	581	573	576														
E2	F	000011C4	4	603	595	598														
E3	F	0000120C	4	626	618	621														
E4	F	00001254	4	648	640	643														
E5 E6	F F	0000129C 000012E4	4	671 693	663 685	666 688														
E7	F	000012E4 0000132C	4	716	708	711														
E8	F	00001326	4	738	<b>730</b>	733														
EA1	Ā	00001374	4	573	700	700														
EA2	Ä	00001100 000011A8	4	595																
EA3	Ā	000011F0	$ar{4}$	618																
EA4	A	00001238	$\overline{4}$	640																
EA5	A	00001280	4	663																
EA6	A	000012C8	4	685																
EA7	A	00001310	4	708																
EA8	A	00001358	4	730																
EADDR EGOLOW	A	00000018	4	464																
EG2LOW	U	000000DD	1	387																
EG2PATT ELEN	U	AABBCCDD 0000014	4	386 463																
PTDWSAV	A D	00000014 000003D0	8	310	299	301														
PTERROR	Ĭ	000003D0 000003A4	4	294	<b>264</b>	301														
PTSAVE	F	000003711 000003C4	4	307	294	304														
PTSVR5	F	000003C8	4	308	295	303														
KL0001	Ū	00000054	Ī	176	192															
KT0001	C	0000022A	26	173	176	193														
VOLDPSW	U	00000140	0	111																
1	A	00001148	4	<b>566</b>	<b>750</b>															
2	A	00001190	4	588	751															
3	A	000011D8	4	611	752															
4	A	00001220	4	633	<b>753</b>															
5	A	00001268	4	656	754															
6 7	A A	000012B0 000012F8	4	678 701	755 756															
/ 8	A A	00001218	4	701 723	756 757															
ESTCC	I	00001340	4	223	218															
ESTING	F	00001004	4	398	210															
NUM	Ĥ	00000004	$\dot{f z}$		240															
SUB	Ā	00000000	4	455	213															
TABLE	F	0000138C	4	749																
0	U	00000000	1	790																
1	U	0000001	1	791	576 734	577	598	599	621	622	643	644	666	667	688	689	711	712	733	
10	II	000000A	1	800	734															
11	II	0000000A	1	801																
12	II	0000000B	1	802																
13	Ŭ	0000000C	1	803																
14	Ŭ	000000E	1	804																
15	Ū	000000F	1	805																
16	TI	0000010	1	806																





SMA Ver. 0.7.0	zvector-e6-13-converttodeci mal FILE NAME	(Zvector E6 VRR-g)		18 Jun 2024 18:	58: 17 I	Page	29
	PILE NAME 29/sharedvfp/tests/zvector-e6-14-	testdecimal.asm					
* NO ERRORS FOU	JND **						