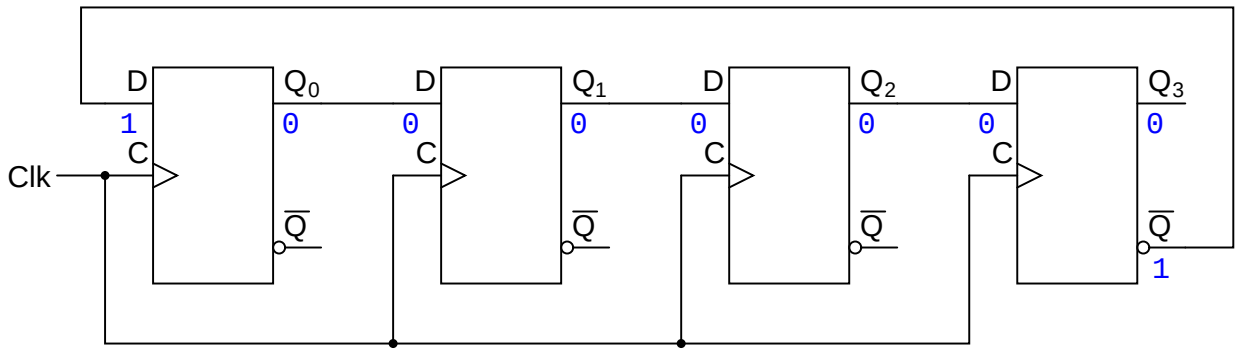
Question 1

Animation: Johnson ring counter

This question consists of a series of images (one per page) that form an animation. Flip the pages with your fingers to view this animation (or click on the "next" button on your viewer) frame-by-frame.

The following animation shows a 4-bit Johnson ring counter circuit. Watch what happens as the clock signal oscillates. Here are some things to look for:

- Note when the logic state at each flip-flop input gets sent to the Q output.
- Why do you think this is called a "ring" counter circuit?



Clock

V_{DD}

Gnd

Q_0

V_{DD}

Gnd

Q_1

V_{DD}

Gnd

Q_2

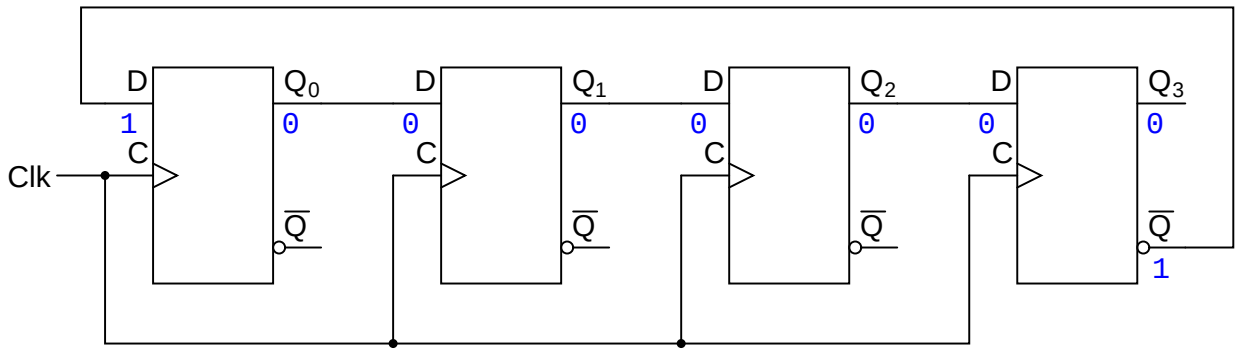
V_{DD}

Gnd

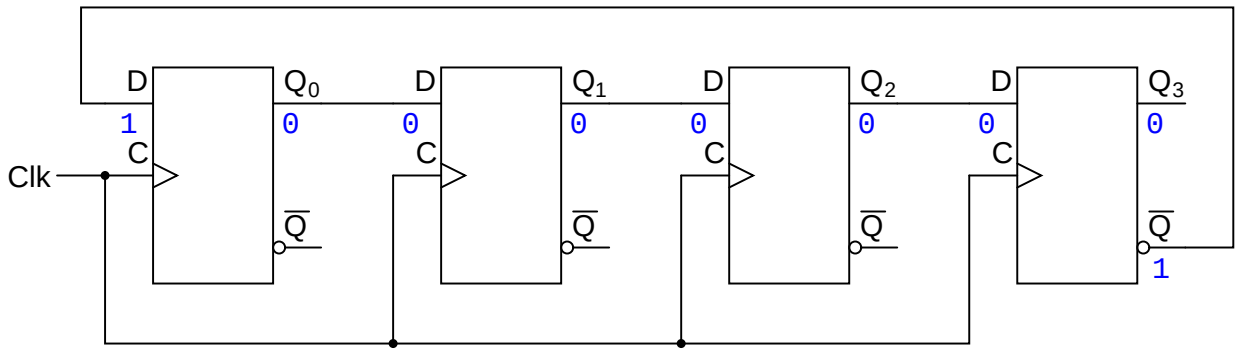
Q_3

V_{DD}

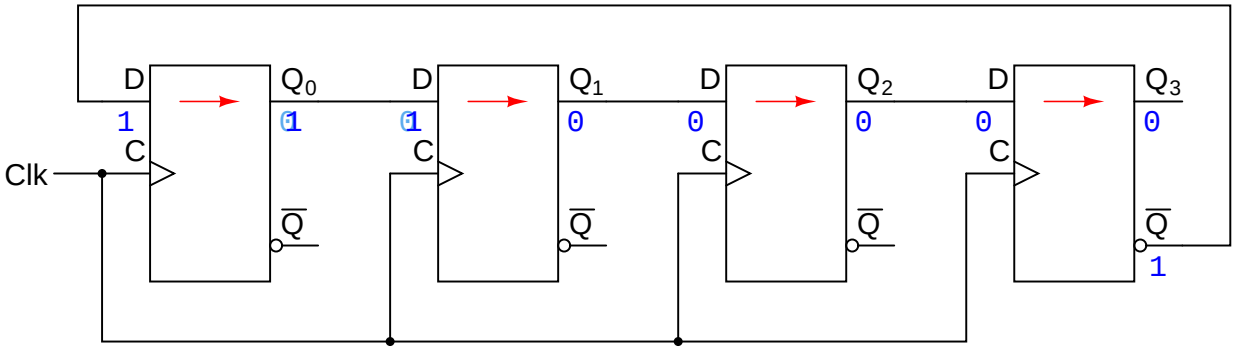
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
1
0
0
0
0
0
0
0
C
C
C
C
Clk
Q
Q
Q
Q
1

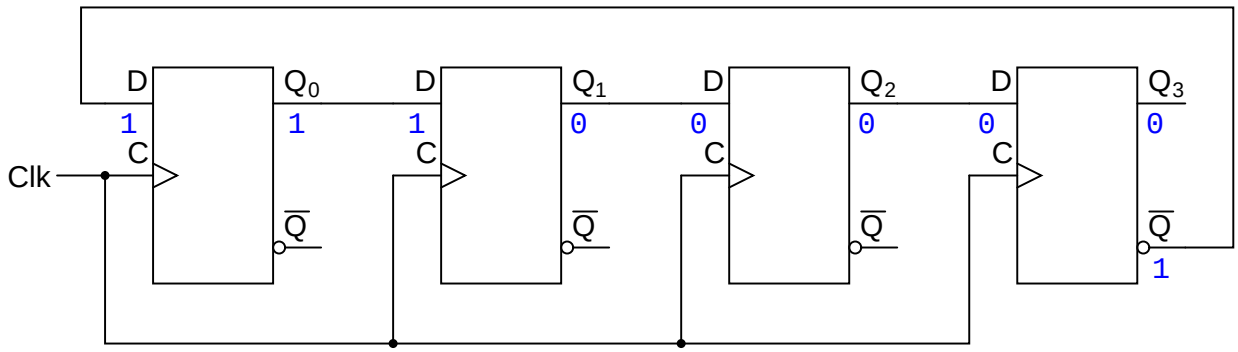
Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
1
0
0
0
0
0
0
0
C
C
C
C
Clk
Q
Q
Q
Q
1

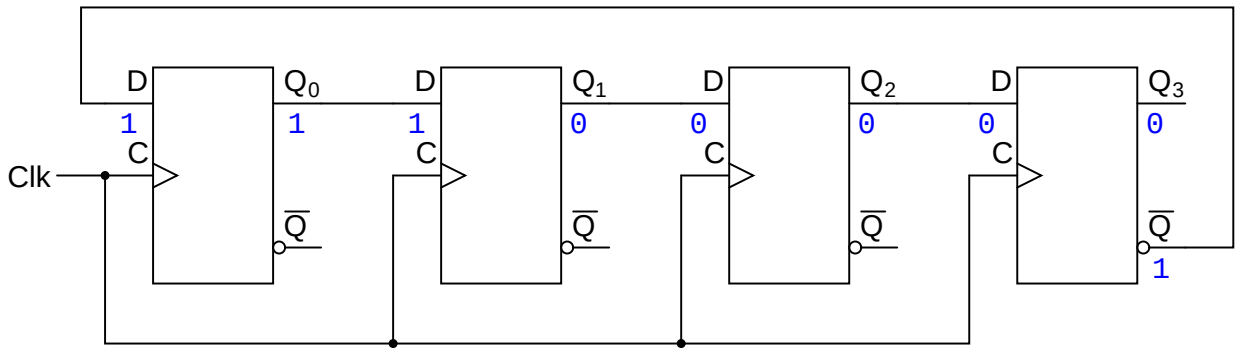
Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd

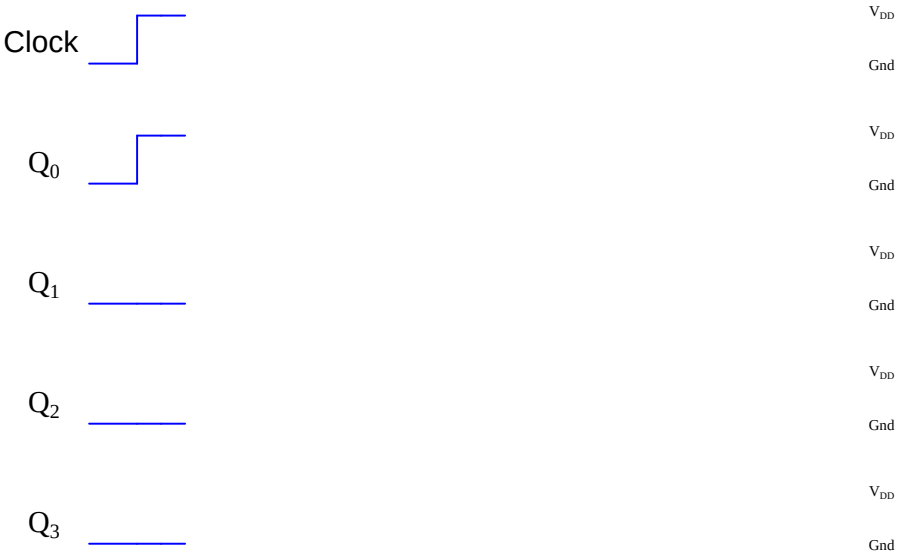

D
Q0
D
Q1
D
Q2
D
Q3
1
0
0
0
0
C
C
C
C
Clk
Q
Q
Q
Q
1

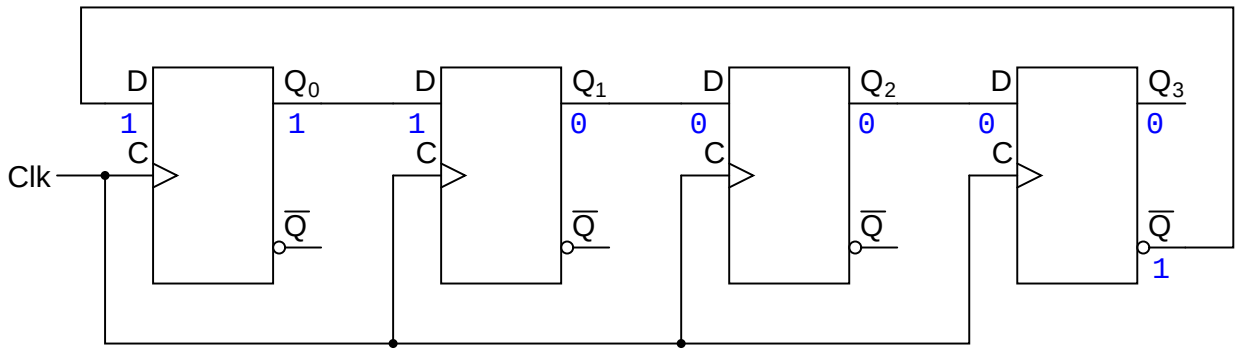
Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd

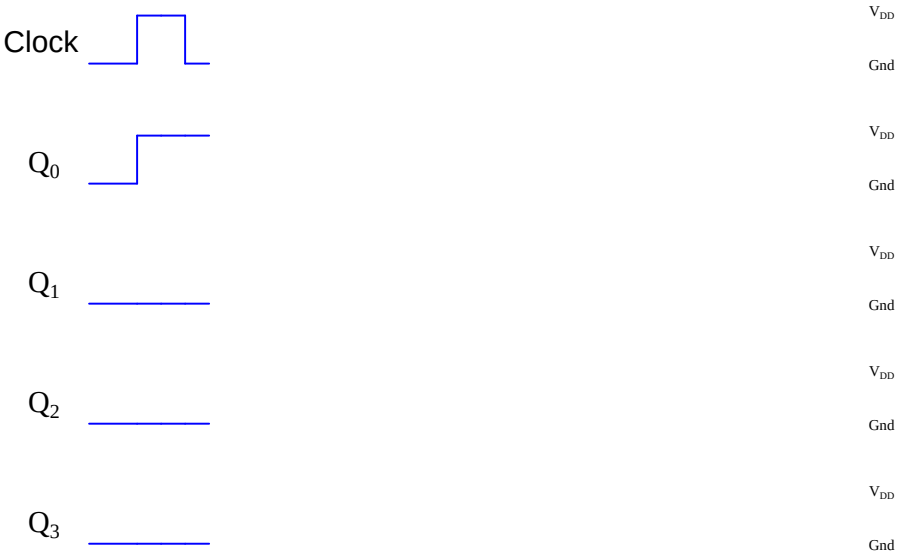

D
Q0
D
Q1
D
Q2
D
Q3
1
1
1
0
0
0
0
0
C
C
C
C
Clk
Q
Q
Q
Q
1

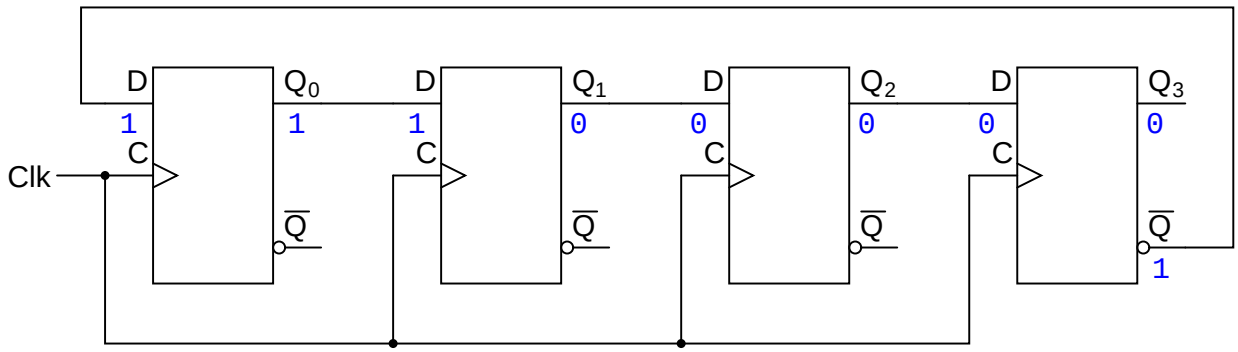
Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
1
1
1
0
0
0
0
0
C
C
C
C
Clk
Q
Q
Q
Q
1

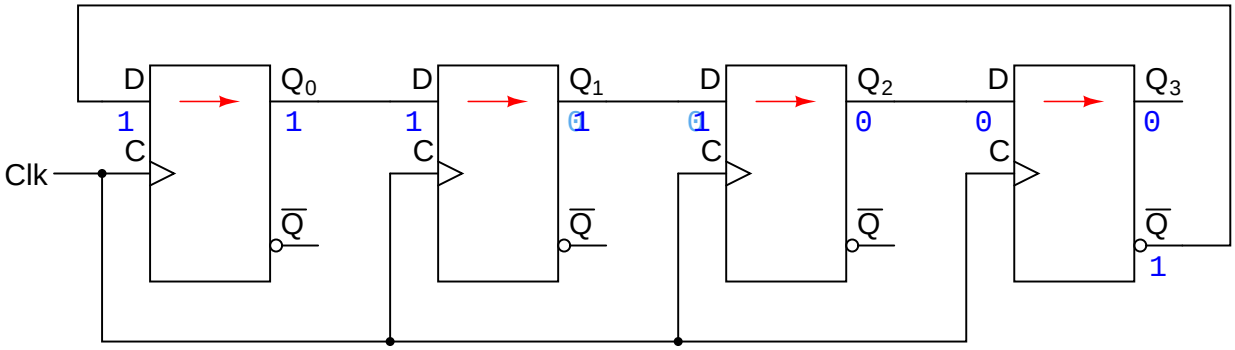

Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd

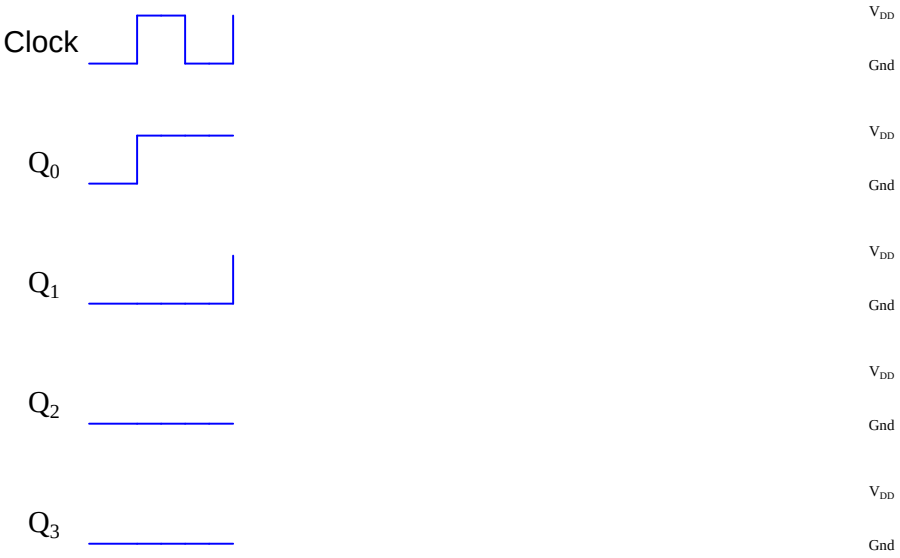

D
Q0
D
Q1
D
Q2
D
Q3
1
1
1
0
0
0
0
0
C
C
C
C
Clk
Q
Q
Q
Q
1

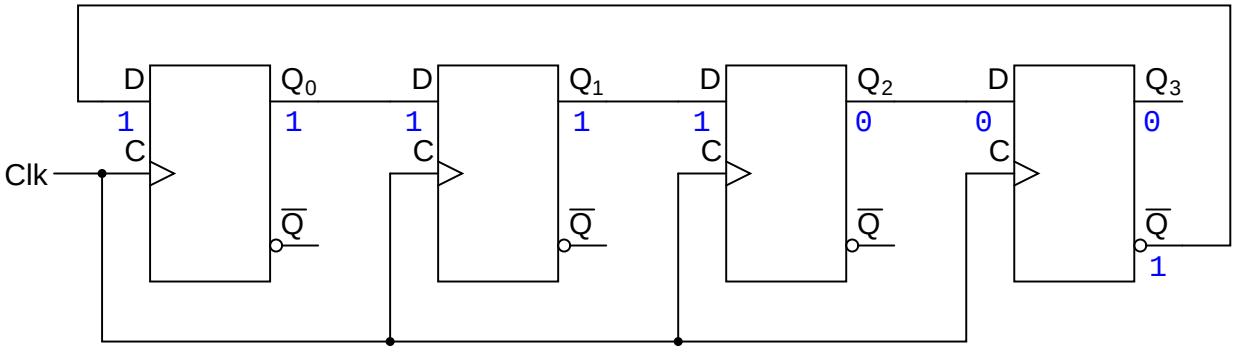

Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
1
1
1
0
0
0
0
0
C
C
C
C
Clk
Q
Q
Q
Q
1

Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
1
1
1
1
0
0
0
C
C
C
C
Clk
Q
Q
Q
Q
1


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
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Q2
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Q3
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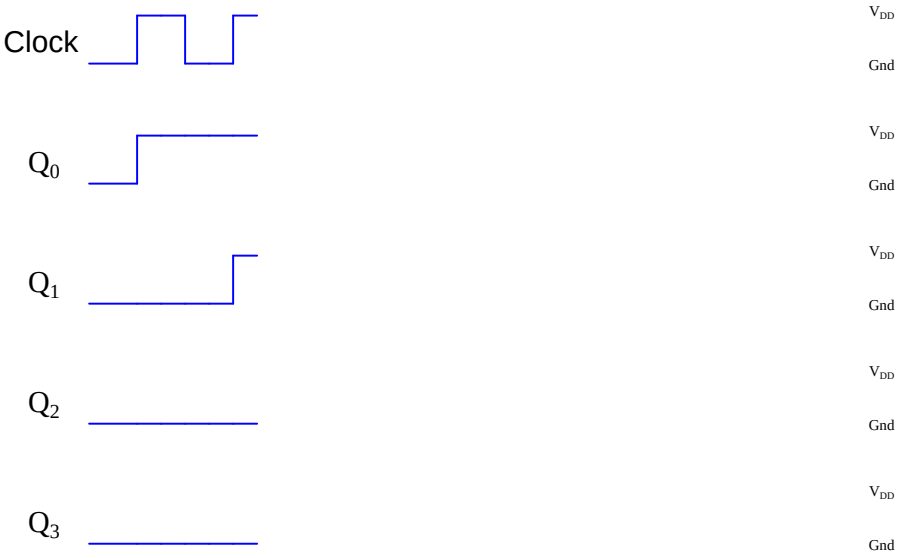
C
C
C
C
Clk
Q
Q
Q
Q
1


Clock
Q0
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Q3
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Gnd
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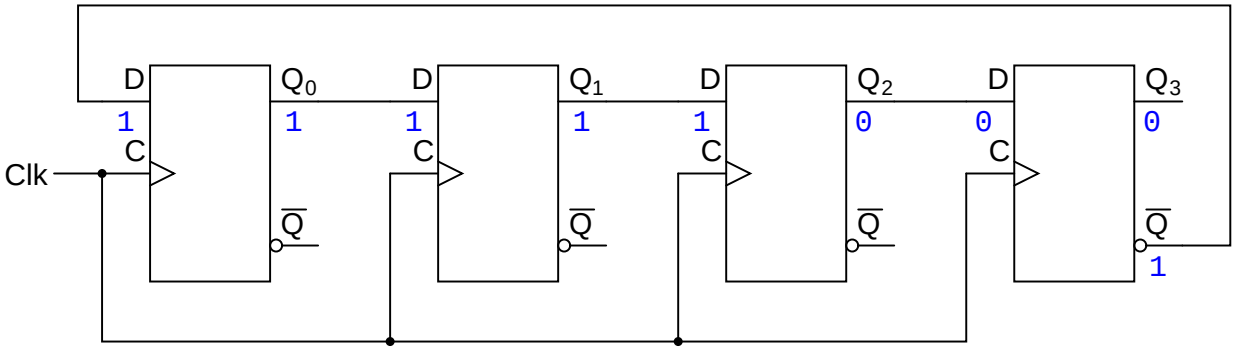
Gnd


D
Q0
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Q
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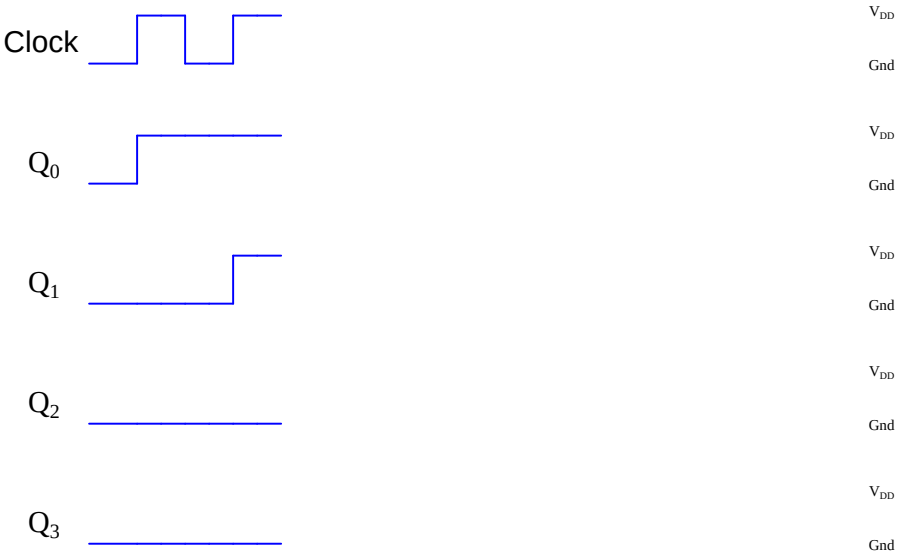
Clock
Q0
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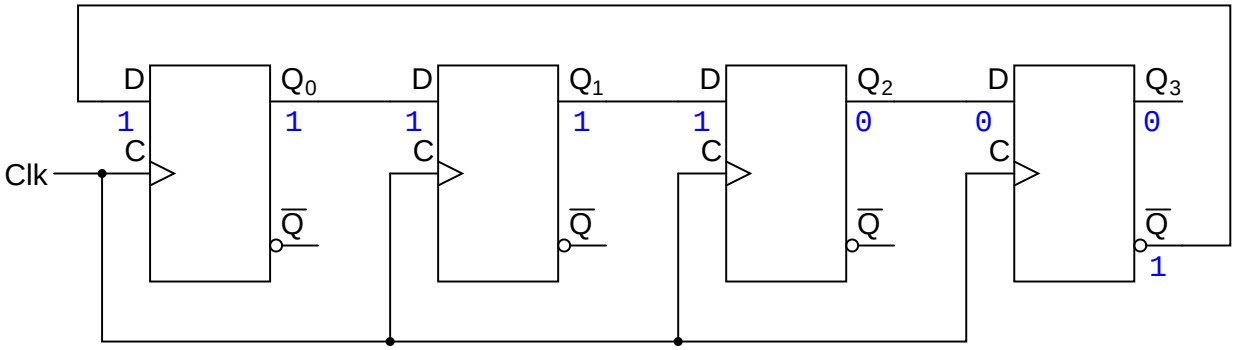
D
Q0
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Clk
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Q
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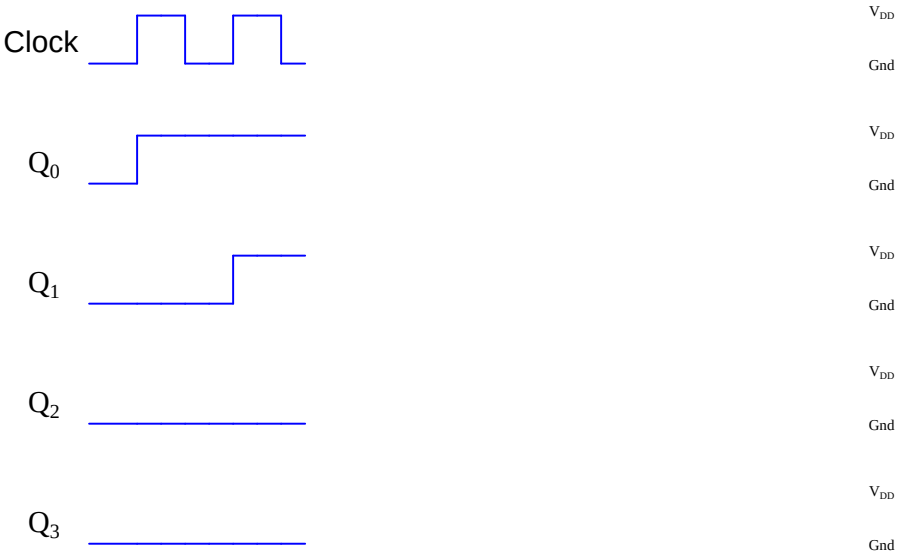
Clock
Q0
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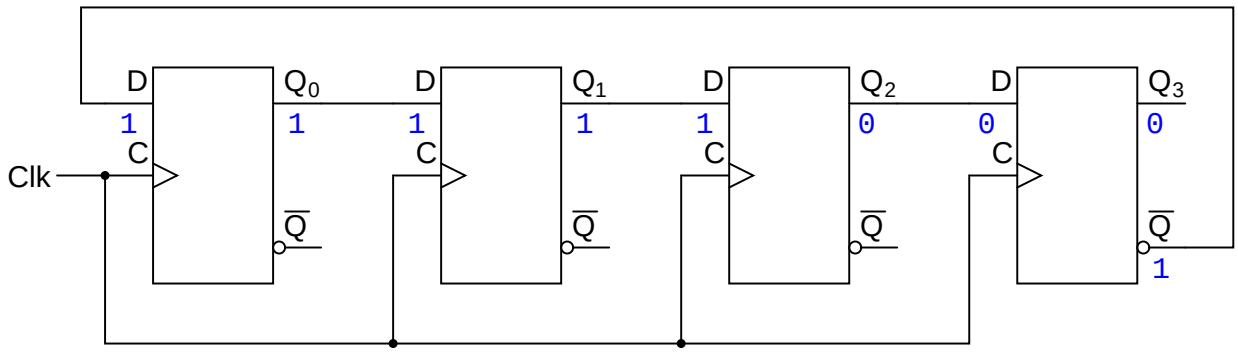
D
Q0
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Q2
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Q3
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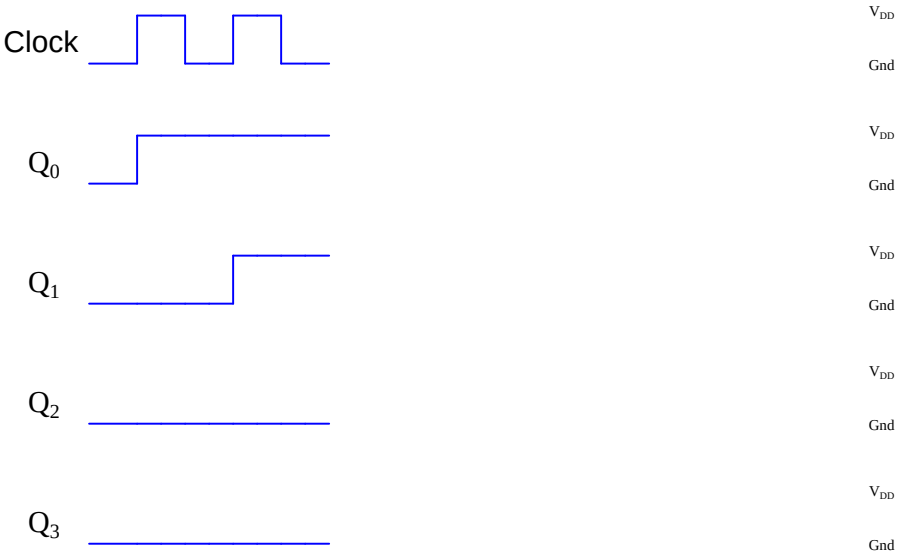
C
C
C
Clk
Q
Q
Q
Q
1


Clock
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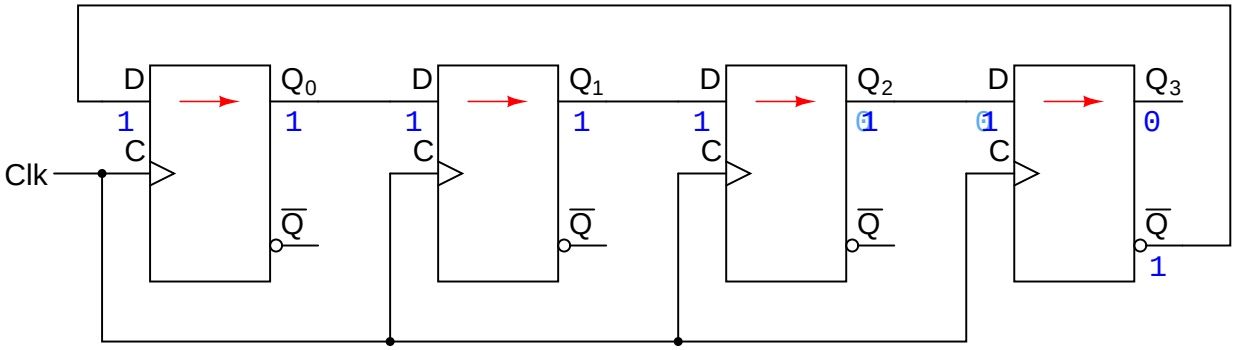
D
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Q
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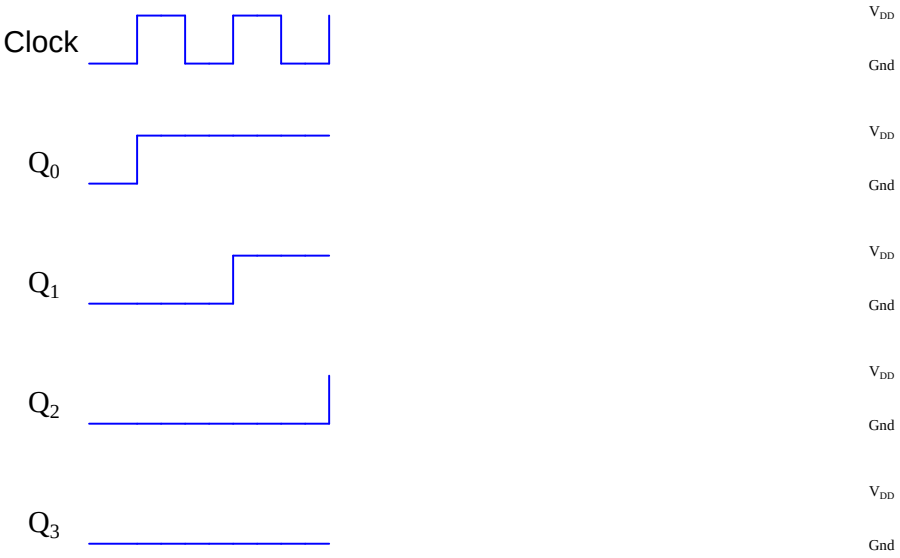
Clock
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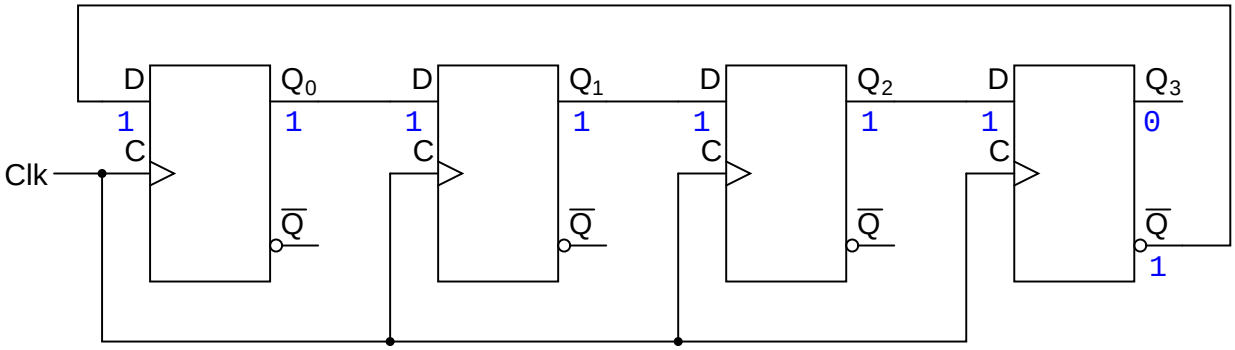
D
Q0
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Q1
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Q2
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Q3
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C
Clk
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Q
Q
Q
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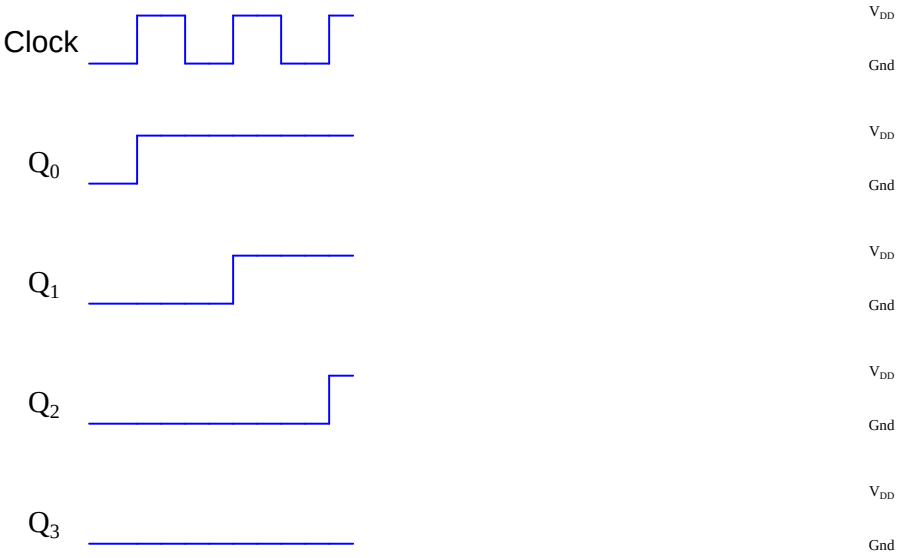
Clock
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Q3
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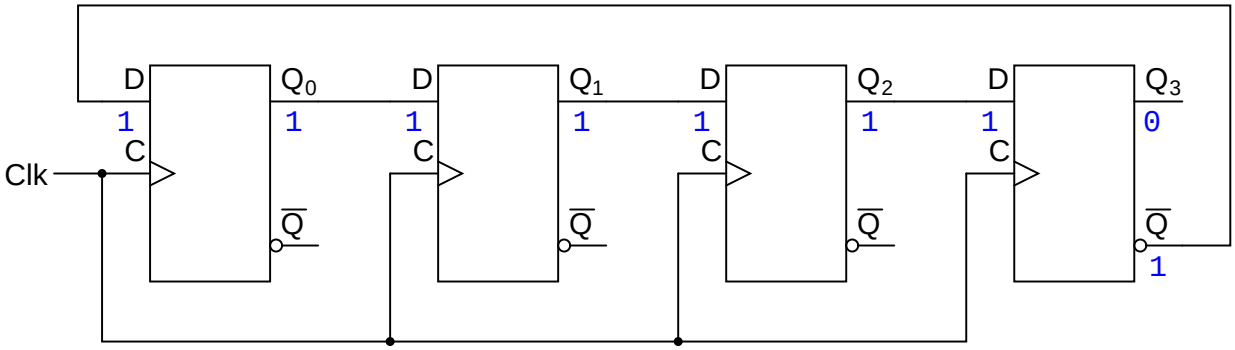
VDD
Gnd


D
Q0
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Q1
D
Q2
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Q3
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1
1
1
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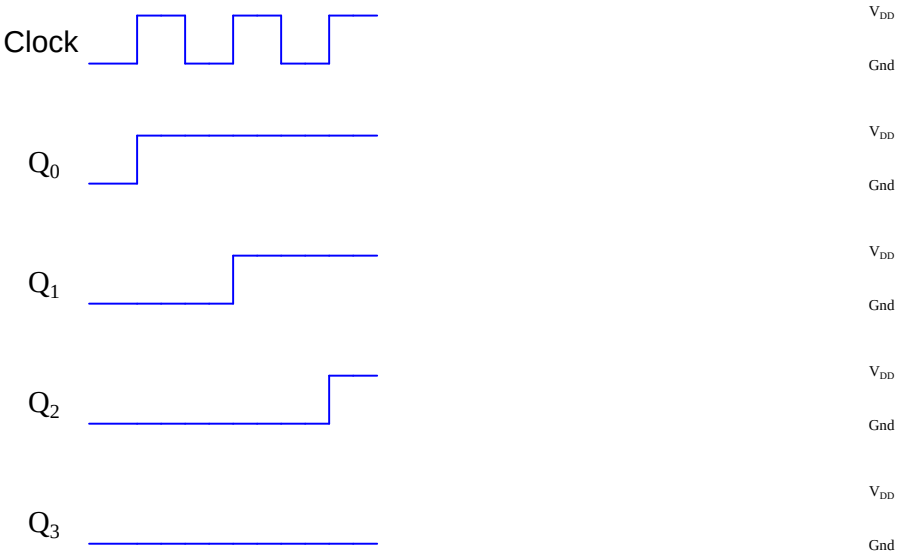
C
C
C
Clk
Q
Q
Q
Q
1


Clock
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Q3
VDD
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VDD
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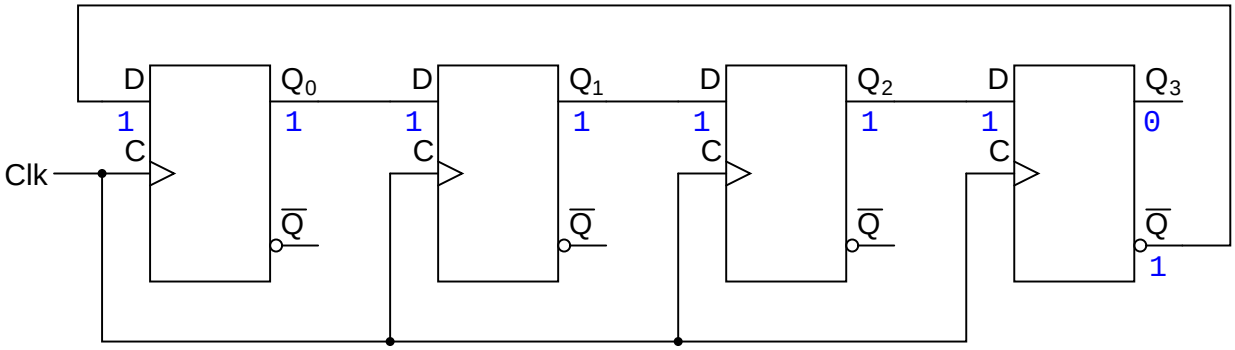
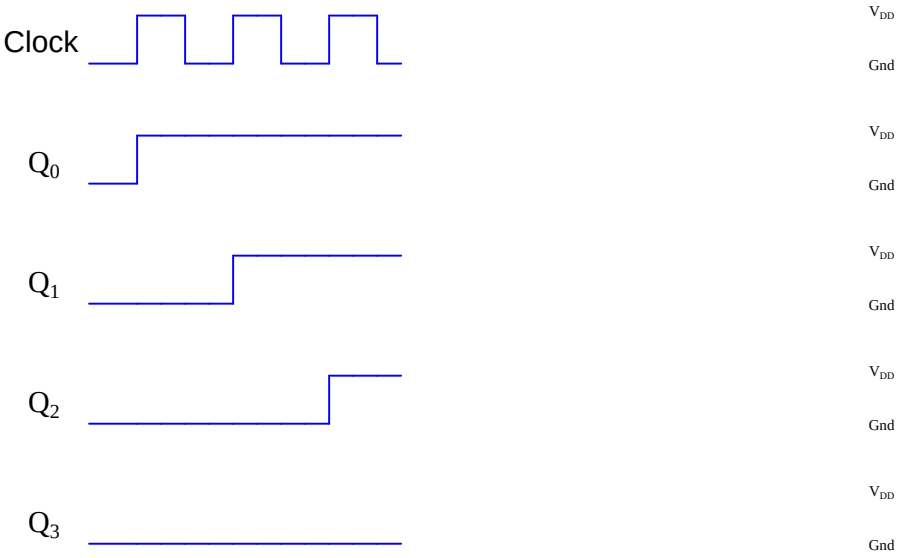
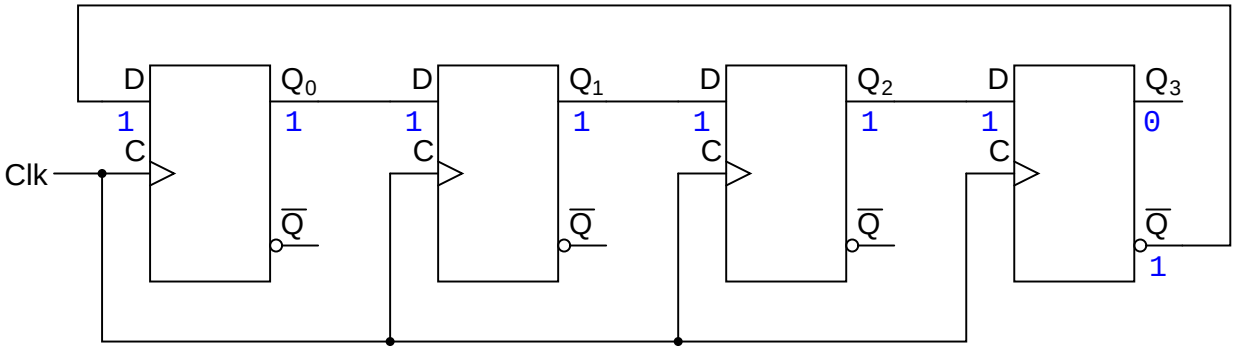
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
1
1
1
1
1
1
1
0
C
C
C
C
Clk
Q
Q
Q
Q
1


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
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0
C
C
C
C
Clk
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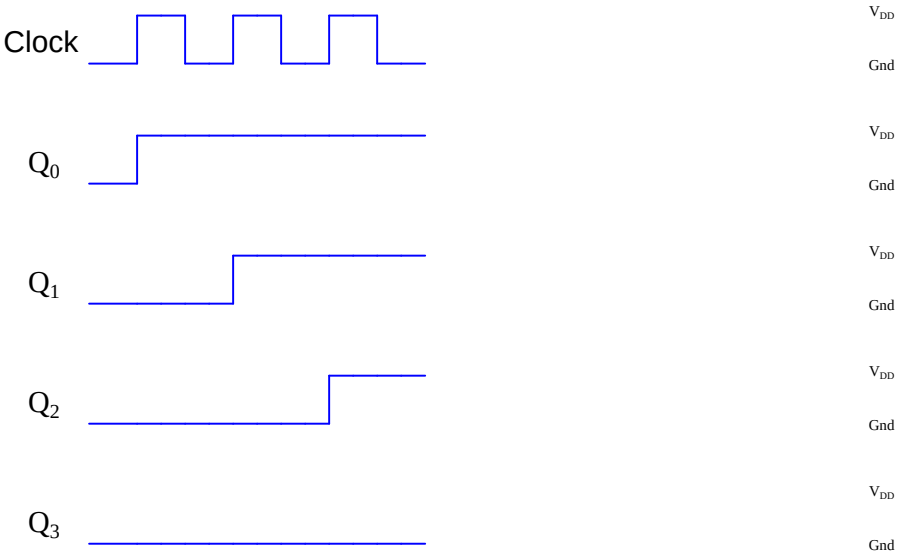
Q
Q
Q
1


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
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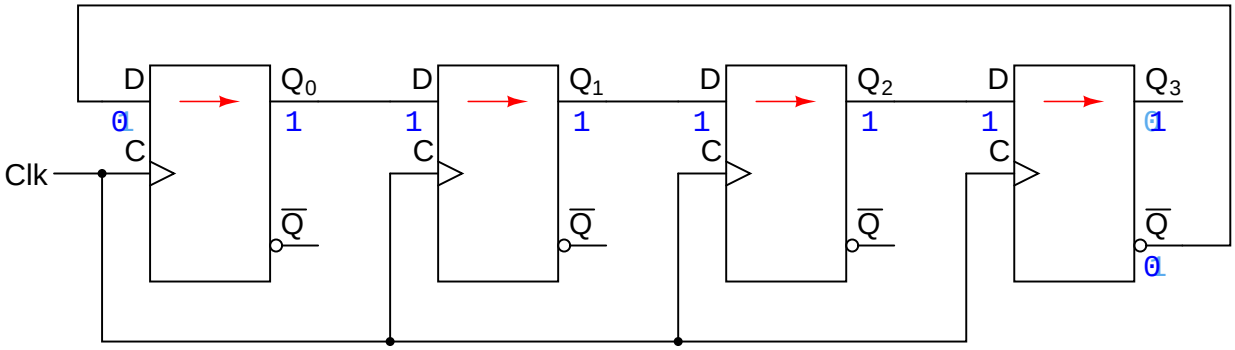
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
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1
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1
1
C
C
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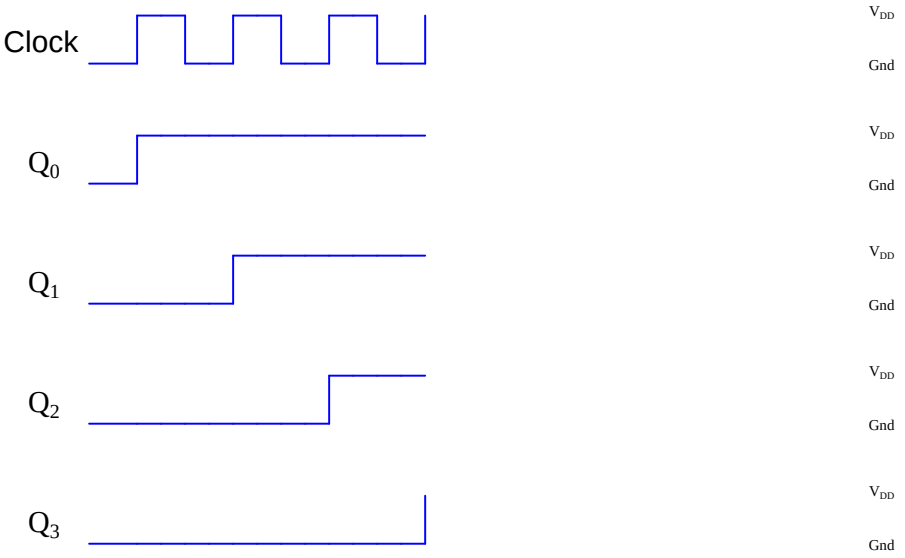
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
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VDD
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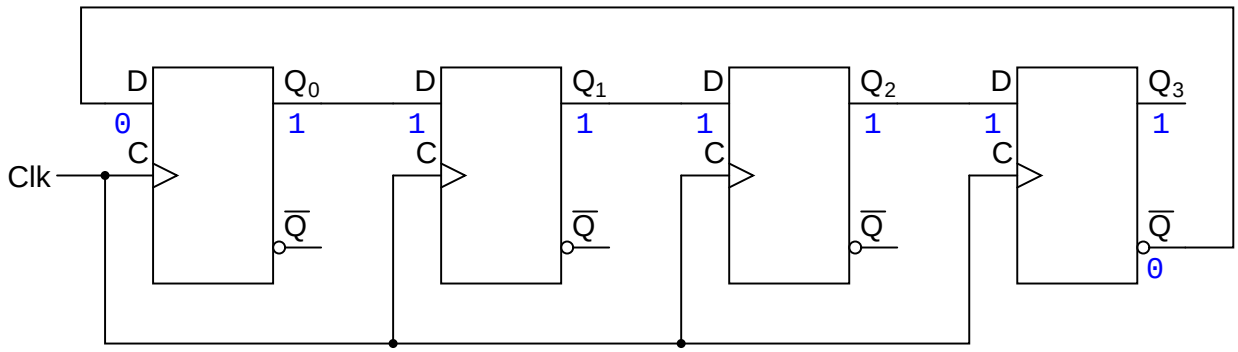
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
0
1
1
1
1
1
1
1
C
C
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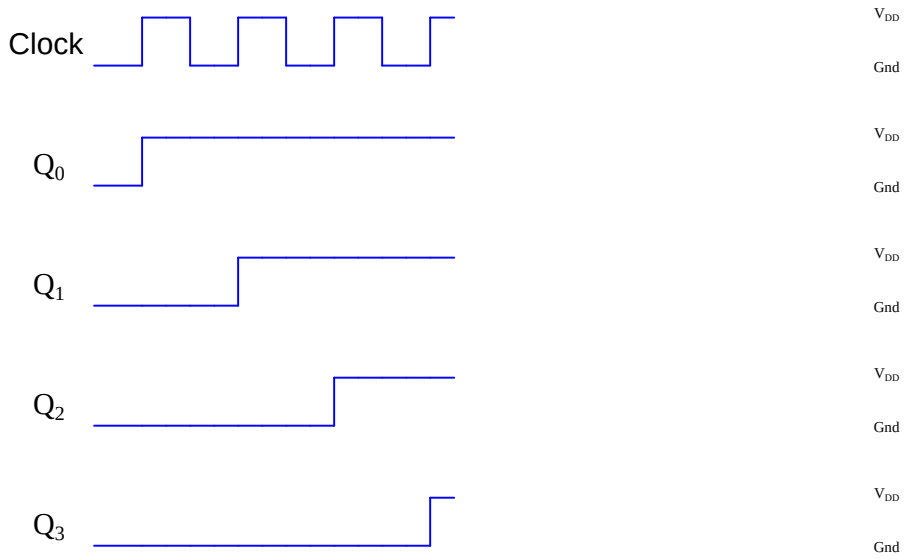
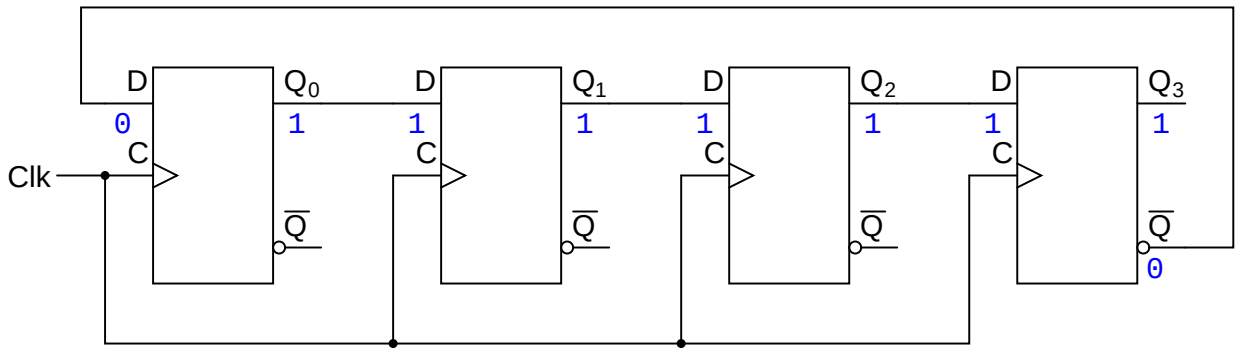
C
Clk
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
0
1
1
1
1
1
1
1
C
C
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C
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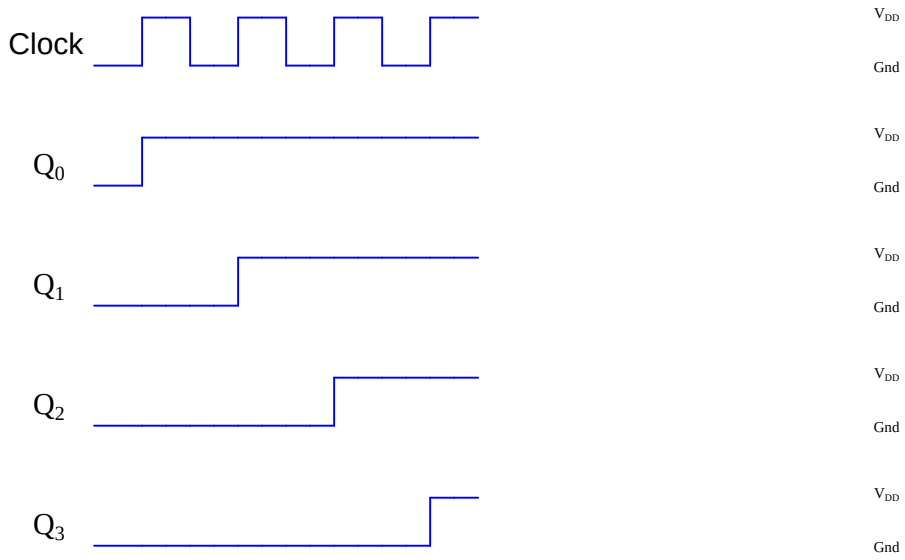
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
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VDD
Gnd
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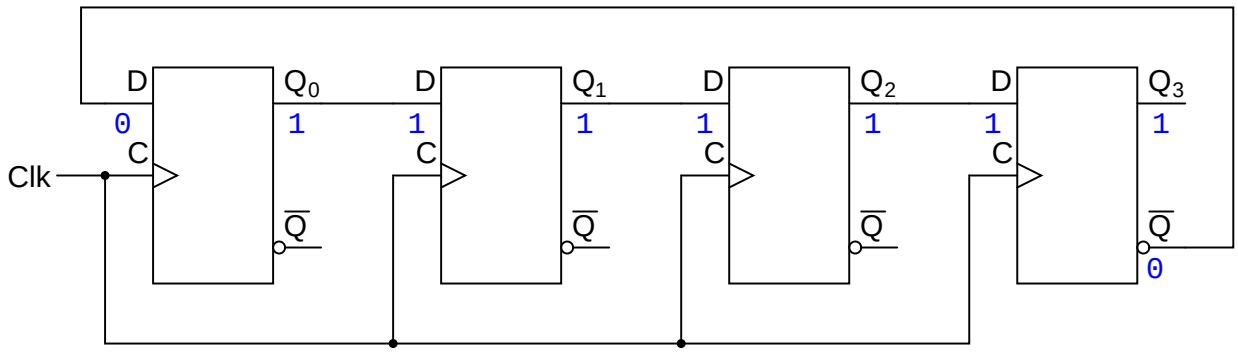
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
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1
1
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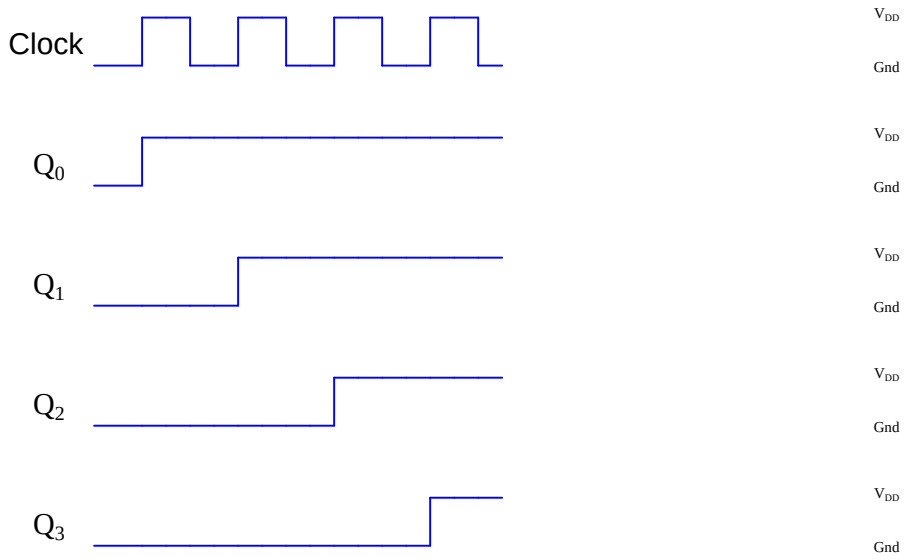
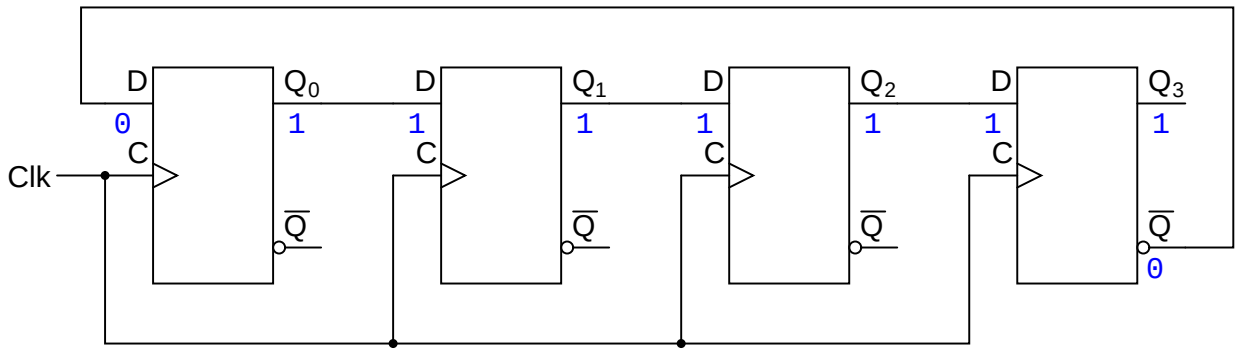
1
1
1
C
C
C
C
Clk
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
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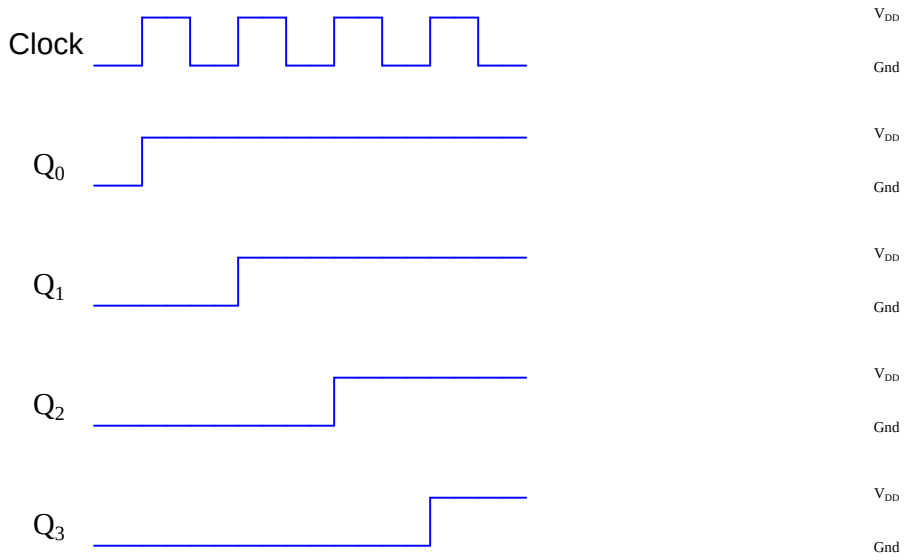
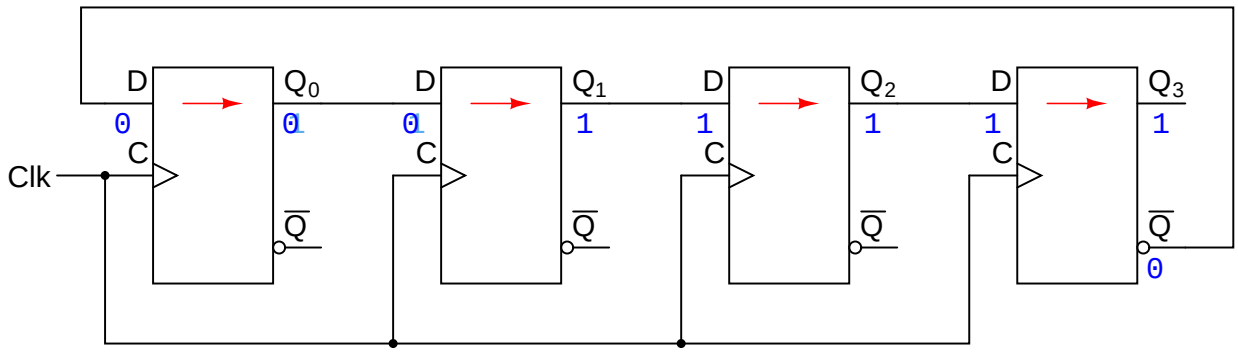
1
1
1
1
1
1
1
C
C
C
C
Clk
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
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Q3
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1
1
1
1
C
C
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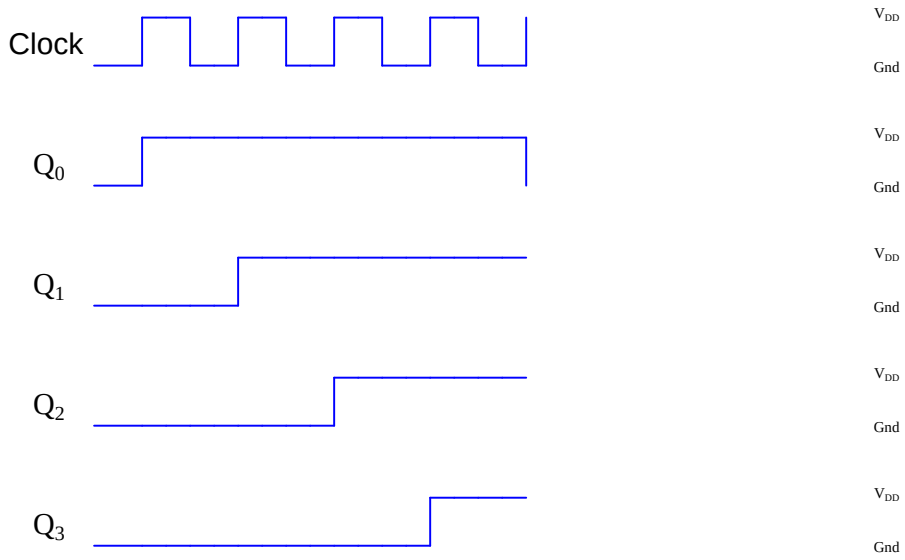
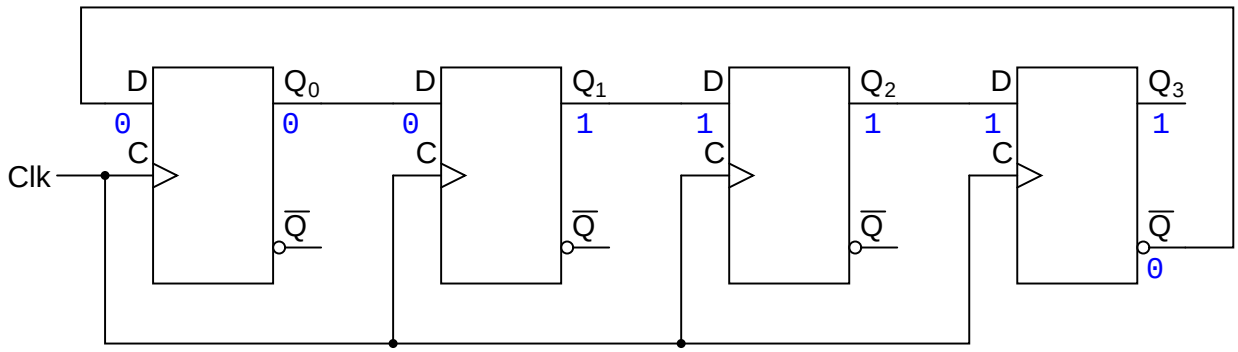
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
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Q3
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0
1
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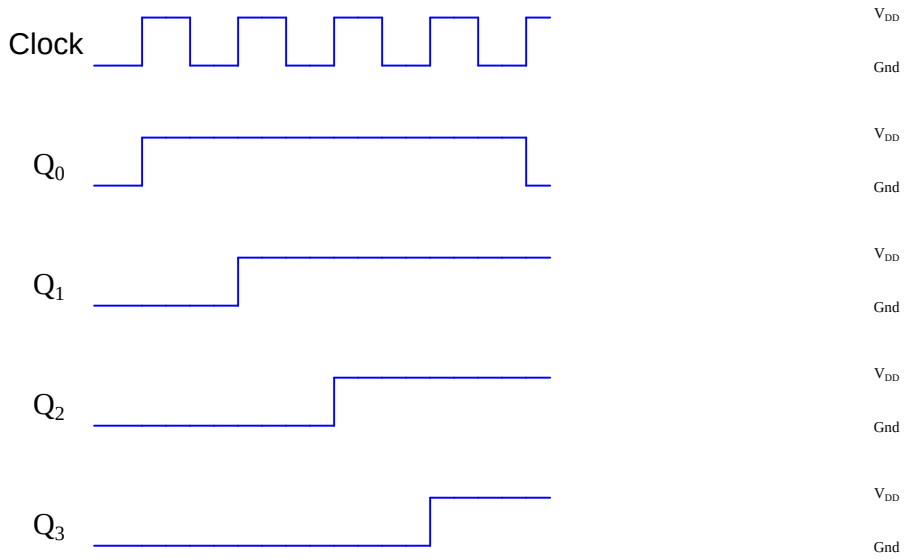
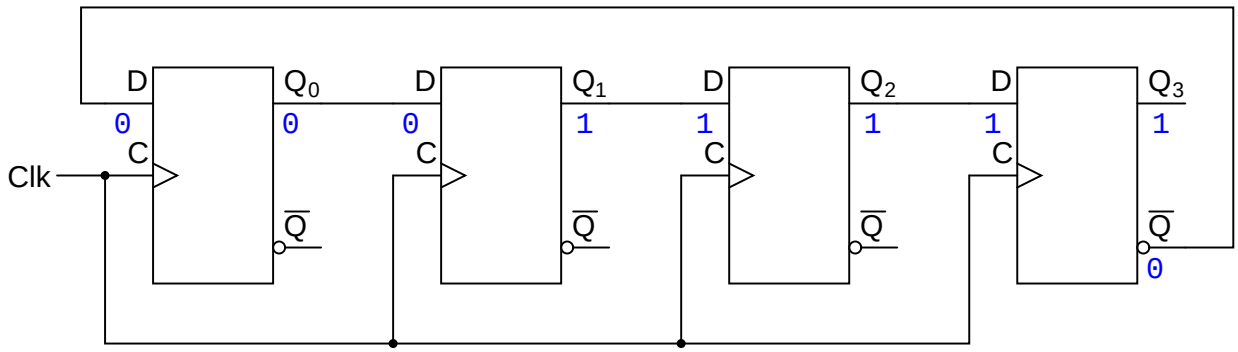
1
1
1
C
C
C
C
Clk
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
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1
1
1
1
1
C
C
C
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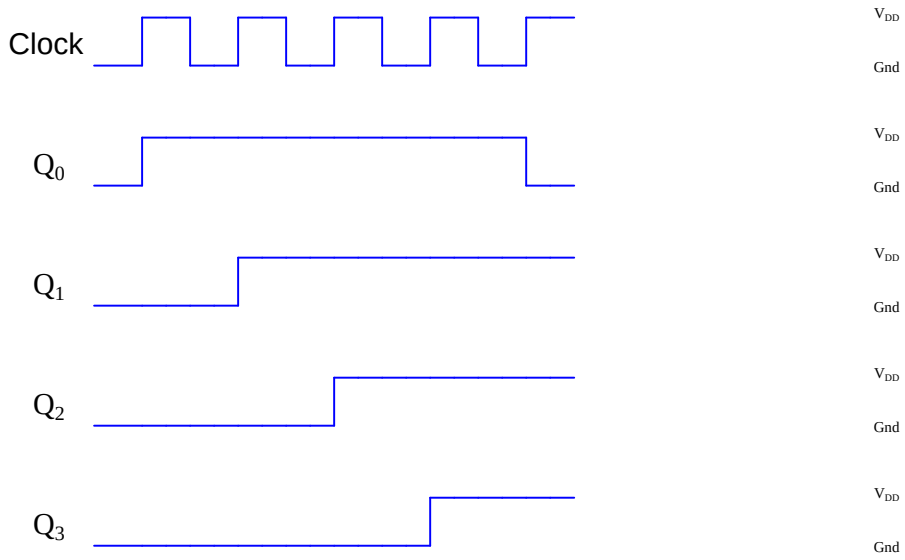
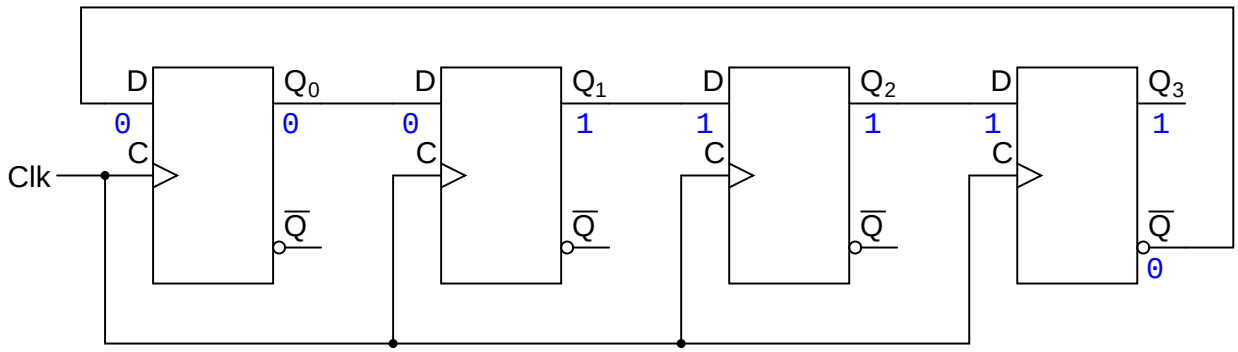
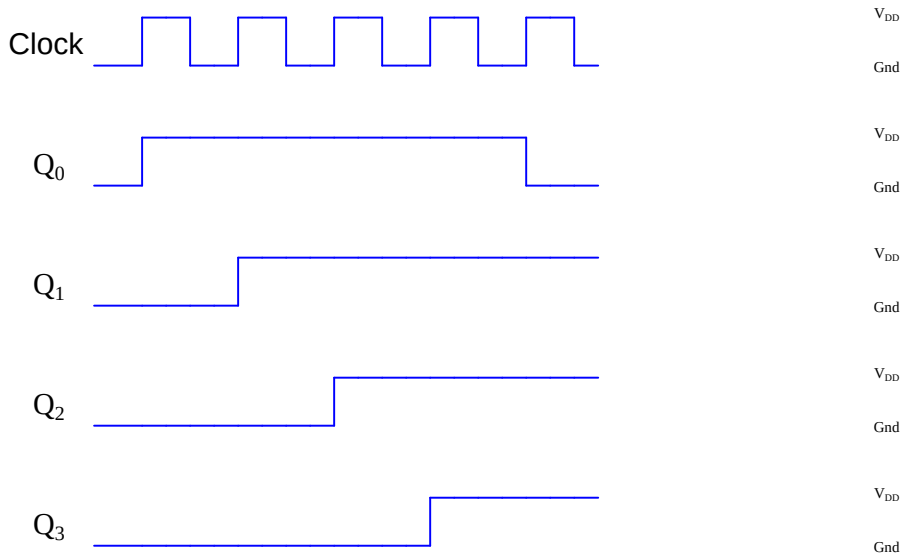
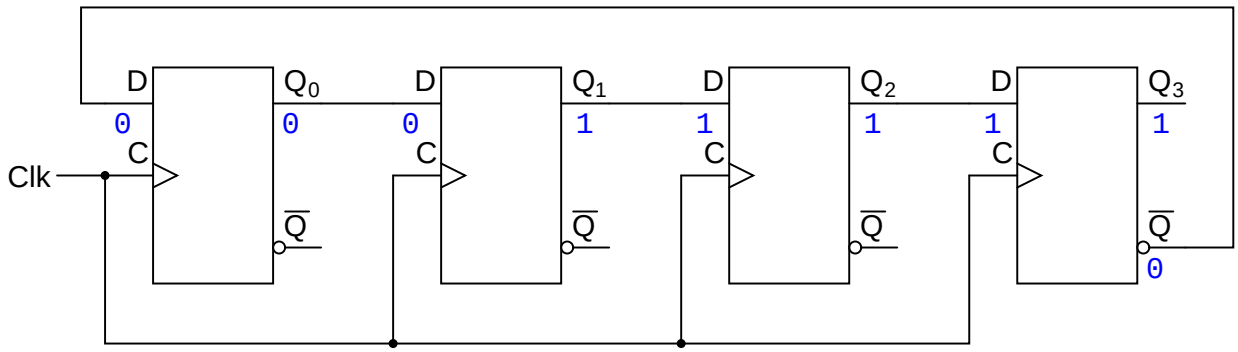
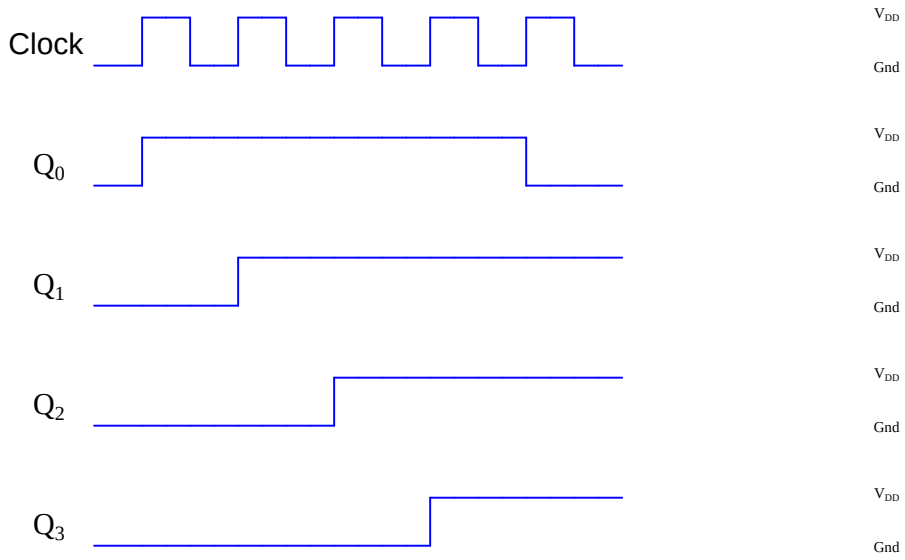
Q
Q
Q
Q
0

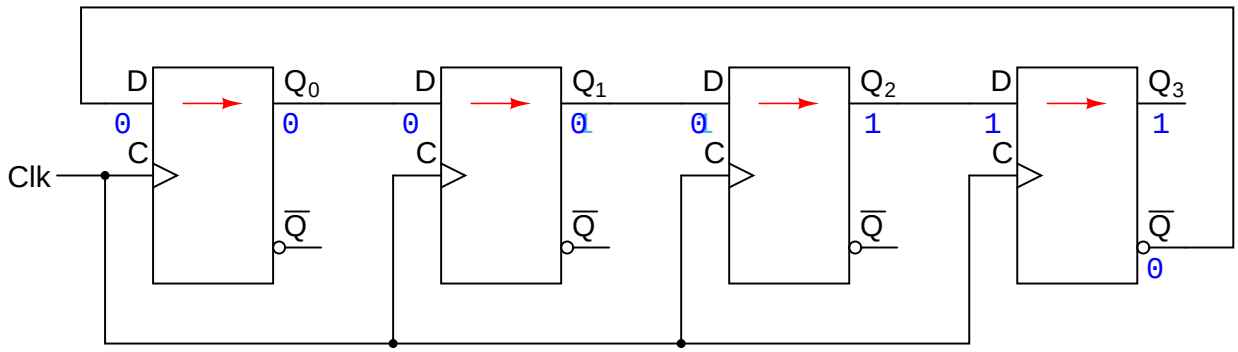

Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
0
0
0
1
1
1
1
1
C
C
C
C
Clk
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
0
0
0
1
1
1
1
1
C
C
C
C
Clk
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
0
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0
0
0
1
1
1
C
C
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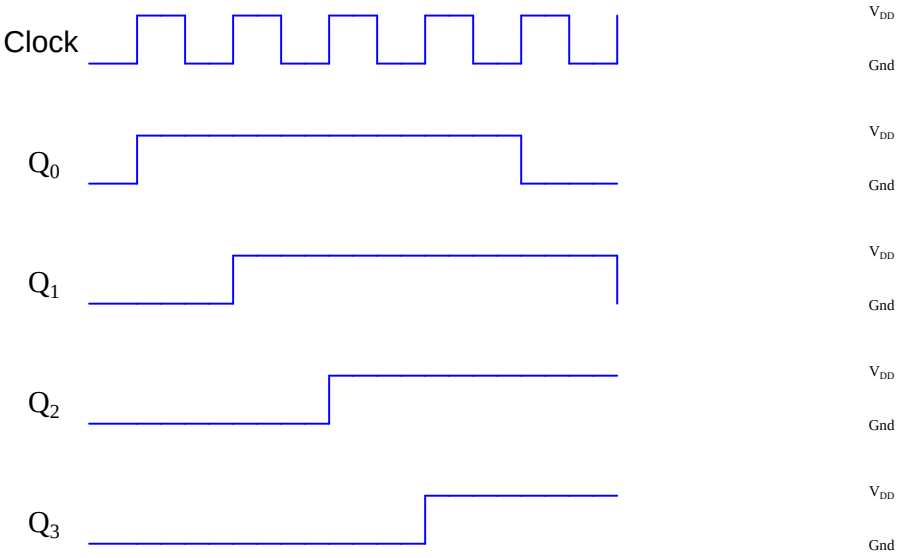
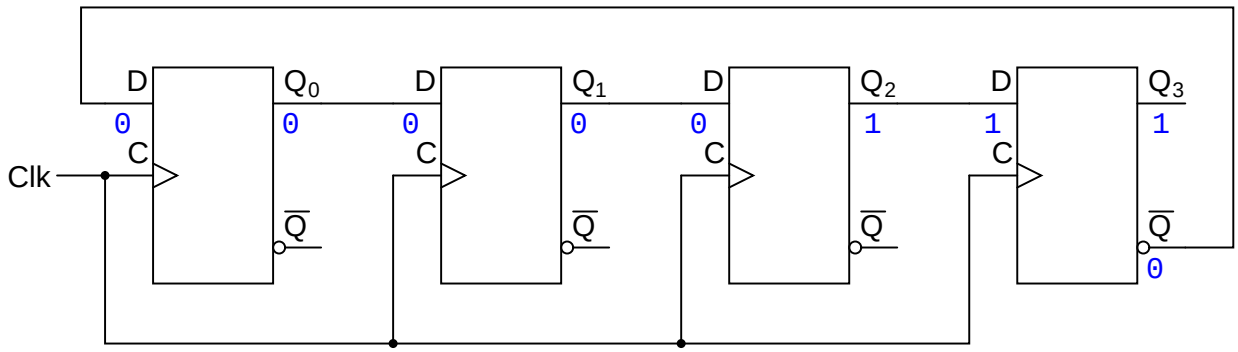
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
0
0
0
0
0
1
1
1
C
C
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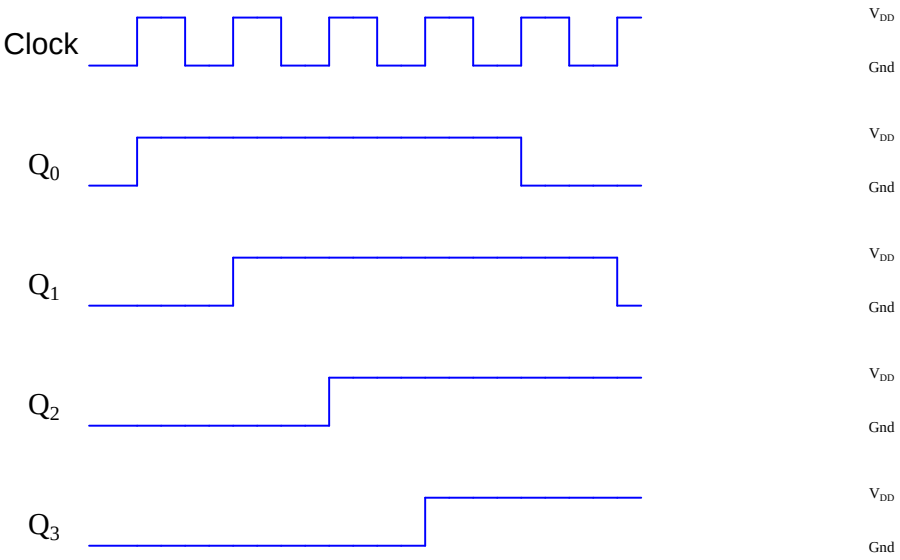
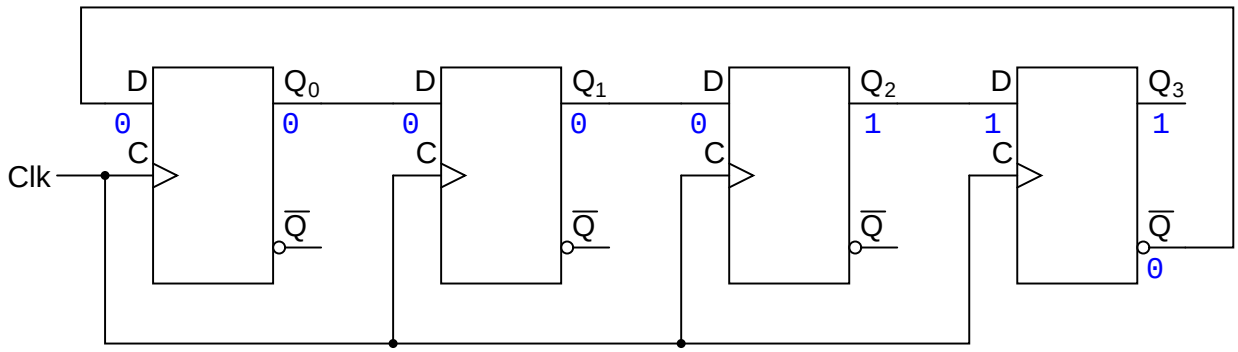
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
0
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0
0
0
1
1
1
C
C
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Q
Q
Q
Q
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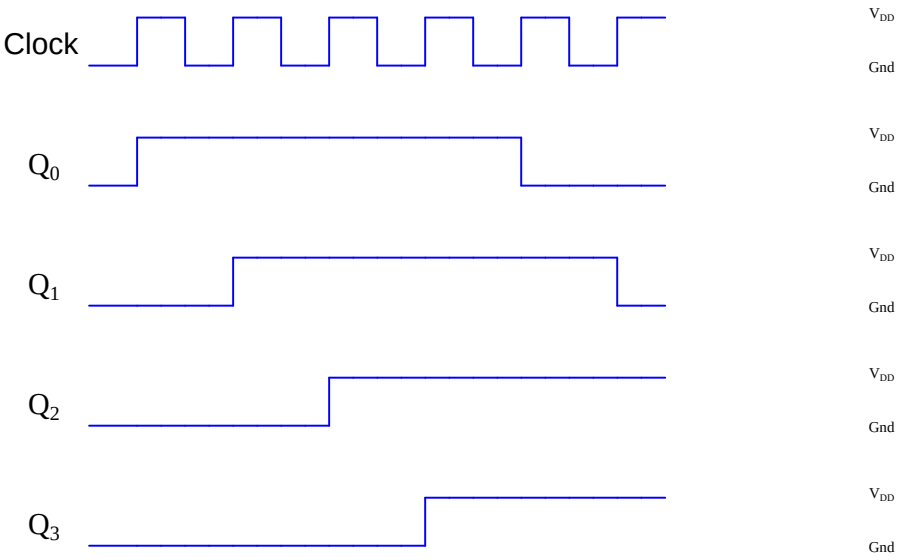
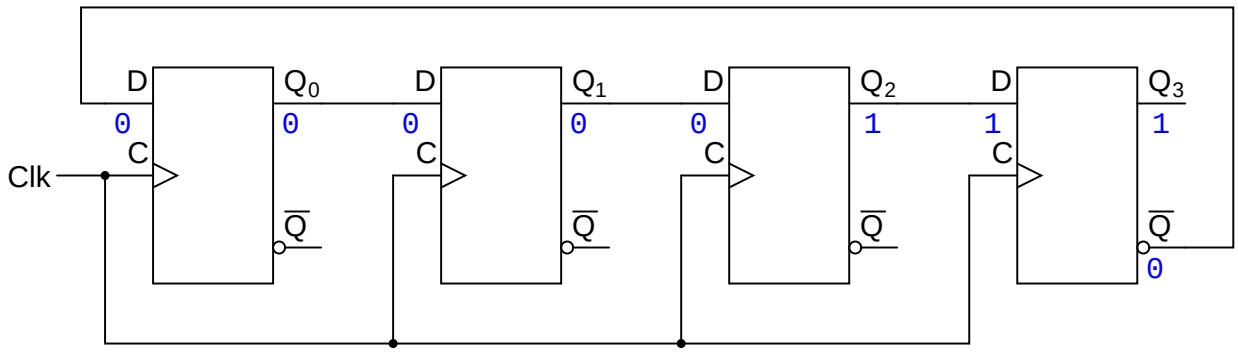

Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
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0
0
0
0
1
1
1
C
C
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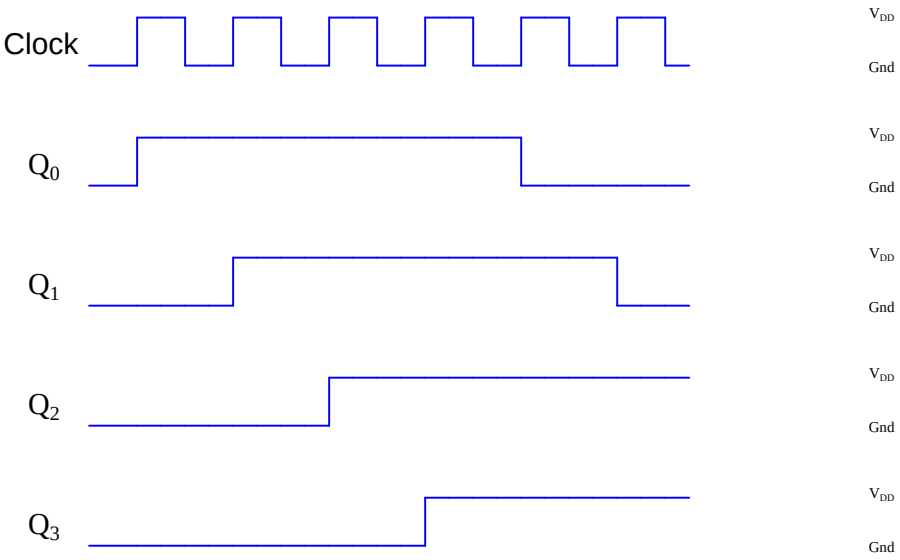
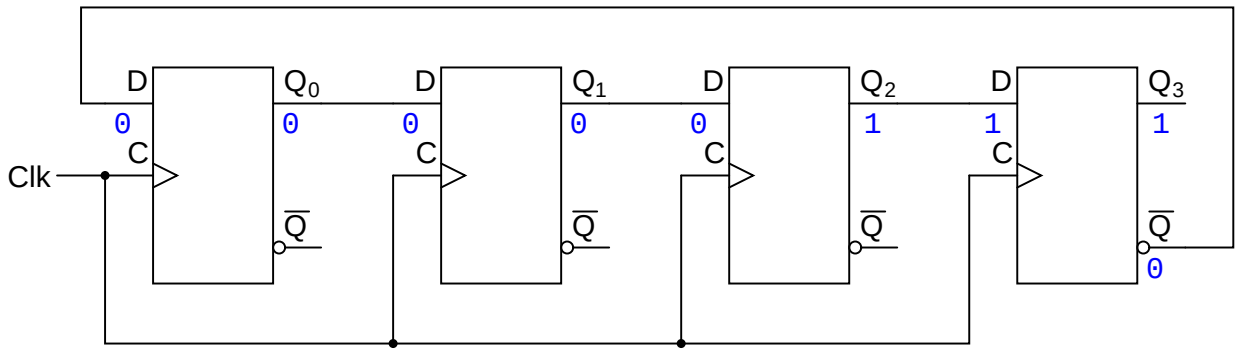
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
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0
0
0
1
1
1
C
C
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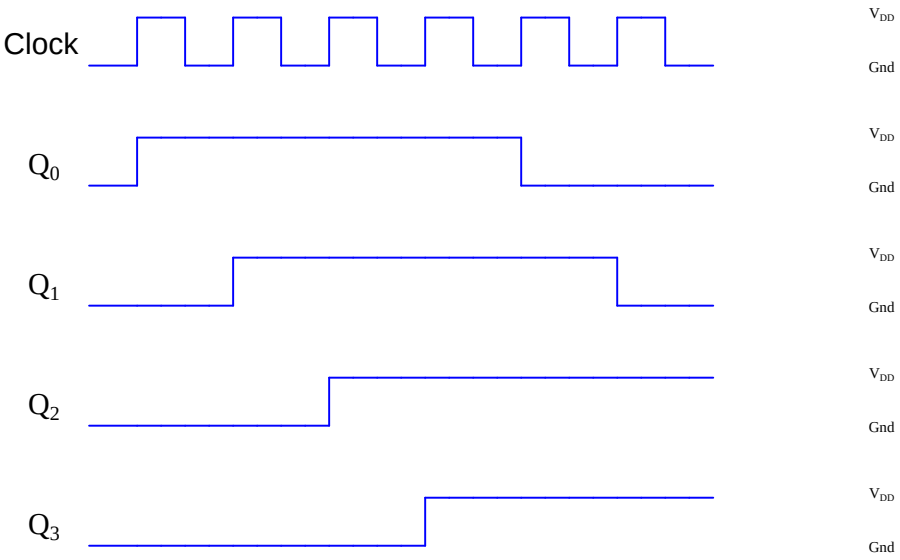
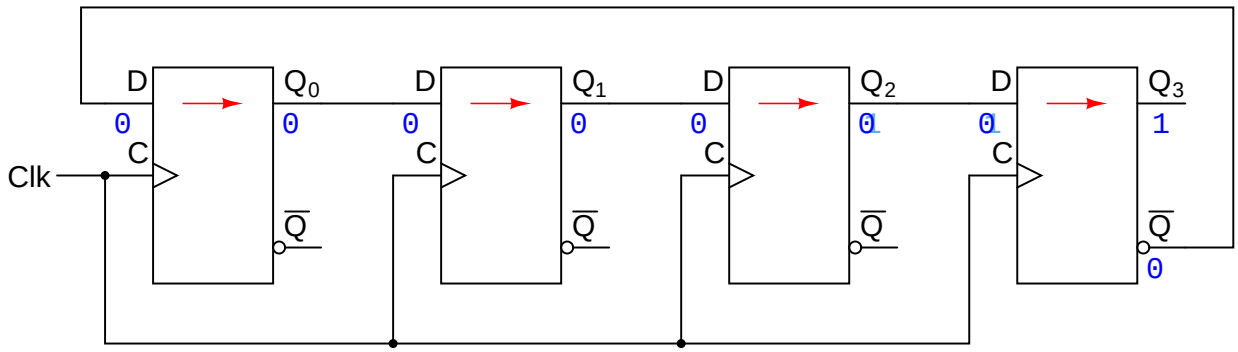
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
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0
0
0
0
0
1
C
C
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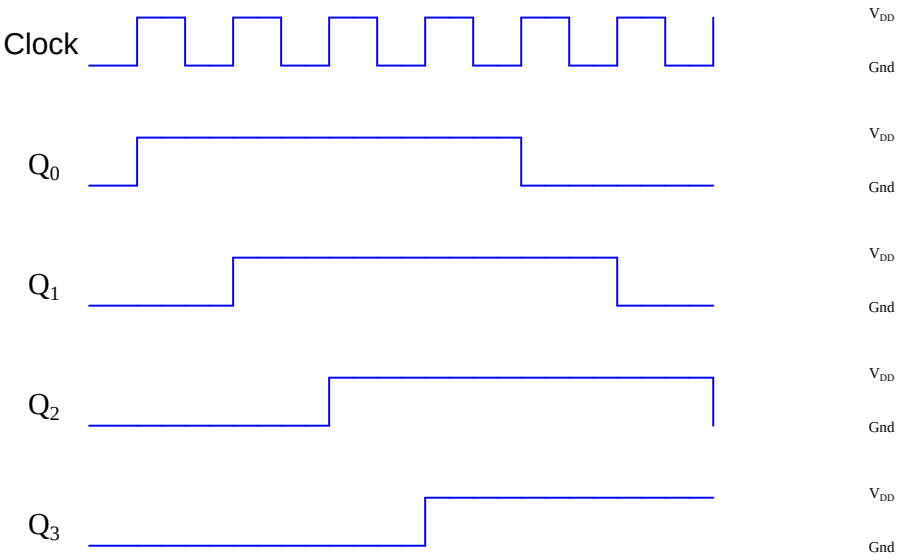
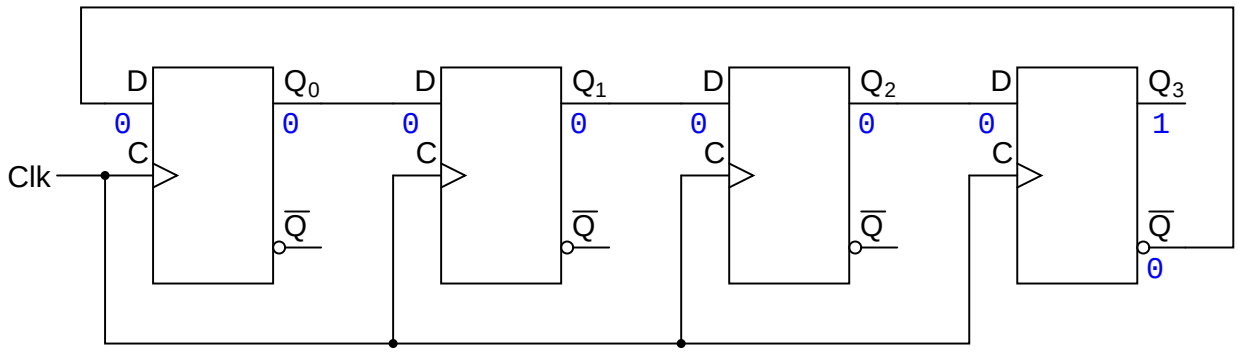
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
0
0
0
0
0
0
0
1
C
C
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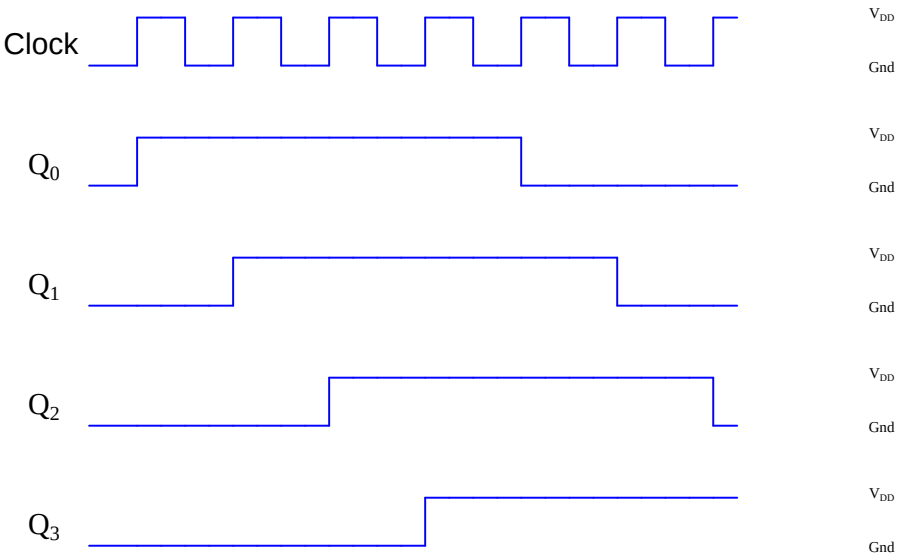
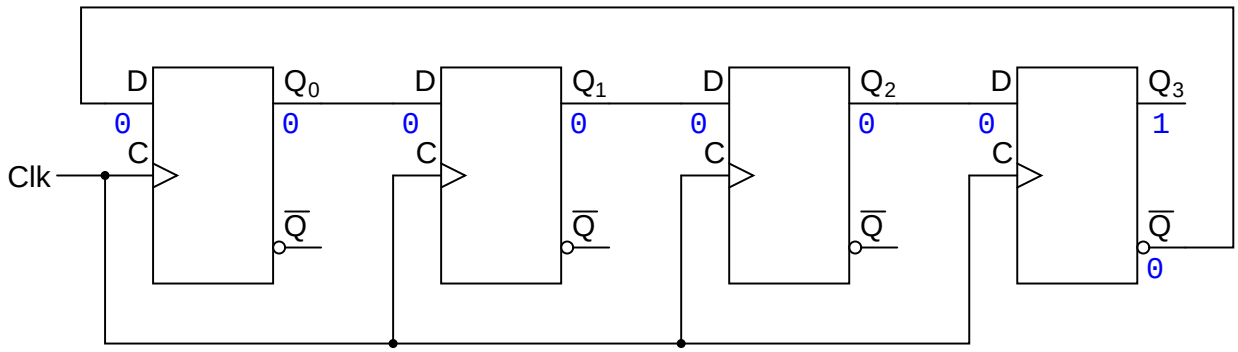
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
0
0
0
0
0
0
0
1
C
C
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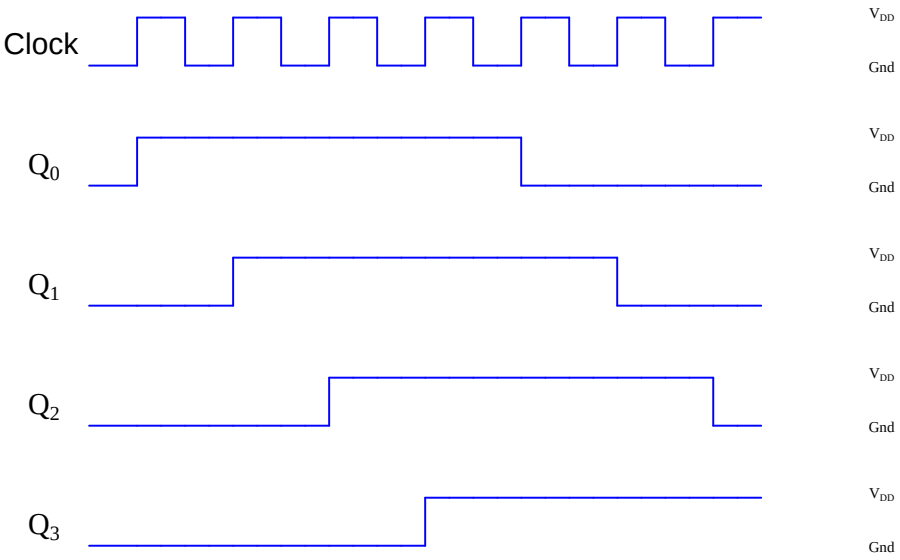
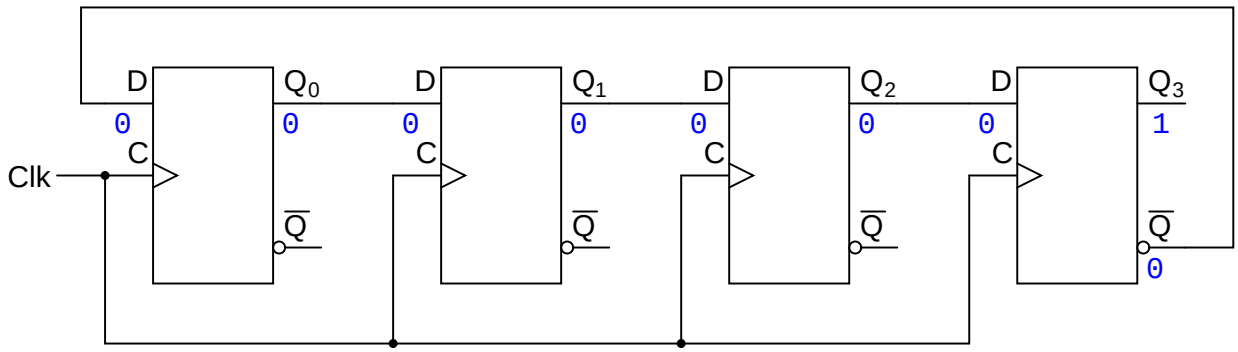
C
Clk
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
0
0
0
0
0
0
0
1
C
C
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C
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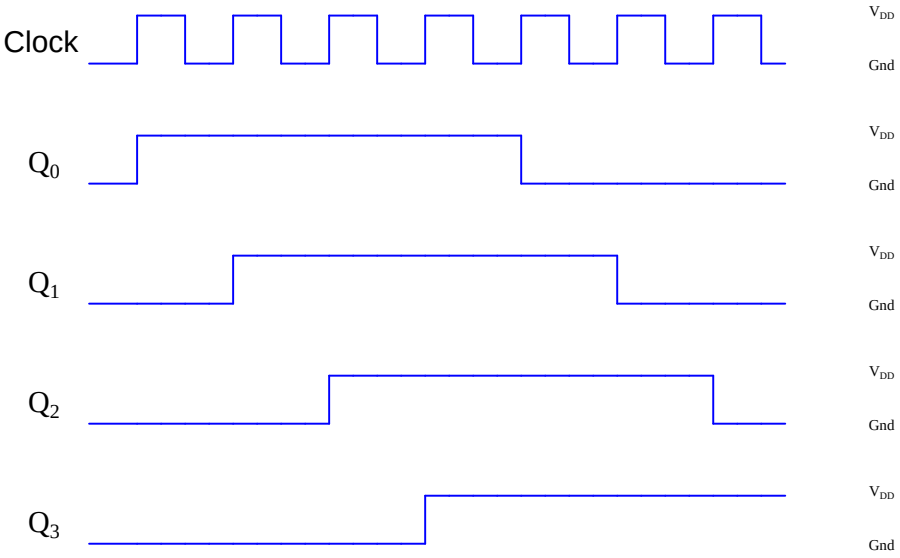
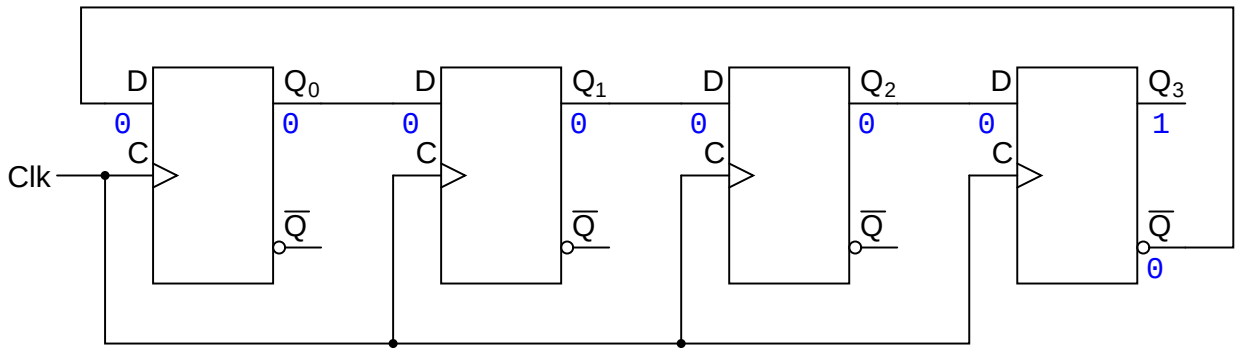
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
0
0
0
0
0
0
0
1
C
C
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C
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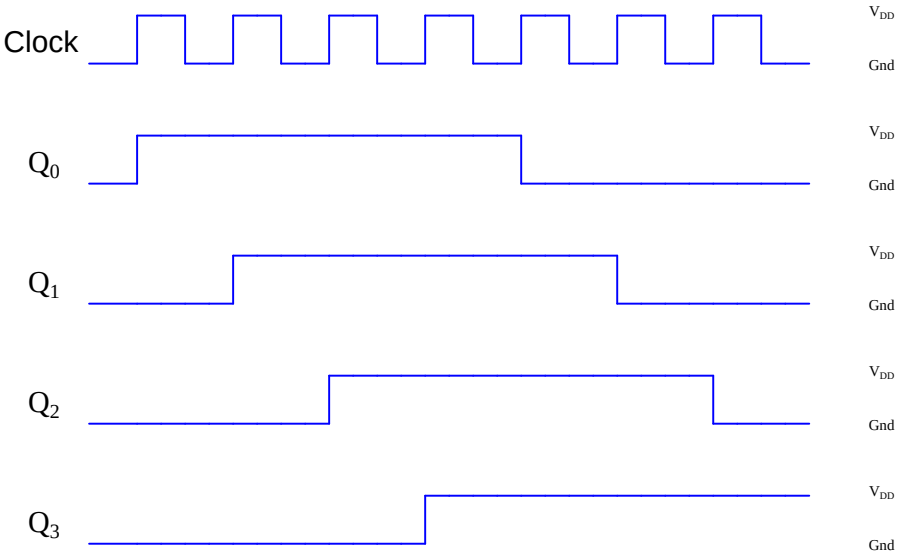
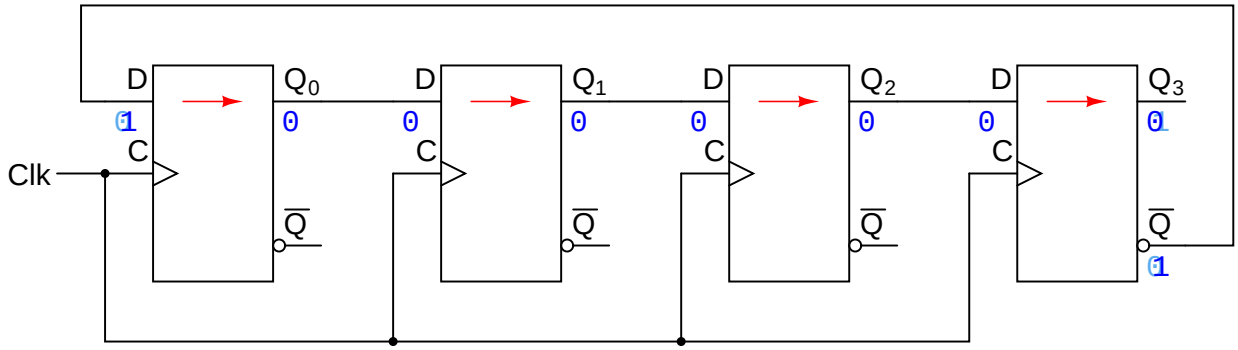
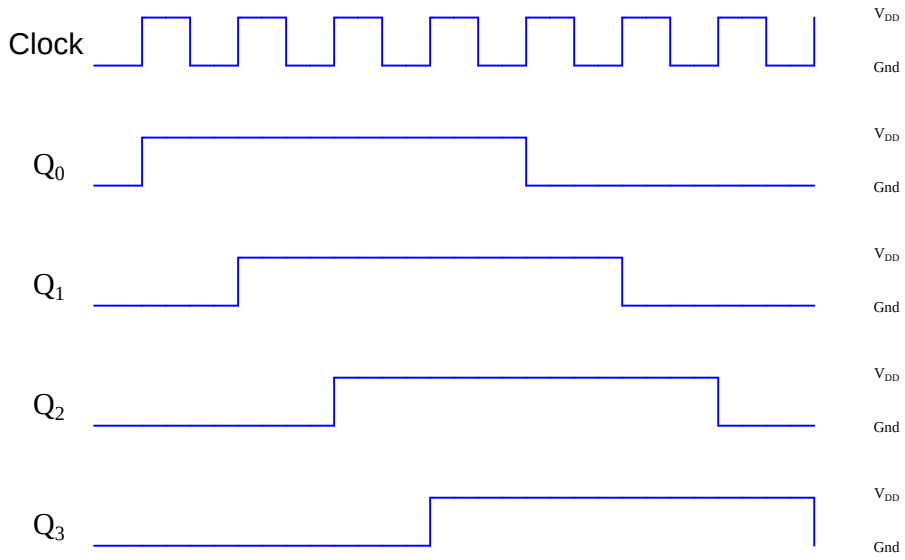
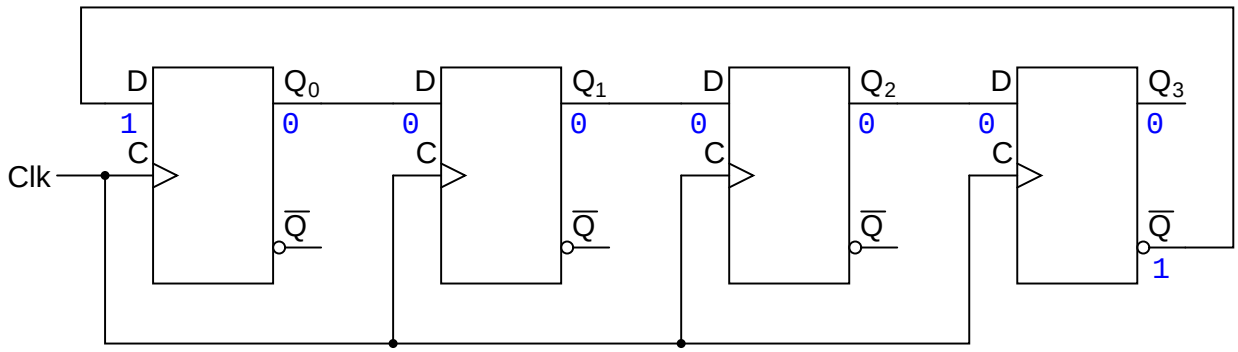
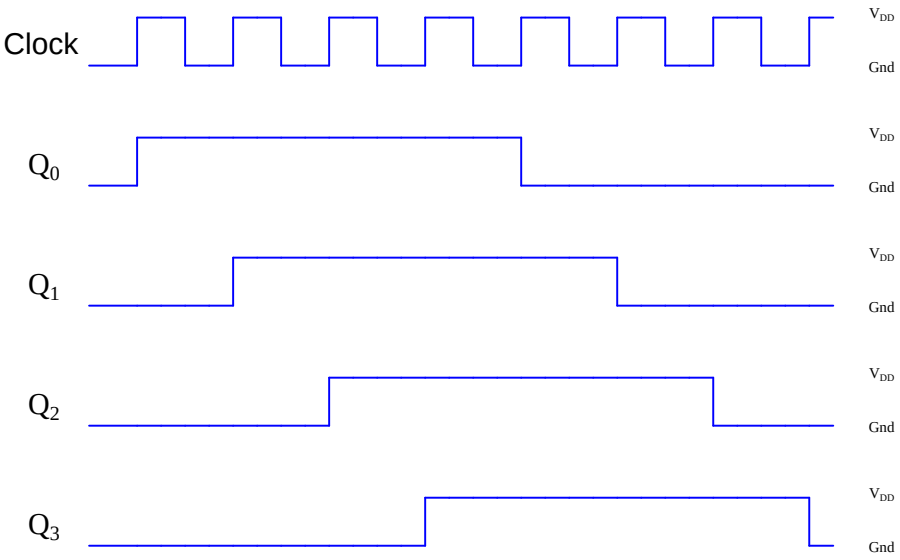
Q
Q
Q
Q
0


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
1
0
0
0
0
0
0
1
C
C
C
C
Clk
Q
Q
Q
Q
1


Clock
Q0
Q1
Q2
Q3
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd
VDD
Gnd


D
Q0
D
Q1
D
Q2
D
Q3
1
0
0
0
0
0
0
0
C
C
C
C
Clk
Q
Q
Q
Q
1


Clock
Q0
Q1
Q2
Q3
VDD
Gnd

file 03234

Answer 1

Note that each rising edge of the clock pulse has its own frame in the animation sequence, to better show you what happens at those crucial times.

Notes 1

The purpose of this animation is to let students study the behavior of this counter circuit and reach their own conclusions. Similar to experimentation in the lab, except that here all the data collection is done visually rather than through the use of test equipment, and the students are able to "see" things that are invisible in real life.

In this animation, I show each rising edge of the clock signal in its own frame, whereas the falling edge of the clock shares a frame with the first half of the "low" state. I do this because these are positive edge-triggered flip-flops, and so the rising edge of the clock pulse is most important. I could have slowed things down on the falling edge of the clock as well, but since there is little "action" happening then, I decided to save a frame and make it a shorter animation.