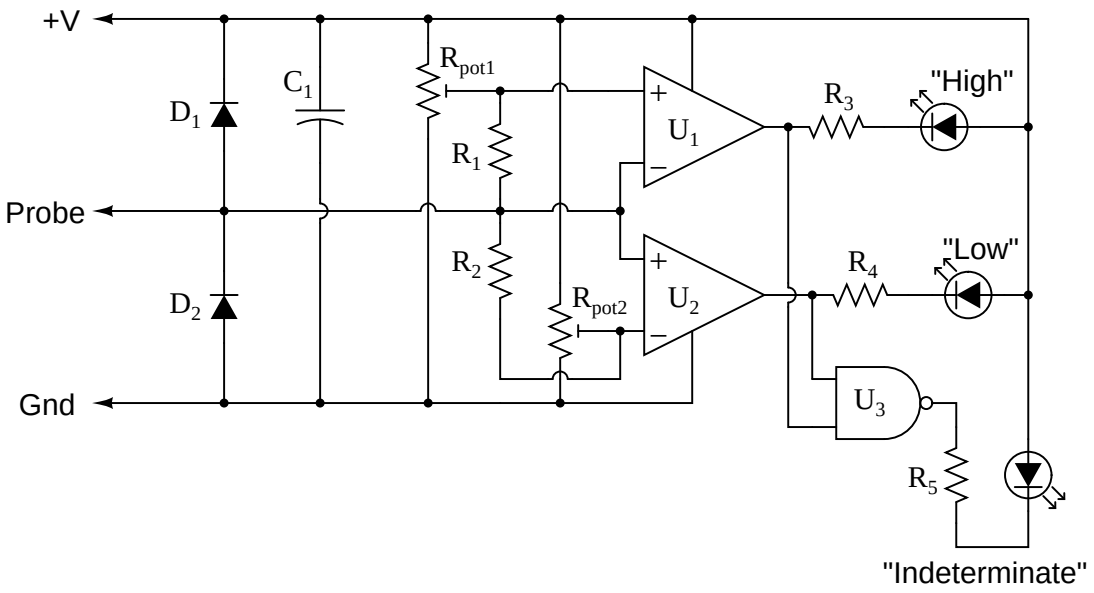
Design Project: Logic probe

Your project is to design and build a simple logic probe, capable of displaying "high," "low," and "indeterminate" logic states for any family of logic (TTL, CMOS, ECL, etc.). Here is a sample schematic diagram for you to follow when designing your system:



Suggested components:

- $R_1 = R_2 = 1$ MΩ
- $R_3 = R_4 = 1$ kΩ
- $R_{pot1} = R_{pot2} = 10$ kΩ
- $C_1 = 10$ μF
- $D_1 = D_2 =$ 1N4148 switching diodes
- $U_1 = U_2 =$ LM339 comparator
- $U_3 =$ One gate in 4011 (CMOS) quad NAND integrated circuit

Of course, you are not restricted to using this exact design. Another neat feature to add to this circuit would be a "pulse" detection LED that lights up only when the input (probe voltage) changes state.

Deadlines (set by instructor):

- Project design completed:
- Components purchased:
- Working prototype:
- Finished system:
- Full documentation:

Questions

Question 1

What factors determine where potentiometers R_{pot1} and R_{pot2} must be set? Why are they "trimmer" potentiometers (as indicated by the special wiper symbol) and not regular panel-mount potentiometers?

file 02852

Question 2

What performance parameters are important to consider for U_1 and U_2, considering their use in a logic probe circuit? Hint: we may want to use this logic probe to troubleshoot CMOS as well as TTL circuits.

file 02853

Question 3

What purpose do resistors R_1 and R_2 serve, and why are they so large (1,000,000 ohms each)?

file 02905

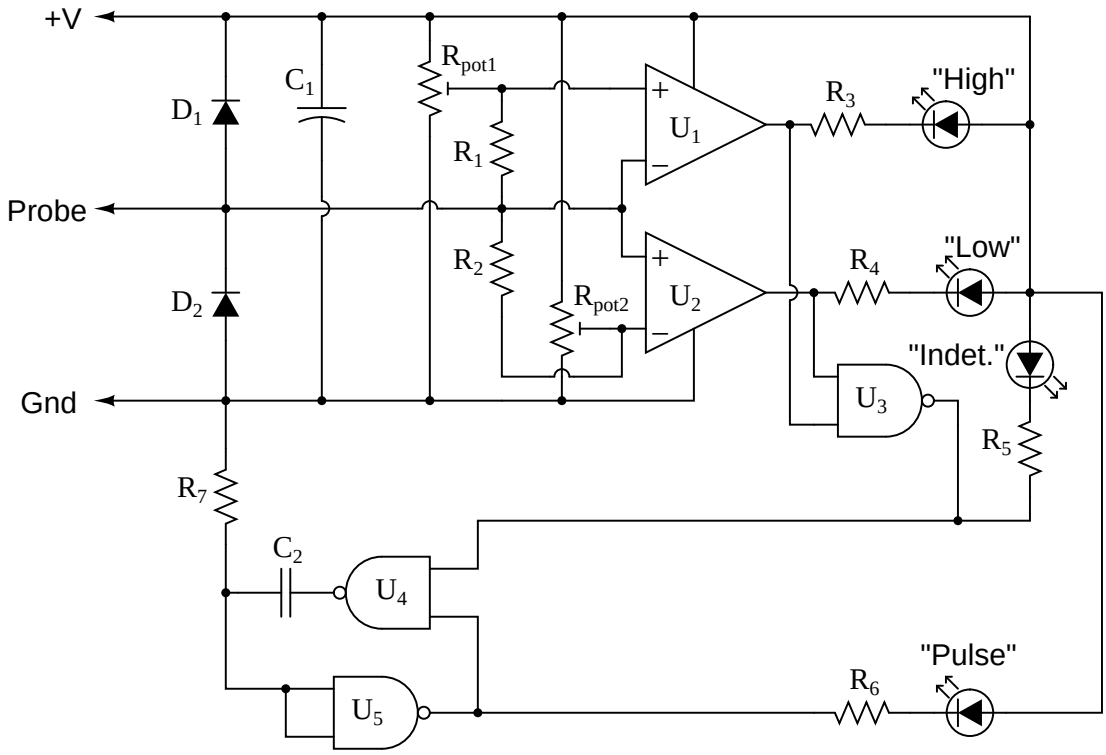
Question 4

Re-design the example circuit so that a NAND logic gate is not required. Instead, think of a way you could use discrete components to do the same job.

file 02854

Question 5

An extra feature you could add to the logic probe circuit is a *pulse indication* LED. This LED momentarily turns on whenever there is a transition from high-to-low or from low-to-high:



Actually, what the pulse indicator circuit detects is a transition to the "indeterminate" state, which always lies between "high" and "low." A pulse indication feature is nice to have in some circumstances, since it shows the presence of pulses which may be too brief to light up either the "high" or "low" LED. The two additional NAND gates "stretch" the pulse time so that the "pulse" LED's blink is long enough to see. The duration of the LED's blink is set by resistor R_7 and capacitor C_2.

Explain how the pulse indication circuitry works.

file 02912

Answers

Answer 1

The acceptable "high" and "low" voltage levels for which ever logic family is being trouble-shot will dictate where these potentiometers must be set.

Answer 2

First and foremost, we need to consider the supply voltage ranges for all integrated circuits used in this circuit. Do *not* use 7400-series TTL NAND gate for U_2 if you ever plan to use this logic probe on digital circuits with power supply voltages in excess of 5 volts!

Answer 3

If they were not in the circuit, the logic probe would indicate a "high" condition with the probe floating. In place, the resistors force an "indeterminate" state with a floating probe.

Answer 4

I'll leave this part up to you!

Answer 5

NAND gates U_4 and U_5 form a monostable multivibrator circuit. A low input sensed by U_4 at the output of U_3 (indicating an indeterminate state) forces U_4 to output a high signal, which is inverted by U_5 to energize the "Pulse" LED and also hold U_4 in that state even when the output of U_3 goes high again. This state cannot last indefinitely, though, because the RC network of R_7 and C_2 brings the input of U_5 to a low state over time, thus "resetting" the pulse indication circuit.

Notes

Notes 1

Do *not* simply tell your students what these acceptable voltage levels are! Let them research datasheets for instances of logic gates within the logic family desired, and let the manufacturers' data tell them what they need to know.

Notes 2

Note how the comparators *sink* current from the LEDs rather than *source* current to them. This design feature was necessary, due to the construction of the LM339. In fact, there are a lot of comparators that can only sink current and not source current due to the internal use of an open-collector output stage.

Notes 3

A less obvious feature of these resistors is that they force the circuit under test to drive a bit of current to (or from) the probe. This is good, as it may help to show a gate with a "weak" output, such as one that is mildly overloaded. Lower values for R_1 and R_2 would accentuate this feature, but would also make it trickier to set the high/low threshold potentiometers (R_{pot1} and R_{pot2}).

Another not-so-obvious design feature is that resistors R_1 and R_2 establish a default input voltage level that is between the two threshold settings established by the potentiometers. In my first design, I connected R_1 and R_2 to the power supply rails, respectively. This set the default (floating) input voltage at $\frac{1}{2}V$, which worked fine for CMOS logic levels but not for TTL. By having the resistors set a default input voltage between the two threshold adjustments, a floating probe is guaranteed to indicate "indeterminate" no matter where the threshold potentiometers are set.

Notes 4

Not only will a discrete transistor have a wider voltage range it can operate over (compared to a logic gate), but it is a good review of transistor circuit theory and a practical example of implementing a simple logic function without the benefit of integrated circuits.

Notes 5

I recommend a 0.47 μF capacitor for C_2 and a 100 kΩ resistor for R_7. The added feature of a pulse indicator LED is particularly nice because it makes use of what would otherwise be unused gates in a 4011 CMOS NAND gate IC. The only added componentry is the fourth LED, current limiting resistor R_6, capacitor C_2, and resistor R_7.