ELTR 145 (Digital 2), section 1

Recommended schedule

Day 1

Topics: *Latch circuits*
Questions: *1 through 10*
Lab Exercise: *S-R latch from individual gates (question 51)*
Demo: show switch bounce using a digital oscilloscope

Day 2

Topics: *555 timer circuit*
Questions: *11 through 20*
Lab Exercise: *555 timer in astable mode (question 52)*

Day 3

Topics: *Gated latch circuits*
Questions: *21 through 30*
Lab Exercise: *Troubleshooting practice (decade counter circuit – question 54)*

Day 4

Topics: *Flip-flops*
Questions: *31 through 40*
Lab Exercise: *Troubleshooting practice (decade counter circuit – question 54)*

Day 5

Topics: *Flip-flops (continued)*
Questions: *41 through 50*
Lab Exercise: *J-K flip-flop IC (question 53)*

Day 6

Exam 1: *includes S-R latch circuit performance assessment*
Lab Exercise: *Troubleshooting practice (decade counter circuit – question 54)*

Troubleshooting practice problems

Questions: *57 through 66*

DC/AC/Semiconductor/Opamp review problems

Questions: *67 through 86*

General concept practice and challenge problems

Questions: *87 through the end of the worksheet*

Impending deadlines

Troubleshooting assessment (counter circuit) due at end of ELTR145, Section 3
Question 55: Troubleshooting log
Question 56: Sample troubleshooting assessment grading criteria

ELTR 145 (Digital 2), section 1

Skill standards addressed by this course section

EIA *Raising the Standard; Electronics Technician Skills for Today and Tomorrow*, June 1994

F Technical Skills – Digital Circuits

F.11 Understand principles and operations of types of flip-flop circuits.
F.12 Fabricate and demonstrate types of flip-flop circuits.
F.13 Troubleshoot and repair flip-flop circuits.
F.17 Understand principles and operations of clock and timing circuits.
F.18 Fabricate and demonstrate clock and timing circuits.
F.19 Troubleshoot and repair clock and timing circuits.

B Basic and Practical Skills – Communicating on the Job

B.01 Use effective written and other communication skills. *Met by group discussion and completion of labwork.*
B.03 Employ appropriate skills for gathering and retaining information. *Met by research and preparation prior to group discussion.*
B.04 Interpret written, graphic, and oral instructions. *Met by completion of labwork.*
B.06 Use language appropriate to the situation. *Met by group discussion and in explaining completed labwork.*
B.07 Participate in meetings in a positive and constructive manner. *Met by group discussion.*
B.08 Use job-related terminology. *Met by group discussion and in explaining completed labwork.*
B.10 Document work projects, procedures, tests, and equipment failures. *Met by project construction and/or troubleshooting assessments.*

C Basic and Practical Skills – Solving Problems and Critical Thinking

C.01 Identify the problem. *Met by research and preparation prior to group discussion.*
C.03 Identify available solutions and their impact including evaluating credibility of information, and locating information. *Met by research and preparation prior to group discussion.*
C.07 Organize personal workloads. *Met by daily labwork, preparatory research, and project management.*
C.08 Participate in brainstorming sessions to generate new ideas and solve problems. *Met by group discussion.*

D Basic and Practical Skills – Reading

D.01 Read and apply various sources of technical information (e.g. manufacturer literature, codes, and regulations). *Met by research and preparation prior to group discussion.*

E Basic and Practical Skills – Proficiency in Mathematics

E.01 Determine if a solution is reasonable.
E.02 Demonstrate ability to use a simple electronic calculator.
E.06 Translate written and/or verbal statements into mathematical expressions.
E.07 Compare, compute, and solve problems involving binary, octal, decimal, and hexadecimal numbering systems.
E.12 Interpret and use tables, charts, maps, and/or graphs.
E.13 Identify patterns, note trends, and/or draw conclusions from tables, charts, maps, and/or graphs.
E.15 Simplify and solve algebraic expressions and formulas.
E.16 Select and use formulas appropriately.
E.21 Use Boolean algebra to break down logic circuits.

Common areas of confusion for students

Difficult concept: *Determining response of a state-dependent logic system.*

The very wording of this "difficult concept" may seem difficult to the reader! What I am saying here is that latches and flip-flops are difficult to figure out because their outputs not only depend on the logic levels of the inputs, but also on the *previous* output states. For this reason, these devices fall into the category of "state machines:" they "remember" what logic state they were last in.

I have but one tool for you to use in understanding state machine circuits: the lowly timing diagram. Truth tables fail to fully capture the essence of state machines unless they are expanded to include column(s) showing the last output(s) as well as the inputs. Timing diagrams keep a record of a circuit's last output states as you check to see what will happen for each new input condition. Learn how to draw and interpret timing diagrams, and you will have a powerful tool to apply toward the study of latches and flip-flop circuits!

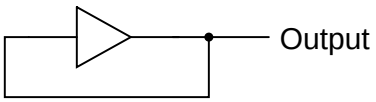
Difficult concept: *The time-constant equation.*

Many students find the time-constant equation difficult because it involves exponents, particularly exponents of Euler's constant e. This exponent is often expressed as a negative quantity, making it even more difficult to understand. The single most popular mathematical mistake I see students make with this equation is failing to properly follow algebraic order of operations. Some students try to overcome this weakness by using calculators which allow parenthetical entries, nesting parentheses in such a way that the calculator performs the proper order of operations. However, if you don't understand order of operations yourself, you will not know where to properly place the parentheses. If you have trouble with algebraic order of operations, there is no solution but to invest the necessary time and learn it!

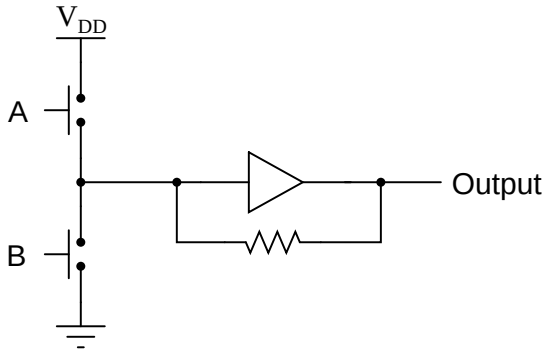
Beyond mathematical errors, though, the most common mistake I see students make with the time constant equation is mis-application. One version of this equation expresses increasing quantities, while another version expresses decreasing quantities. You must already know what the variables are going to do in your time-constant circuit before you know which equation to use! You must also be able to recognize one version of this equation from the other: not by memory, lest you should forget; but by noting what the result of the equation does as time (t) increases. Here again there will be trouble if you are not adept applying algebraic order of operations.

Question 1

What do you think this logic buffer gate will do, with the output signal "feeding back" to the input?



What do you think this buffer will do when each input switch is separately pressed?



Why does the second buffer circuit need a resistor in the feedback loop?
file 02896

Answer 1

The first circuit will "latch" in whatever logic state it powers up in. The second circuit will be "set" or "reset" according to which pushbutton switch is actuated, then latch in that state when neither switch is being pressed. The resistor prevents the gate from "seeing" a short circuit at its output when a pushbutton switch is actuated to change states.

Challenge question: how would you determine an appropriate size for the resistor? Don't just guess – base your answer on specific performance parameters of the gate!

Notes 1

This is a very crude sort of latch circuit, but it is easier to understand than the typical cross-connected NOR or NAND gate latches commonly introduced to circuits. One of the major ideas in this question is the concept of *positive feedback*, and how this form of feedback leads to hysteretic behavior. If appropriate, refer your students to SCRs and other thyristors as previous examples of hysteretic devices based on positive feedback.

Question 2

When studying latch circuits, you will come across many references to *set* and *reset* logic states. Give a simple definition for each of these terms in the context of latch and flip-flop circuits.

file 02897

Answer 2

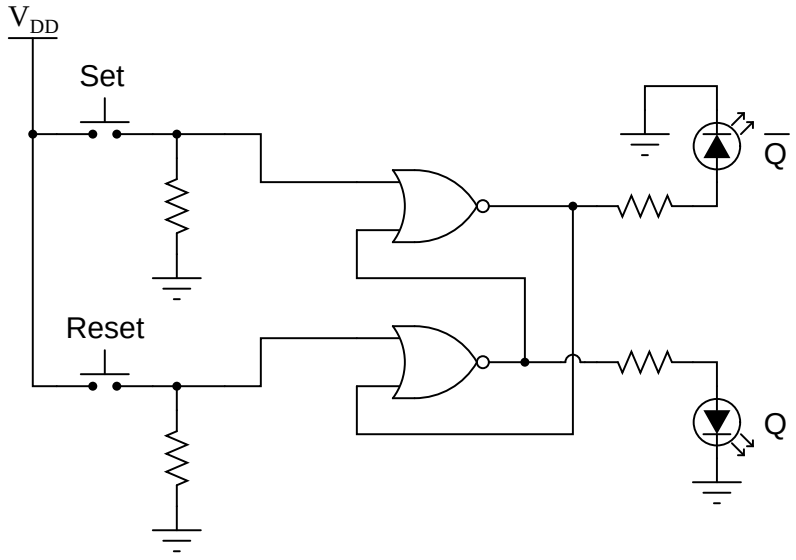
A latch is considered *set* when its output (Q) is high, and *reset* when its output (Q) is low.

Notes 2

Having a consistent definition for "set" and "reset" is important, especially as students study multiple latch circuit topologies and active-low inputs!

Question 3

The circuit shown here is called an *S-R latch*:



Complete the truth table for this latch circuit:

Set	Reset	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

file 01349

Answer 3

Set	Reset	Q	$\overline{Q}$
0	0	*Latch*	
0	1	0	1
1	0	1	0
1	1	0	0

Follow-up question: The final state of this truth table (where the "Set" and "Reset" inputs are both high) is usually referred to as *invalid*. Explain why.

Notes 3

The "latch" state is the most interesting in this circuit. Discuss what this means with your students, especially since it is impossible to describe the "latch" state in terms of fixed 1's and 0's.

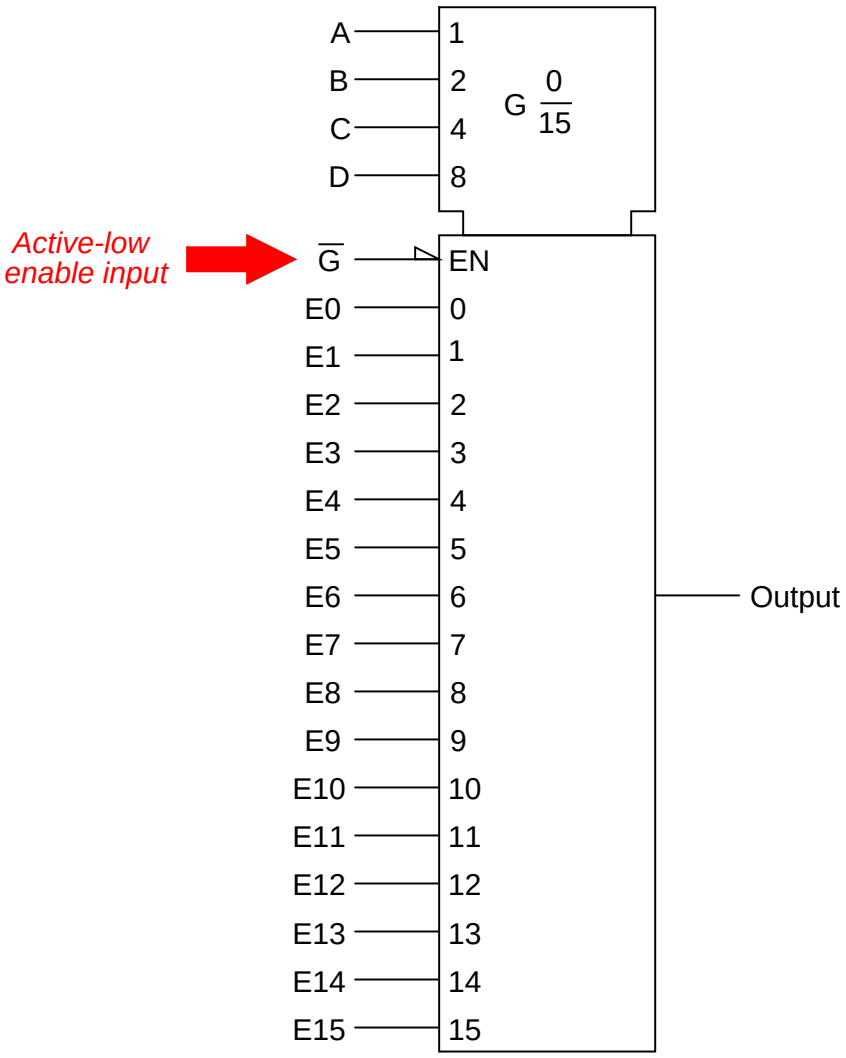
Question 4

Some digital circuits are considered to have *active-low* inputs, while others have *active-high* inputs. Explain what each of these terms means, and how we might identify which type of input(s) a digital circuit has.

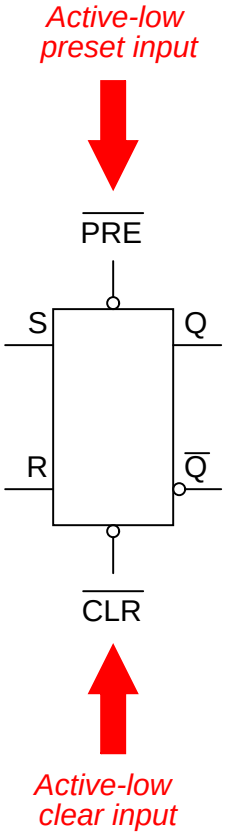
file 02898

Answer 4

An "active-low" input is one where that particular gate function is activated or invoked on a *low* logic state. Active-low inputs are identified by inversion bubbles (or inversion wedges) drawn at the IC input terminals. For example, the Enable input (EN) for the following integrated circuit is active-low, meaning the chip is enabled when that input line is held at ground potential:



This S-R latch circuit has active-low preset ($\overline{\text{PRE}}$) and clear ($\overline{\text{CLR}}$) inputs, meaning the latch circuit will be preset and cleared when each of these inputs are grounded, respectively:



Active-high inputs, conversely, engage their respective functions when brought to power supply rail (V_{DD} or V_{CC}) potential. As one might expect, an active-high input will *not* have an inversion bubble or wedge next to the input terminal.

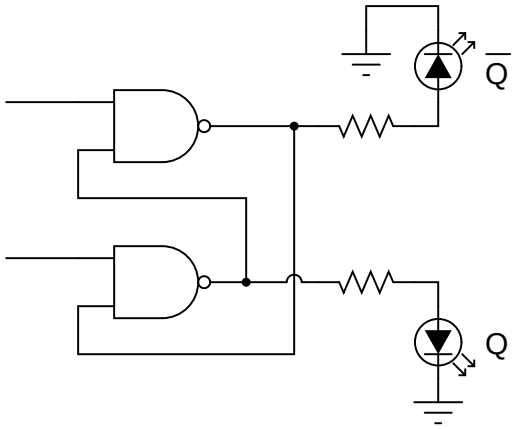
Challenge question: to the surprise of many students, there are a great number of digital logic circuit types built with active-low inputs. Explain why. Hint: most of these circuit types and functions were pioneered with TTL logic rather than CMOS logic.

Notes 4

Active-low inputs tend to confuse many students, hence my unusually long and descriptive answer.

Question 5

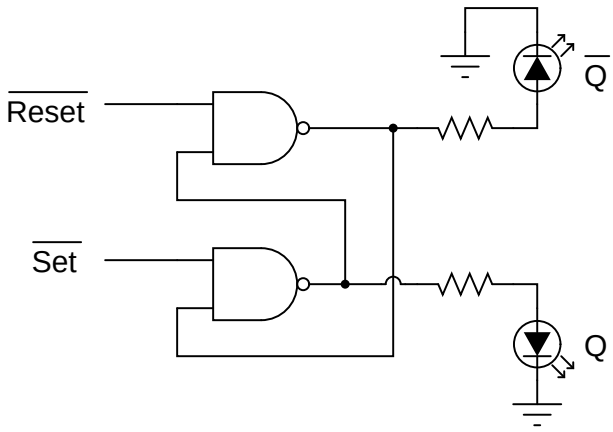
The circuit shown here is called an *S-R latch*:



Identify which of the two input lines is the *Set*, and which is the *Reset*, and then write a truth table describing the function of this circuit.

file 01351

Answer 5



$\overline{\text{Set}}$	$\overline{\text{Reset}}$	Q	$\overline{\text{Q}}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	*Latch*	

Follow-up question: why are the inputs referred to as $\overline{\text{Set}}$ and $\overline{\text{Reset}}$, rather than just Set and Reset?

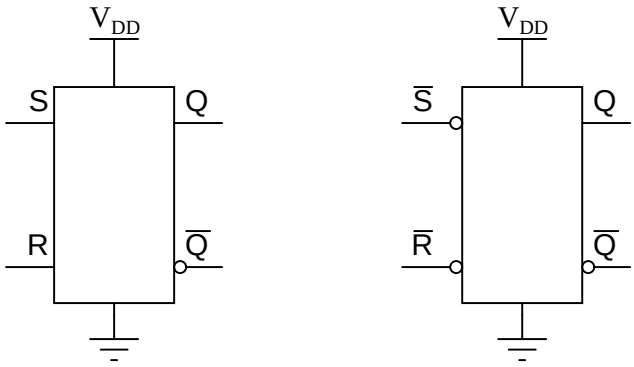
Notes 5

The "latch" state is the most interesting in this circuit. Discuss what this means with your students, especially since it is impossible to describe the "latch" state in terms of fixed 1's and 0's. Also ask your students to identify the "invalid" state of this latch circuit, and to explain why it is called "invalid".

Discuss the active-low nature of this latch circuit's inputs. Explain to your students that many digital functions have active-low inputs, and that it is common to denote those inputs by writing a Boolean complementation bar over the input's name.

Question 6

Latch circuits are often drawn as complete units in their own block symbols, rather than as a collection of individual gates:



This simplifies schematic drawings where latches are used, much as the use of gate symbolism (as opposed to drawing individual transistors and resistors) simplifies the diagrams of more elementary digital circuits.

From the block symbols shown in this question, is there any way to determine which of the S-R latches is built with NOR gates, and which one is built with NAND gates?

file 01352

Answer 6

This is a bit of a trick question. If NOR and NAND are the only gate choices available, then the left latch is made from NOR gates and the right latch is made from NAND gates. However, it is possible to make S-R latches out of gates other than NOR or NAND.

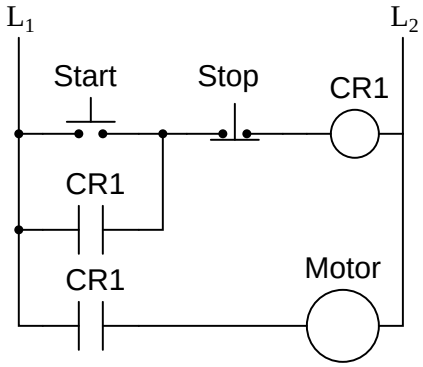
Challenge question: can you think of other gate types that could be used to build S-R latch circuits? Hint: there are at least *two* alternatives to NOR and NAND!

Notes 6

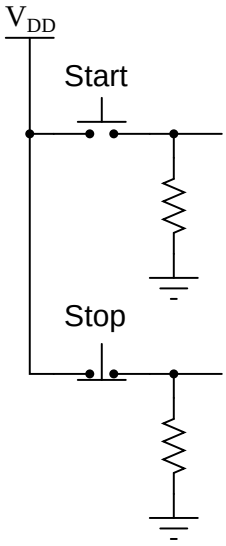
If students become stuck on the challenge question, just whisper "DeMorgan's Theorem" to them and watch what happens!

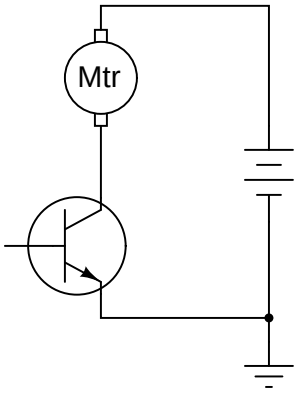
Question 7

The following relay logic circuit is for starting and stopping an electric motor:



Draw the CMOS logic gate equivalent of this motor start-stop circuit, using these two pushbutton switches as inputs:

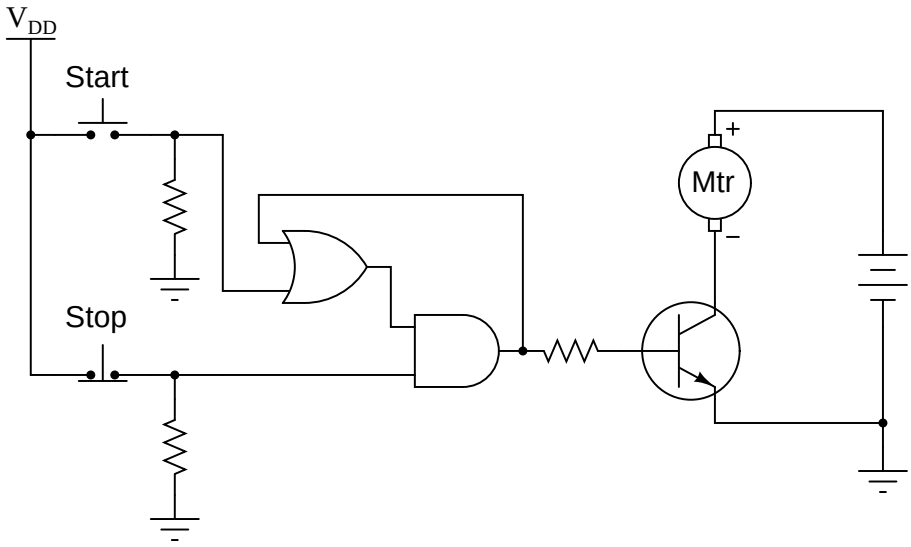




Make sure that your schematic is complete, showing how the logic gate will drive the electric motor (through the power transistor shown).

file 01348

Answer 7



Follow-up question: why is the "Stop" switch always normally-closed in motor control circuits, whether it be relay logic or semiconductor logic? It is easy enough to invert a signal if we wish to, either by using a relay or by using a NOT gate, so shouldn't the choice of switch "normal" status be arbitrary?

Challenge question: why not operate the electric motor off the same V_{DD} power source that the gates are powered by? If we had to do such a thing, what circuit additions would you propose to minimize any potential trouble?

Notes 7

Discuss the follow-up question with your students. Why is the "Stop" switch always normally-closed, if we have the freedom to choose normally-open contacts? Why not standardize the pushbutton switches, making them both the same type? The answer has to do with circuit faults, and what is considered the safest mode of failure.

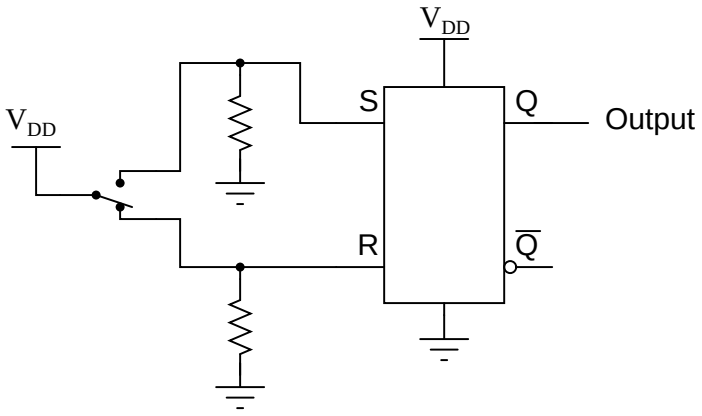
I suspect many students will neglect to include the base resistor in their designs. This resistor is important, though, for the sake of the driving gate. You might even want to spend some class time with your students calculating an appropriate value of resistance, given such parameters as:

- Motor "run" current = 300 mA
- Transistor $\beta = 50$
- $V_{DD} = 6$ volts DC

The challenge question may be too advanced for students who have not yet experienced the pains of trying to operate power devices and logic devices off the same DC bus. Suffice it to say, it is a good design rule to keep separate DC power supplies for logic and load circuitry, even if they are the exact same voltage!

Question 8

One practical application of S-R latch circuits is *switch debouncing*. Explain what "bounce" refers to in mechanical switches, and also explain how this circuit eliminates it:



Also, show where an oscilloscope could be connected to display any switch "bounce," and explain how the oscilloscope would have to be configured to capture this transient event.

file 01353

Answer 8

The "latching" ability of the S-R latch circuit holds the output state steady during the mechanical switch's bouncing action, allowing a "clean" output transition to take place.

Connecting the input probe of an oscilloscope to either the S or R input of the latch will show bounce, if it occurs. To capture this event, the 'scope would have to be configured for single-sweep mode, and have the triggering controls properly set. A digital storage oscilloscope is essential for this type of work!

Follow-up question: how do you suggest choosing appropriate pull-down resistor sizes for this circuit, or any CMOS circuit for that matter?

Notes 8

Many textbooks use switch debouncing as a practical example of S-R latch function, so I won't bother giving hints as to how this circuit works. Let the students do their own research, and let them explain it to you during discussion.

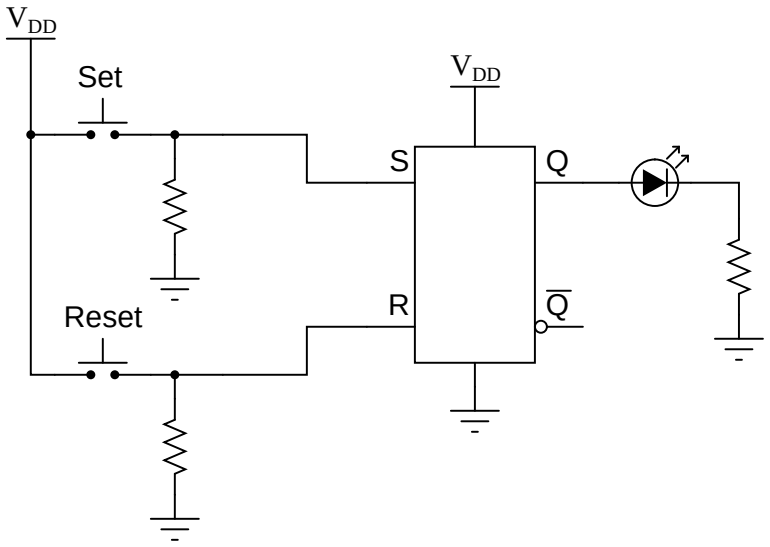
If students need practical examples of how switch "bouncing" can be bad, suggest digital counter circuits, where a mechanical switch causes a counter to increment (or decrement) once per actuation. If the switch bounces, the counter will increment (or decrement) more than once per switch actuation, which is undesirable.

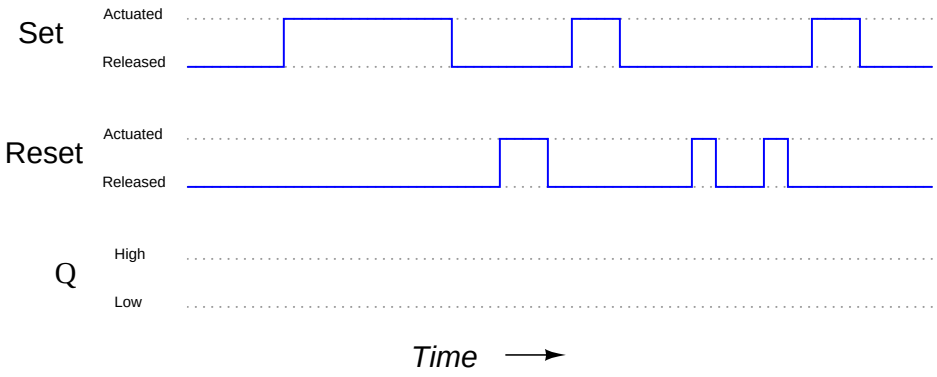
Oscilloscope triggering is one of those features that separates novice 'scope users from competent 'scope users. Anyone can learn to display a repetitive waveform on an oscilloscope with a minimum of adjustment. Many modern digital oscilloscopes even have "auto-configure" features to lock in such waveforms for display. However, to set up triggering on one-time events requires that the user understand not only the oscilloscope's functions, but also the nature of the event to be captured.

Note to your students how the $\overline{Q}$ output of the latch doesn't go anywhere. Often, we have applications where the second output of a latch is unused. Ask your students whether or not this constitutes a problem. (If you get blank stares from asking this question, remind students that unused CMOS inputs have to be grounded or tied to V_{DD}, or else damage may occur. Ask them whether or not the same rule applies to gate outputs.) This will be a good review of internal gate circuit construction.

Question 9

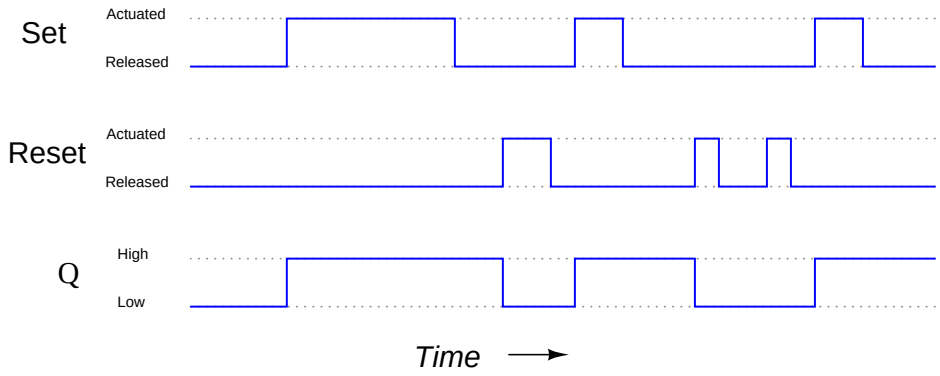
Complete the timing diagram, showing the state of the Q output over time as the Set and Reset switches are actuated. Assume that Q begins in the low state on power-up:



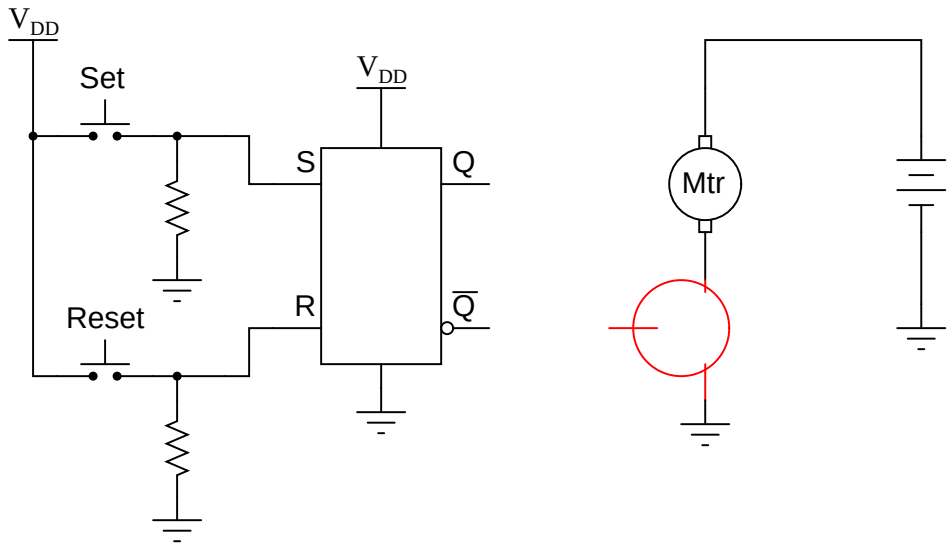


file 02899

Answer 9



Follow-up question: complete a schematic diagram showing how the $\overline{Q}$ output of the latch could turn on an electric motor through a bipolar junction transistor. Also, determine whether the latch circuit would be *sourcing* or *sinking* current to the transistor when the motor is running:

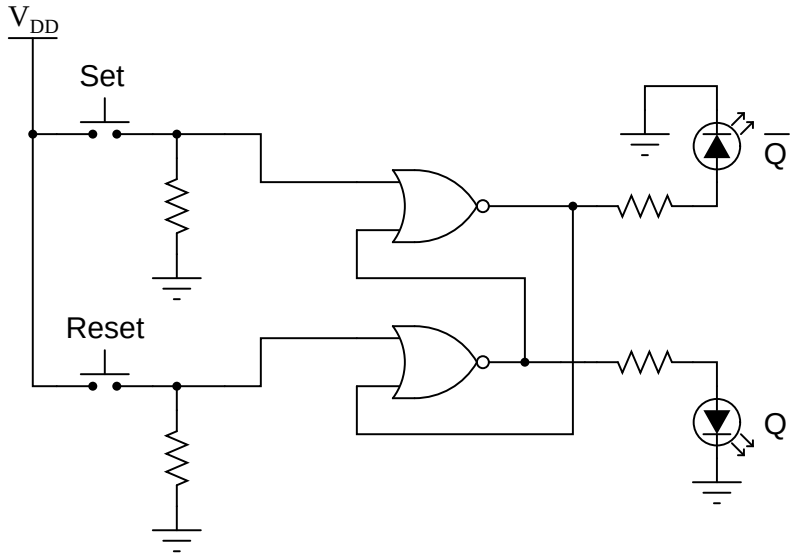


Notes 9

Nothing special here in this question. Perhaps the main point is to familiarize students with the concept of a timing diagram, and how to transfer the truth table function of a specific logic circuit to a time-domain plot.

Question 10

A student builds this simple S-R latch for their lab experiment:



When the student powers up this circuit, she notices something strange. Sometimes the latch powers up in the *set* state (Q high and $\overline{Q}$ low), and other times it powers up in the *reset* state (Q low and $\overline{Q}$ high). The power-up state of their circuit seems to be unpredictable.

What state *should* their circuit power up in? Did the student make an error building the latch circuit?

file 01378

Answer 10

The circuit is fine, and working properly. The normal power-up state of a latch circuit is unpredictable, so long as both the inputs are inactive.

Notes 10

Although the circuit itself is simple, the phenomenon is not. Tell your students that what they're dealing with here is something called a *race condition*, where two or more gates try to "race" each other to reach a certain logic state. Analyze the power-up state of this circuit with your students, and they will see that an unstable condition exists when both inputs are inactive!

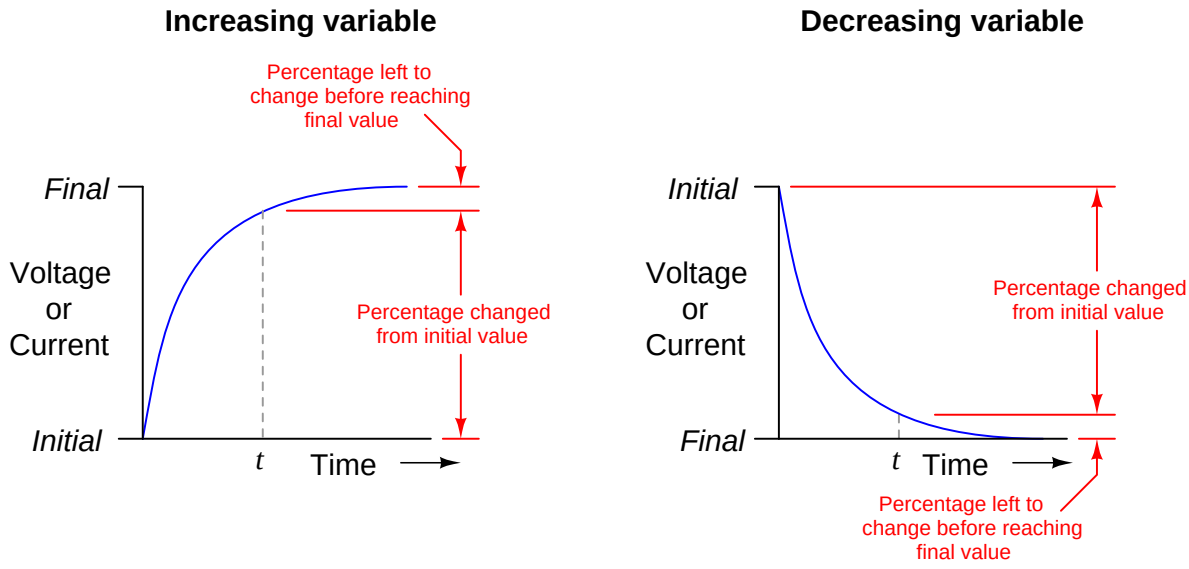
Question 11

The following expression is frequently used to calculate values of changing variables (voltage and current) in RC and LR timing circuits:

$$e^{-\frac{t}{\tau}} \qquad \text{or} \qquad \frac{1}{e^{\frac{t}{\tau}}}$$

If we evaluate this expression for a time of $t = 0$, we find that it is equal to 1 (100%). If we evaluate this expression for increasingly larger values of time ($t \to \infty$), we find that it approaches 0 (0%).

Based on this simple analysis, would you say that the expression $e^{-\frac{t}{\tau}}$ describes the percentage that a variable has changed from its initial value in a timing circuit, or the percentage that it has *left* to change before it reaches its final value? To frame this question in graphical terms . . .



Which percentage does the expression $e^{-\frac{t}{\tau}}$ represent in each case? Explain your answer.

file 02946

Answer 11

Whether the variable in question is increasing or decreasing over time, the expression $e^{-\frac{t}{\tau}}$ describes the percentage that a variable has left to change before it reaches its final value.

Follow-up question: what could you add to or modify about the expression to make it describe the percentage that a variable has already changed from its initial value? In other words, alter the expression so that it is equal to 0% at $t = 0$ and approaches 100% as t grows larger ($t \to \infty$).

Notes 11

It is very important for students to understand what this expression means and how it works, lest they rely solely on memorization to use it in their calculations. As I always tell my students, rote memorization *will* fail you! If a student does not comprehend why the expression works as it does, they will be helpless to retain it as an effective "tool" for performing calculations in the future.

A good way to suggest students approach a problem such as this is to imagine t increasing in value. As t grows larger, what happens to the expression's overall value? Then, compare which of the two percentages (percentage traversed, or percentage remaining) follow the same trend. One not need touch a calculator to figure this out!

Question 12

Calculate the voltage across a 470 μF capacitor after discharging through a 10 kΩ resistor for 9 seconds, if the capacitor's original voltage (at $t = 0$) was 24 volts.

Also, express this amount of time (9 seconds) in terms of how many *time constants* have elapsed.

file 00452

Answer 12

$E_C = 3.537$ volts @ $t = 9$ seconds.

9 s = 1.915 time constants (1.915τ)

Notes 12

Here, students must choose which equation to use for the calculation, calculate the time constant for the circuit, and put all the variables in the right place to obtain the correct answer. Discuss all these steps with your students, allowing them to explain how they approached the question.

Question 13

Calculate the amount of time it takes for a 33 μF capacitor to charge from 0 volts to 20 volts, if powered by a 24 volt battery through a 10 kΩ resistor.

file 01814

Answer 13

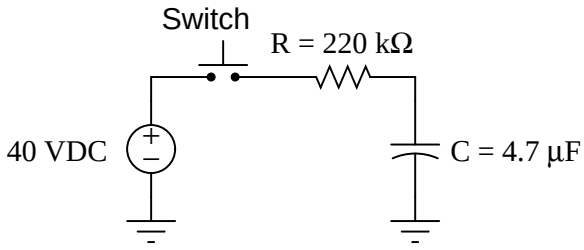
0.591 seconds

Notes 13

In order for students to solve this problem, they must algebraically manipulate the "normal" time-constant formula to solve for time instead of solving for voltage.

Question 14

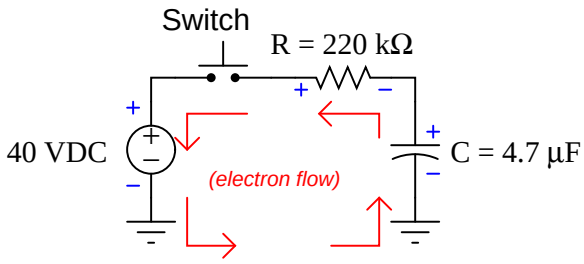
Determine the amount of time needed after switch closure for the capacitor voltage (V_C) to reach the specified levels:



V_C	Time
0 volts	
10 volts	
20 volts	
30 volts	
40 volts	

Trace the direction of electron flow in the circuit, and also mark all voltage polarities.
file 02942

Answer 14



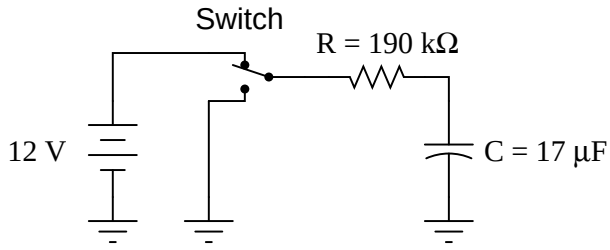
V_C	Time
0 volts	0 ms
10 volts	297.5 ms
20 volts	716.7 ms
30 volts	1.433 s
40 volts	> 5 s

Notes 14

Some students may write 5.17 seconds as the time required to charge to 40 volts (5 time constants' worth of time). If so, remind them that the "standard" of 5τ is arbitrary, and that theoretically the capacitor *never* actually reaches full charge.

Question 15

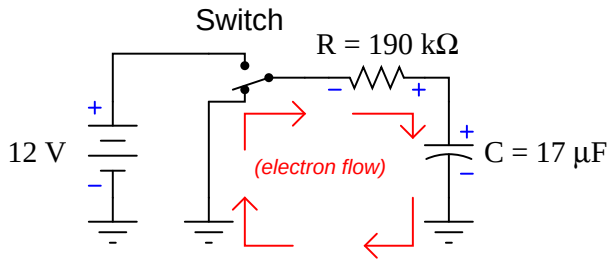
Determine the amount of time needed for the capacitor voltage (V_C) to fall to the specified levels after the switch is thrown to the "discharge" position, assuming it had first been charged to full battery voltage:



V_C	Time
10 volts	
8 volts	
6 volts	
4 volts	
2 volts	

Trace the direction of electron flow in the circuit, and also mark all voltage polarities.
file 02943

Answer 15



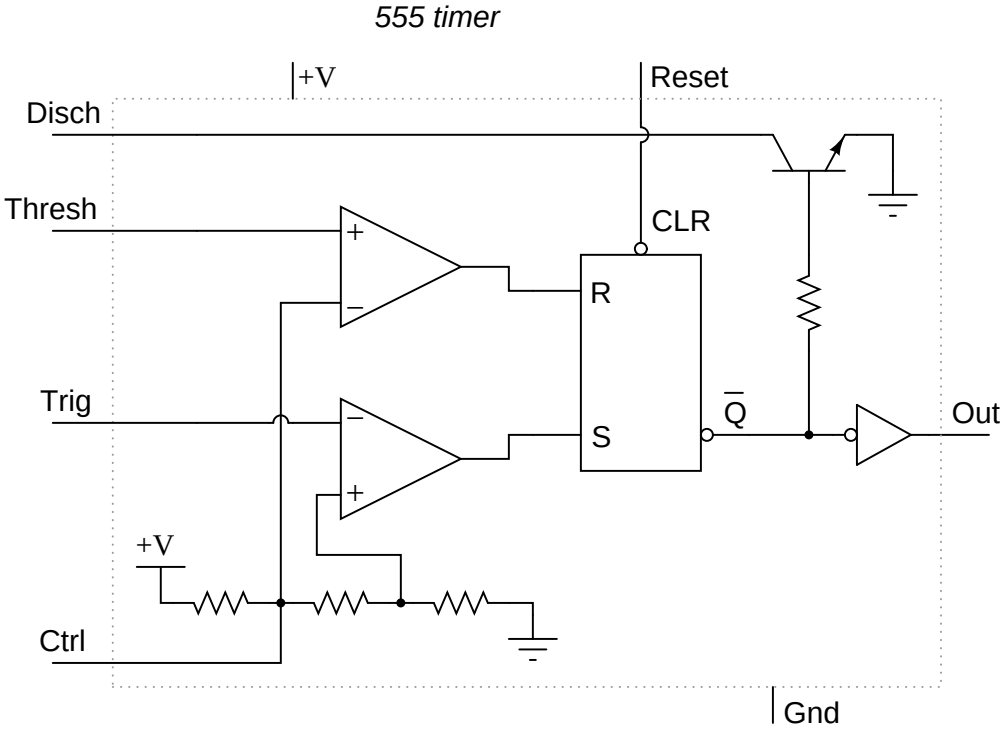
V_C	Time
10 volts	588.9 ms
8 volts	1.31 s
6 volts	2.24 s
4 volts	3.55 s
2 volts	5.79 s

Notes 15

Ask your students to explain how they set up each calculation.

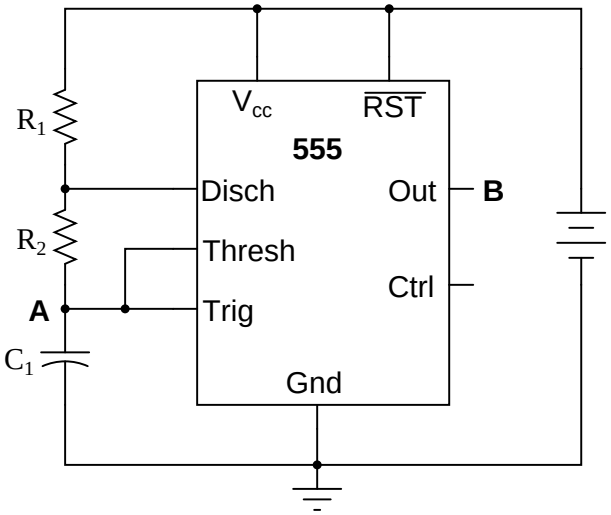
Question 16

The type "555" integrated circuit is a highly versatile *timer*, used in a wide variety of electronic circuits for time-delay and oscillator functions. The heart of the 555 timer is a pair of comparators and an S-R latch:

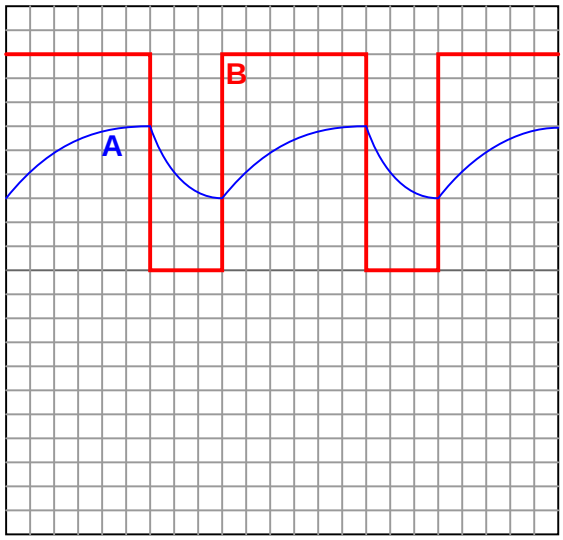


The various inputs and outputs of this circuit are labeled in the above schematic as they often appear in datasheets ("Thresh" for *threshold*, "Ctrl" or "Cont" for *control*, etc.).

To use the 555 timer as an astable multivibrator, simply connect it to a capacitor, a pair of resistors, and a DC power source as such:



If were were to measure the voltage waveforms at test points **A** and **B** with a dual-trace oscilloscope, we would see the following:



Explain what is happening in this astable circuit when the output is "high," and also when it is "low." file 01418

Answer 16

When the output is high, the capacitor is charging through the two resistors, its voltage increasing. When the output is low, the capacitor is discharging through one resistor, current sinking through the 555's "Disch" terminal.

Follow-up question: algebraically manipulate the equation for this astable circuit's operating frequency, so as to solve for R_2.

$$f = \frac{1}{(\ln 2)(R_1 + 2R_2)C}$$

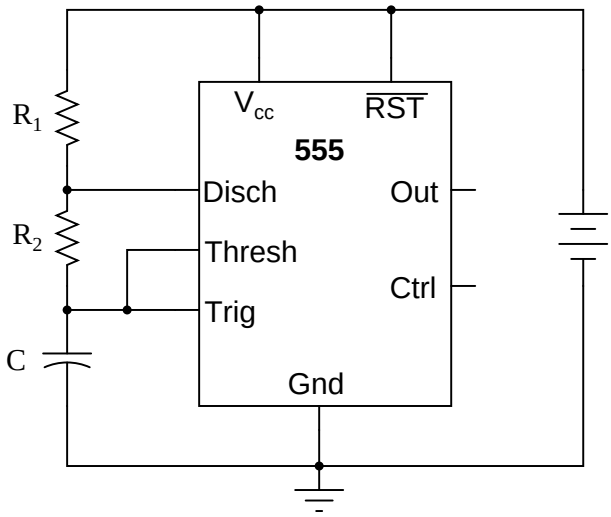
Challenge question: explain why the duty cycle of this circuit's output is always greater than 50%.

Notes 16

This popular configuration of the 555 integrated circuit is well worth spending time analyzing and discussing with your students.

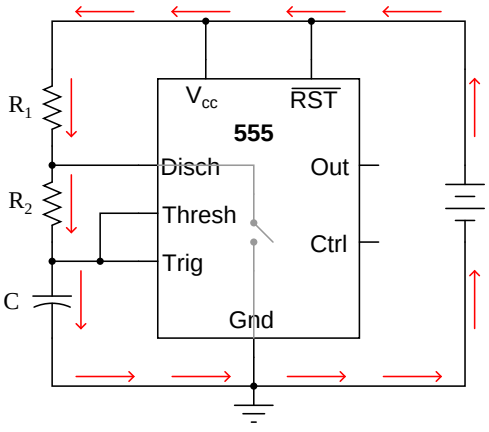
Question 17

The model "555" integrated circuit is a very popular and useful "chip" used for timing purposes in electronic circuits. The basis for this circuit's timing function is a resistor-capacitor (RC) network:

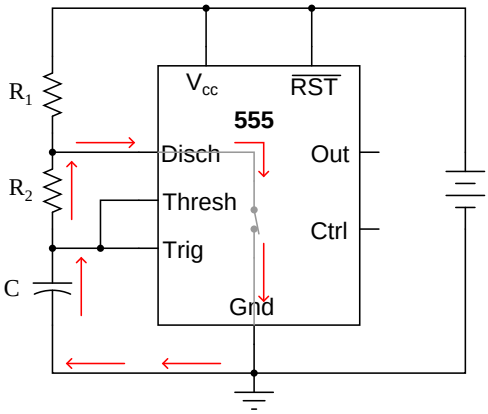


In this configuration, the "555" chip acts as an *oscillator*: switching back and forth between "high" (full voltage) and "low" (no voltage) output states. The time duration of one of these states is set by the charging action of the capacitor, through both resistors (R_1 and R_2 in series). The other state's time duration is set by the capacitor discharging through one resistor (R_2):

Capacitor charging through R1 and R2 (series)



Capacitor discharging through R2 only



Note: all currents shown in the direction of conventional flow

Obviously, the charging time constant must be $\tau_{charge} = (R_1+R_2)C$, while the discharging time constant is $\tau_{discharge} = R_2C$. In each of the states, the capacitor is either charging or discharging 50% of the way between its starting and final values (by virtue of how the 555 chip operates), so we know the expression $e^{\frac{-t}{\tau}} = 0.5$, or 50 percent.†

† For those who must know why, the 555 timer in this configuration is designed to keep the capacitor voltage cycling between $\frac{1}{3}$ of the supply voltage and $\frac{2}{3}$ of the supply voltage. So, when the capacitor is

Develop two equations for predicting the "charge" time and "discharge" time of this 555 timer circuit, so that anyone designing such a circuit for specific time delays will know what resistor and capacitor values to use.

file 01807

Answer 17

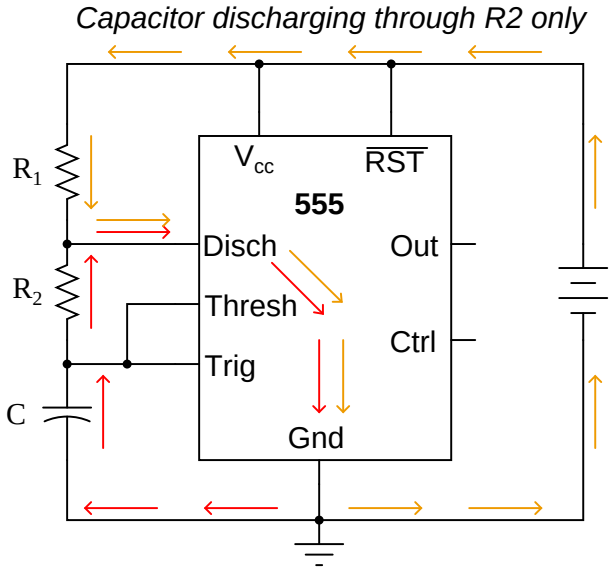
$$t_{charge} = -\ln 0.5(R_1 + R_2)C$$

$$t_{discharge} = -\ln 0.5 R_2 C$$

Notes 17

Although it may seem premature to introduce the 555 timer chip when students are just finishing their study of DC, I wanted to provide a practical application of RC circuits, and also of algebra in generating useful equations. If you deem this question too advanced for your student group, by all means skip it.

Incidentally, I simplified the diagram where I show the capacitor discharging: there is actually another current at work here. Since it wasn't relevant to the problem, I omitted it. However, some students may be adept enough to catch the omission, so I show it here:



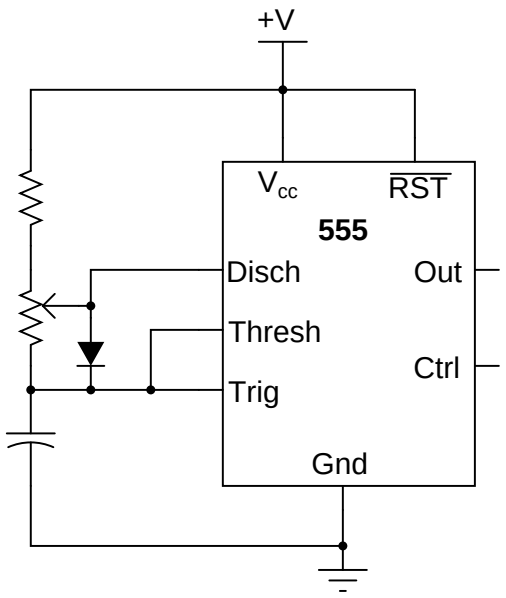
Note that this second current (through the battery) does not go anywhere near the capacitor, and so is irrelevant to the discharge cycle time.

---

charging from $\frac{1}{3}V_{CC}$ to its (final) value of full supply voltage (V_{CC}), having this charge cycle interrupted at $\frac{2}{3}V_{CC}$ by the 555 chip constitutes charging to the half-way point, since $\frac{2}{3}$ of half-way between $\frac{1}{3}$ and 1. When discharging, the capacitor starts at $\frac{2}{3}V_{CC}$ and is interrupted at $\frac{1}{3}V_{CC}$, which again constitutes 50% of the way from where it started to where it was (ultimately) headed.

Question 18

This astable 555 circuit has a potentiometer allowing for variable duty cycle:



With the diode in place, the output waveform's duty cycle may be adjusted to less than 50% if desired. Explain why the diode is necessary for that capability. Also, identify which way the potentiometer wiper must be moved to decrease the duty cycle.

file 01419

Answer 18

The diode allows part of the potentiometer's resistance to be bypassed during the capacitor's charging cycle, allowing (potentially) less resistance in the charging circuit than in the discharging circuit.

To decrease the duty cycle, move the wiper up (toward the fixed resistor, away from the capacitor).

Challenge question: write an equation solving for the average current drawn by the 555 timer circuit as it charges and discharges the capacitor while generating a 50% duty cycle pulse. Assume that no current is drawn from the power supply by the circuit while the capacitor is discharging, and use this approximation of the capacitor "Ohm's Law" equation for figuring average current through the charge cycle:

$$i = C\frac{dv}{dt} \quad \text{True "Ohm's Law" for a capacitor}$$

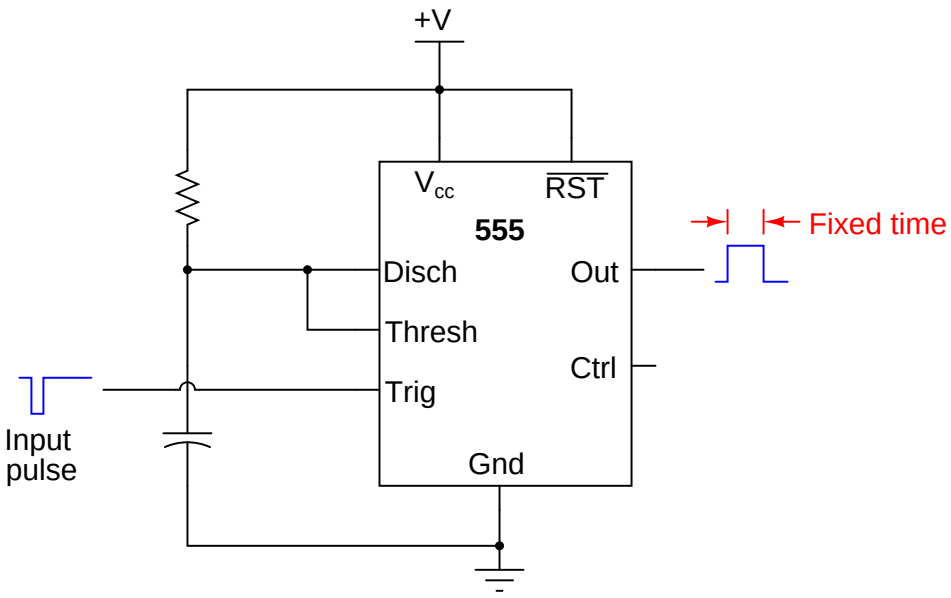
$$I_{avg} = C\frac{\Delta V}{\Delta t} \quad \text{Capacitive "Ohm's Law" solving for } \textit{average} \text{ current}$$

Notes 18

This question really probes students' conceptual understanding of the 555 timer, used as an astable multivibrator (oscillator). If some students just can't seem to grasp the function of the diode, illuminate their understanding by having them trace the charging and discharging current paths. Once they understand which way current goes in both cycles of the timer, they should be able to recognize what the diode does and why it is necessary.

Question 19

A popular use of the 555 timer is as a *monostable* multivibrator. In this mode, the 555 will output a pulse of fixed length when commanded by an input pulse:



How low does the triggering voltage have to go in order to initiate the output pulse? Also, write an equation specifying the width of this pulse, in seconds, given values of R and C. Hint: the magnitude of the supply voltage is irrelevant, so long as it does not vary during the capacitor's charging cycle. Show your work in obtaining the equation, based on equations of RC time constants. Don't just copy the equation from a book or datasheet!

file 01420

Answer 19

The triggering pulse must dip below $\frac{1}{3}$ of the supply voltage in order to initiate the timing sequence.

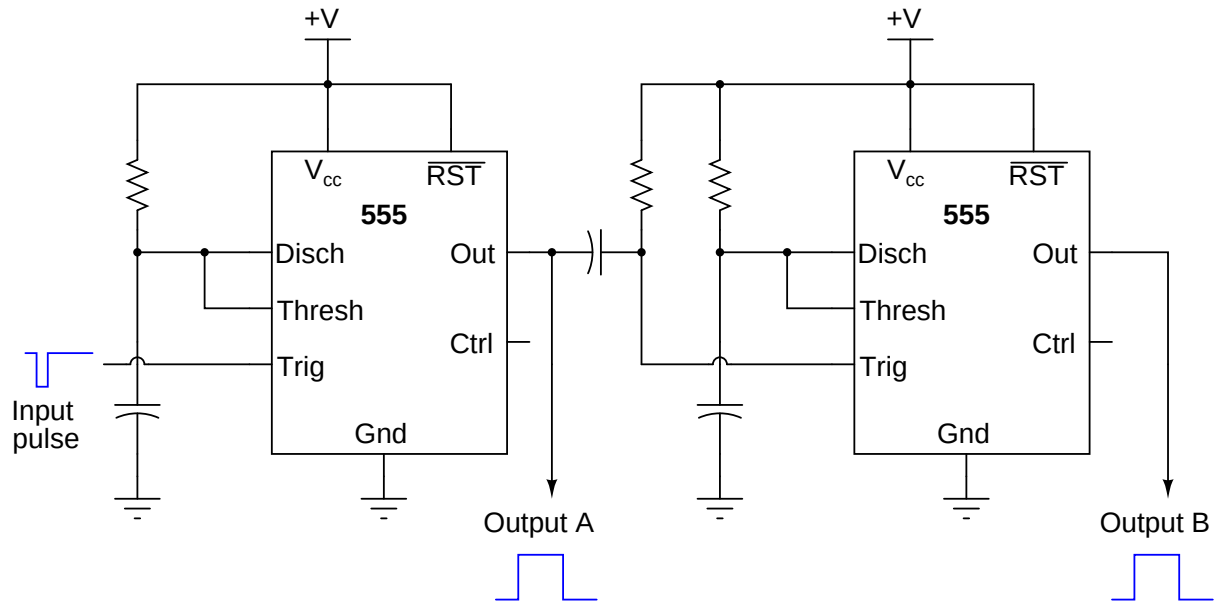
$$t_{pulse} = 1.1RC$$

Notes 19

Have your students show you how they mathematically derived their answer based on their knowledge of how capacitors charge and discharge. Many textbooks and datasheets provide this same equation, but it is important for students to be able to derive it themselves from what they already know of capacitors and RC time constants. Why is this important? Because in ten years they won't remember this specialized equation, but they will probably still remember the general time constant equation from all the time they spent learning it in their basic DC electricity courses (and applying it on the job). My motto is, "never remember what you can figure out."

Question 20

A *sequential* timer circuit may be constructed from multiple 555 timer ICs cascaded together. Examine this circuit and determine how it works:



Can you think of any practical applications for a circuit such as this?
file 02944

Answer 20

Each 555 timer's cycle is triggered by the negative edge of the pulse on the *trigger* terminal. A passive differentiator network between each 555 timer ensures that only a brief negative-going pulse is sent to the trigger terminal of the next timer from the output terminal of the one before it.

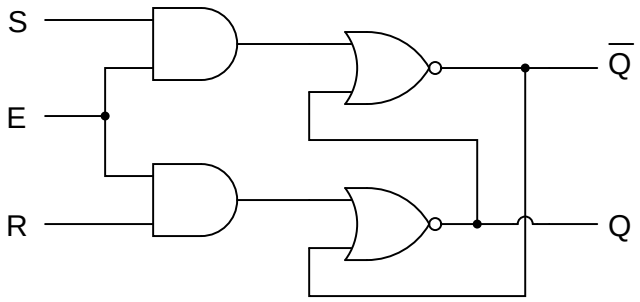
Follow-up question: when timer circuits are cascaded like this, do their time delays *add* or *multiply* to make the total delay time? Be sure to explain your reasoning.

Notes 20

Practical applications abound for such a circuit. One whimsical application is to energize sequential tail-light bulbs for an automobile, to give an interesting turn-signal visual effect. A sequential timer circuit was used to do just this on certain years of (classic) Ford Cougar cars. Other, more utilitarian, applications for sequential timers include start-up sequences for a variety of electronic systems, traffic light controls, and automated household appliances.

Question 21

The circuit shown here is a *gated* S-R latch. Write the truth table for this latch circuit, and explain the function of the "Enable" (E) input:



E	S	R	Q	$\overline{Q}$
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

file 01354

Answer 21

When the Enable input is low (0), the circuit ignores the Set and Reset inputs:

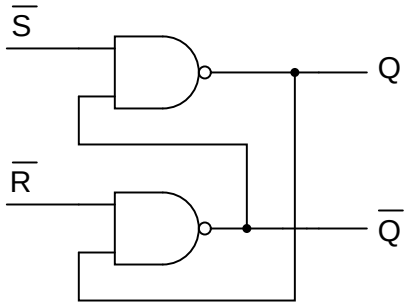
E	S	R	Q	$\overline{Q}$
0	0	0	*Latch*	
0	0	1	*Latch*	
0	1	0	*Latch*	
0	1	1	*Latch*	
1	0	0	*Latch*	
1	0	1	0	1
1	1	0	1	0
1	1	1	0	0

Notes 21

Just one more level of gating added to an S-R latch circuit!

Question 22

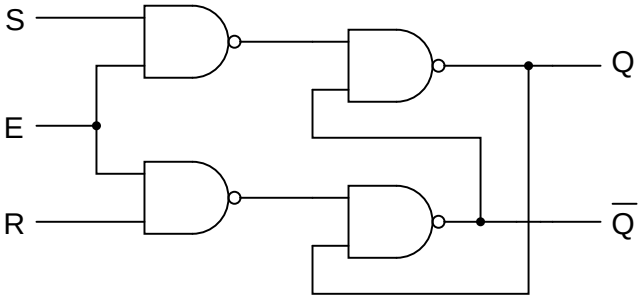
Here is an S-R latch circuit, built from NAND gates:



Add two more NAND gates to this circuit, converting it into a *gated* S-R latch, with an Enable (E) input, and write the truth table for the new circuit.

file 01355

Answer 22



E	S	R	Q	$\overline{Q}$
0	0	0	*Latch*	
0	0	1	*Latch*	
0	1	0	*Latch*	
0	1	1	*Latch*	
1	0	0	*Latch*	
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

Follow-up question: explain why the inputs to the latch circuit are not active-low as they were before the addition of the two extra NAND gates. In other words, why does this latch now have S and R inputs rather than $\overline{S}$ and $\overline{R}$ inputs as it did before?

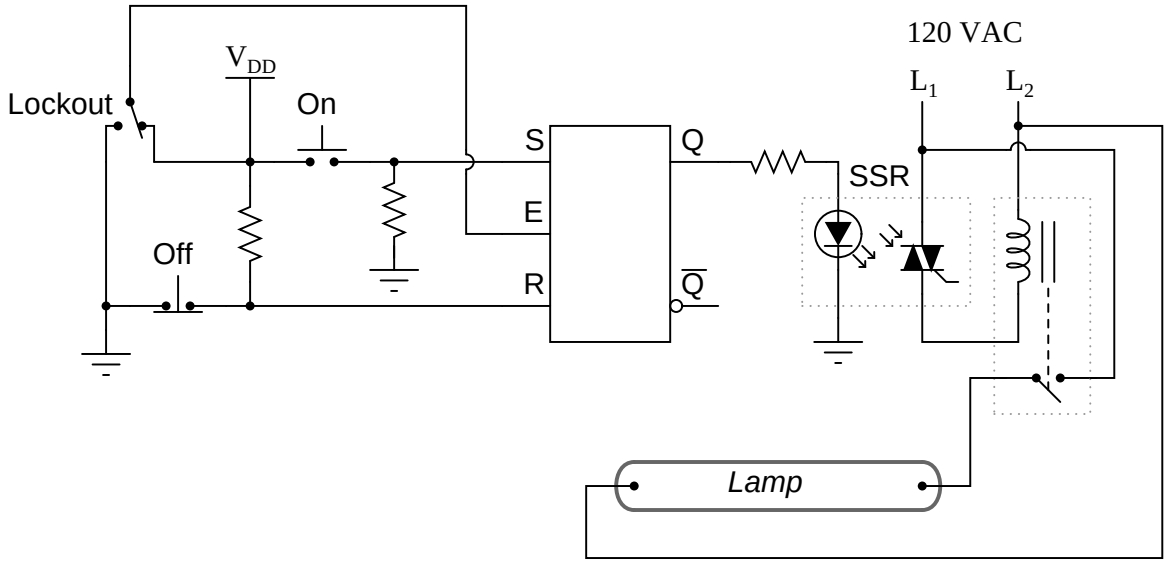
Notes 22

Ask your students if they see any practical advantage to this latch circuit over a gated latch built from NOR gates. What if they had to build a latch circuit from individual gates, rather than as a complete integrated circuit in and of itself? Would one design be preferable over the other?

Then, ask your students to compare the truth tables of the two different types of gated latches. Is there any difference in operation at all between the latch built with NAND gates and the latch built with NOR gates?

Question 23

Here, a gated S-R latch is being used to control the electric power to a powerful ultraviolet lamp, used for sterilization of instruments in a laboratory environment:



Based on your knowledge of how gated S-R latches function, what is the purpose of the "Lockout" switch? Also, explain how the CMOS latch is able to exert control over the high-power lamp (i.e. explain the operation of the interposing devices between the latch and the lamp).

Now, suppose the lab personnel want to add a feature to the ultraviolet sterilization chamber: an electric solenoid door lock, so that personnel can open the door to the chamber only if the following conditions are met:

- Lamp is *off*
- "Lockout" switch is sending a "low" signal to the latch's Enable input

Modify this circuit so that it energizes the door lock solenoid, allowing access to the chamber, only if the above conditions are both true.

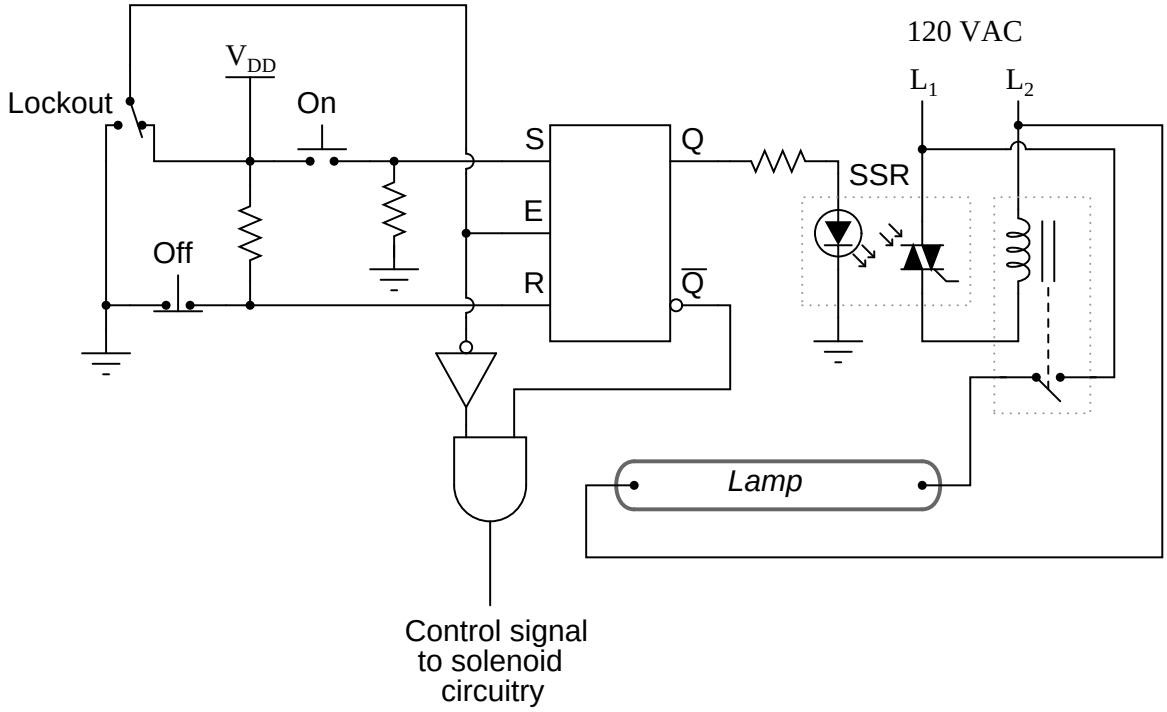
file 01356

Answer 23

The "Lockout" switch effectively disables the "On" and "Off" controls when it sends a "low" signal to the latch's Enable input.

This circuit uses both a solid-state relay (SSR) and an electromechanical relay for interposing between the latch and the lamp. These devices allow the low-power latch circuit to exert control over the high-power lamp.

Here is one possibility for the door lock control:



Follow-up question: there are better (safer) ways to accomplish this same function. For instance, suppose the TRIAC inside the SSR were to fail shorted, maintaining power to the lamp even when the latch goes into the "reset" mode. Would the door-lock logic shown here prevent someone from opening the door and getting exposed to the strong ultraviolet light? Explain your answer!

Challenge question: why not just use one interposing device: either an SSR, or an electromagnetic relay? Why *both* types of devices in the same circuit?

Notes 23

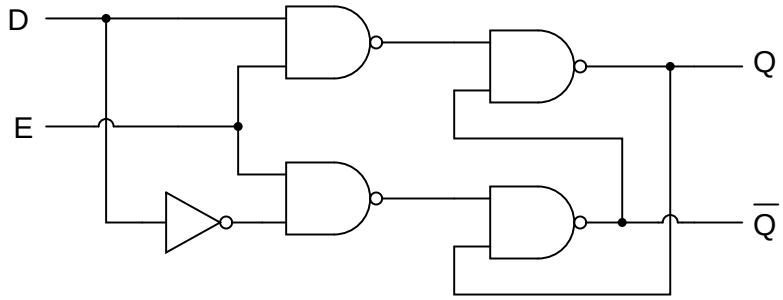
The purpose of the "Lockout" switch is fairly simple, and should be easy for the students to explain. On the other hand, the design and implementation of a door lock safety circuit is a more complex question, deserving of discussion because it involves several important and realistic considerations:

- How do we go from a simple verbal description of logical conditions (lamp off, enable low) to an actual gate circuit?
- What is the safest strategy to use in determining when it is safe to open the door?
- How should the door lock logic interpose to the solenoid itself (this is not shown in the answer!)?
- How would the principles of lock-out/tag-out apply to this system, if we were approaching the problem from the perspective of maintenance personnel rather than lab (operations) personnel?

The challenge question gets students thinking in terms of real-life currents and voltages, and the limitations of each device.

Question 24

A variation on the gated S-R latch circuit is something called the *D-latch*:



E	D	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

Complete the truth table for this D latch circuit, and identify which rows in the truth table represent the *set*, *reset*, and *latch* states, respectively.

file 01357

Answer 24

E	D	Q	$\overline{Q}$	
0	0	*Latch*		
0	1	*Latch*		
1	0	0	1	*Reset*
1	1	1	0	*Set*

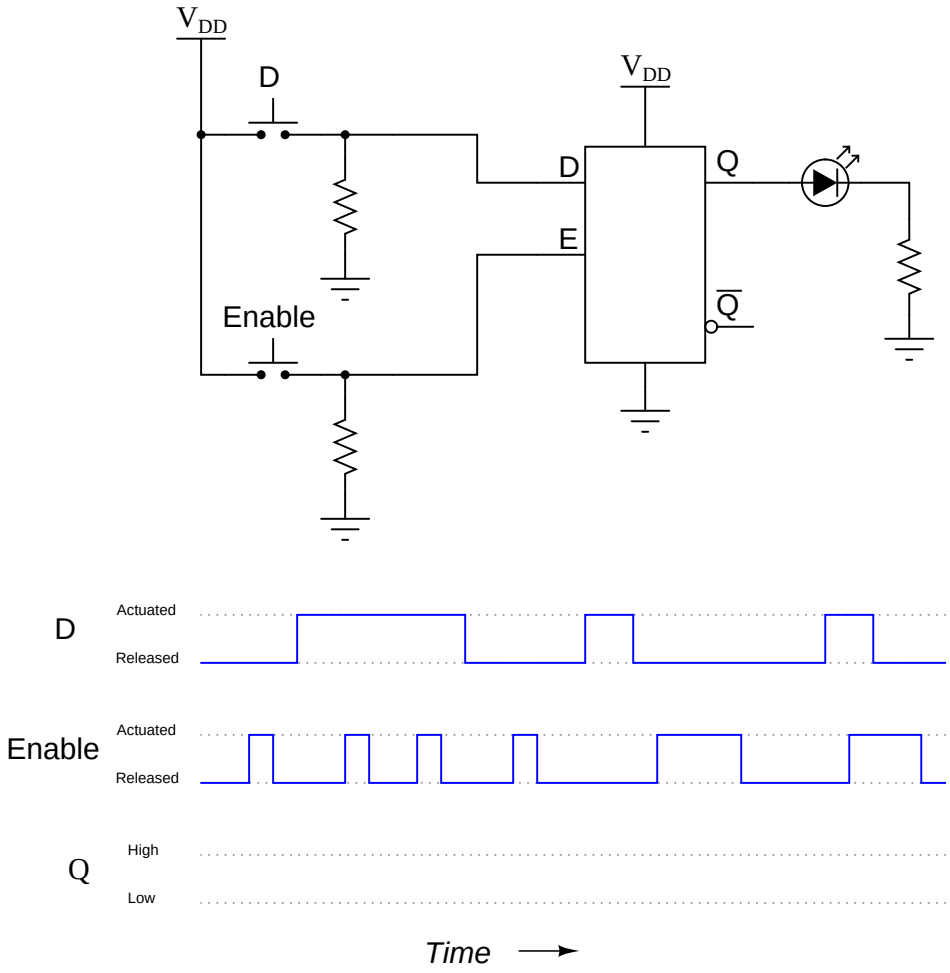
Notes 24

Since this gate does not actually have "Set" and "Reset" inputs, ask your students to explain what conditions define the "set" and "reset" states. Note that these state labels may be applied to *any* type of latch circuit.

To many of your students, this latch circuit may seem rather useless. Explain to them that this basic latch may be used to form *memory cells*, with each D latch storing 1 binary bit of information! Ask your students to explain, in their own words, how the latching action of this circuit constitutes a memory function. Under what condition(s) will the stored information in a D latch memory cell be lost?

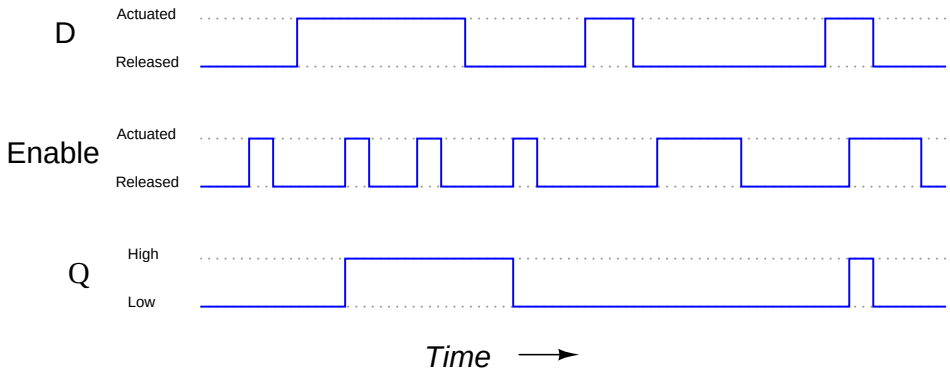
Question 25

Complete the timing diagram, showing the state of the Q output over time as the input switches are actuated. Assume that Q begins in the low state on power-up:

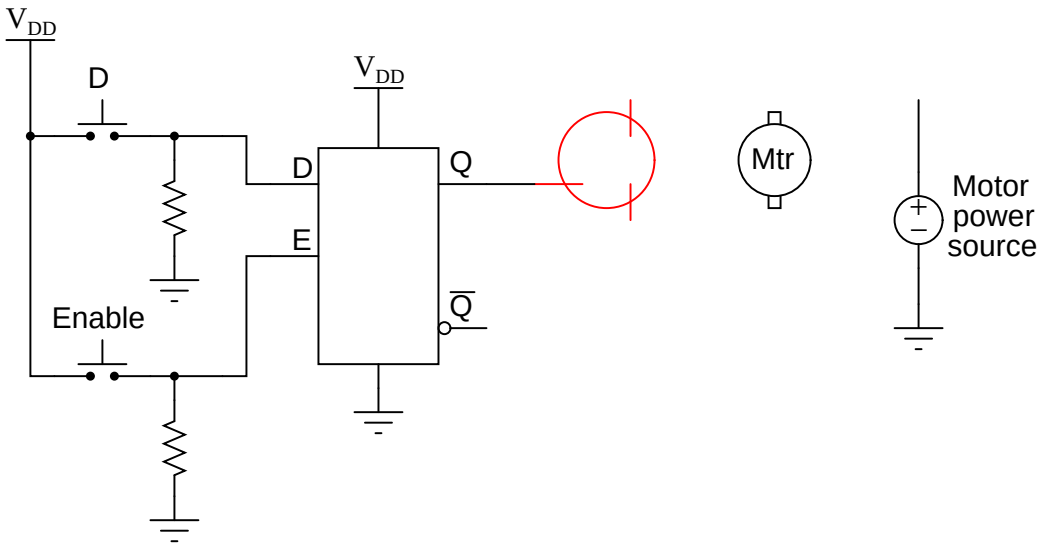


file 02901

Answer 25



Follow-up question: complete a schematic diagram showing how this latch circuit could turn a motor on and off through a MOSFET.



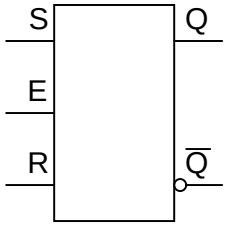
Also, comment on whether your MOSFET *sources* current to the motor or *sinks* current from the motor.

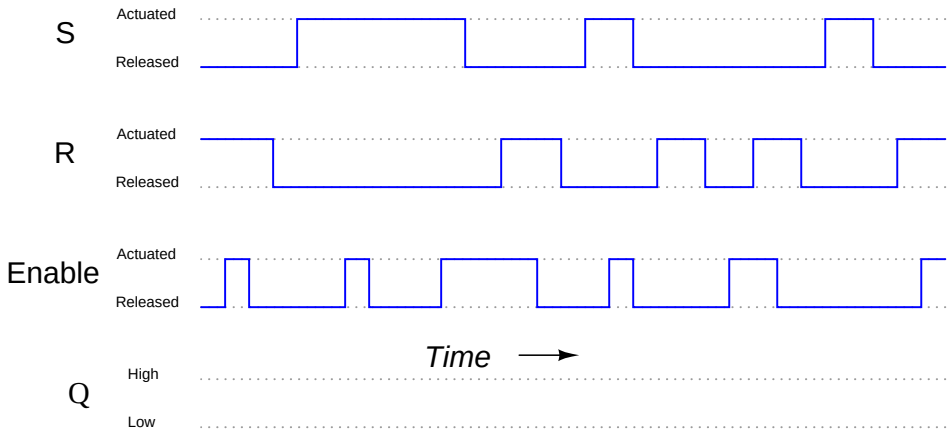
Notes 25

Some students may be confused about the width of the last pulse on the Q output. Remind them that Q follows D for as long as the Enable input is activated!

Question 26

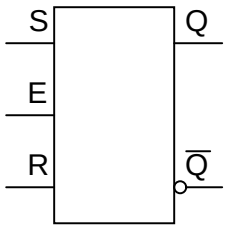
Complete the timing diagram, showing the state of the Q output over time as the input switches are actuated. Assume that Q begins in the low state on power-up:

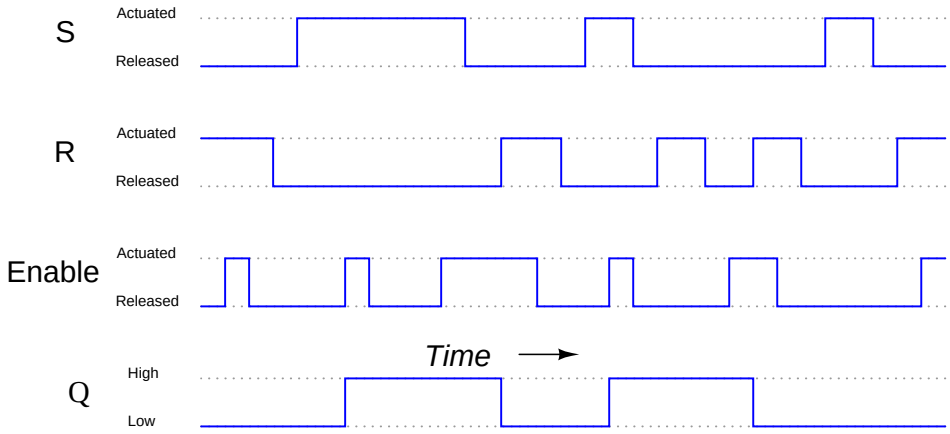




file 02913

Answer 26



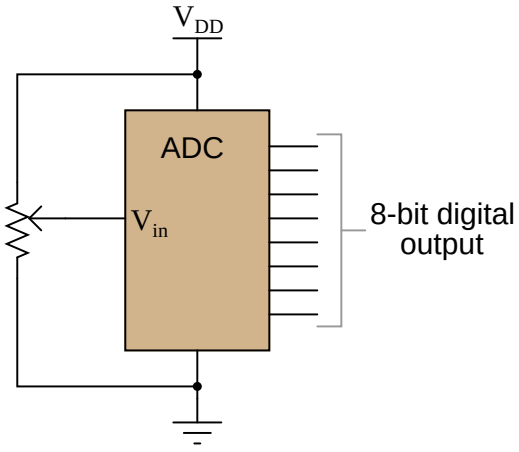


Notes 26

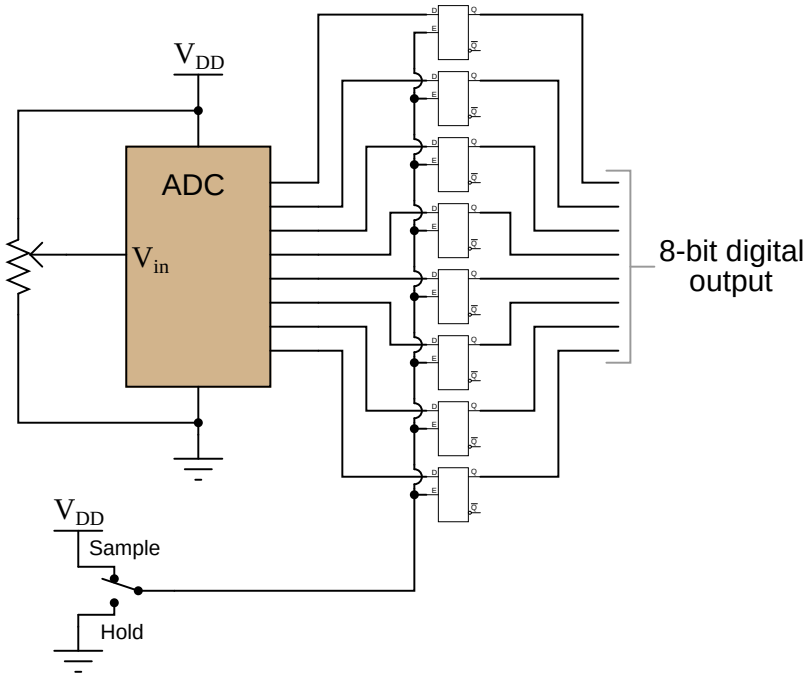
Have your students explain exactly how they arrived at the solution they did for the output waveform. Are they making use of a truth table for the S-R latch to figure out what happens? Are they doing it by memory? Can they discriminate between an output state change initiated by either the Set or Reset inputs versus one initiated by the enable going high?

Question 27

An *analog-to-digital converter* is a circuit that inputs a variable (analog) voltage or current, and outputs multiple bits of binary data corresponding to the magnitude of that measured voltage or current. In the circuit shown here, an ADC inputs a voltage signal from a potentiometer, and outputs an 8-bit binary "word," which may then be read by a computer, transmitted digitally over a communications network, or stored on digital media:



As the input voltage changes, the binary number output by the ADC will change as well. Suppose, though, that we want to have *sample-and-hold* capability added to this data acquisition circuit, to allow us to "freeze" the output of the ADC at will. Explain how using eight D latch circuits will give us this capability:



file 01358

Answer 27

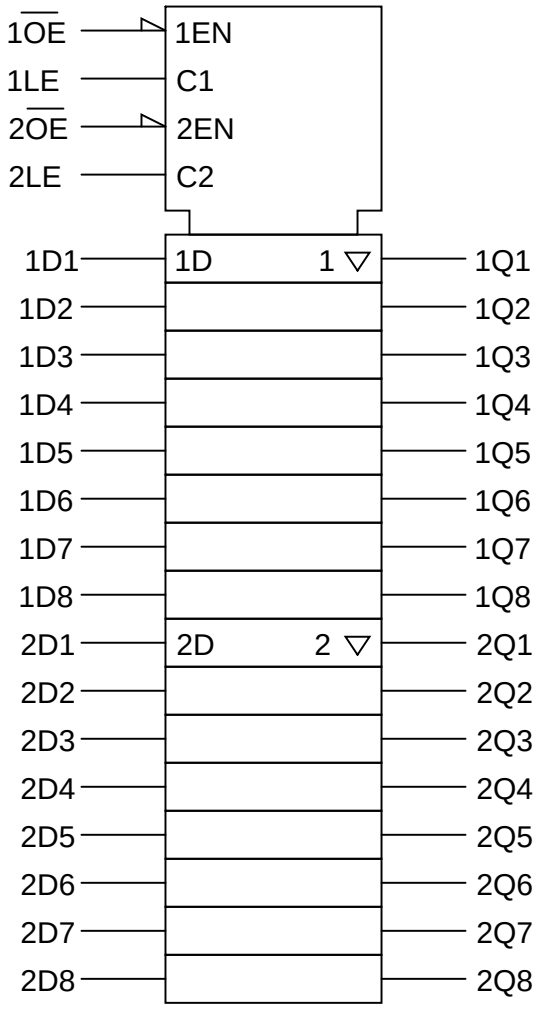
When the Sample/Hold switch is in the "low" position, the D latches all fall into the "latch" state, holding that last valid input states on their Q outputs.

Notes 27

Sample-and-hold circuitry is quite common in modern data acquisition and other types of electronic systems. In this case, sample-and-hold showcases a practical use of D latch circuits. If your students have not yet heard of analog-to-digital converters, it might be a good idea to discuss some of their general principles. No knowledge of their internal workings is necessary in order to comprehend the circuit shown in the question, however.

Question 28

Gated latch circuits often come packaged in multiple quantities, with common gate inputs, so that more than one of the latches within the integrated circuit will be enabled and disabled simultaneously. Examine this logic symbol, representative of the 74AC16373, a 16-bit D-type latch with tri-state outputs:



Note how the sixteen D latches are divided into two groups of eight. Explain the functions of the four inputs at the very top of the symbol (1EN, C1, 2EN, and C2). Which of these input lines correspond to the "Enable" inputs seen on single D-type latch circuits? Also, describe what the "wedge" shapes represent on the 1EN and 2EN input lines.

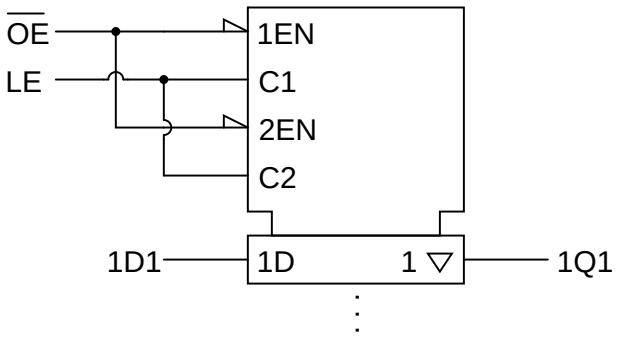
Suppose you wished to have all sixteen latch circuits enabled as one, rather than as two groups of eight. Show what you would have to do to this circuit in order to achieve this goal.

file 01359

Answer 28

Inputs C1 and C2 perform the standard "Enabling" function for the D-type latches within this integrated circuit. The 1EN and 2EN inputs control the tri-state outputs. Their "wedge" symbols mean "complemented," and are equivalent to the "bubbles" seen on traditional gate symbols.

To make all sixteen latches enable and disable as one, bridge the enable inputs as such:



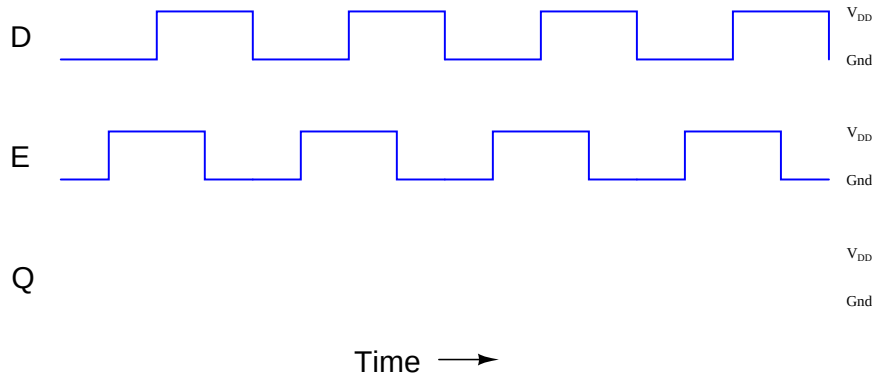
Notes 28

This question not only introduces students to the concept of multiple latches in a single integrated circuit, but it also shows an example of IEEE/ANSI "block" symbolism. Your students, having become well adjusted to the idea of independent research by now, should have obtained the datasheet for this circuit (74AC16373) as part of their study. The information contained in the datasheet should prove to be quite informative in answering their questions about enable input functions, tri-state outputs, and the like. If they haven't obtained datasheets, and cannot understand the answers to the question(s), don't just tell them – have them look it up for themselves!

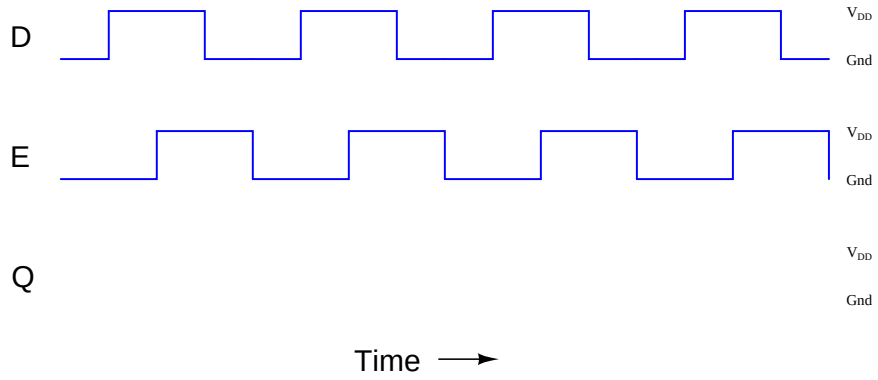
Question 29

In many types of digital systems, a set of square-wave signals are phase-shifted from each other by 90^o. Such a phase relationship is called *quadrature*.

Determine the output of a D-type latch for this pair of quadrature signals, applied to the D and E inputs over time:

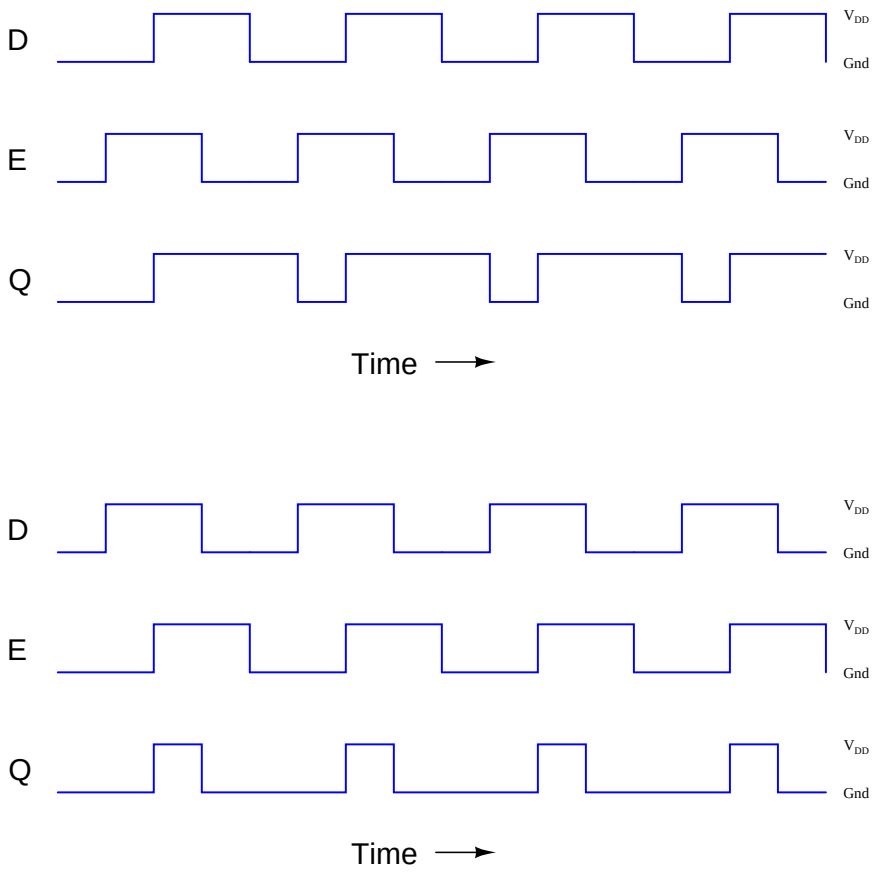


Then, determine the output of a D-type latch when the phase relationship is reversed, (D leading E by 90^o, instead of E leading D by 90^o):



file 01360

Answer 29

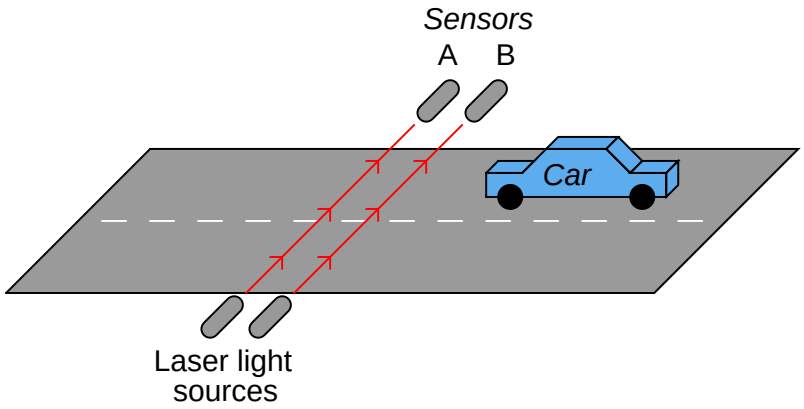


Notes 29

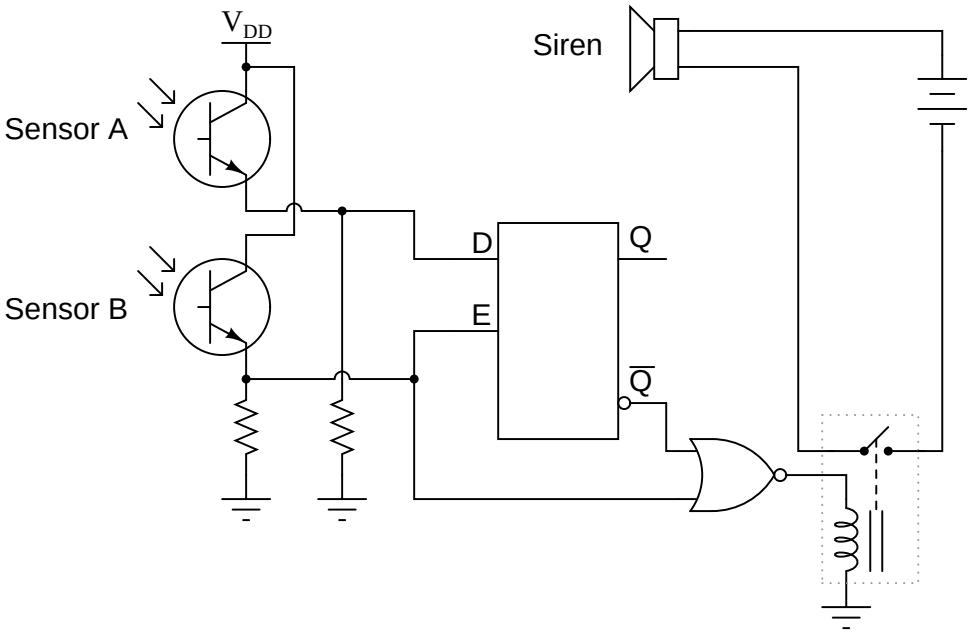
Students need to be proficient in analyzing pulse diagrams, especially with latch circuits (and later, with flip-flops), because these types of circuits often find application in pulse-driven systems.

Question 30

This one-way street is equipped with an alarm to signal drivers going the wrong way. The sensors work by light beams being broken when an automobile passes between them. The distance between the sensors is less than the length of a normal car, which means as a car passes by, first one beam is broken, then both beams become broken, then only the last beam is broken, then neither beam is broken. The sensors are phototransistors sensitive only to the narrow spectrum of light emitted by the laser light sources, so that ambient sunlight will not "fool" them:



Both sensors connect to inputs on a D-type latch, which is then connected to some other circuitry to sound an alarm when a car goes down the road the wrong way:



The first question is this: which way is the *correct* way to drive down this street? From left to right, or from right to left (as shown in the illustration)?

The second question is, how will the system respond if sensor A's laser light source fails? What will happen if sensor B's laser light source fails?

file 01361

Answer 30

Left-to-right is the correct driving direction for this street.

If sensor A's light source fails, the alarm will never activate. A failed light source for sensor B will have different effects on the system, depending on whether sensor A was sending a "high" or a "low" signal to the latch circuit at the time B's light source failed. I'll let you figure out which way triggers the alarm!

Notes 30

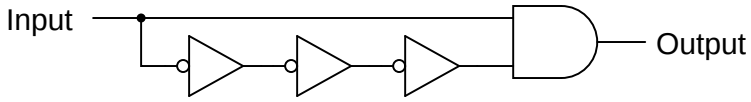
This question is a great problem-solving exercise. Students must figure out how to set it up so that they may apply the rules of latch circuits and gate circuits, then they must analyze it correctly! Devote plenty of classroom time to a discussion of this problem.

Students may show a reluctance to draw a timing diagram when they approach this problem, even when they realize the utility of such a diagram. Instead, many will try to figure the circuit out just by looking at it. Note the emphasis on the word "try." This circuit is much more difficult to figure out without a timing diagram! Withhold your explanation of this circuit until each student shows you a timing diagram for it. Emphasize the fact that this step, although it consumes a bit of time, is actually a time-saver in the end.

It is easy as an instructor to focus so intently on teaching electronic theory that other practical matters become neglected. Electronic technicians and engineers do not simply work on circuits; they work on *systems* that happen to employ electronic circuits. Ultimately, nearly every electronic circuit they work with will have some relationship to the physical world. Problem solving exercises in school must include scenarios similar to real life, where conditions and functions other than electronics have a role in determining the solution. Only by exposing students to problems requiring them to think beyond pure electronics will they become adequately prepared to meet the challenges of their future careers.

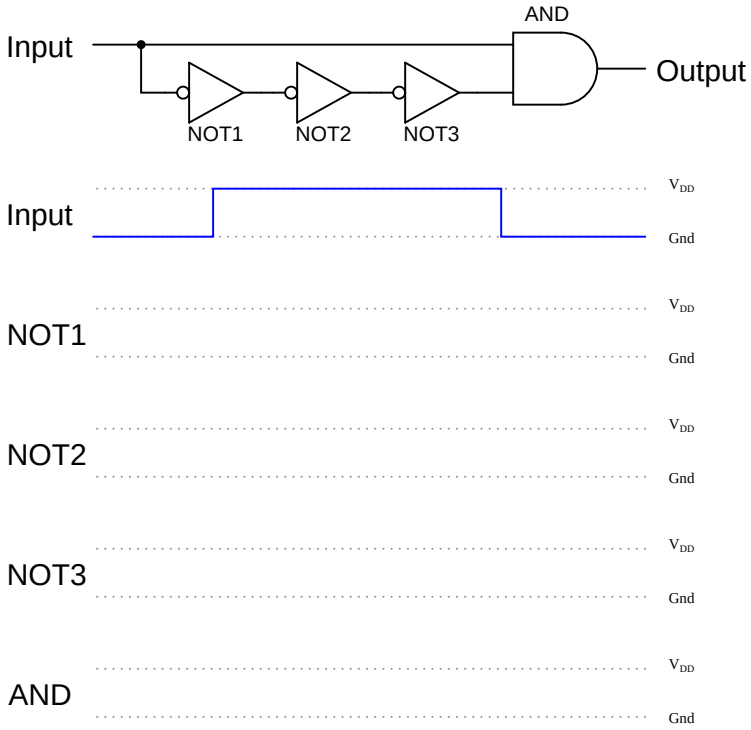
Question 31

Usually, propagation delay is considered an undesirable characteristic of logic gates, which we simply have to live with. Other times, it is a useful, even necessary, trait. Take for example this circuit:



If the gates constituting this circuit had zero propagation delay, it would perform no useful function at all. To verify this sad fact, analyze its steady-state response to a "low" input signal, then to a "high" input signal. What state is the AND gate's output always in?

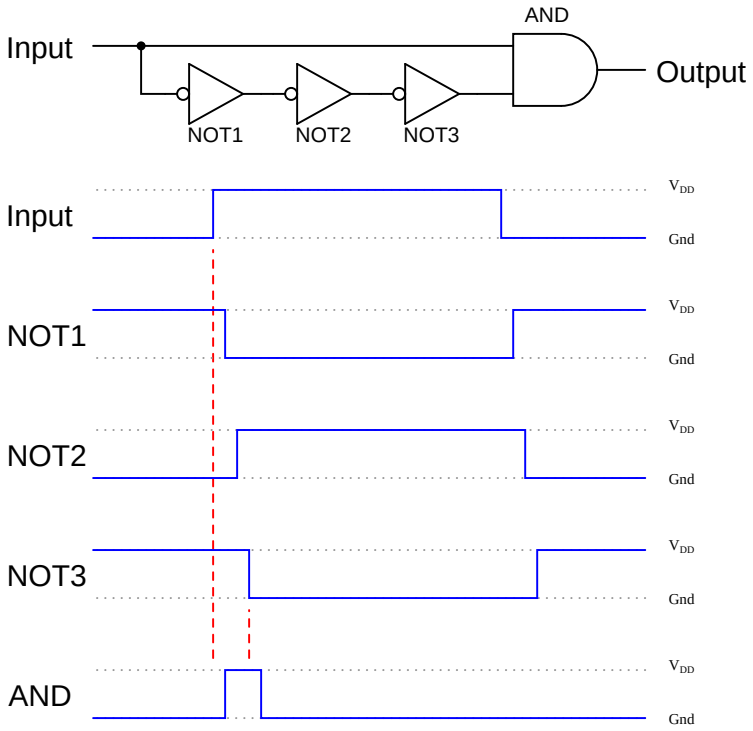
Now, consider propagation delay in your analysis by completing a timing diagram for each gate's output, as the input signal transitions from low to high, then from high to low:



What do you notice about the state of the AND gate's output now?

file 01362

Answer 31



Follow-up question: describe exactly what conditions are necessary to obtain a "high" signal from the output of this circuit, and what determines the duration of this "high" pulse.

Notes 31

Tell your students that this circuit is a special type of *one-shot*, outputting a single pulse of limited duration for each leading-edge transition of the input signal.

Ask your students what we might do if we wanted to make the output pulse of this one-shot circuit longer (or shorter).

Question 32

Explain how you would use an oscilloscope to measure the propagation delay of a semiconductor logic gate. Draw a schematic diagram, if necessary. Are the propagation delay times typically equal for a digital gate transitioning from "low" to "high", versus from "high" to "low"? Consult datasheets to substantiate your answer.

Also, comment on whether or not electromechanical relays have an equivalent parameter to propagation delay. If so, how do you suppose the magnitude of a relay's delay compares to that of a semiconductor gate, and why?

file 01371

Answer 32

I'll leave the experimental design details up to you. However, I will tell you that you do not necessarily have to use a digital storage oscilloscope to "capture" a transient waveform to measure propagation delay, if you apply a little creativity. Hint: use a signal generator to send a high-frequency square wave to the gate of your choice, and use a non-storage oscilloscope to monitor the results.

And yes, electromechanical relays also have intrinsic delay times, which tend to be *far* greater than those encountered with semiconductor logic gates.

Notes 32

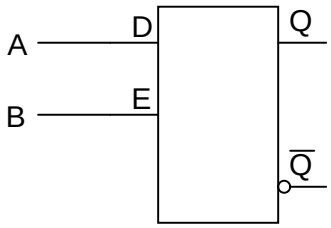
This question makes an excellent in-class demonstration. It shows this practical parameter in terms the students should be able to kinesthetically relate to.

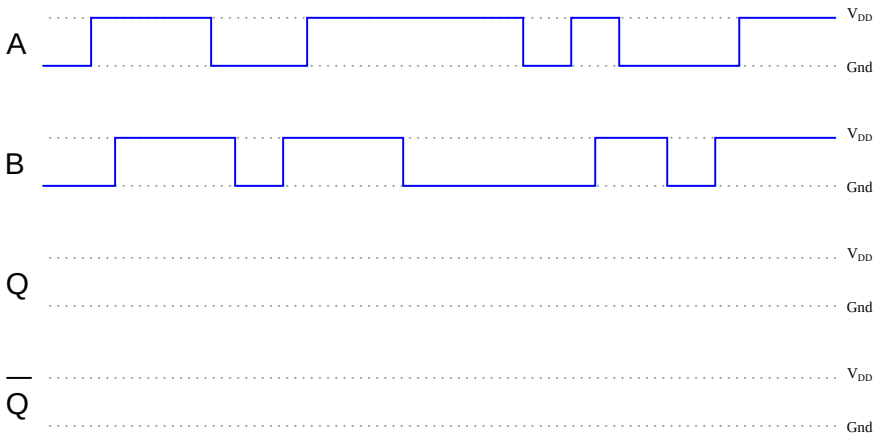
Hold your students accountable for researching datasheets, rather than just looking up the information in a textbook. Ultimately, reading datasheets and applications notes written by the manufacturers will keep them abreast of the latest technology much more effectively than textbooks, since most textbooks I've seen tend to lag behind state-of-the-art by a few years at the least. There is wealth of information to be gained from manufacturers' literature, so prepare your students to use it!

Explain to your students that relays not only have actuation delay, but most of them also exhibit significant contact *bounce* as well. Contact bounce is a problem especially where relays send signals to solid-state logic circuitry, to a much greater extent than where relays send signals to other relays. Special-purpose relays can be obtained whose designs minimize actuation time and bounce, but both characteristics are far worse than any equivalent effects in semiconductor logic gates.

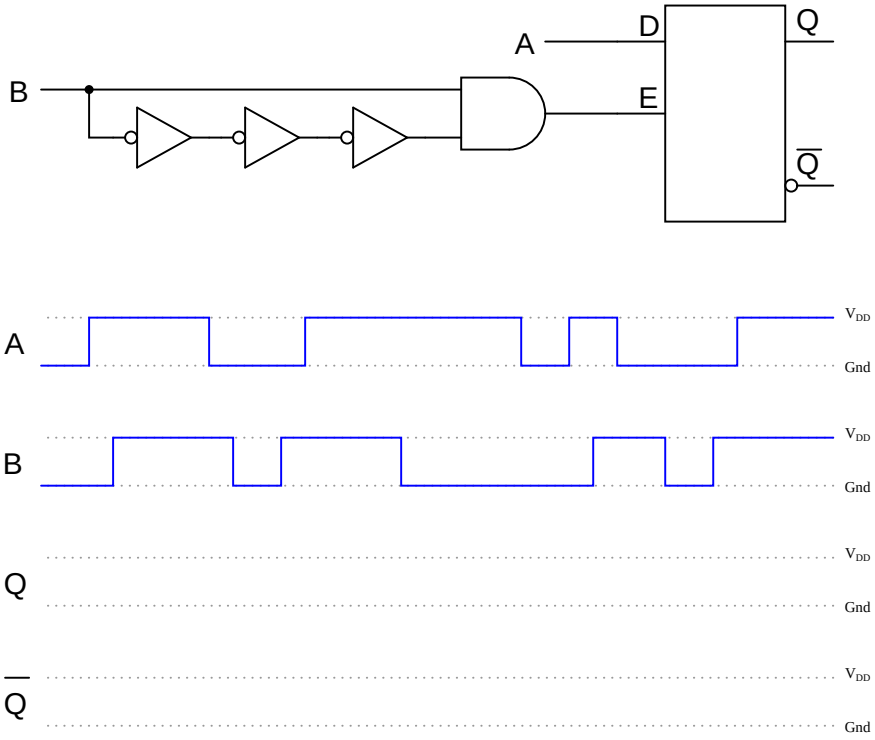
Question 33

Determine the Q and $\overline{Q}$ output states of this D-type gated latch, given the following input conditions:





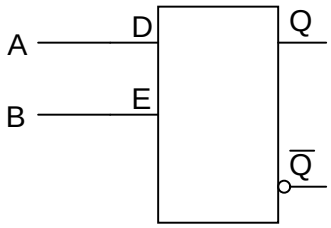
Now, suppose we add a propagation-delay-based one-shot circuit to the Enable line of this D-type gated latch. Re-analyze the output of the circuit, given the same input conditions:

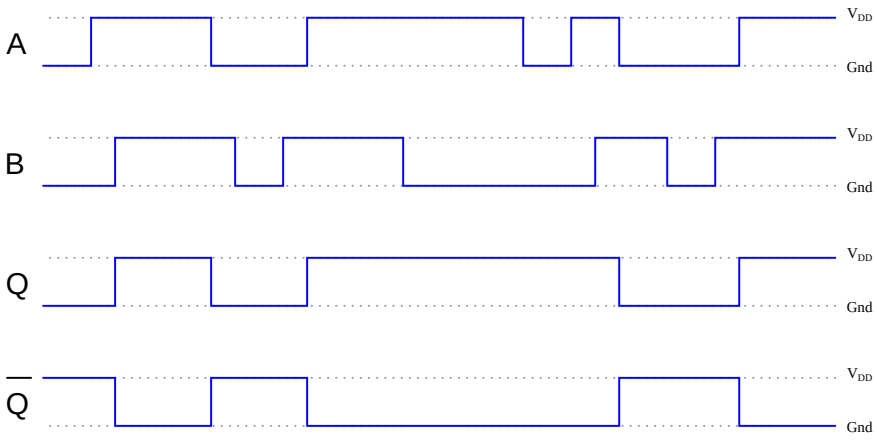


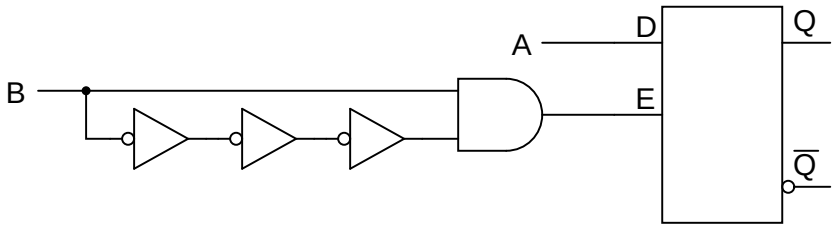
Comment on the differences between these two circuits' responses, especially with reference to the enabling input signal (B).

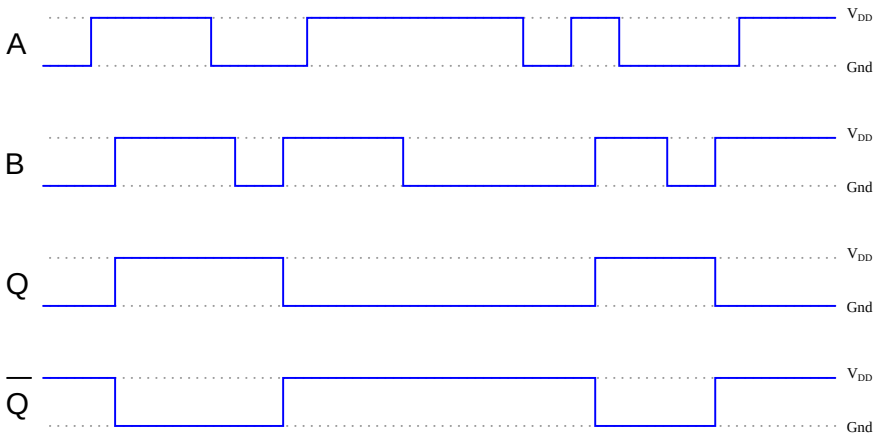
file 01364

Answer 33


A
B
D
E
Q
$\overline{Q}$


A
B
Q
$\overline{Q}$
V_{DD}
Gnd


B
A
D
E
Q
$\overline{Q}$


A
B
Q
$\overline{Q}$
V_{DD}
Gnd

Follow-up question: one of these circuits is referred to as *edge-triggered*. Which one is it?

Challenge question: in reality, the output waveforms for both these scenarios will be shifted slightly due to propagation delays within the constituent gates. Re-draw the true outputs, accounting for these delays.

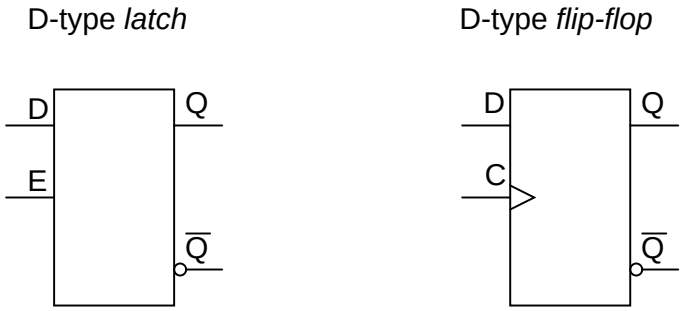
Notes 33

Discuss with your students the concept of edge-triggering, and how it is implemented in (one of) the circuits in this question. Ask them to describe any tips they may have discovered for analyzing pulse waveforms. Specifically, are there any particular times where we need to pay close attention to the D input signal to determine what the outputs do, and any times where we can ignore the D input status?

The challenge question regarding propagation delays is meant to remind students that the perfectly synchronized timing diagrams seen in textbooks are not exactly what happens in real life. Ask your students to elaborate on what real-life conditions would make such propagation delays relevant. Are there applications of digital circuits where we can all but ignore such delays?

Question 34

Shown here are two digital components: a D-type *latch* and a D-type *flip-flop*:



Other than the silly name, what distinguishes a "flip-flop" from a latch? How do the two circuits differ in function?

file 01365

Answer 34

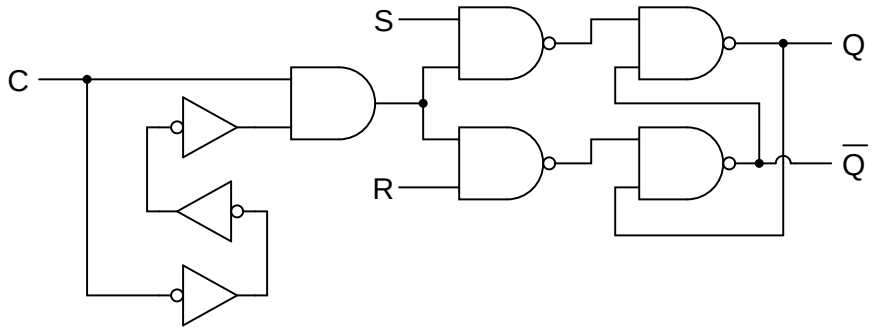
A "flip-flop" is a latch that changes output only at the rising or falling *edge* of the clock pulse.

Notes 34

Note to your students that the timing input of a flip-flop is called a *clock* rather than an *enable*. Ask them to identify what differences in symbolism show this distinction between the two devices.

Question 35

Explain how the addition of a propagation-delay-based one-shot circuit to the enable input of an S-R latch changes its behavior:



Specifically, reference your answer to a truth table for this circuit.
file 01366

Answer 35

The outputs of this device are allowed to change state only when the "clock" signal (C) is transitioning from low to high:

C	S	R	Q	$\overline{Q}$
↓	0	0	*Latch*	
↓	0	1	0	1
↓	1	0	1	0
↓	1	1	*Invalid*	

Challenge question: what exactly happens in the "invalid" state for this S-R flip-flop?

Notes 35

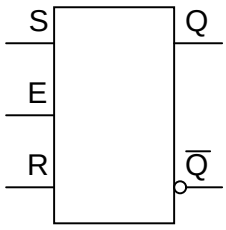
Discuss with your students what happens in this circuit when the clock signal is doing anything other than transitioning from low to high. What condition(s) are equivalent in a regular S-R gated latch circuit?

The challenge question is especially tricky to answer. "Invalid" states are easy to determine in regular S-R latch circuits, gated or ungated. However, because an S-R *flip-flop* is only momentarily "gated" by the edge of the clock signal, the states its outputs fall to after that edge event has passed is much more difficult to determine.

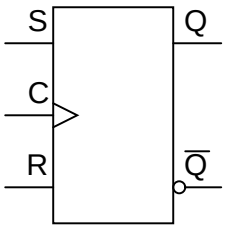
Question 36

Plain S-R latch circuits are "set" by activating the S input and de-activating the R input. Conversely, they are "reset" by activating the R input and de-activating the S input. Gated latches and flip-flops, however, are a little more complex:

S-R gated latch



S-R flip-flop



Describe what input conditions have to be present to force each of these multivibrator circuits to *set* and to *reset*.

For the S-R gated latch:

- Set by . . .
- Reset by . . .

For the S-R flip-flop:

- Set by . . .
- Reset by . . .

file 02935

Answer 36

For the S-R gated latch:

- Set by making S high, R low, and E high.
- Reset by making R high, S low, and E high.

For the S-R flip-flop:

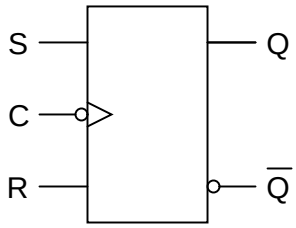
- Set by making S high, R low, and C transition from low to high.
- Reset by making R high, S low, and C transition from low to high.

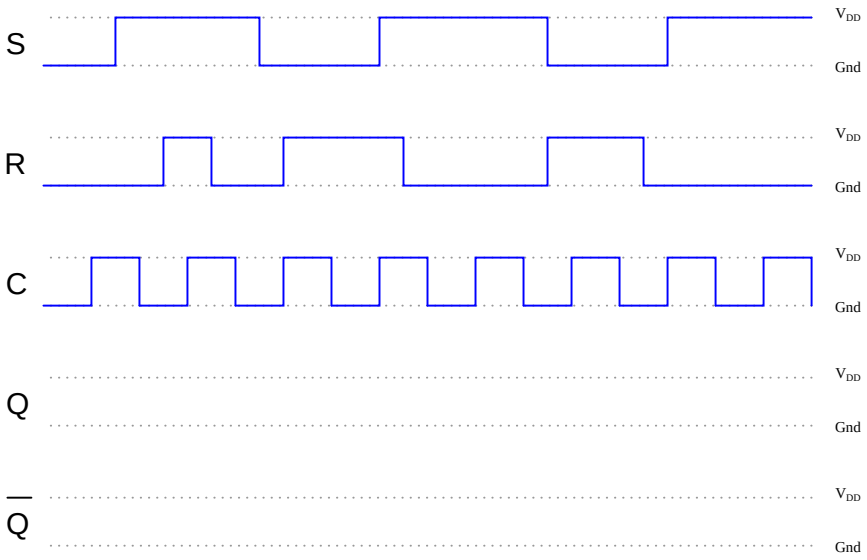
Notes 36

The purpose of this question is to review the definitions of "set" and "reset," as well as to differentiate latches from flip-flops.

Question 37

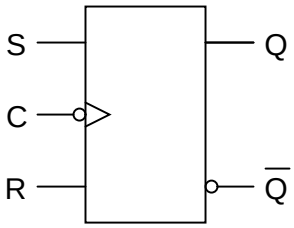
Determine the output states for this S-R flip-flop, given the pulse inputs shown:

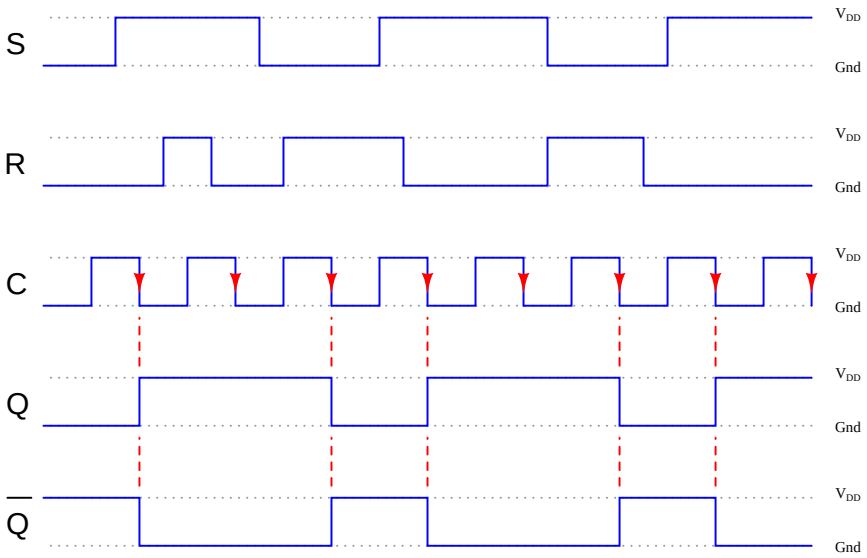




file 01367

Answer 37



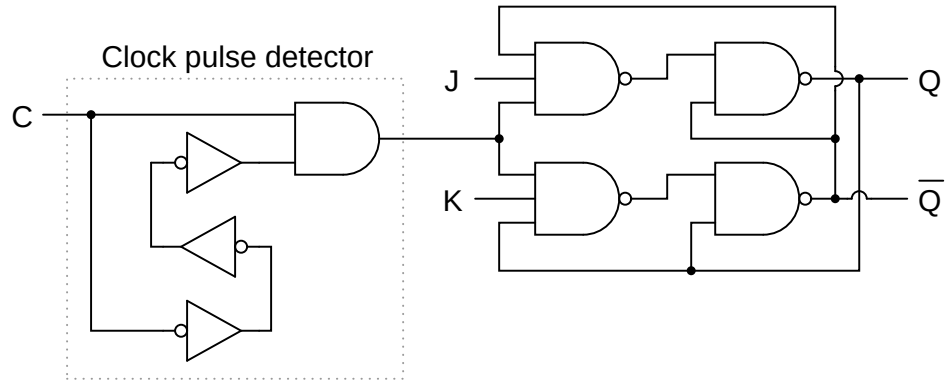


Notes 37

In order to successfully answer this question, students will have to identify what the "bubble" means on the clock input, and relate that to the timing diagram. Ask your students to share any tips they may have regarding the analysis of timing diagrams, specifically what points in the diagram are critical (i.e. what points in time are the only points where the outputs may actually change states).

Question 38

An extremely popular variation on the theme of an S-R flip-flop is the so-called *J-K flip-flop* circuit shown here:



Note that an S-R flip-flop becomes a J-K flip-flop by adding another layer of feedback from the outputs back to the enabling NAND gates (which are now three-input, instead of two-input). What does this added feedback accomplish? Express your answer in the form of a truth table.

One way to consider the feedback lines going back to the first NAND gates is to regard them as extra *enable* lines, with the Q and $\overline{Q}$ outputs selectively enabling just one of those NAND gates at a time.

file 01368

Answer 38

C	J	K	Q	$\overline{Q}$
↓	0	0	*Latch*	
↓	0	1	0	1
↓	1	0	1	0
↓	1	1	*Toggle*	

Follow-up question: comment on the difference between this truth table, and the truth table for an S-R flip-flop. Are there any operational advantages you see to J-K flip-flops over S-R flip-flops that makes them so much more popular?

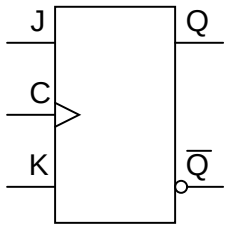
Notes 38

I have found that J-K flip-flop circuits are best analyzed by setting up input conditions (1's and 0's) on a schematic diagram, and then following all the gate output changes at the next clock pulse transition. A technique that really works well in the classroom for doing this is to project a schematic diagram on a clean whiteboard using an overhead projector or computer projector, then writing the 1 and 0 states with pen on the board. This allows you to quickly erase the 1's and 0's after each analysis without having to re-draw the schematic diagram. As always, I recommend you have students actually do the writing, with you taking the role of a coach, helping them rather than simply doing the thinking for them.

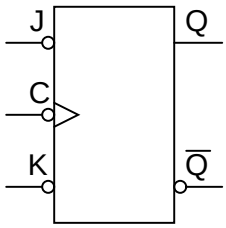
Question 39

Determine what input conditions are necessary to set, reset, and toggle these two J-K flip-flops:

Active-high inputs



Active-low inputs



For the J-K flip-flop with active-high inputs:

- Set by . . .
- Reset by . . .
- Toggle by . . .

For the J-K flip-flop with active-low inputs:

- Set by . . .
- Reset by . . .
- Toggle by . . .

file 02936

Answer 39

In *either* case, you cause the flip-flop to go into these three modes by doing the following:

- Set by *activating* J, *deactivating* K, and *clocking* C.
- Reset by *activating* K, *deactivating* J, and *clocking* C.
- Toggle by *activating* J and K simultaneously, and *clocking* C.

Specifically, though, here is what you would need to do to each flip-flop, stated in terms of "high" and "low" logic states:

For the J-K flip-flop with active-high inputs:

- Set by making J high, K low, and C transition from low to high.
- Reset by making K high, J low, and C transition from low to high.
- Toggle by making J high, K high, and C transition from low to high.

For the J-K flip-flop with active-low inputs:

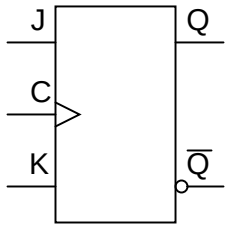
- Set by making K high, J low, and C transition from high to low.
- Reset by making J high, K low, and C transition from high to low.
- Toggle by making J low, K low, and C transition from high to low.

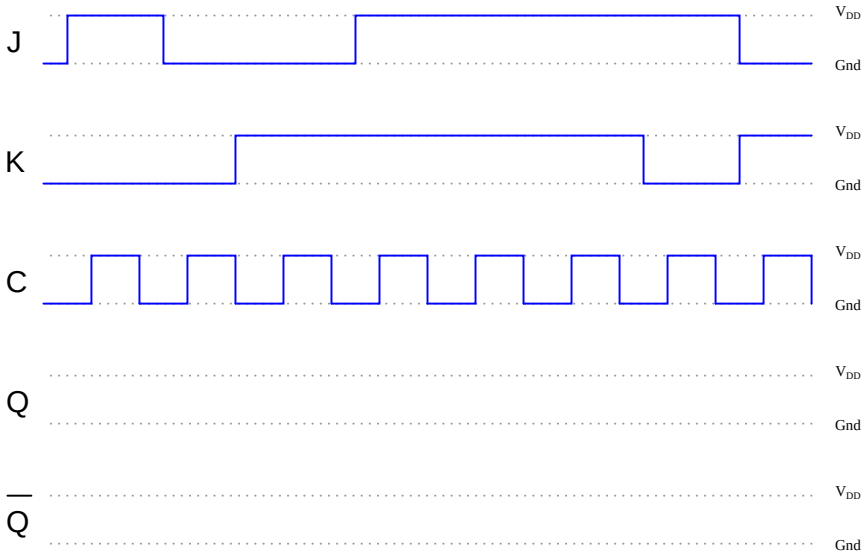
Notes 39

This question reviews the basic modes of J-K flip-flops, as well as the significance of active-low inputs.

Question 40

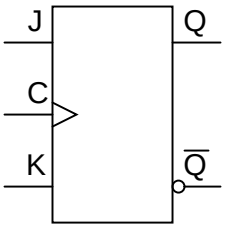
Determine the output states for this J-K flip-flop, given the pulse inputs shown:

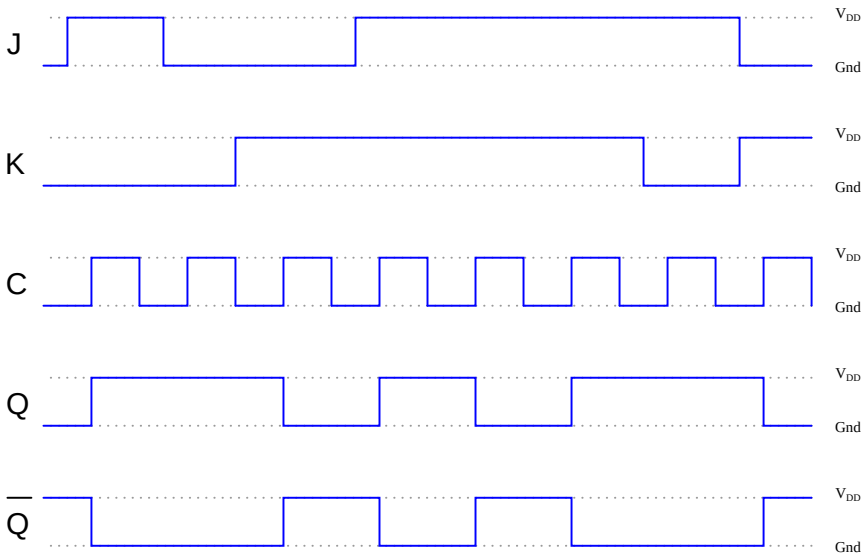




file 02934

Answer 40



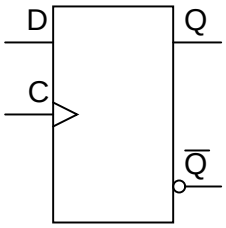


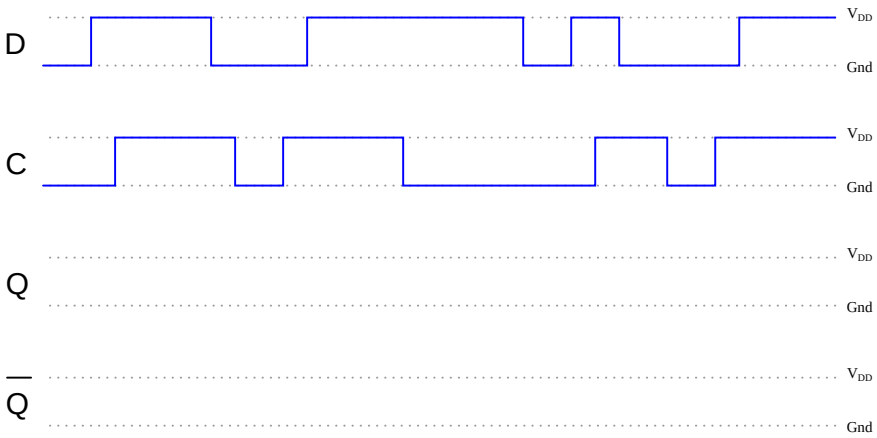
Notes 40

Ask students to identify those regions on the timing diagram where the flip-flop is being *set*, *reset*, and *toggled*.

Question 41

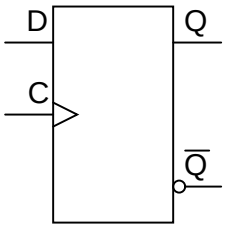
Determine the output states for this D flip-flop, given the pulse inputs shown:

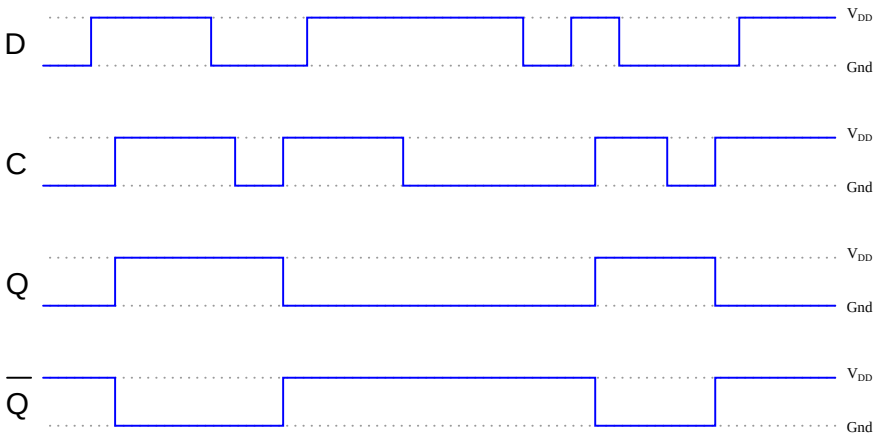




file 02940

Answer 41



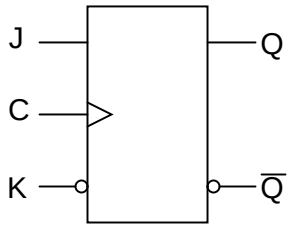


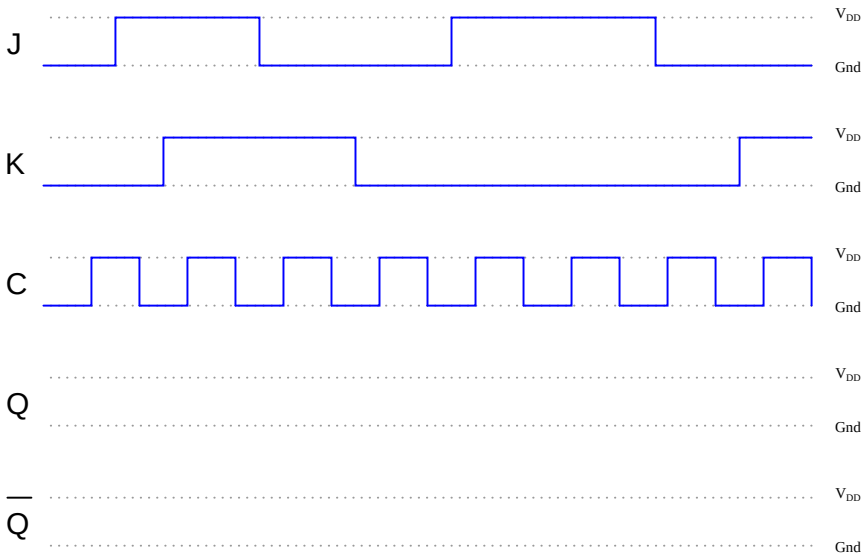
Notes 41

Ask students to identify those regions on the timing diagram where the flip-flop is being *set* and *reset*.

Question 42

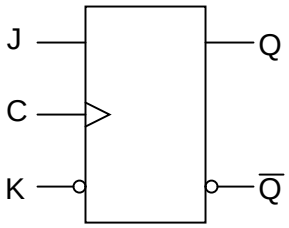
Determine the output states for this J-K flip-flop, given the pulse inputs shown:

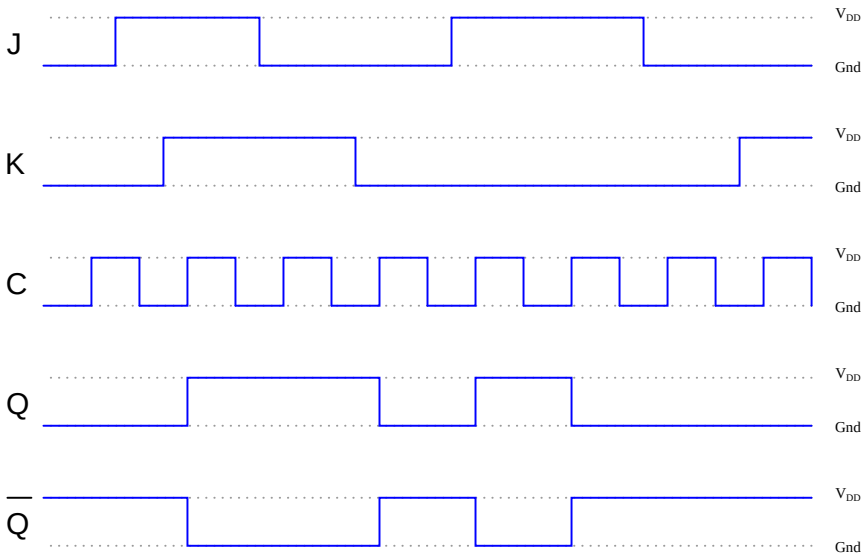




file 02939

Answer 42



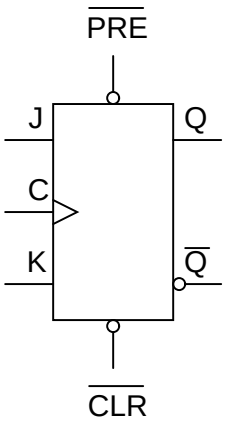


Notes 42

Ask students to identify those regions on the timing diagram where the flip-flop is being *set*, *reset*, and *toggled*.

Question 43

Flip-flops often come equipped with *asynchronous input lines* as well as synchronous input lines. This J-K flip-flop, for example, has both "preset" and "clear" asynchronous inputs:



Describe the functions of these inputs. Why would we ever want to use them in a circuit? Explain what the "synchronous" inputs are, and why they are designated by that term.

Also, note that both of the asynchronous inputs are *active-low*. As a rule, asynchronous inputs are almost always active-low rather than active-high, even if all the other inputs on the flip-flop are active-high. Why do you suppose this is?

file 01370

Answer 43

"Asynchronous" inputs force the outputs to either the "set" or "reset" state independent of the clock. "Synchronous" inputs have control over the flip-flop's outputs only when the clock pulse allows.

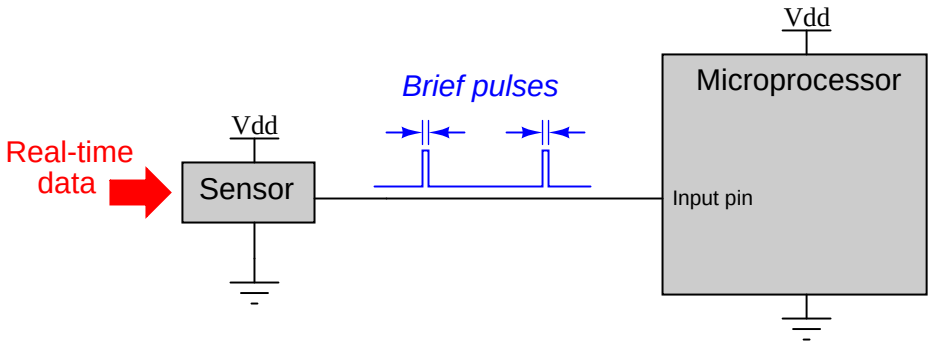
As for why the asynchronous inputs are active-low, I won't directly give you the answer. But I will give you a hint: consider a *TTL* implementation of this flip-flop.

Notes 43

Note to your students that sometimes the Preset and Clear inputs are called *direct set* and *direct reset*, respectively. Review with your students what it means for an input to be "active-low" versus "active-high." Ask them what consequences might arise if a circuit designer misunderstood the input states and failed to provide the right type of signal to the circuit.

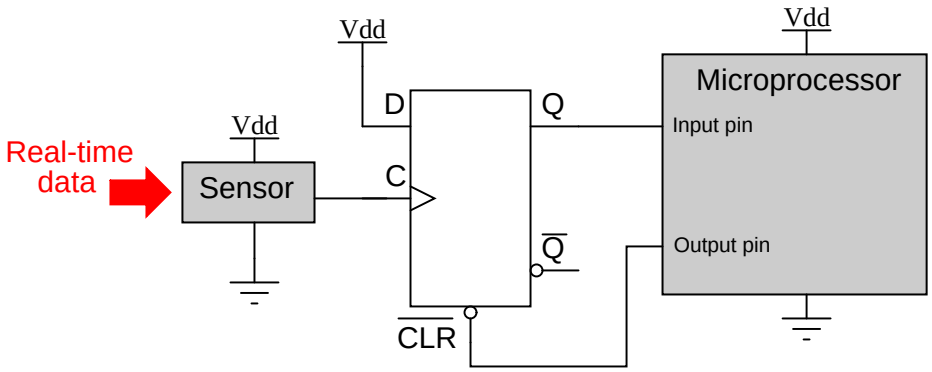
Question 44

A scientist is using a microprocessor system to monitor the boolean ("high" or "low") status of a particle sensor in her high-speed nuclear experiment. The problem is, the nuclear events detected by the sensor come and go much faster than the microprocessor is able to sample them. Simply put, the pulses output by the sensor are too brief to be "caught" by the microprocessor every time:



She asks several technicians to try and fix the problem. One tries altering the microprocessor's program to achieve a faster sampling rater, to no avail. Another recalibrates the particle sensor to react slower, but this only results in missed data (because the real world data does not slow down accordingly!). No solution tried so far works, because the fundamental problem is that the microprocessor is just too slow to "catch" the extremely short pulse events coming from the particle sensor. What is required is some kind of external circuit to "read" the sensor's state at the leading edge of a sample pulse, and then hold that digital state long enough for the microprocessor to reliably register it.

Finally, another electronics technician comes along and proposes this solution, but then goes on vacation, leaving you to implement it:



Explain how this D-type flip-flop works to solve the problem, and what action the microprocessor has to take on the output pin to make the flip-flop function as a detector for multiple pulses.

file 01464

Answer 44

The flip-flop becomes "set" every time a pulse comes from the sensor. The microprocessor must clear the flip-flop after reading the captured pulse, so the flip-flop will be ready to capture and hold a new pulse.

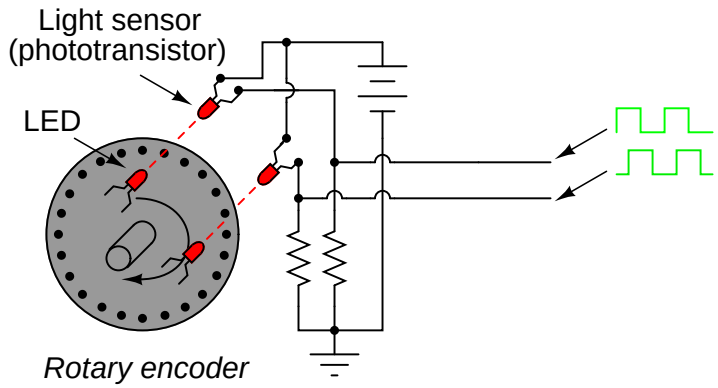
Challenge question: what logic family of flip-flop would you recommend be used for this application, given the need for extremely fast response? Don't just say "TTL," either. Research the fastest modern logic family in current manufacture!

Notes 44

This is a very practical application for a D-type flip-flop, and also an introduction to one of the pitfalls of microprocessor-based data acquisition systems. Explain to your students that the finite time required for a microprocessor to cycle through its program may lead to conditions such as this where real-time events are missed because the microprocessor was "busy" doing other things at the time.

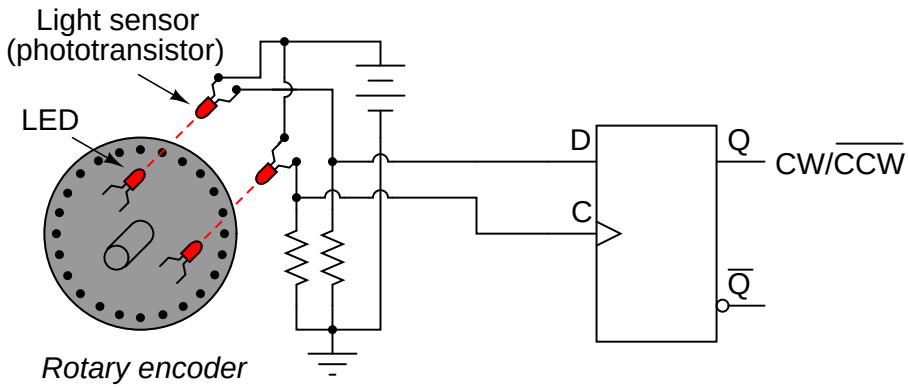
Question 45

A common type of rotary encoder is one built to produce a *quadrature* output:



The two LED/phototransistor pairs are arranged in such a way that their pulse outputs are always 90^o out of phase with each other. Quadrature output encoders are useful because they allow us to determine direction of motion as well as incremental position.

Building a quadrature direction detector circuit is easy, if you use a D-type flip-flop:



Analyze this circuit, and explain how it works.

file 01384

Answer 45

The operation of this circuit is quite easy to understand if you draw a pulse diagram for it and analyze the flip-flop's output over time. When the encoder disk spins clockwise, the Q output goes high; when counterclockwise, the Q goes low.

Follow-up question: comment on the notation used for this circuit's output. What does the label "$CW/\overline{CCW}$" tell you, without having to analyze the circuit at all?

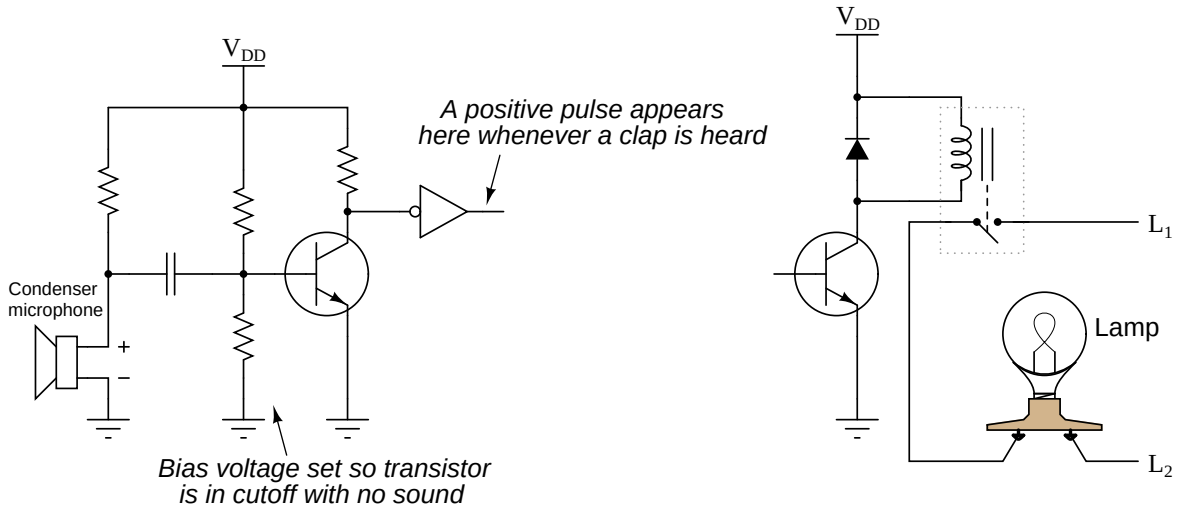
Notes 45

Quadrature direction-detection circuits such as this become important when encoders are linked to digital counter circuits. The complemented notation is also very common in counter circuits.

Students may show a reluctance to draw a timing diagram when they approach this problem, even when they realize the utility of such a diagram. Instead, many will try to figure the circuit out just by looking at it. Note the emphasis on the word "try." This circuit is much more difficult to figure out without a timing diagram! Withhold your explanation of this circuit until each student shows you a timing diagram for it. Emphasize the fact that this step, although it consumes a bit of time, is actually a time-saver in the end.

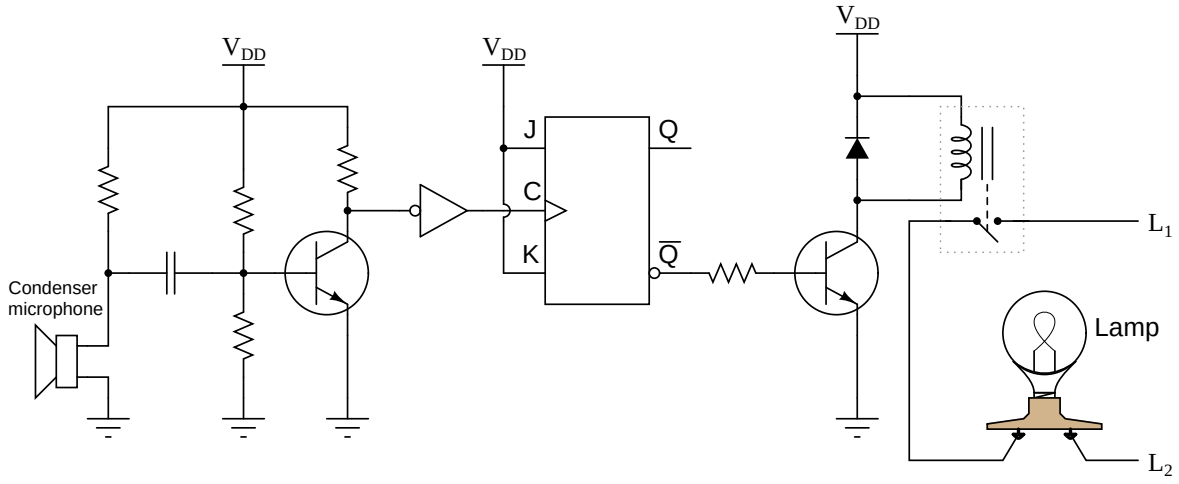
Question 46

Suppose a student wants to build a sound-controlled lamp control circuit, whereby a single clap or other loud burst of noise turns the lamp on, and another single clap turns it off. The sound-detection and lamp-drive circuitry is shown here:



Add a J-K flip-flop to this schematic diagram to implement the toggling function.
file 01369

Answer 46



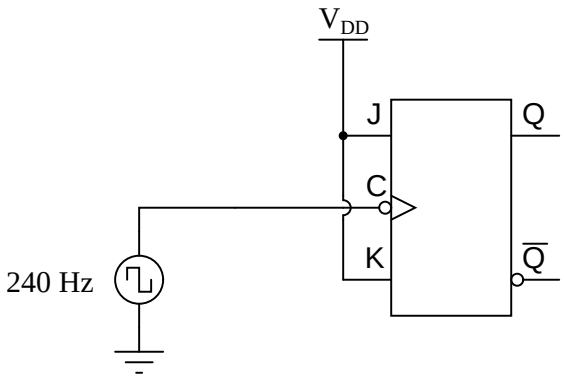
Notes 46

Some students may ask whether there is any significance to using the $\overline{Q}$ output rather than the Q. Discuss this with your students: whether they think it will make any difference, or if it was just an arbitrary choice made by the circuit's designer. Then, ask them how they would go about *proving* their judgment.

There are plenty of "what if" failure scenarios you could ask your students about here, challenging them to analyze this circuit with a troubleshooting perspective. If time permits, have some fun with this.

Question 47

If the clock frequency driving this flip-flop is 240 Hz, what is the frequency of the flip-flop's output signals (either Q or $\overline{Q}$)?



file 01372

Answer 47

$f_{out} = 120$ Hz

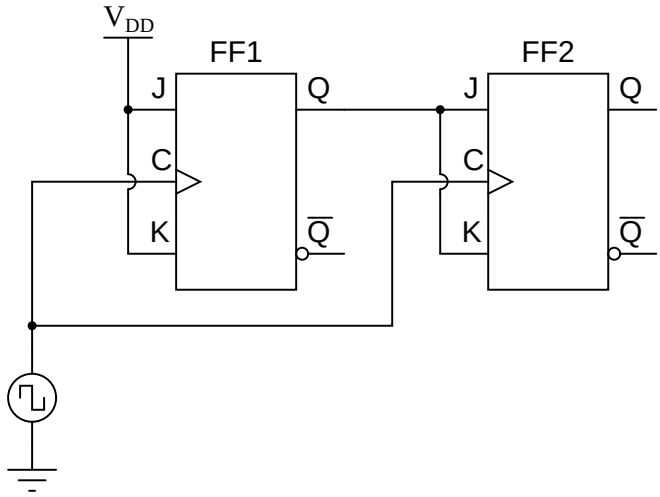
Follow-up question: how could you use another flip-flop to obtain a square-wave signal of 60 Hz from this circuit?

Notes 47

Ask your students to think of some practical applications for this type of circuit. For those who are musically inclined, ask them what the *musical* relationship is between notes whose frequencies are an exact 2:1 ratio (hint: it's the same interval as *eight* white keys on a piano keyboard). How could a circuit such as this possibly be used in a musical synthesizer?

Question 48

The flip-flop circuit shown here is classified as *synchronous* because both flip-flops receive clock pulses at the exact same time:



Define the following parameters:

- Set-up time
- Hold time
- Propagation delay time
- Minimum clock pulse duration

Then, explain how each of these parameters is relevant in the circuit shown.
file 01385

Answer 48

The clock frequency must be slow enough that there is adequate *set-up time* before the next clock pulse. The *propagation delay time* of FF1 must also be larger than the *hold time* of FF2. And, of course, the pulse width of the clock signal must be long enough for both flip-flops to reliably "clock."

Notes 48

I could have simply asked students to define the terms, but where's the fun in that? Seriously, though, these concepts will make far more sense to students when they are viewed in a practical context. After all, the whole purpose of teaching these concepts is so students will be able to *apply* them, right?

Question 49

Locate a manufacturer's datasheet for a flip-flop IC, and research the following parameters:

- Flip-flop type (S-R, D, J-K)
- Part number
- ANSI/IEEE standard symbol
- How many asynchronous inputs
- Minimum setup and hold times (shown in timing diagrams)

file 02937

Answer 49

I'll let you do the research on this question!

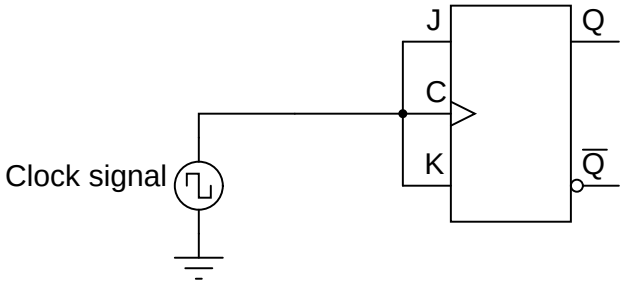
Notes 49

In case students claim they "could not find any parts to research," suggest the following:

- 74107
- 74109
- 74112
- 40174
- 40175

Question 50

A student has an idea to make a J-K flip-flop toggle: why not just connect the J, K, and Clock inputs together and drive them all with the same square-wave pulse? If the inputs are active-high and the clock is positive edge-triggered, the J and K inputs should both go "high" at the same moment the clock signal transitions from low to high, thus establishing the necessary conditions for a toggle (J=1, K=1, clock transition):



Unfortunately, the J-K flip-flop refuses to toggle when this circuit is built. No matter how many clock pulses it receives, the Q and $\overline{Q}$ outputs remain in their original states – the flip-flop remains "latched." Explain the practical reason why the student's flip-flop circuit idea will not work.

file 02938

Answer 50

With all inputs tied together, there is zero setup time on the J and K inputs before the clock pulse rises.

Notes 50

The purpose of this question is to get students to think about setup time, and to see its importance by providing a scenario where the circuit will not work because this parameter has been ignored.

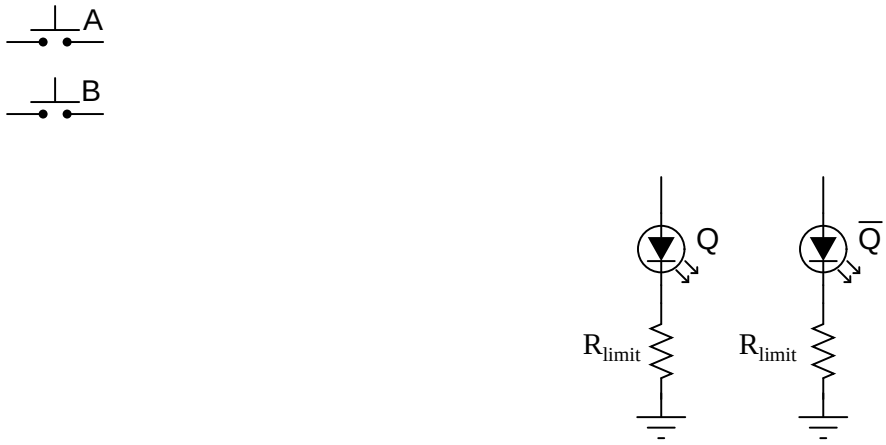
Question 51

Competency: **S-R latch circuit** Version:

Description

Build an S-R latch circuit using either NAND or NOR gates

Schematic



Truth table

Predicted

A	B	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

Actual

A	B	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

file 01621

Answer 51

Use circuit simulation software to verify your predicted and actual truth tables.

Notes 51

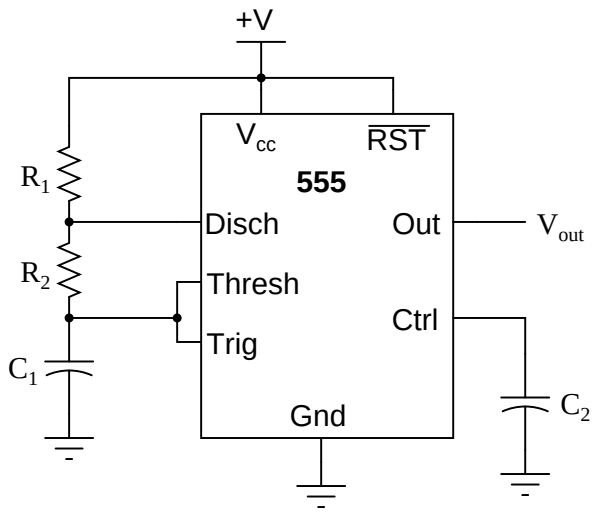
Pushbutton switches are recommended over toggle switches for demonstrating a latch circuit. When the contacts are momentary, the latching characteristics of the circuit becomes more evident to see.

If students use LEDs to indicate the Q and $\overline{Q}$ output states, they may experience trouble with the circuit not latching as it should. This is an excellent example of gate output *loading*, and the importance of proper logic level voltages. If such problems are encountered, advise the student(s) to use over-sized (too large) LED dropping resistors. This will cause the LEDs to be dim, but restore workable voltage levels so that "high" output states are actually interpreted as "high" when fed back to the gate inputs.

Question 52

Competency: **Astable 555 timer** Version:

Schematic



Given conditions

+V = R_1 = R_2 =

-V = C_1 = C_2 =

Parameters

	Predicted	Measured
t_{high}		
t_{low}		
f_{out}		

Fault analysis

Suppose component [ ] fails ☐ open ☐ other _____ ☐ shorted

What will happen in the circuit?

file 02861

Answer 52

Use circuit simulation software to verify your predicted and measured parameter values.

Notes 52

An extension of this exercise is to incorporate troubleshooting questions. Whether using this exercise as a performance assessment or simply as a concept-building lab, you might want to follow up your students' results by asking them to predict the consequences of certain circuit faults.

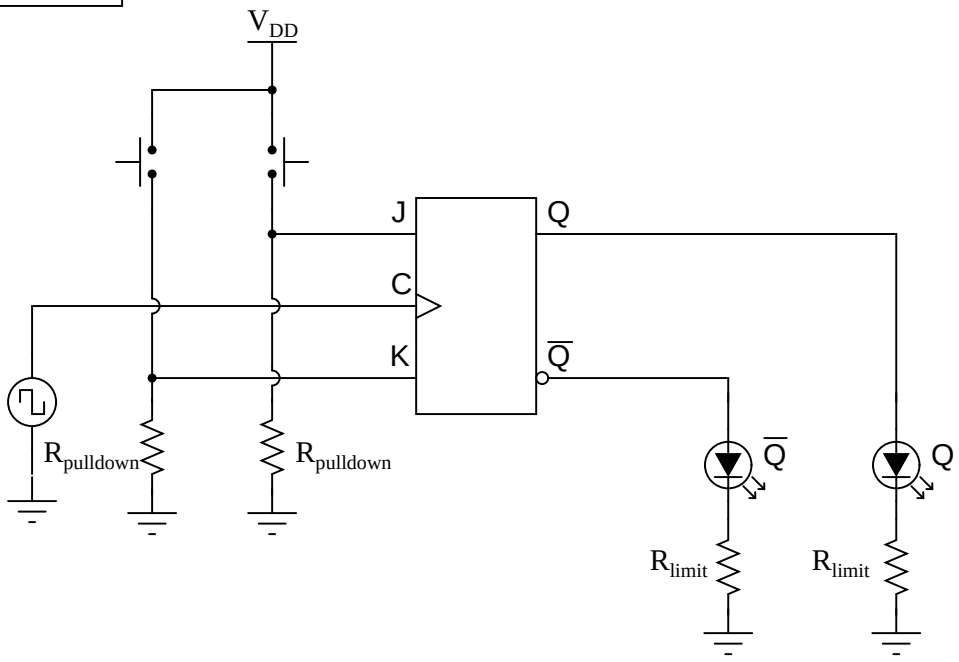
Question 53

Competency: **J-K flip-flop IC** Version:

Description

Demonstrate the "set," "reset," and "toggle" modes of a J-K flip-flop integrated circuit.

Schematic



Parameters

"Set" mode demonstrated ☐

"Reset" mode demonstrated ☐

"Toggle" mode demonstrated ☐

file 02900

Answer 53

Use circuit simulation software to verify your predicted and actual truth tables.

Notes 53

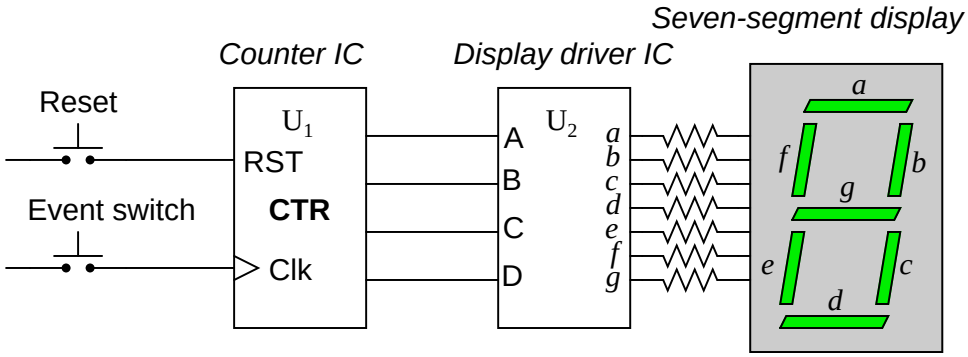
In this activity, students are asked to figure out how to wire the inputs of the J-K flip-flop circuit, and also how to demonstrate the three modes (Set, Reset, and Toggle). Students will have to properly set up their square-wave signal generators to create a workable clock pulse. This not only means a clock pulse at the correct voltage levels, but also one that is slow enough to allow them to clearly see the toggling of the flip-flop.

A great thing to do here is have students use a logic probe to sense the clock pulse and compare that frequency with the blinking of the Q and $\overline{Q}$ LEDs.

Question 54

Competency: **Decade counter circuit** Version:

Schematic



Details purposely omitted from schematic diagram

Given conditions

U_1 = U_2 =

Parameters

Counter increments with each physical event, counting from 0 to 9 and then resetting back to 0 again. Count sequence exhibits no skipped counts and no missed events.

☐ YES

☐ NO

file 03851

Answer 54

Use circuit simulation software to verify your predicted and measured parameter values.

Notes 54

I have purposely left the details of the schematic diagram vague, so that students must do a lot of datasheet research on their own to figure out how to make an event counter circuit. You may choose to give your students part numbers for the integrated circuits, or choose not to, depending on how capable your students are. The point is, they must figure out how to make the ICs work based on what they read from the manufacturer.

Something else students will probably have to do is de-bounce the event switch. Some event switches are inherently bounceless, while others are definitely not. Switch debouncing is something your students need to learn about and integrate into this circuit.

An extension of this exercise is to incorporate troubleshooting questions. Whether using this exercise as a performance assessment or simply as a concept-building lab, you might want to follow up your students' results by asking them to predict the consequences of certain circuit faults.

Question 55

Troubleshooting log

Actions / Measurements / Observations (i.e. *What I did and/or noticed . . .*)	**Conclusions** (i.e. *What this tells me . . .*)

file 03933

Answer 55

I do not provide a grading rubric here, but elsewhere.

Notes 55

The idea of a troubleshooting log is three-fold. First, it gets students in the habit of documenting their troubleshooting procedure and thought process. This is a valuable habit to get into, as it translates to more efficient (and easier-followed) troubleshooting on the job. Second, it provides a way to document student steps for the assessment process, making your job as an instructor easier. Third, it reinforces the notion that each and every measurement or action should be followed by reflection (conclusion), making the troubleshooting process more efficient.

Question 56

NAME: _____ **Troubleshooting Grading Criteria**

You will receive the highest score for which *all* criteria are met.

100 % *(Must meet or exceed all criteria listed)*
A. Absolutely flawless procedure
B. No unnecessary actions or measurements taken

90 % *(Must meet or exceed these criteria in addition to all criteria for 85% and below)*
A. No reversals in procedure (i.e. changing mind without sufficient evidence)
B. Every single action, measurement, and relevant observation properly documented

80 % *(Must meet or exceed these criteria in addition to all criteria for 75% and below)*
A. No more than one unnecessary action or measurement
B. No false conclusions or conceptual errors
C. No missing conclusions (i.e. at least one documented conclusion for action / measurement / observation)

70 % *(Must meet or exceed these criteria in addition to all criteria for 65%)*
A. No more than one false conclusion or conceptual error
B. No more than one conclusion missing (i.e. an action, measurement, or relevant observation without a corresponding conclusion)

65 % *(Must meet or exceed these criteria in addition to all criteria for 60%)*
A. No more than two false conclusions or conceptual errors
B. No more than two unnecessary actions or measurements
C. No more than one undocumented action, measurement, or relevant observation
D. Proper use of all test equipment

60 % *(Must meet or exceed these criteria)*
A. Fault accurately identified
B. Safe procedures used at all times

50 % *(Only applicable where students performed significant development/design work – i.e. not a proven circuit provided with all component values)*
A. Working prototype circuit built and demonstrated

0 % *(If any of the following conditions are true)*
A. Unsafe procedure(s) used at any point

file 03932

Answer 56

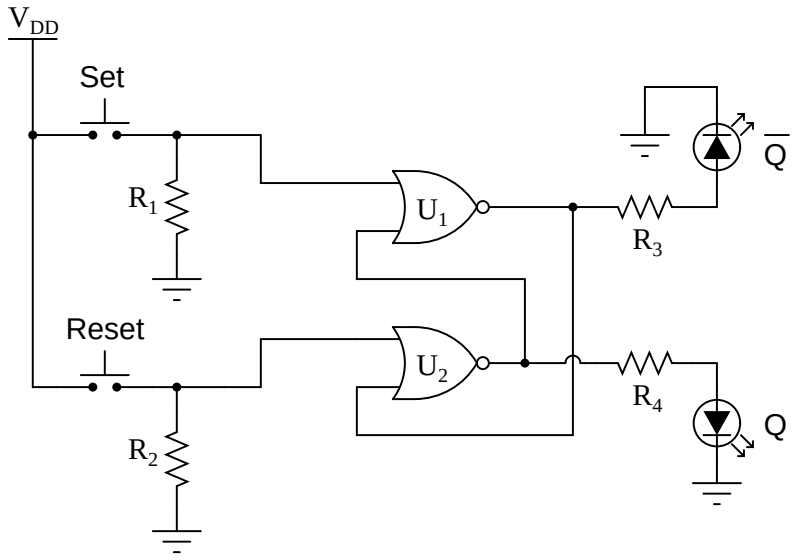
Be sure to document all steps taken and conclusions made in your troubleshooting!

Notes 56

The purpose of this assessment rubric is to act as a sort of "contract" between you (the instructor) and your student. This way, the expectations are all clearly known in advance, which goes a long way toward disarming problems later when it is time to grade.

Question 57

Identify at least one component fault that would cause the "$\overline{Q}$" LED to always remain off, no matter what was done with the input switches.



For each of your proposed faults, explain *why* it will cause the described problem.
file 03892

Answer 57

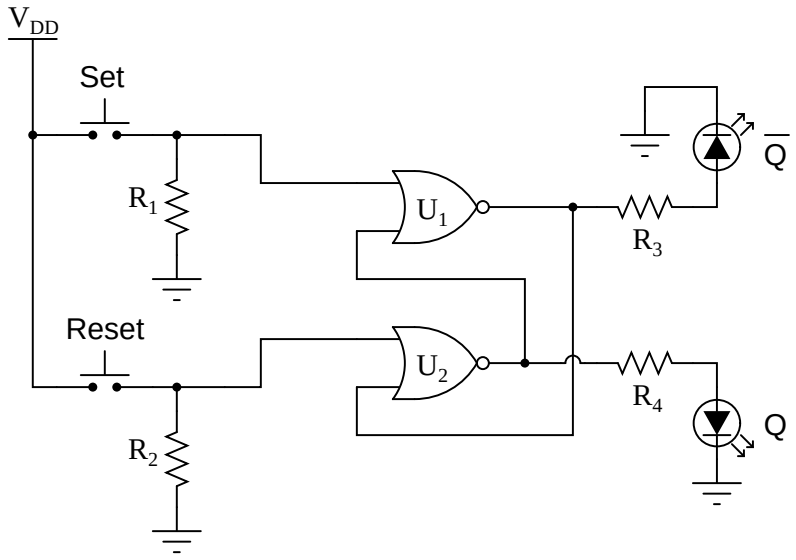
- Resistor R_3 failed open.
- NOR gate U_1 output failed low.
- Resistor R_1 failed open (provided enough ambient electrical noise to activate a floating gate input).
- "Set" switch contacts failed shorted.

Notes 57

Latch circuits can be confusing due to their use of positive feedback. Questions such as this are important tools for helping develop your students' understanding of latch circuits.

Question 58

Identify at least one component fault that would cause the "Q" LED to always stay on, no matter what was done with the input switches.



For each of your proposed faults, explain *why* it will cause the described problem.
file 03891

Answer 58

- NOR gate U_2 output failed high.
- Wire break between "Reset" switch and resistor R_2 (although if this was the only fault it may allow the Q LED to energize at power-up, just not de-energize after the "Set" button had been pressed).

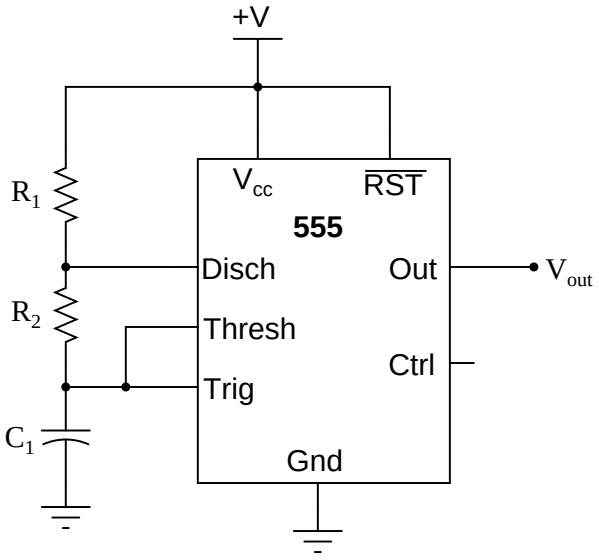
Follow-up question: explain why the nature of the problem rules out the possibility of the only fault being something related to the feedback connections between U_1 and U_2.

Notes 58

Latch circuits can be confusing due to their use of positive feedback. Questions such as this are important tools for helping develop your students' understanding of latch circuits.

Question 59

Predict how the operation of this astable 555 timer circuit will be affected as a result of the following faults. Specifically, identify what will happen to the capacitor voltage (V_{C1}) and the output voltage (V_{out}) for each fault condition. Consider each fault independently (i.e. one at a time, no multiple faults):



- Resistor R_1 fails open:
- Solder bridge (short) across resistor R_1:
- Resistor R_2 fails open:
- Solder bridge (short) across resistor R_2:
- Capacitor C_1 fails shorted:

For each of these conditions, explain *why* the resulting effects will occur.
file 03890

Answer 59

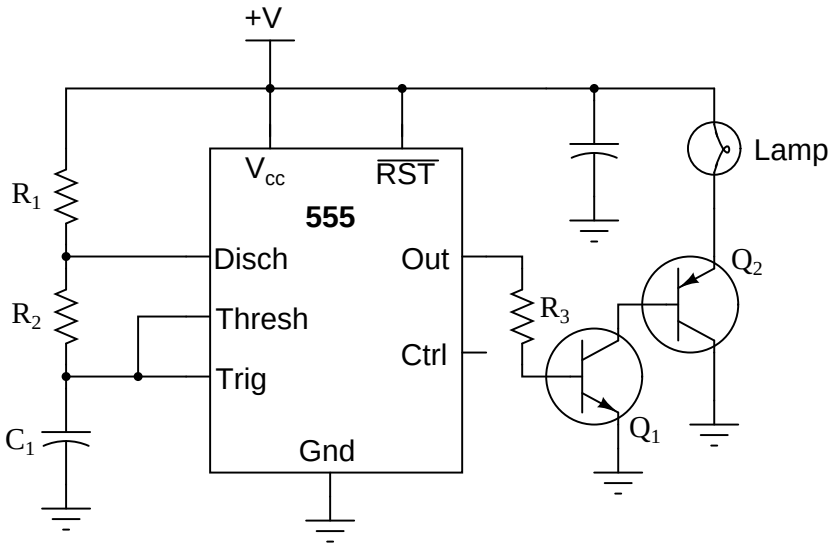
- Resistor R_1 fails open: *Capacitor voltage holds at last value, output voltage holds at last value.*
- Solder bridge (short) across resistor R_1: *Timer IC will become damaged at the first discharge cycle.*
- Resistor R_2 fails open: *Capacitor voltage holds at last value, output voltage holds at last value.*
- Solder bridge (short) across resistor R_2: *Oscillation frequency nearly doubles, and the duty cycle increases to nearly 100%.*
- Capacitor C_1 fails shorted: *Capacitor voltage goes to 0 volts DC, output voltage stays "high".*

Notes 59

The purpose of this question is to approach the domain of circuit troubleshooting from a perspective of knowing what the fault is, rather than only knowing what the symptoms are. Although this is not necessarily a realistic perspective, it helps students build the foundational knowledge necessary to diagnose a faulted circuit from empirical data. Questions such as this should be followed (eventually) by other questions asking students to identify likely faults based on measurements.

Question 60

This circuit uses a "555" integrated circuit to produce a low-frequency square-wave voltage signal (seen between the "Out" terminal of the chip and ground), which is used to turn a pair of transistors on and off to flash a large lamp. Predict how this circuit will be affected as a result of the following faults. Consider each fault independently (i.e. one at a time, no multiple faults):



- Transistor Q_1 fails open (collector-to-emitter):
- Transistor Q_2 fails open (collector-to-emitter):
- Resistor R_3 fails open:
- Transistor Q_1 fails shorted (collector-to-emitter):

For each of these conditions, explain *why* the resulting effects will occur.
file 03715

Answer 60

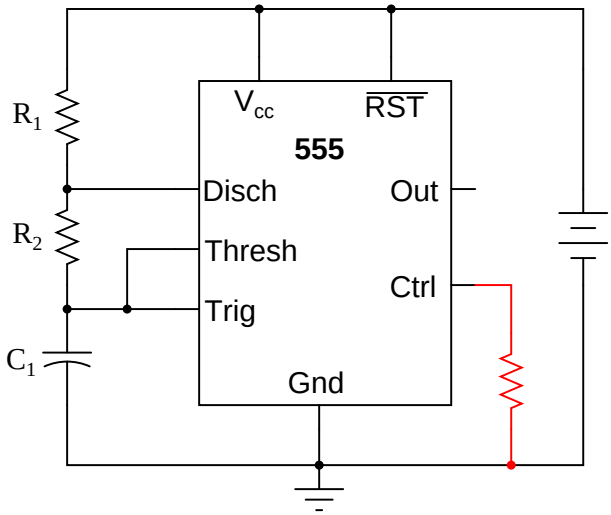
- Transistor Q_1 fails open (collector-to-emitter): *Lamp remains off, no current through any terminal of* Q_2.
- Transistor Q_2 fails open (collector-to-emitter): *Lamp remains off, no current through any terminal of* Q_2, *normal base current through* Q_1, *no current through collector of* Q_1.
- Resistor R_3 fails open: *Lamp remains off, no current through any terminal of* Q_1 *or* Q_2.
- Transistor Q_1 fails shorted (collector-to-emitter): *Lamp remains on, full "on" current levels through terminals of* Q_1 *and* Q_2.

Notes 60

The purpose of this question is to approach the domain of circuit troubleshooting from a perspective of knowing what the fault is, rather than only knowing what the symptoms are. Although this is not necessarily a realistic perspective, it helps students build the foundational knowledge necessary to diagnose a faulted circuit from empirical data. Questions such as this should be followed (eventually) by other questions asking students to identify likely faults based on measurements.

Question 61

What would happen to the operation of this astable 555 timer circuit if a resistor were accidently connected between the "Control" terminal and ground? Explain the reason for your answer.



file 01435

Answer 61

The addition of a resistor between the Control terminal and ground would increase the frequency of the circuit, as well as decrease the peak-to-peak amplitude of the "sawtooth" wave signal across the timing capacitor.

Follow-up question: does the addition of this resistor affect the output signal (pin 3) amplitude as well? Explain why or why not. If it amplitude is affected, does it increase or decrease with the resistor in place?

Notes 61

Ask your students to explain *why* frequency and amplitude changes in this circuit. It is far too easy for a student to simply repeat the answer given by the worksheet! Hold your students accountable to reasoning through the operation of a circuit like this.

Question 62

A student builds their first astable 555 timer circuit, using a TLC555CP chip. Unfortunately, it seems to have a problem. Sometimes, the output of the timer simply stops oscillating, with no apparent cause. Stranger yet, the problem often occurs at the precise time anyone moves their hand within a few inches of the circuit board (without actually touching anything!).

What could the student have done wrong in assembling this circuit to cause such a problem? What steps would you take to troubleshoot this problem?

file 01433

Answer 62

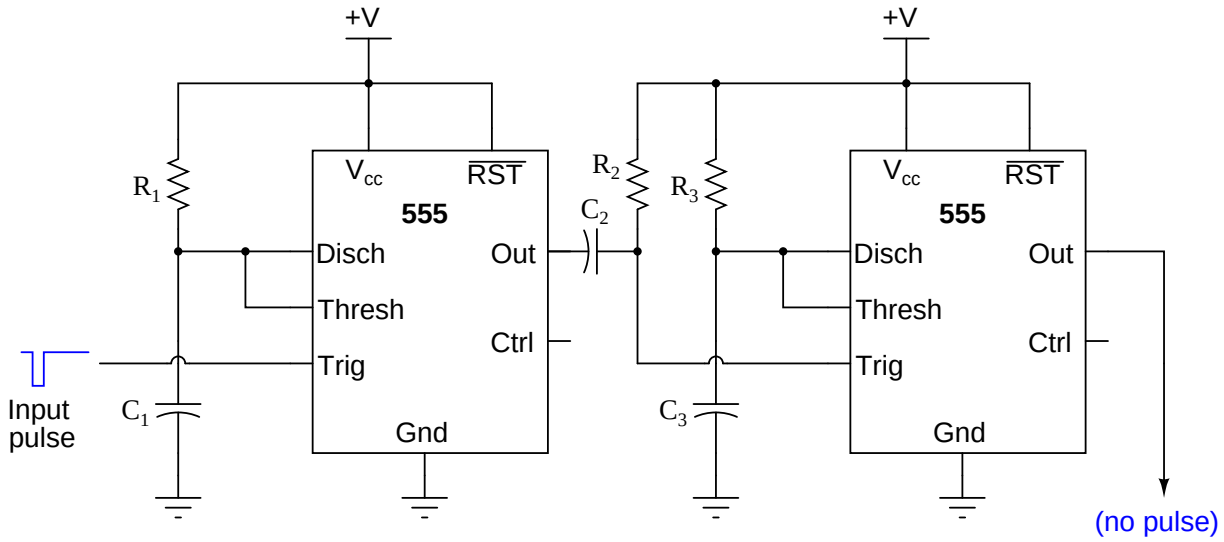
I won't reveal the most probable cause, but I will give you this hint: the TLC555CP integrated circuit ("chip") uses CMOS technology.

Notes 62

Every year it seems I have at least one student who experiences this particular problem, usually as a result of hasty circuit assembly (not making all necessary connections to pins on the chip). This is a good question to brainstorm with your class on, exploring possible causes and methods of diagnosis.

Question 63

Identify at least one component fault that would cause the final 555 timer output to always remain low:



For each of your proposed faults, explain *why* it will cause the described problem.
file 03893

Answer 63

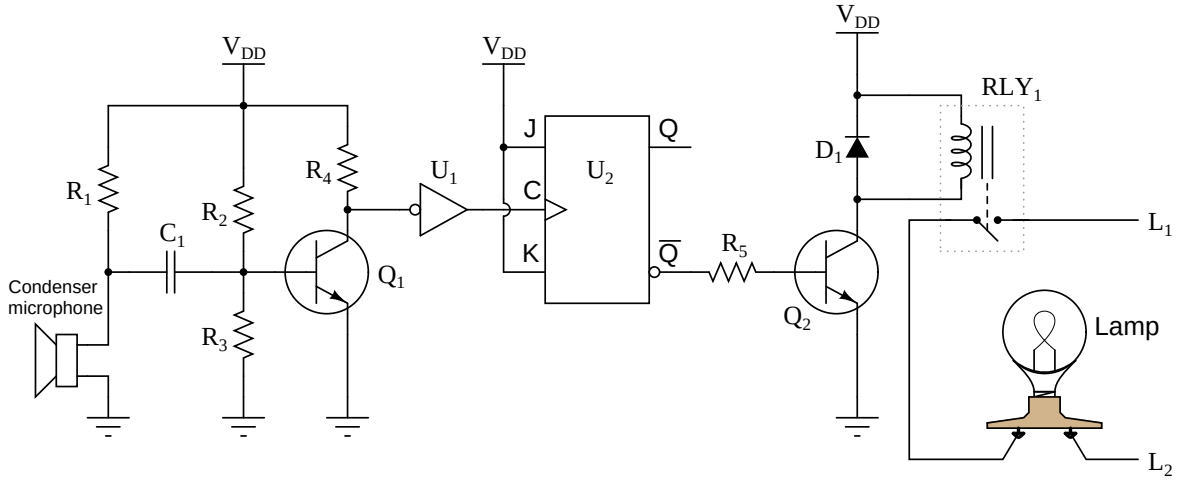
- Resistor R_1 failed open.
- Solder bridge past resistor R_2.
- No power to either 555 timer IC.

Notes 63

Be sure to discuss the reasons why each of your students' proposed component faults would cause the final output to never go high. The possibilities range from the obvious to the obscure, and exploring them will strengthen your students' understanding of the 555 as a monostable multivibrator.

Question 64

Predict how the operation of this sound-activated lamp circuit will be affected as a result of the following faults. Consider each fault independently (i.e. one at a time, no multiple faults):



- Resistor R_1 fails open:
- Resistor R_3 fails open:
- Diode D_1 fails open:
- Transistor Q_2 fails shorted between collector and emitter:
- Solder bridge past resistor R_5:

For each of these conditions, explain *why* the resulting effects will occur.
file 03894

Answer 64

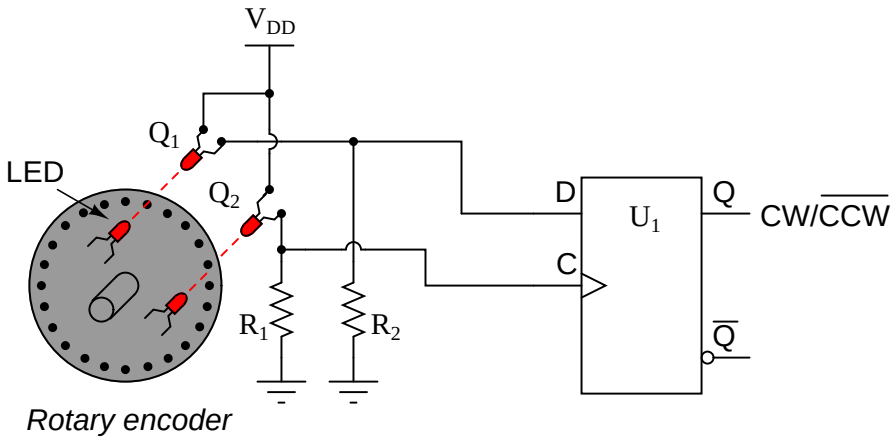
- Resistor R_1 fails open: *Lamp status does not change.*
- Resistor R_3 fails open: *Lamp status does not change.*
- Diode D_1 fails open: *Circuit works fine for a few cycles, then fails with the lamp either remaining on or remaining off (due to failed transistor Q_2).*
- Transistor Q_2 fails shorted between collector and emitter: *Lamp remains on.*
- Solder bridge past resistor R_5: *Possible failure of flip-flop U_2 or transistor Q_2 after extended periods of time with the lamp on.*

Notes 64

The purpose of this question is to approach the domain of circuit troubleshooting from a perspective of knowing what the fault is, rather than only knowing what the symptoms are. Although this is not necessarily a realistic perspective, it helps students build the foundational knowledge necessary to diagnose a faulted circuit from empirical data. Questions such as this should be followed (eventually) by other questions asking students to identify likely faults based on measurements.

Question 65

Identify at least one component fault that would cause the flip-flop to indicate "clockwise" all the time, regardless of encoder motion:



For each of your proposed faults, explain *why* it will cause the described problem.
file 03895

Answer 65

- Phototransistor Q_1 failed shorted.
- Resistor R_2 failed open.
- Flipflop U_1 output failed high.

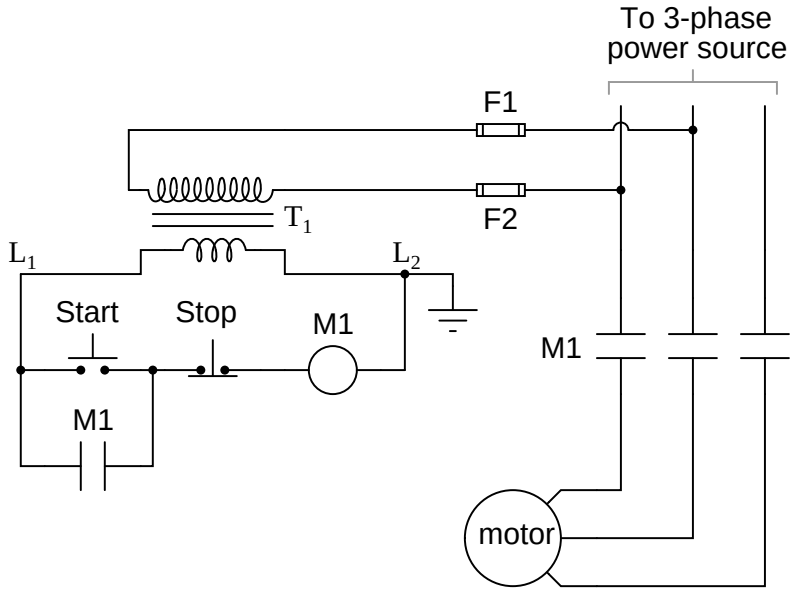
Follow-up question: explain why the presence of ambient light near the phototransistors could also cause this problem to occur.

Notes 65

Be sure to discuss with your students the reasons why their proposed faults would cause the stated problem.

Question 66

Identify at least one fault that would cause the motor to turn off immediately once the "Start" pushbutton switch was released, instead of "latch" in the run mode as it should:



For each of your proposed faults, explain *why* it will cause the described problem.
file 03896

Answer 66

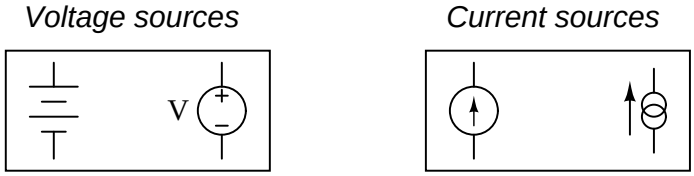
- M1 control contact failed open.
- Wire(s) between M1 control contact and control circuit broken open.

Notes 66

This form of motor control circuit is *very* popular in industry. It is well worth your students' time to study it and understand both how and why it works.

Question 67

Ideal *voltage sources* and ideal *current sources*, while both being sources of electrical power, behave very differently from one another:



Explain how each type of electrical source would behave if connected to a variable-resistance load. As this variable resistance were increased and decreased, how would each type of source respond?

file 03226

Answer 67

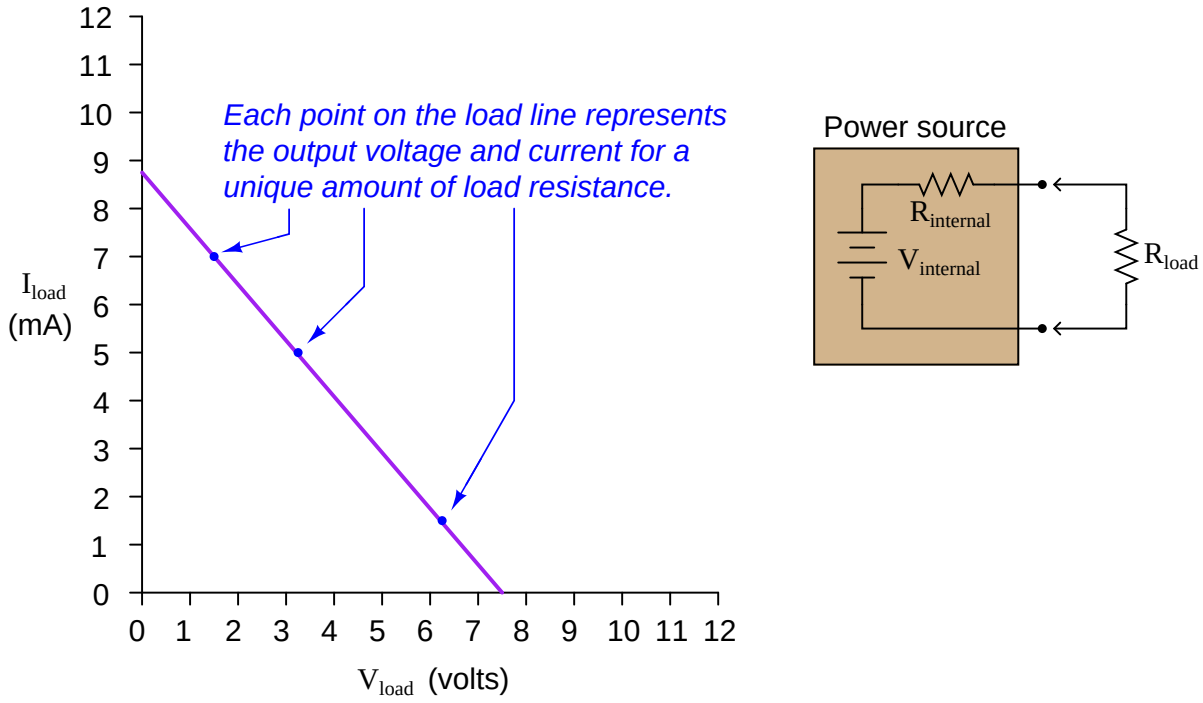
An ideal voltage source will output as much or as little current as necessary to maintain a constant voltage across its output terminals, for any given load resistance. An ideal current source will output as much or as little voltage as necessary to maintain a constant current through it, for any given load resistance.

Notes 67

Ask your students to think of a few "thought experiment" scenarios where voltage and current sources could be put to test. Have them invent voltage and current values for these voltage and current sources, respectively, then calculate all other circuit parameters given several different values of load resistance.

Question 68

A very common sort of graph used in electronics work is the *load line*, showing all possibilities of load voltage and load current that a particular power source is able to supply to a load:

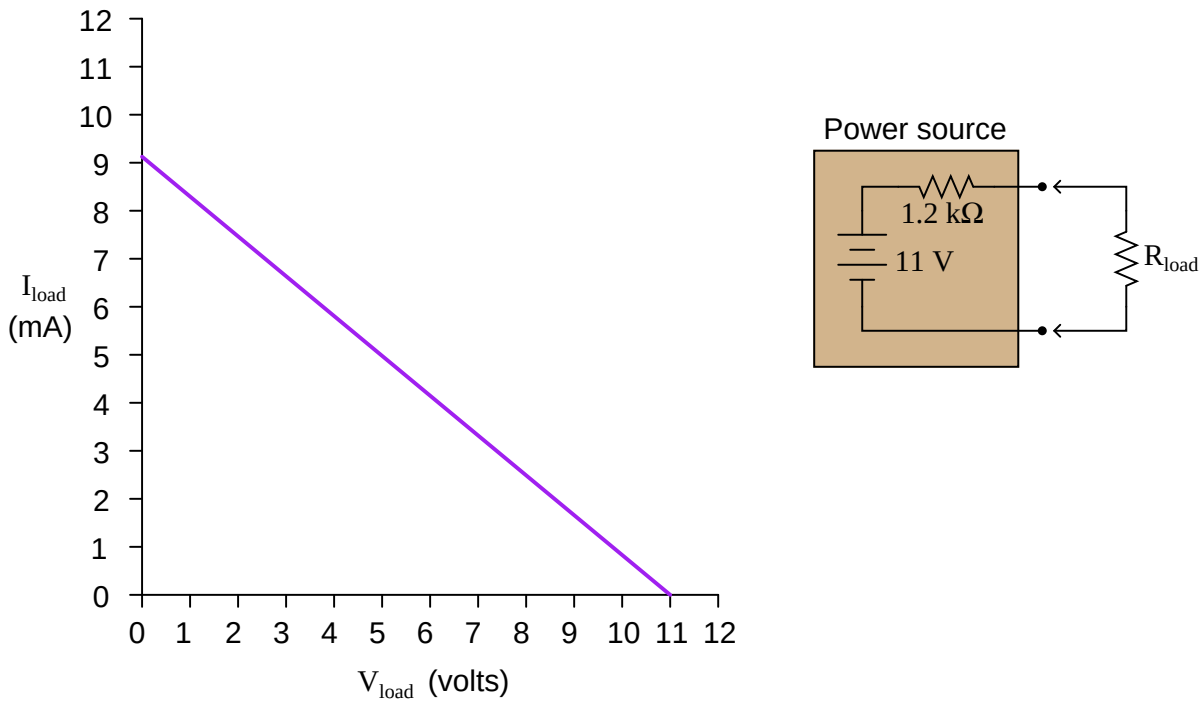


Note how the load line shows the voltage "sag" of the power source in relation to the amount of current drawn by the load. At high currents, the output voltage will be very low (upper-left end of load line). At low currents, the output voltage will be near its maximum (lower-right end of load line). If all internal components of the power source are *linear* in nature, the load line will always be perfectly straight.

Plot the load line for a power source having an internal voltage ($V_{internal}$) of 11 volts and an internal resistance ($R_{internal}$) of 1.2 kΩ. Superimpose your load line onto the load line graph shown above. Hint: it only takes two points to define a line!

file 03513

Answer 68



Hint: the easiest points on find on this load line are the points representing open-circuit and short-circuit conditions (i.e. $R_{load} = \infty\ \Omega$ and $R_{load} = 0\ \Omega$, respectively).

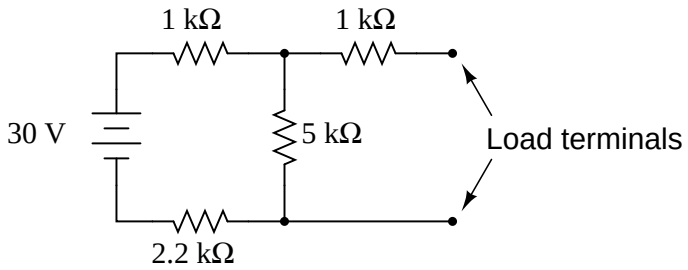
Follow-up questions: what will happen to the load line if we change the internal resistance of the power source circuit? What will happen to the load line if we change the internal voltage value of the power source circuit?

Notes 68

The purpose of this question is to lend an analytical geometric perspective to the subject of power source behavior, by showing how the output voltage and current may be plotted on a graph. The condition of circuit linearity is important, as it permits us to confidently plot the load line by finding only two points on it.

Question 69

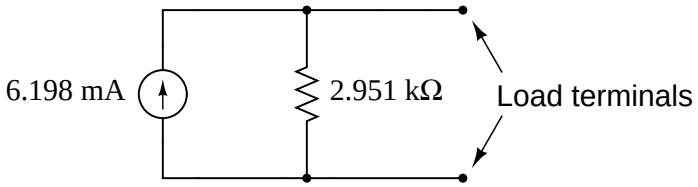
Give a step-by-step procedure for reducing this circuit to a Norton equivalent circuit (one current source in parallel with one resistor):



file 03230

Answer 69

I will let you research the procedure for determining Norton equivalent circuits, and explain it in your own words. Here is the equivalent circuit for the circuit given in the question:

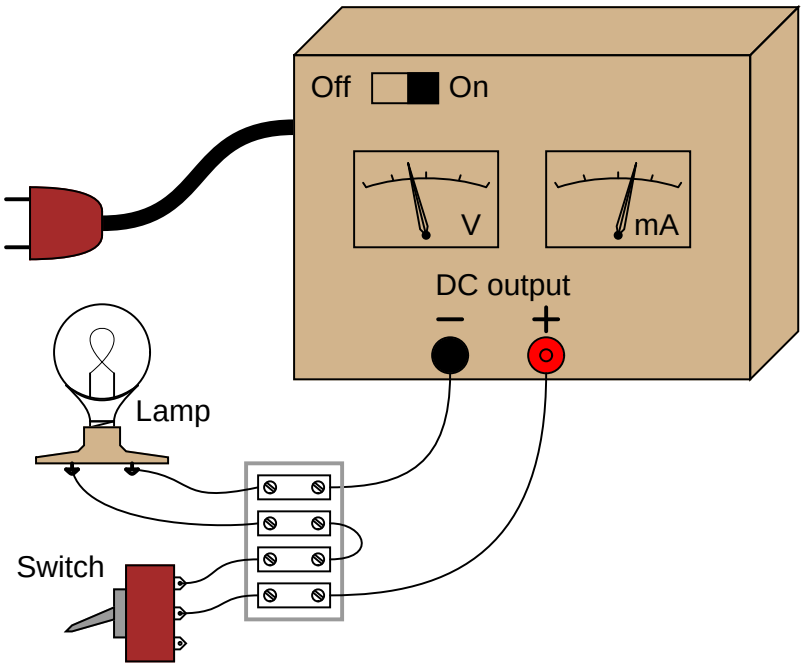


Notes 69

It should be easy for your students to research an algorithm (step-by-step procedure) for determining a Norton equivalent circuit. Let them do the work, and explain it to you and their classmates!

Question 70

Suppose you had an AC/DC power supply, which performed as follows (open-circuit and loaded test conditions):



Switch off:

V_{out} = 14.3 volts DC

I_{out} = 0 mA DC

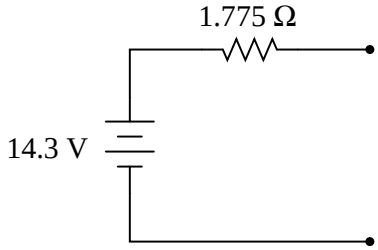
Switch on:

V_{out} = 12.8 volts DC

I_{out} = 845 mA DC

Draw a Thévenin equivalent circuit to model the behavior of this power supply.
file 03693

Answer 70



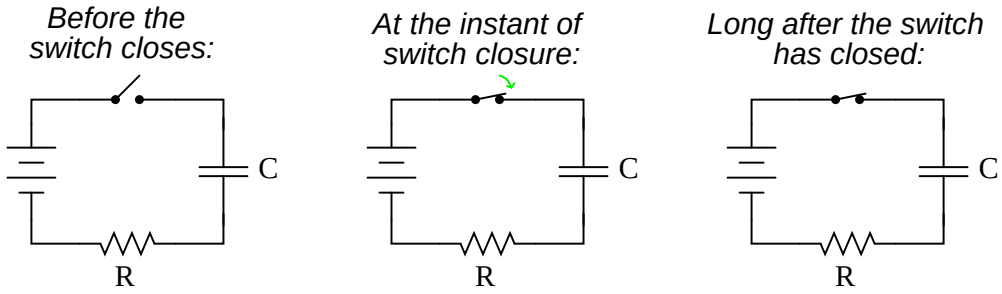
Follow-up question: is the switch shown in the *on* or *off* position, in the pictorial diagram?

Notes 70

Discuss with your students how Thévenin's theorem allows us to model fairly complex power-supply circuits as simply a voltage source and series resistance (at least approximately). Discuss also the limitations of this modeling, especially in light of the condition of linearity for the proper application of Thévenin's theorem.

Question 71

Qualitatively determine the voltages across all components as well as the current through all components in this simple RC circuit at three different times: (1) just before the switch closes, (2) at the instant the switch contacts touch, and (3) after the switch has been closed for a long time. Assume that the capacitor begins in a completely discharged state:



Express your answers qualitatively: "maximum," "minimum," or perhaps "zero" if you know that to be the case.

Before the switch closes:

$V_C =$
$V_R =$
$V_{switch} =$
$I =$

At the instant of switch closure:

$V_C =$
$V_R =$
$V_{switch} =$
$I =$

Long after the switch has closed:

$V_C =$
$V_R =$
$V_{switch} =$
$I =$

Hint: a graph may be a helpful tool for determining the answers!
file 01811

Answer 71

Before the switch closes:

$V_C =$ zero
$V_R =$ zero
$V_{switch} =$ maximum
$I =$ zero

At the instant of switch closure:

$V_C =$ zero
$V_R =$ maximum
$V_{switch} =$ zero
$I =$ maximum

Long after the switch has closed:

V_C = maximum
V_R = zero
V_{switch} = zero
I = zero

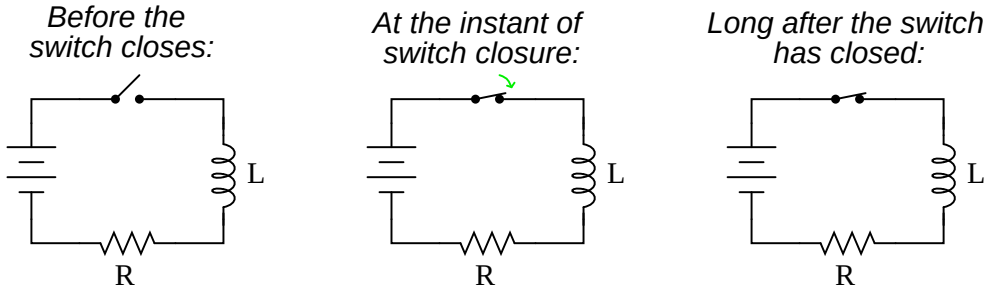
Follow-up question: which of these variables remained the same immediately before and immediately after switch closure? Explain why.

Notes 71

The purpose of this question is to preview the concept of "initial" and "final" values in RC circuits, before they learn to use the "universal time constant formula."

Question 72

Qualitatively determine the voltages across all components as well as the current through all components in this simple LR circuit at three different times: (1) just before the switch closes, (2) at the instant the switch contacts touch, and (3) after the switch has been closed for a long time.



Express your answers qualitatively: "maximum," "minimum," or perhaps "zero" if you know that to be the case.

Before the switch closes:

$V_L =$
$V_R =$
$V_{switch} =$
$I =$

At the instant of switch closure:

$V_L =$
$V_R =$
$V_{switch} =$
$I =$

Long after the switch has closed:

$V_L =$
$V_R =$
$V_{switch} =$
$I =$

Hint: a graph may be a helpful tool for determining the answers!

file 01812

Answer 72

Before the switch closes:

$V_L =$ zero
$V_R =$ zero
$V_{switch} =$ maximum
$I =$ zero

At the instant of switch closure:

$V_L =$ maximum
$V_R =$ zero
$V_{switch} =$ zero
$I =$ zero

Long after the switch has closed:

V_L = zero
V_R = maximum
V_{switch} = zero
I = maximum

Follow-up question: which of these variables remained the same immediately before and immediately after switch closure? Explain why.

Notes 72

The purpose of this question is to preview the concept of "initial" and "final" values in RC circuits, before they learn to use the "universal time constant formula."

Question 73

What value of resistor would need to be connected in series with a 33 μF capacitor in order to provide a *time constant* (τ) of 10 seconds? Express your answer in the form of a five-band precision resistor color code (with a tolerance of +/- 0.1%).

file 00436

Answer 73

Org, Blk, Org, Org, Vio

Notes 73

In order for students to answer this question, they must research the RC time constant equation and review the 5-band resistor color code.

Question 74

An electronic service technician prepares to work on a high-voltage power supply circuit containing one large capacitor. On the side of this capacitor are the following specifications:

3000 WVDC $\quad 0.75\mu$F

Obviously this device poses a certain amount of danger, even with the AC line power secured (lock-out/tag-out). Discharging this capacitor by directly shorting its terminals with a screwdriver or some other piece of metal might be dangerous due to the quantity of the stored charge. What needs to be done is to discharge this capacitor at a modest rate.

The technician realizes that she can discharge the capacitor at any rate desired by connecting a resistor in parallel with it (holding the resistor with electrically-insulated pliers, of course, to avoid having to touch either terminal). What size resistor should she use, if she wants to discharge the capacitor to less than 1% charge in 15 seconds? State your answer using the standard 4-band resistor color code (tolerance = +/- 10%).

file 01525

Answer 74

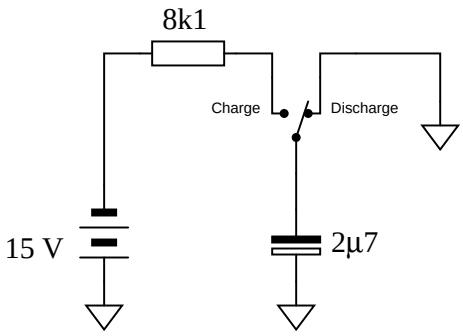
Yellow, Black, Green, Silver (assuming 5 time constants' worth of time: just less than 1% charge). Yellow, Orange, Green, Silver for a discharge down to 1% in 15 seconds.

Notes 74

In order to answer this question, students must not only be able to calculate time constants for a simple RC circuit, but they must also remember the resistor color code so as to choose the right size based on color. A very practical problem, and important for safety reasons too!

Question 75

The following circuit allows a capacitor to be rapidly discharged and slowly charged:



Suppose that the switch was left in the "discharge" position for some substantial amount of time. Then, someone moves the switch to the "charge" position to let the capacitor charge. Calculate the amount of capacitor voltage and capacitor current at exactly 45 milliseconds after moving the switch to the "charge" position.

$V_C =$ _____ @ $t = 45$ ms

$I_C =$ _____ @ $t = 45$ ms

file 03557

Answer 75

$V_C =$ -13.08 volts @ $t = 45$ ms

$I_C =$ 236.6 μA @ $t = 45$ ms

Follow-up question: show the directions of charge and discharge current in this circuit.

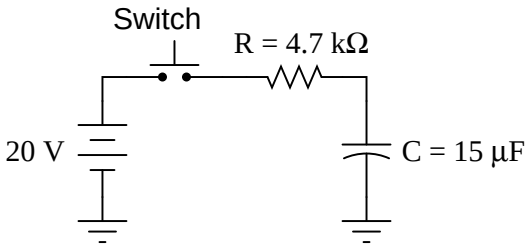
Notes 75

Here, students must choose which equation(s) to use for the calculation, calculate the time constant for the circuit, and put all the variables in the right place to obtain the correct answers. Discuss all these steps with your students, allowing them to explain how they approached the question.

If anyone asks, let them know that the capacitor symbol shown represents a polarized (electrolytic) capacitor.

Question 76

Determine the capacitor voltage and capacitor current at the specified times (time $t = 0$ milliseconds being the exact moment the switch contacts close). Assume the capacitor begins in a fully discharged state:



Time	V_C (volts)	I_C (mA)
0 ms		
30 ms		
60 ms		
90 ms		
120 ms		
150 ms		

file 03556

Answer 76

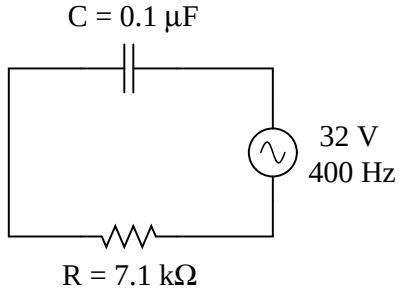
Time	V_C (volts)	I_C (mA)
0 ms	0	4.255
30 ms	6.932	2.781
60 ms	11.46	1.817
90 ms	14.42	1.187
120 ms	16.35	0.7757
150 ms	17.62	0.5069

Notes 76

Be sure to have your students share their problem-solving techniques (how they determined which equation to use, etc.) in class.

Question 77

Calculate the power factor of this circuit:



file 02179

Answer 77

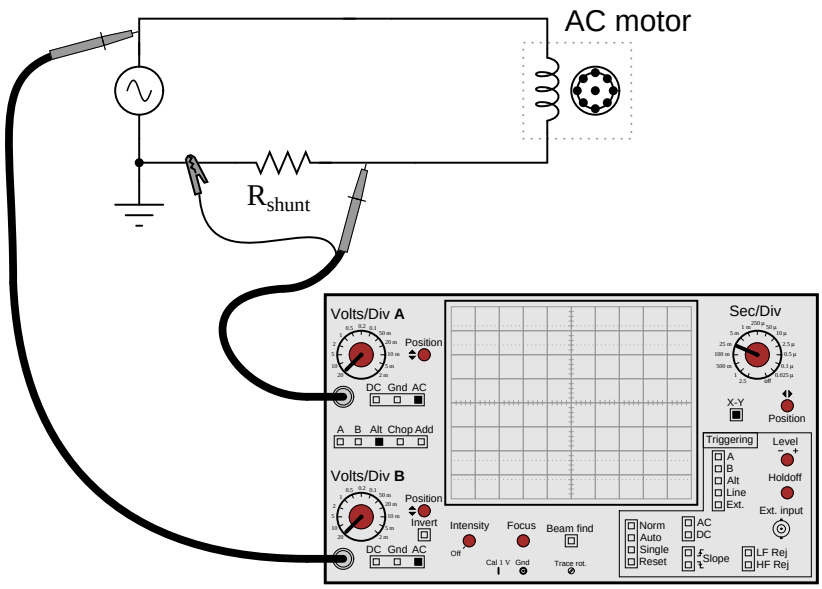
P.F. = 0.872

Notes 77

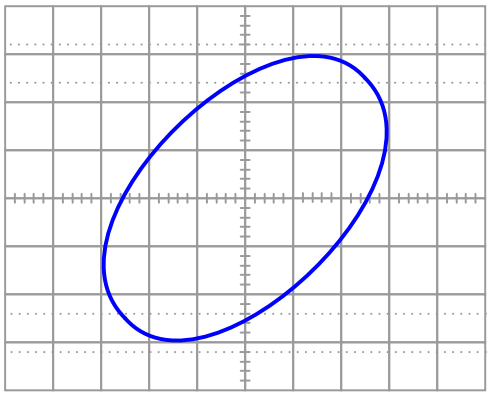
In order to solve for power factor, your students must find at least one formula to use for calculating it. There is definitely more than one method of solution here, so be sure to ask multiple students to share their strategies for the benefit of all.

Question 78

An oscilloscope is connected to a low-current AC motor circuit to measure both voltage and current, and plot them against one another as a Lissajous figure:



The following Lissajous figure is obtained from this measurement:



From this figure, calculate the phase angle (Θ) and the power factor for this motor circuit.
file 02183

Answer 78

$\Theta \approx 57^o$ P.F. ≈ 0.54

Follow-up question: is this the only way we could have used the oscilloscope to measure phase shift between voltage and current, or is there another mode of operation besides plotting Lissajous figures?

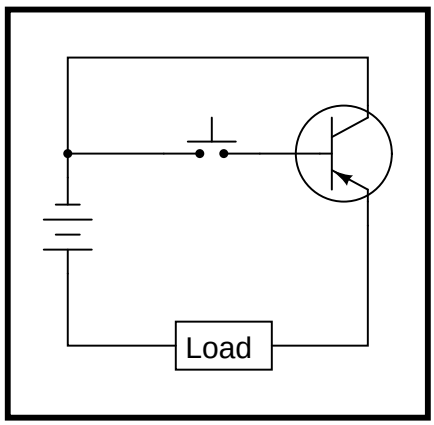
Notes 78

Ask your students to explain the function of the resistor R_{shunt} shown in the schematic diagram. Discuss whether or not this resistor should have a very low or a very high resistance value. Also discuss the placement of the oscilloscope's ground clip, which is very important in a potentially lethal AC power circuit.

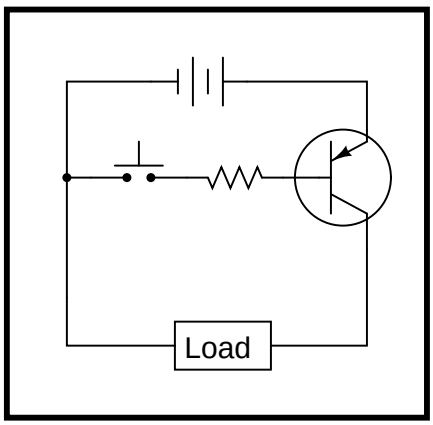
Question 79

Some of the following transistor switch circuits are properly configured, and some are not. Identify which of these circuits will function properly (i.e. turn on the load when the switch closes) and which of these circuits are mis-wired:

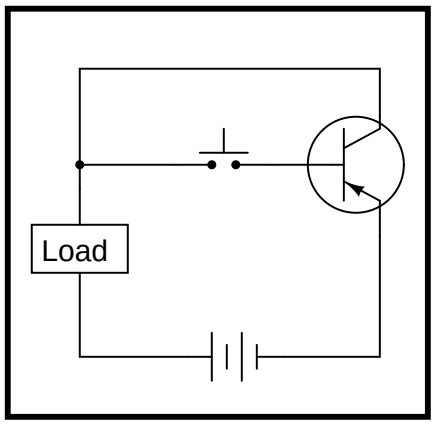
Circuit 1



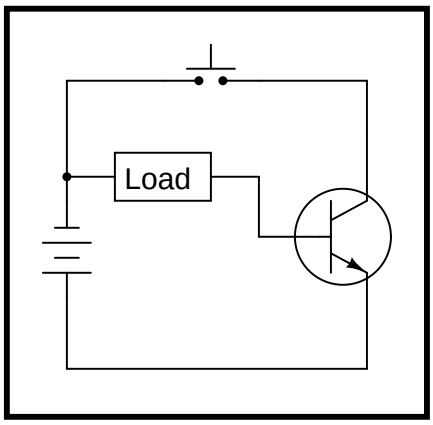
Circuit 2



Circuit 3

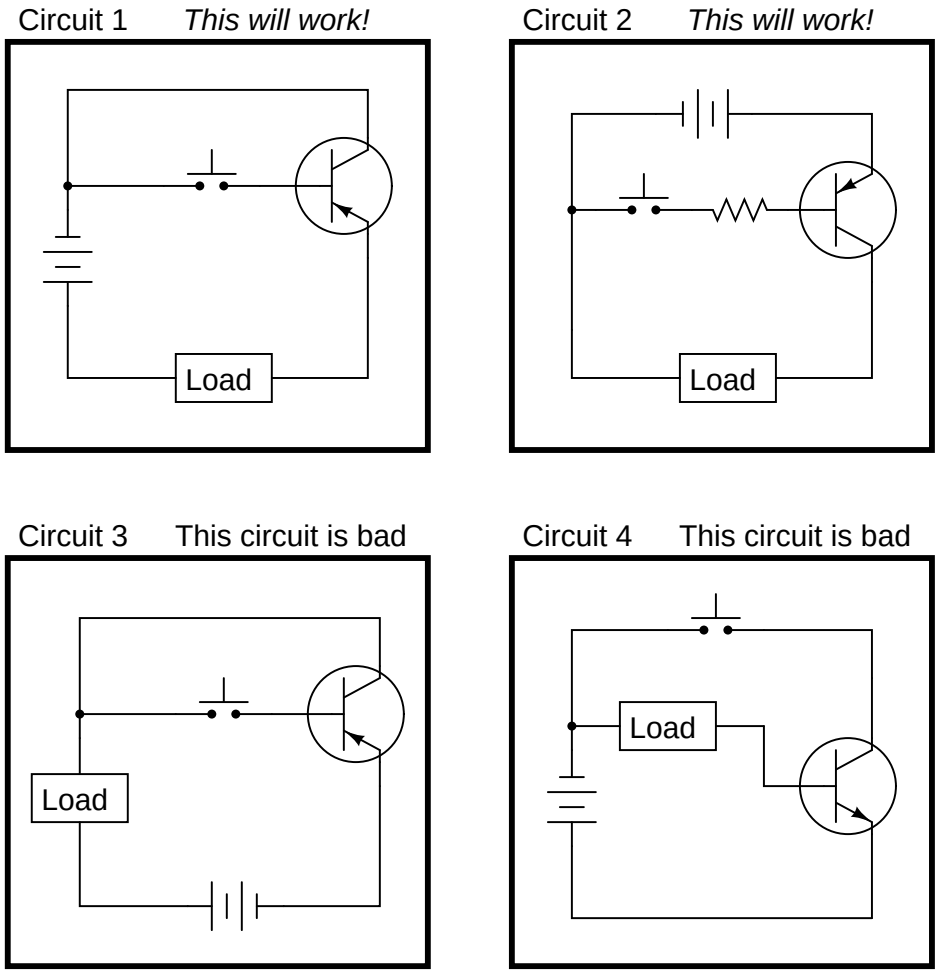


Circuit 4



file 02326

Answer 79



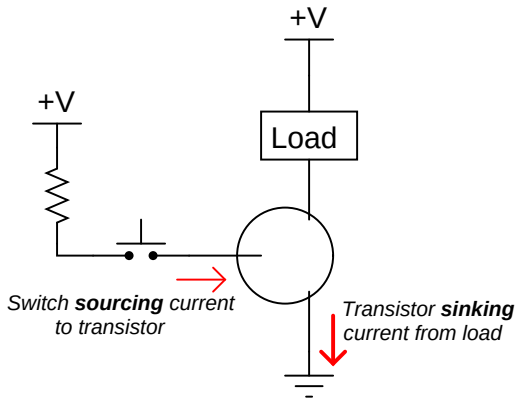
Notes 79

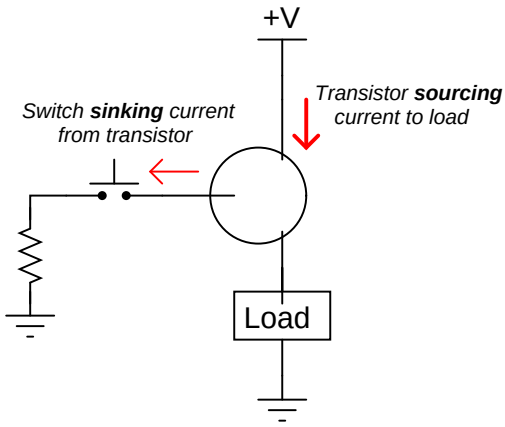
This is a very important concept for students to learn if they are to do any switch circuit design – a task not limited to engineers. Technicians often must piece together simple transistor switching circuits to accomplish specific tasks on the job, so it is important for them to be able to design switching circuits that will work.

Have your students describe to the class how they were able to determine the status of each circuit, so that everyone may learn new ways of looking at this type of problem. Also have them describe what would have to be changed in the "bad" circuits to make them functional.

Question 80

Choose the right type of bipolar junction transistor for each of these switching applications, drawing the correct transistor symbol inside each circle:

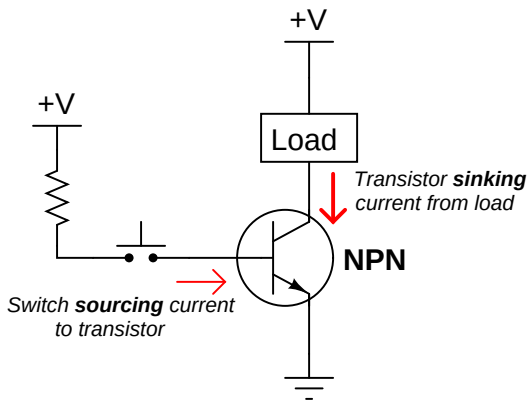


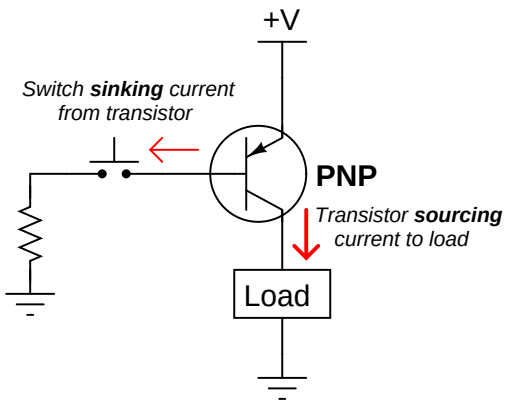


Also, explain why resistors are necessary in both these circuits for the transistors to function without being damaged.

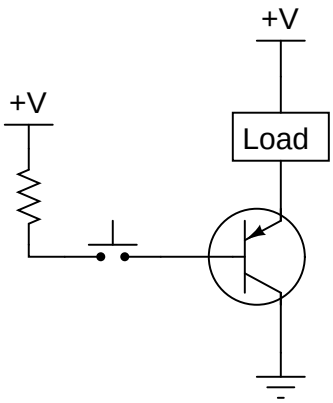
file 02408

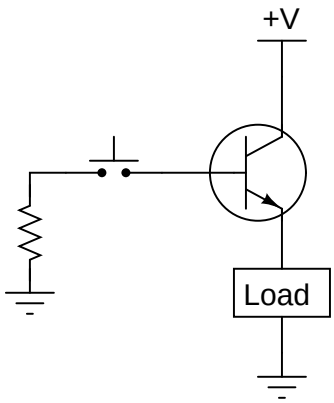
Answer 80





Follow-up question: explain why neither of the following transistor circuits will work. When the pushbutton switch is actuated, the load remains de-energized:





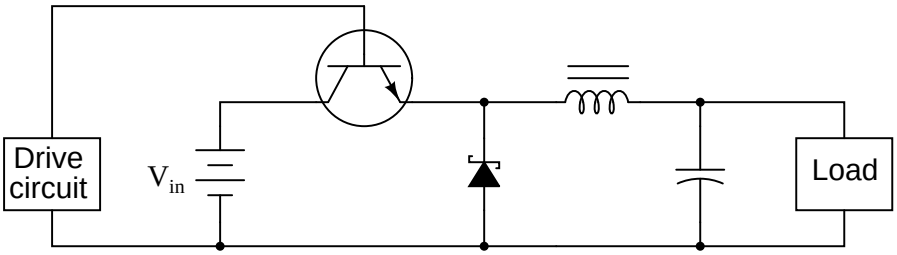
Notes 80

Discuss with your students the meaning of the words "sourcing" and "sinking" in case they are not yet familiar with them. These are very common terms used in electronics (especially digital and power circuitry!), and they make the most sense in the context of conventional flow current notation.

In order for students to properly choose and place each transistor to make the circuits functional, they must understand how BJTs are triggered on (forward-biasing of the base-emitter junction) and also which directions the currents move through BJTs. The two example circuits shown in this question are very realistic.

Question 81

The schematic diagram shown here is for a *"buck" converter circuit*, a type of DC-DC "switching" power conversion circuit:

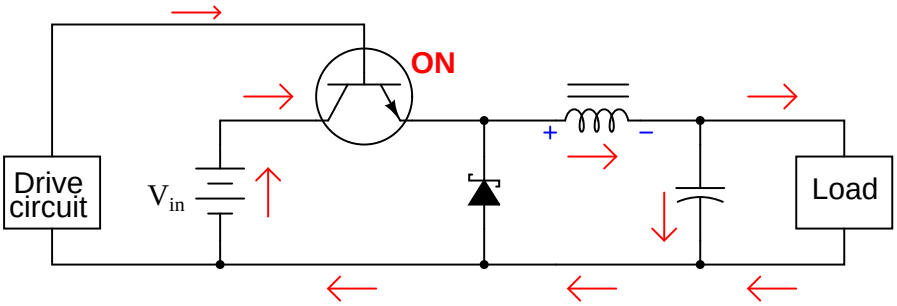


In this circuit, the transistor is either fully on or fully off; that is, driven between the extremes of saturation or cutoff. By avoiding the transistor's "active" mode (where it would drop substantial voltage while conducting current), very low transistor power dissipations can be achieved. With little power wasted in the form of heat, "switching" power conversion circuits are typically very efficient.

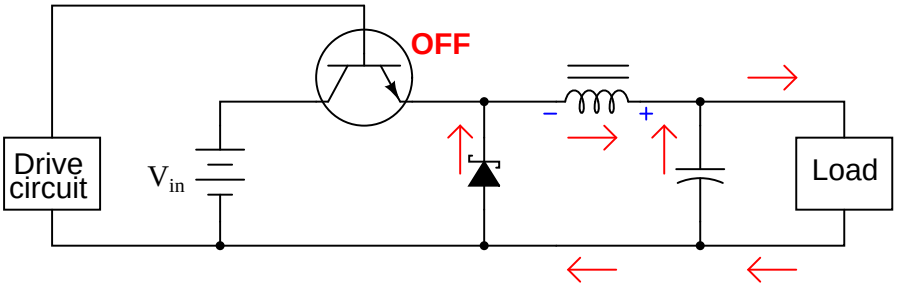
Trace all current directions during both states of the transistor. Also, mark the inductor's voltage polarity during both states of the transistor.

file 01102

Answer 81



Note: all currents shown using conventional flow notation



Follow-up question: how does the load voltage of this converter relate to the supply (battery) voltage? Does the load receive more or less voltage than that provided by the battery?

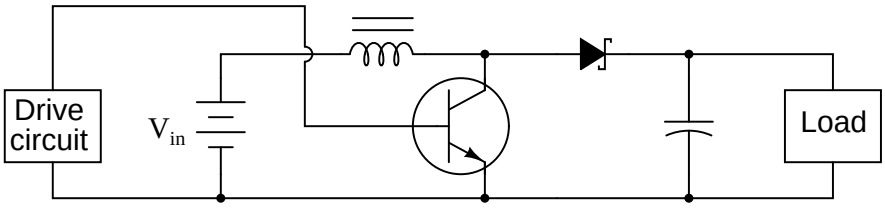
Challenge question: why do you suppose a Schottky diode is used in this circuit, as opposed to a regular (PN) rectifying diode?

Notes 81

Ask your students why they think this circuit is called a *buck* converter. "Buck" usually refers to something that is in opposition. What is being opposed in this circuit?

Question 82

The schematic diagram shown here is for a *"boost" converter circuit*, a type of DC-DC "switching" power conversion circuit:

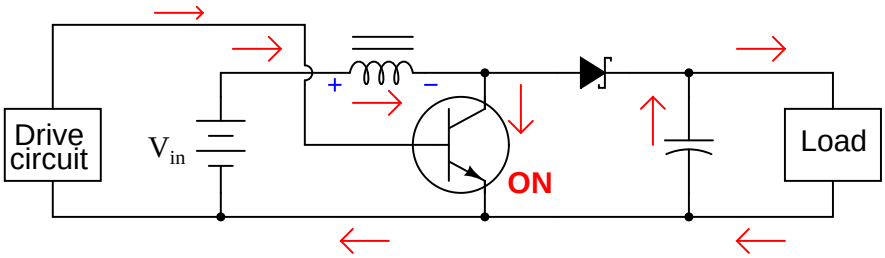


In this circuit, the transistor is either fully on or fully off; that is, driven between the extremes of saturation or cutoff. By avoiding the transistor's "active" mode (where it would drop substantial voltage while conducting current), very low transistor power dissipations can be achieved. With little power wasted in the form of heat, "switching" power conversion circuits are typically very efficient.

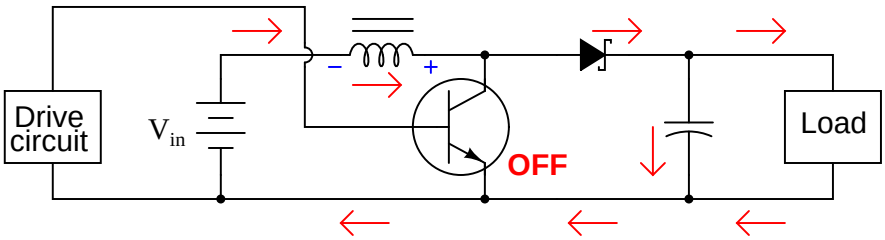
Trace all current directions during both states of the transistor. Also, mark the inductor's voltage polarity during both states of the transistor.

file 01103

Answer 82



Note: all currents shown using conventional flow notation



Follow-up question: how does the load voltage of this converter relate to the supply (battery) voltage? Does the load receive more or less voltage than that provided by the battery?

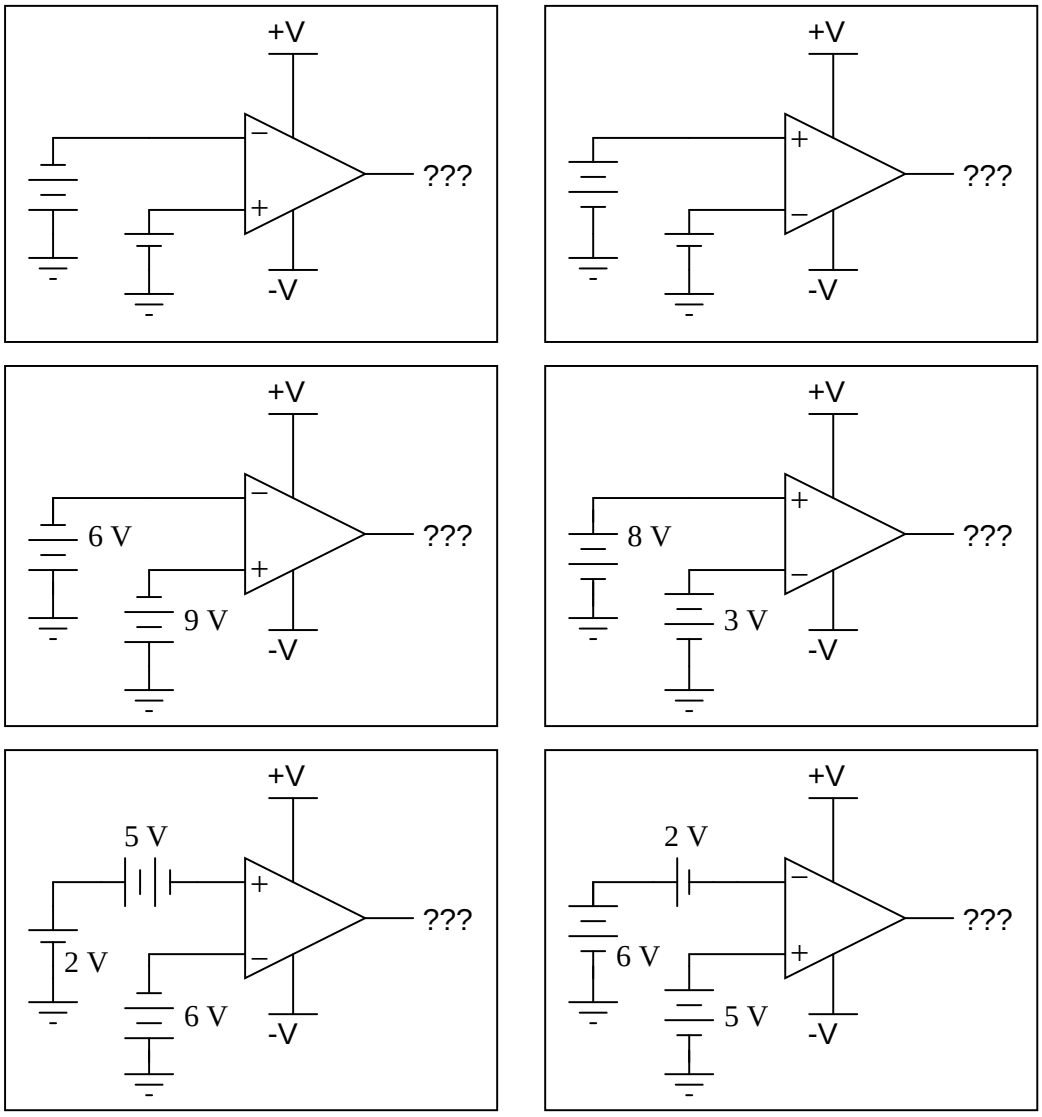
Challenge question: why do you suppose a Schottky diode is used in this circuit, as opposed to a regular (PN) rectifying diode?

Notes 82

Ask your students why they think this circuit is called a *boost* converter. "Boost" usually refers to something that is aiding something else. What is being aided in this circuit?

Question 83

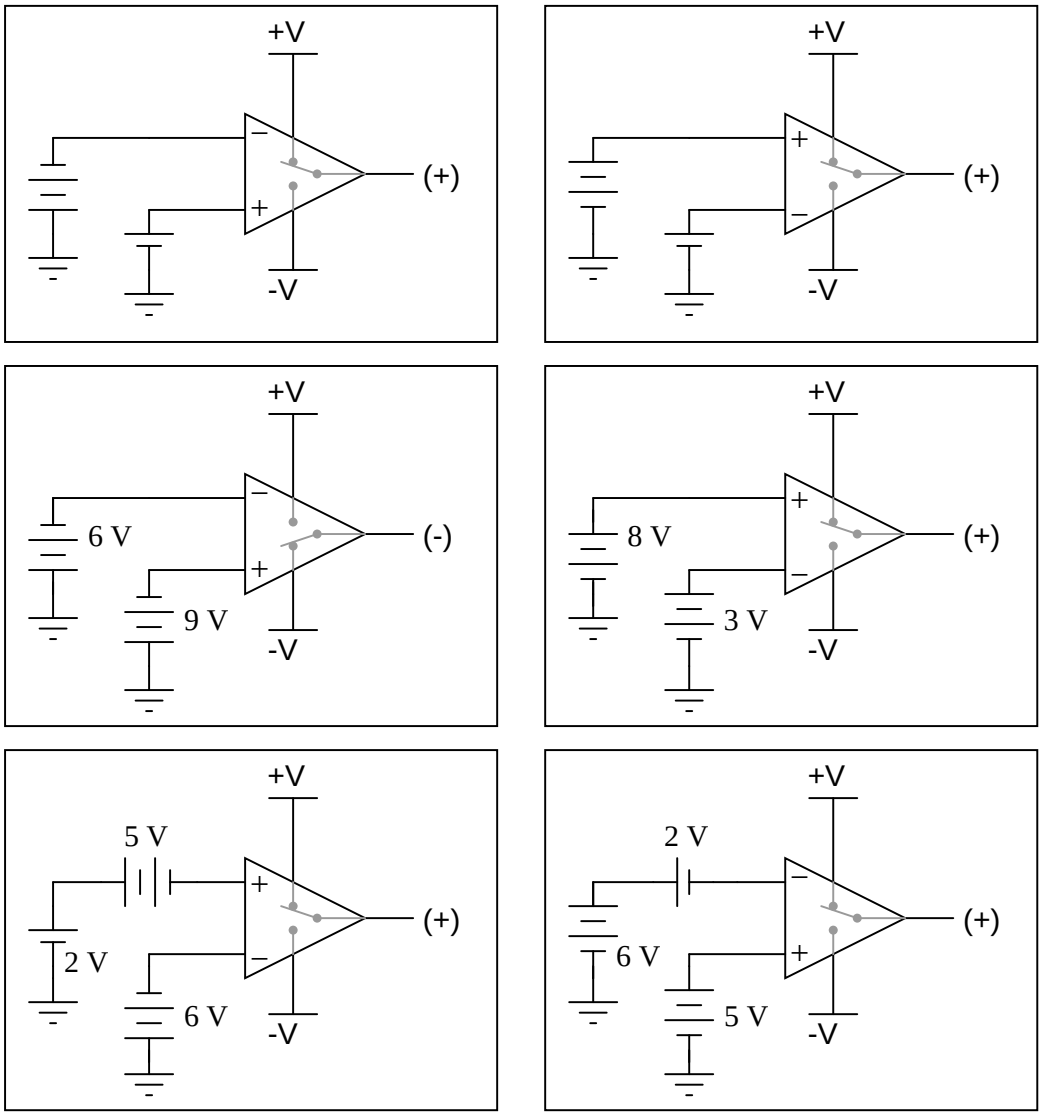
Determine the output voltage polarity of this op-amp (with reference to ground), given the following input conditions:



file 03762

Answer 83

In these illustrations, I have likened the op-amp's action to that of a single-pole, double-throw switch, showing the "connection" made between power supply terminals and the output terminal.

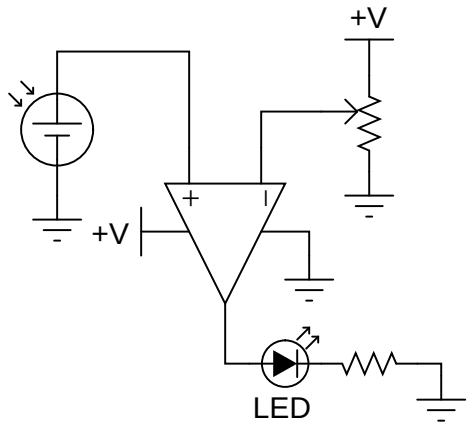


Notes 83

Determining which "way" the output of an op-amp drives under different input voltage conditions is confusing to many students. Discuss this with them, and ask them to present any principles or analogies they use to remember "which way is which."

Question 84

In this circuit, a solar cell converts light into voltage for the opamp to "read" on its noninverting input. The opamp's inverting input connects to the wiper of a potentiometer. Under what conditions does the LED energize?



file 00872

Answer 84

The LED energizes under bright-light conditions, de-energizing when the light decreases below the threshold set by the potentiometer.

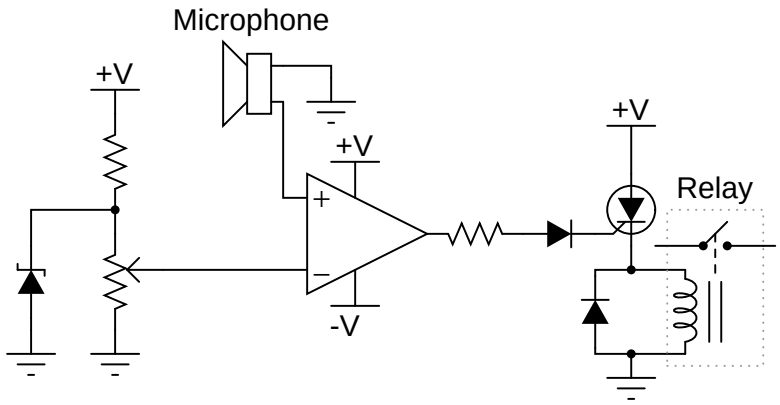
Follow-up question: determine what would have to be changed in this circuit to make the LED turn on when the solar cell becomes *dark*.

Notes 84

There is more than one way to accomplish the task posed by the follow-up question. Be sure to ask your students for their ideas on how to reverse the LED's operation!

Question 85

Explain the operation of this sound-activated relay circuit:



file 00879

Answer 85

The relay will energize if a loud enough sound is detected by the microphone. The threshold volume is set by the potentiometer.

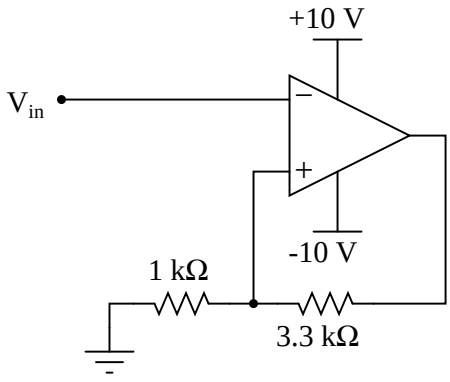
Follow-up question: how could we equip this circuit with the ability to turn the relay off once it has been turned on?

Notes 85

There is a lot going on in this circuit that is not addressed in the answer I give. The basic purpose of the circuit should be fairly clear to understand, but the function of several components deserve further explanation. Ask your students to explain the functions of the diode on the comparator's output, the diode in parallel with the relay coil, the zener diode in parallel with the potentiometer, and the SCR.

Question 86

Assume that the comparator in this circuit is only capable of "swinging" its output to within 1 volt of its power supply rail voltages. Calculate the upper and lower threshold voltages, given the resistor values shown:



V_{UT} = V_{LT} =

file 02662

Answer 86

V_{UT} = +2.093 volts

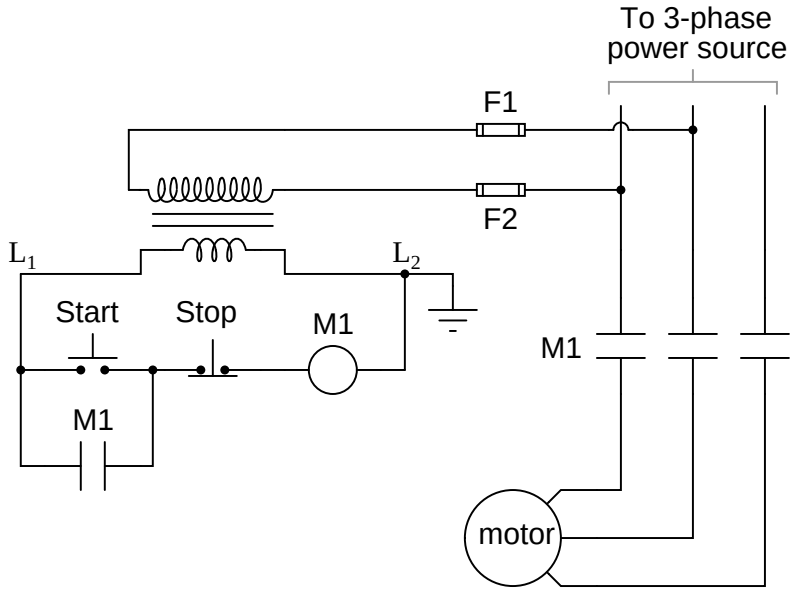
V_{LT} = -2.093 volts

Notes 86

As many opamps and comparators are incapable of rail-to-rail output swings, this question is quite realistic.

Question 87

A very common form of *latch* circuit is the simple "start-stop" relay circuit used for motor controls, whereby a pair of momentary-contact pushbutton switches control the operation of an electric motor. In this particular case, I show a low-voltage control circuit and a 3-phase, higher voltage motor:



Explain the operation of this circuit, from the time the "Start" switch is actuated to the time the "Stop" switch is actuated. The normally-open M1 contact shown in the low-voltage control circuit is commonly called a *seal-in contact*. Explain what this contact does, and why it might be called a "seal-in" contact.

file 01347

Answer 87

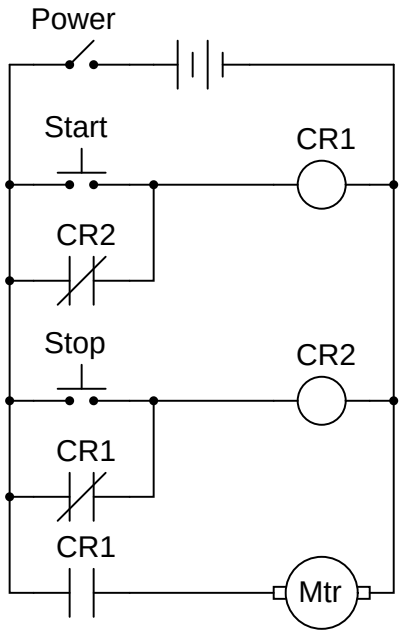
Even though the "Start" and "Stop" switches are momentary, the "seal-in" contact makes the circuit *latch* in one of two states: either motor energized or motor de-energized.

Notes 87

Motor "start-stop" circuits are very common in industry, and apply to applications beyond electric motors. Ask your students if they can think of any application for a circuit such as this.

Question 88

A student decides to build a motor start/stop control circuit based on the logic of a NOR gate S-R latch, rather than the usual simple "seal-in" contact circuit:



The circuit works fine, except that sometimes the motor starts all by itself when the circuit is first powered up! Other times, the motor remains off after power-up. In other words, the power-up state of this circuit is unpredictable.

Explain why this is so, and what might be done to prevent the motor from powering up in the "run" state.

file 01379

Answer 88

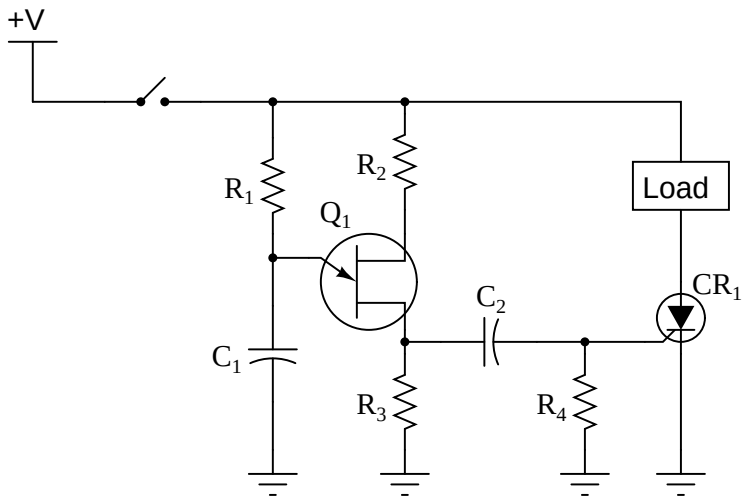
What you have here is something called a *race condition*, where two or more relays "race" each other to attain mutually exclusive states. This is a difficult problem to fix, but the solution (and yes, there is more than one valid solution!) invariably involves "rigging" the race so that one of the relays is guaranteed to "win."

Notes 88

Analyze the power-up states of this circuit with your students, and the "race" condition will become apparent. Such problems can be very difficult to locate and fix in real life, so it is good to expose students to them early in their education, and in contexts where the circuitry is not too confusing.

Question 89

The following schematic diagram shows a timer circuit made from a UJT and an SCR:



Together, the combination of R_1, C_1, R_2, R_3, and Q_1 form a *relaxation oscillator*, which outputs a square wave signal. Explain how a square wave oscillation is able to perform a simple time-delay for the load, where the load energizes a certain time *after* the toggle switch is closed. Also explain the purpose of the RC network formed by C_2 and R_4.

file 03222

Answer 89

Remember that CR_1 only needs one pulse at its gate to turn (and latch) it on! C_2 and R_4 form a *passive differentiator* to condition the square wave signal from the UJT oscillator.

Follow-up question: how would you suggest we modify this circuit to make the time delay adjustable?

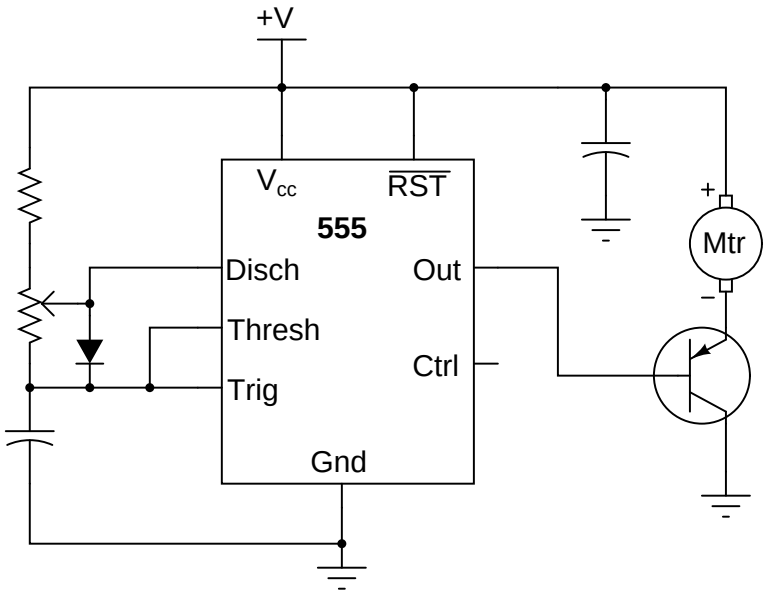
Notes 89

Knowing that the UJT forms an oscillator, it is tempting to think that the load will turn on and off repeatedly. The first sentence in the answer explains why this will not happen, though.

I got the basic idea for this circuit from the second edition of Electronics for Industrial Electricians, by Stephen L. Herman.

Question 90

Pulse Width Modulation, or *PWM*, is a very popular means of controlling power to an electrical load such as a light bulb or a DC motor. With PWM control, the duty cycle of a high-frequency digital (on/off) signal is varied, with the effect of varying power dissipation at the load:



One of the major advantages to using PWM to proportion power to a load is that the final switching transistor operates with minimal heat dissipation. If we were to use a transistor in its linear ("active") mode, it would dissipate far more heat when controlling the speed of this motor! By dissipating less heat, the circuit wastes less power.

Explain why the power transistor in this circuit runs cooler when buffering the PWM signal from the 555 timer, rather than if it were operated in linear mode. Also, identify which direction the potentiometer wiper must be moved to increase the speed of the motor.

Challenge question: suppose we needed to control the power of a DC motor, when the motor's operating voltage was far in excess of the 555 timer's operating voltage. Obviously, we need a separate power supply for the motor, but how would we safely interface the 555's output with the power transistor to control the motor speed? Draw a schematic diagram to accompany your answer.

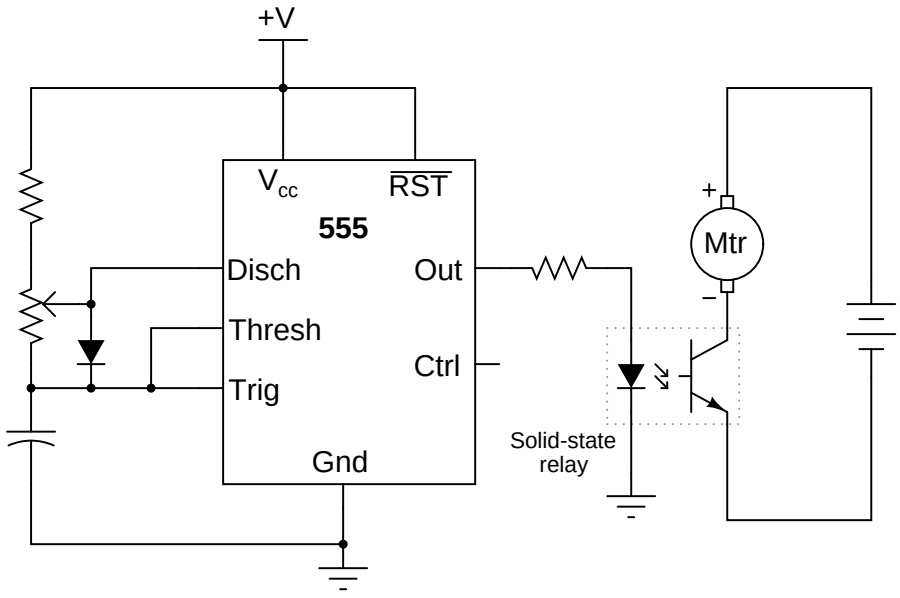
file 01436

Answer 90

I'll let you research the answer to why PWM is a more energy-efficient way to control load power. This is a very important concept in power electronics!

To increase the speed of the motor, move the potentiometer wiper *up* (as pictured in the schematic).

Here is one possible solution to the problem of interfacing a 555 timer to a high-voltage DC motor:



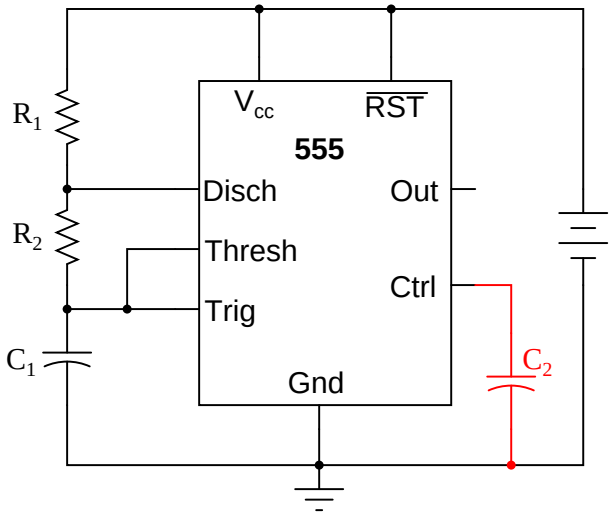
Notes 90

There is much literature available discussing PWM power control, and its advantages over linear power control. Your students should have no difficulty finding it on their own!

Discuss with them the proposed solution to the high-voltage motor problem. What purpose(s) do/does the solid-state relay serve? Is there a way to achieve PWM control over the motor without using an optocoupled device? If so, how? Let your students show their solutions and discuss the practicality of each.

Question 91

It is common to see a capacitor connected between the "Control" terminal and ground in 555 timer circuits, especially when precise timing is important.



Explain what purpose the capacitor C_2 serves in this circuit.
file 01434

Answer 91

C_2 acts as a decoupling capacitor, to help stabilize the threshold and trigger reference voltages internal to the 555.

Challenge question: what operational parameters of the circuit define the necessary capacitance value of C_2?

Notes 91

Decoupling power supply pins on a chip is important, but here students get to see another variation of decoupling. If time permits, work through a sample problem with your students sizing capacitor C_2, given a certain operating frequency of the astable circuit. Note: this will give you another opportunity to use Thévenin's Theorem . . .

Question 92

Special integrated circuits called *delay elements* or *delay gates* are manufactured to provide nanoseconds' worth of intentional time delays in digital circuits. Identify a part number for such an IC, research its datasheet, and describe an application where one might be needed.

file 02945

Answer 92

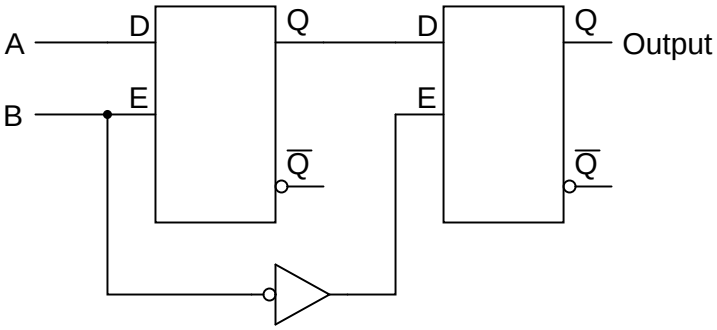
One part number for you to research is 74LS31. Such delay elements might be used to provide ample set-up and/or hold times for signals entering flip-flop.

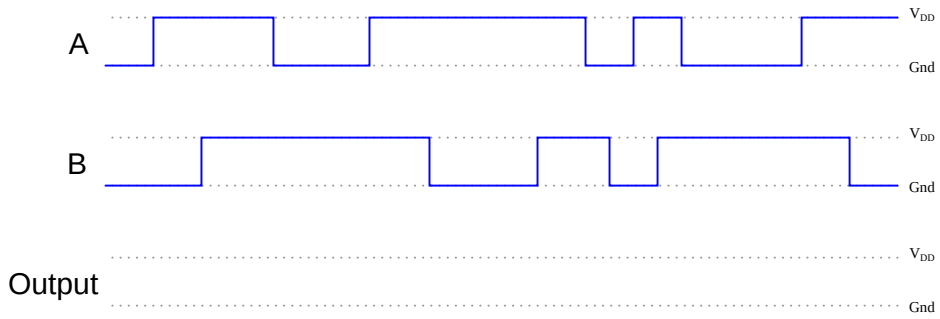
Notes 92

Discuss with your students why such devices exist, in light of the existence of 555 timers. Why couldn't a 555 timer be used for the same purpose as the 74LS31?

Question 93

Determine the final output states over time for the following circuit, built from D-type gated latches:

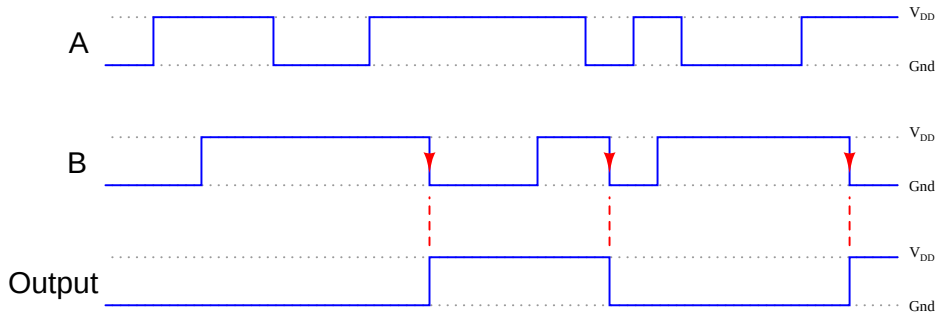




At what specific times in the pulse diagram does the final output assume the input's state? How does this behavior differ from the normal response of a D-type latch?

file 01363

Answer 93



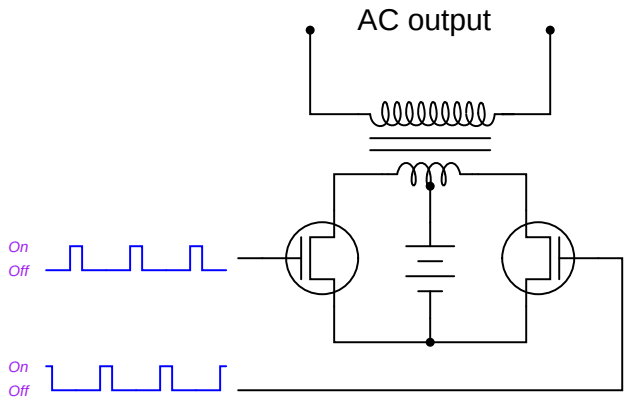
The final output assumes the same logic state as the input only when the enable input signal (B) *transitions* from "high" to "low".

Notes 93

Note that by adding another latch, the overall behavior only slightly resembles the behavior of a D-type latch. With the addition of the second latch, we've changed this circuit into a *flip-flop*, specifically of the *master-slave* variety.

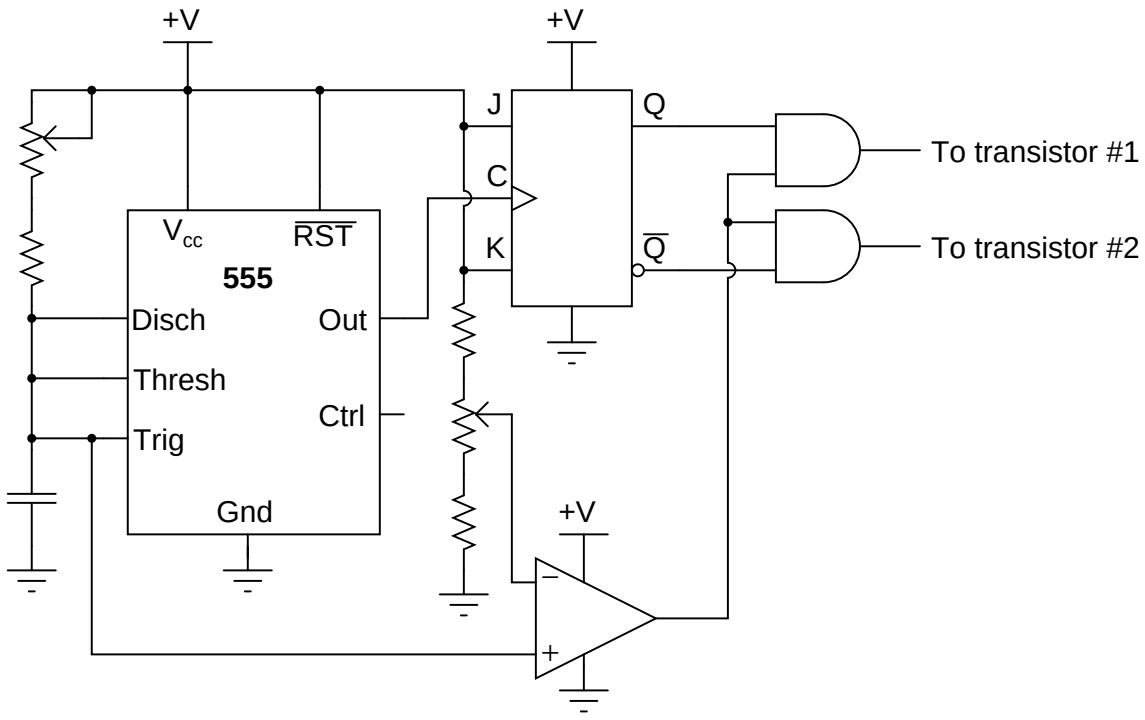
Question 94

A common topology for DC-AC power converter circuits uses a pair of transistors to switch DC current through the center-tapped winding of a step-up transformer, like this:



Note: protective devices to guard against transient overvoltages have been omitted from this diagram for simplicity!

In order for this form of circuit to function properly, the transistor "firing" signals must be precisely synchronized to ensure the two are never turned on simultaneously. The following schematic diagram shows a circuit to generate the necessary signals:

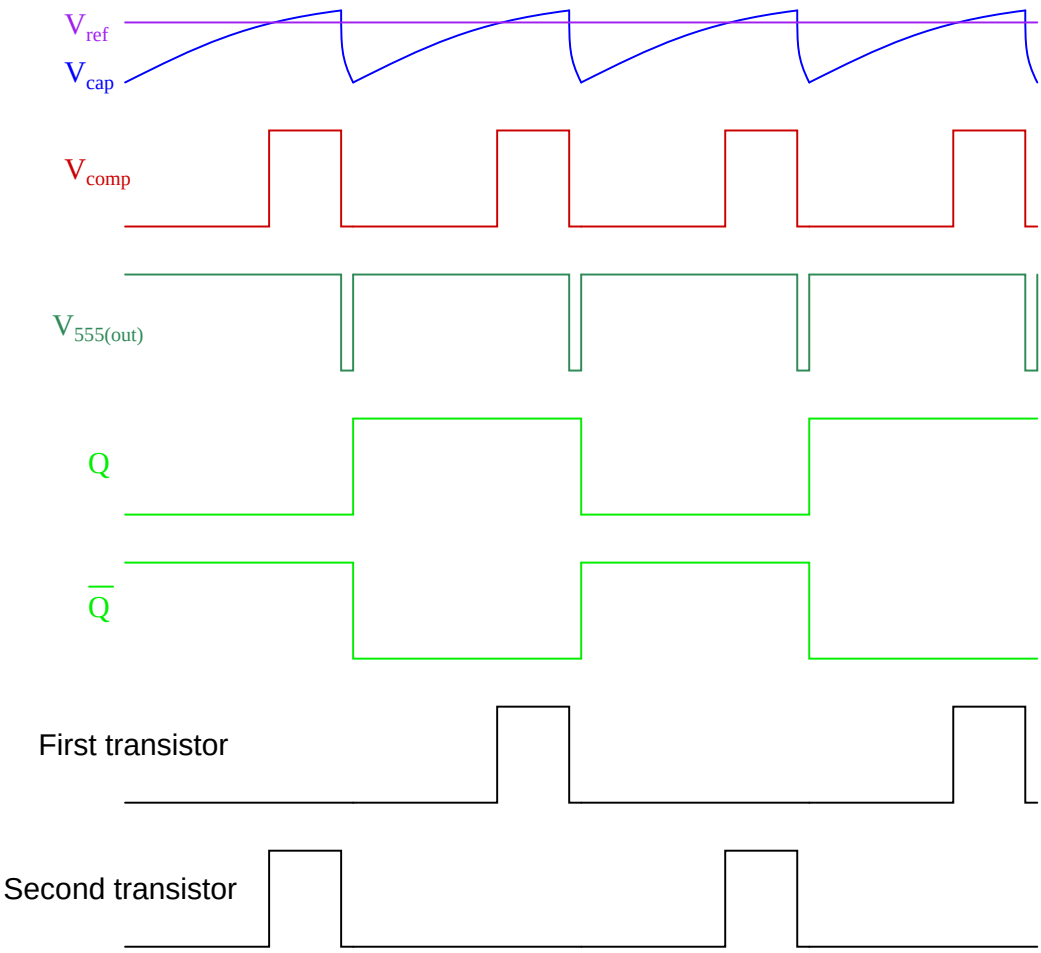


Explain how this circuit works, and identify the locations of the frequency control and pulse duty-cycle control potentiometers.

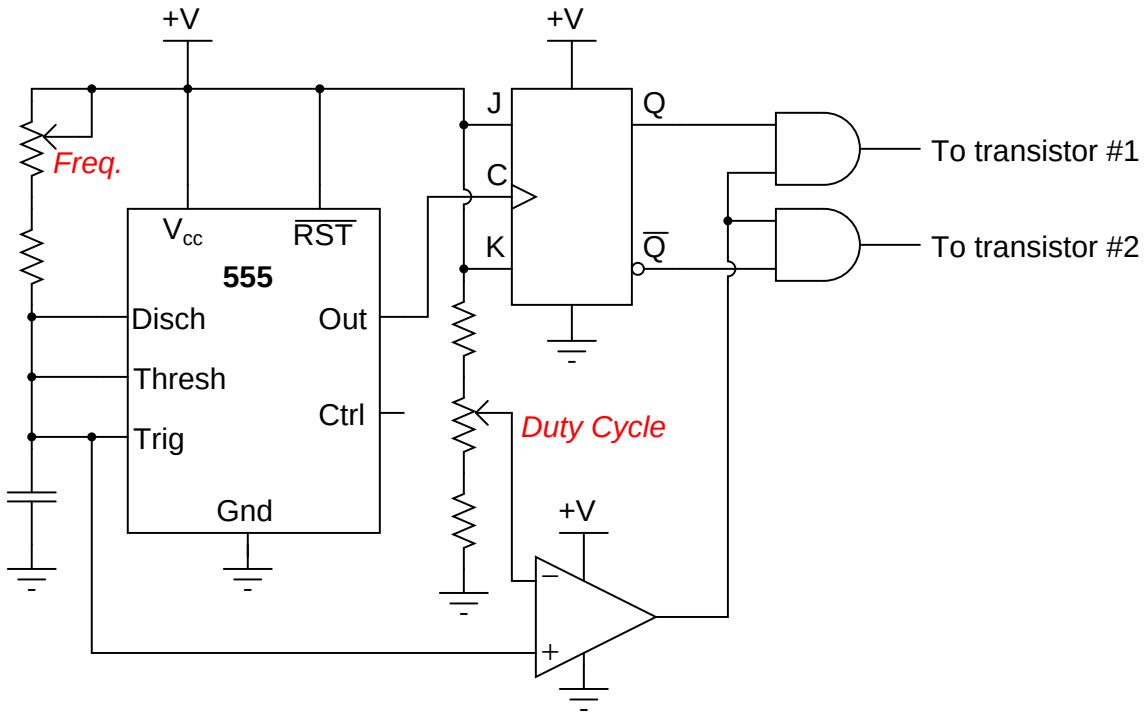
file 03452

Answer 94

A timing diagram is worth a thousand words:



- V_{ref} = DC reference voltage set by duty cycle potentiometer
- V_{cap} = Voltage measured at top terminal of the 555's capacitor
- V_{comp} = Comparator output voltage
- $V_{555(out)}$ = 555 timer output voltage
- Q = Noninverted output of J-K flip-flop
- $\overline{Q}$ = Inverted output of J-K flip-flop



Follow-up question: which direction would you have to move the frequency potentiometer to increase the output frequency of this circuit? Which direction would you have to move the duty cycle potentiometer to increase that as well?

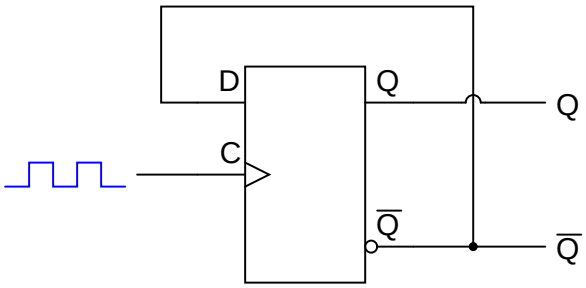
Challenge question: suppose you were prototyping this circuit without the benefit of an oscilloscope. How could you test the circuit to ensure the final output pulses to the transistors are never simultaneously in the "high" logic state? Assume you had a parts assortment complete with light-emitting diodes and other passive components.

Notes 94

This question is an exercise in schematic diagram and timing diagram interpretation. By the way, I have built and tested this circuit and I can say it works very well.

Question 95

Although the *toggle* function of the J-K flip-flop is one of its most popular uses, this is not the only type of flip-flop capable of performing a toggle function. Behold the surprisingly versatile D-type flip-flop configured to do the same thing:



Explain how this circuit performs the "toggle" function more commonly associated with J-K flip-flops.
file 03453

Answer 95

At each clock pulse, the flip-flop must switch to the opposite state because D receives inverted feedback from $\overline{Q}$.

Notes 95

The main purpose of this question is to get students to see that toggling is not the exclusive domain of J-K flip-flops. This fact may be particularly handy to know if one needs a toggle function in a circuit but only has a D-type flip-flop available, not a J-K flip-flop.