ELTR 145 (Digital 2), section 2

Recommended schedule

Day 1

Topics: *Counter circuits*
Questions: *1 through 10*
Lab Exercise: *2-bit counter from flip-flops (question 56)*

Day 2

Topics: *Counter circuits (continued)*
Questions: *11 through 20*
Lab Exercise: *4-bit up/down counter IC (question 57)*

Day 3

Topics: *Shift registers*
Questions: *21 through 30*
Lab Exercise: *Troubleshooting practice (decade counter circuit – question 60)*

Day 4

Topics: *Shift registers and serial data communication*
Questions: *31 through 40*
Lab Exercise: *Frequency divider circuit (question 58)*

Day 5

Topics: *Memory technologies*
Questions: *41 through 55*
Lab Exercise: *4-bit universal shift register IC (question 59)*

Day 6

Exam 2: *includes Counter circuit performance assessment*
Lab Exercise: *Troubleshooting practice (decade counter circuit – question 60)*

Troubleshooting practice problems

Questions: *63 through 72*

DC/AC/Semiconductor/Opamp review problems

Questions: *73 through 92*

General concept practice and challenge problems

Questions: *93 through the end of the worksheet*

Impending deadlines

Troubleshooting assessment (counter circuit) due at end of ELTR145, Section 3
Question 61: Troubleshooting log
Question 62: Sample troubleshooting assessment grading criteria

ELTR 145 (Digital 2), section 2

Skill standards addressed by this course section

EIA *Raising the Standard; Electronics Technician Skills for Today and Tomorrow*, June 1994

F Technical Skills – Digital Circuits

F.14 Understand principles and operations of types of registers and counters.
F.15 Fabricate and demonstrate types of registers and counters.
F.16 Troubleshoot and repair types of registers and counters.

B Basic and Practical Skills – Communicating on the Job

B.01 Use effective written and other communication skills. *Met by group discussion and completion of labwork.*
B.03 Employ appropriate skills for gathering and retaining information. *Met by research and preparation prior to group discussion.*
B.04 Interpret written, graphic, and oral instructions. *Met by completion of labwork.*
B.06 Use language appropriate to the situation. *Met by group discussion and in explaining completed labwork.*
B.07 Participate in meetings in a positive and constructive manner. *Met by group discussion.*
B.08 Use job-related terminology. *Met by group discussion and in explaining completed labwork.*
B.10 Document work projects, procedures, tests, and equipment failures. *Met by project construction and/or troubleshooting assessments.*

C Basic and Practical Skills – Solving Problems and Critical Thinking

C.01 Identify the problem. *Met by research and preparation prior to group discussion.*
C.03 Identify available solutions and their impact including evaluating credibility of information, and locating information. *Met by research and preparation prior to group discussion.*
C.07 Organize personal workloads. *Met by daily labwork, preparatory research, and project management.*
C.08 Participate in brainstorming sessions to generate new ideas and solve problems. *Met by group discussion.*

D Basic and Practical Skills – Reading

D.01 Read and apply various sources of technical information (e.g. manufacturer literature, codes, and regulations). *Met by research and preparation prior to group discussion.*

E Basic and Practical Skills – Proficiency in Mathematics

E.01 Determine if a solution is reasonable.
E.02 Demonstrate ability to use a simple electronic calculator.
E.06 Translate written and/or verbal statements into mathematical expressions.
E.07 Compare, compute, and solve problems involving binary, octal, decimal, and hexadecimal numbering systems.
E.12 Interpret and use tables, charts, maps, and/or graphs.
E.13 Identify patterns, note trends, and/or draw conclusions from tables, charts, maps, and/or graphs.
E.15 Simplify and solve algebraic expressions and formulas.
E.16 Select and use formulas appropriately.

Common areas of confusion for students

Common mistake: *How set-up time for flip-flops influences stage-to-stage propagation.*

When many students first examine cascaded, synchronous flip-flop circuits (where the Q output of one enters the input of the next), they wonder why pulses don't just ripple through the whole chain of flip-flops with one clock pulse. The reason this does not happen is that each flip-flop has a finite amount of *set-up time* required for the input state to be stable before it is recognized at the active edge of a new clock pulse. Even with instantaneous flip-flop output state changes, the cascaded signal still cannot reach the input of the next flip-flop *before* the clock pulse arrives at that next flip-flop. Therefore, the fastest a logic state can progress from one flip-flop to another in a synchronous counter circuit is one flip-flop per clock pulse.

Questions

Question 1

Count from zero to fifteen, in binary, keeping the bits lined up in vertical columns like this:

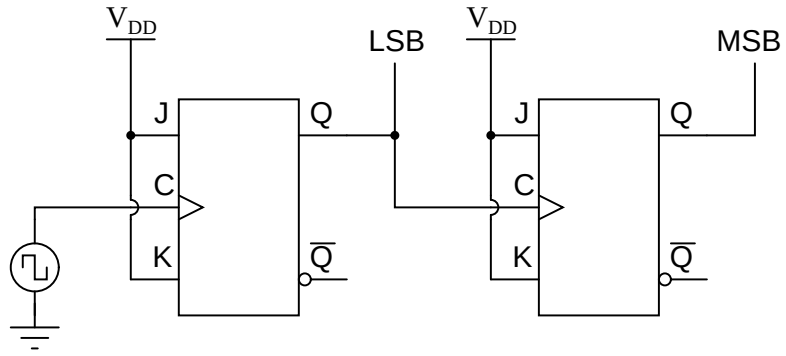
```
0000
0001
0010
. . .
```

Now, reading from top to bottom, notice the alternating patterns of 0's and 1's in each place (i.e. one's place, two's place, four's place, eight's place) of the four-bit binary numbers. Note how the least significant bit alternates more rapidly than the most significant bit. Draw a timing diagram showing the respective bits as waveforms, alternating between "low" and "high" states, and comment on the *frequency* of each of the bits.

file 01373

Question 2

Shown here is a simple two-bit binary counter circuit:



The Q output of the first flip-flop constitutes the least significant bit (LSB), while the second flip-flop's Q output constitutes the most significant bit (MSB).

Based on a timing diagram analysis of this circuit, determine whether it counts in an *up* sequence (00, 01, 10, 11) or a *down* sequence (00, 11, 10, 01). Then, determine what would have to be altered to make it count in the other direction.

file 01374

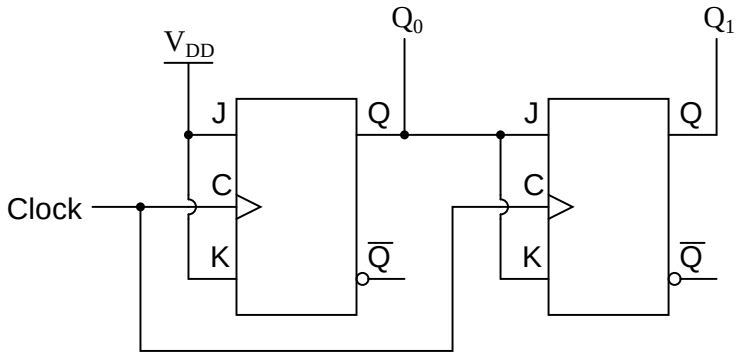
Question 3

Counter circuits built by cascading the output of one flip-flop to the clock input of the next flip-flop are generally referred to as *ripple* counters. Explain why this is so. What happens in such a circuit that earns it the label of "ripple"? Is this effect potentially troublesome in circuit operation, or is it something of little or no consequence?

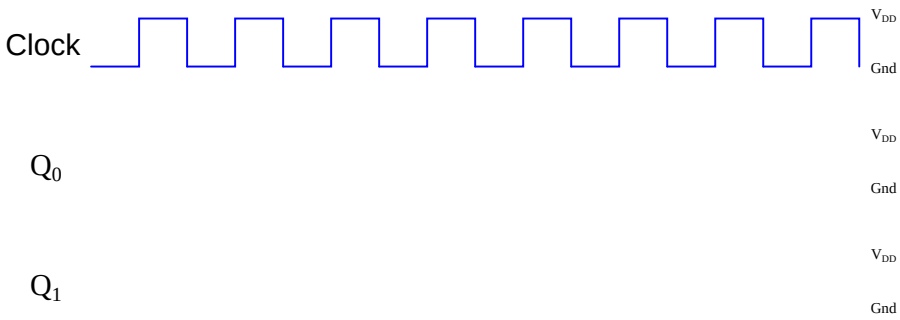
file 01388

Question 4

A style of counter circuit that completely circumvents the "ripple" effect is called the *synchronous* counter:



Complete a timing diagram for this circuit, and explain why this design of counter does not exhibit "ripple" on its output lines:

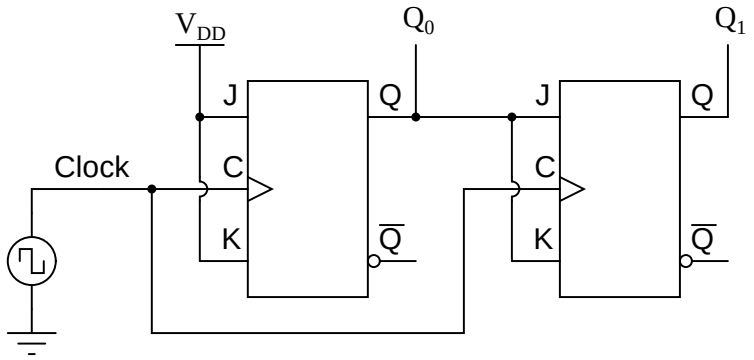


Challenge question: to *really* understand this type of counter circuit well, include propagation delays in your timing diagram.

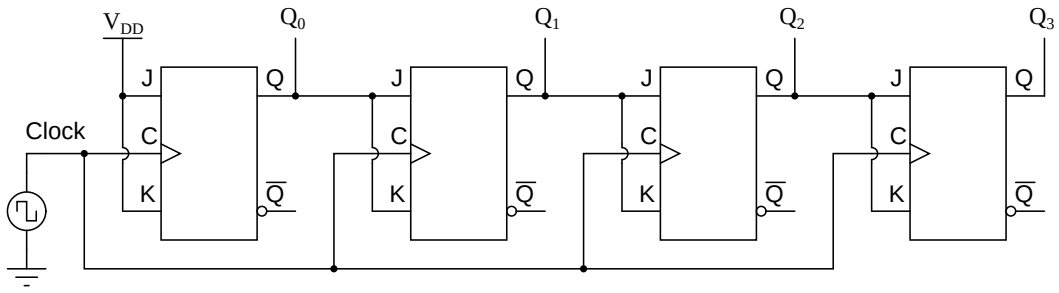
file 01396

Question 5

A student just learned how a two-bit synchronous binary counter works, and he is excited about building his own. He does so, and the circuit works perfectly.



After that success, student tries to expand on their success by adding more flip-flops, following the same pattern as the two original flip-flops:

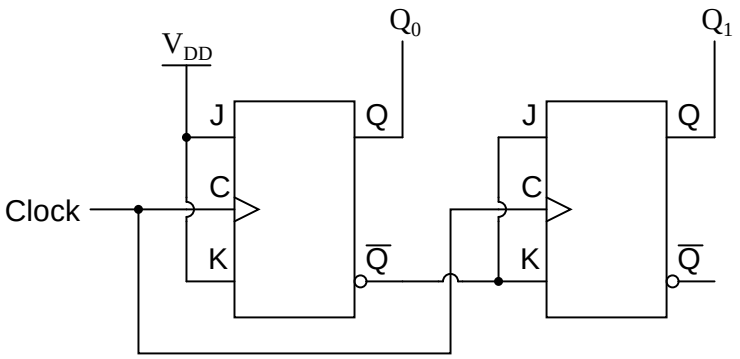


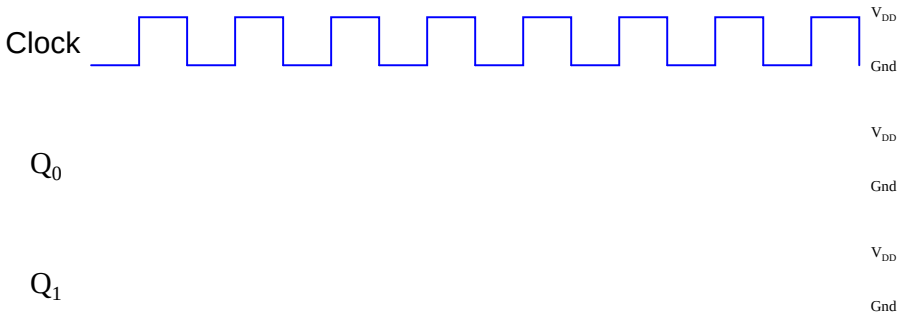
Unfortunately, this circuit didn't work. The sequence it generates is not a binary count. Determine what the counting sequence of this circuit is, and then try to figure out what modifications would be required to make it count in a proper binary sequence.

file 01397

Question 6

Complete a timing diagram for this synchronous counter circuit, and identify the direction of its binary count:

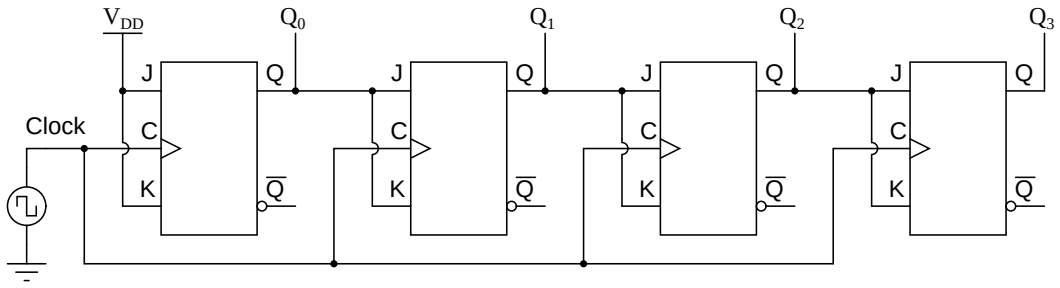




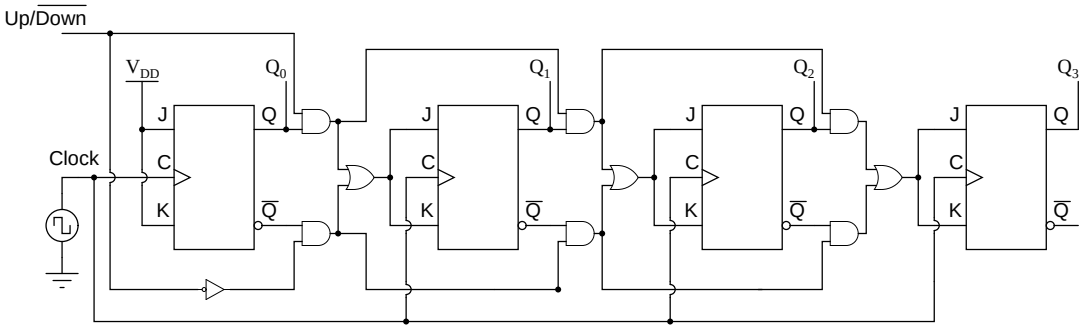
file 01398

Question 7

Synchronous counter circuits tend to confuse students. The circuit shown here is the design that most students think ought to work, but actually doesn't:



Shown here is an up/down synchronous counter design that *does* work:

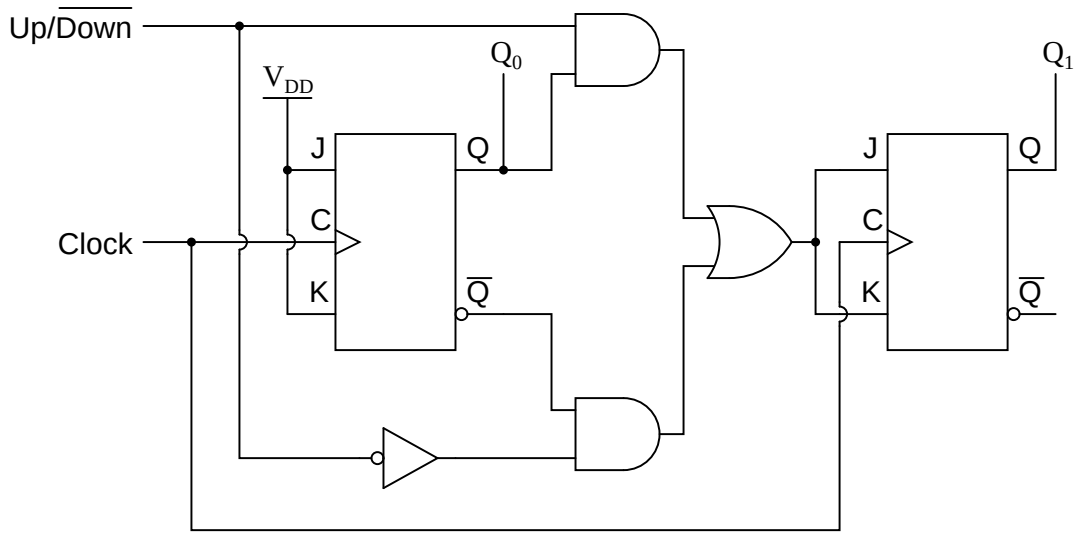


Explain why this circuit is able to function properly (counting in either direction), while the first circuit is not able to count properly at all. What do those "extra" gates do to make the counter circuit function as it should. Hint: to more easily compare the up/down counter to the faulty up counter initially shown, connect the Up/$\overline{\text{Down}}$ control line high, and then disregard any lines and gates that become disabled as a result.

file 01400

Question 8

The following circuit is a two-bit synchronous binary up/down counter:

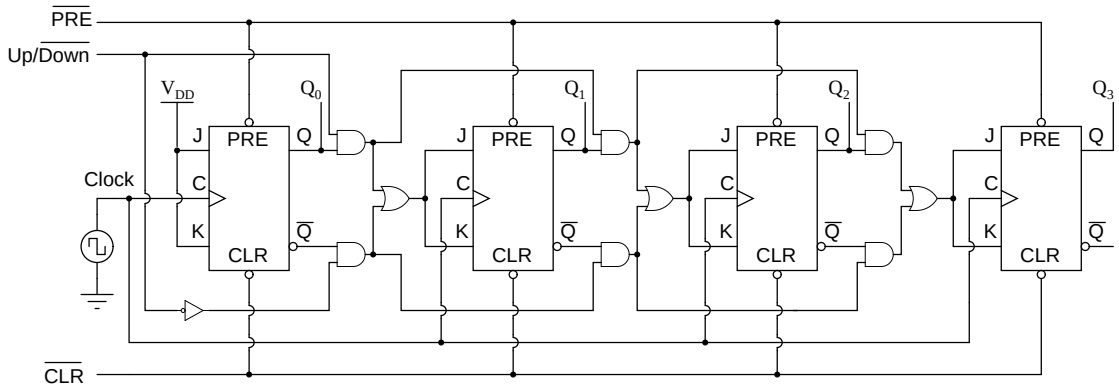


Explain what would happen if the upper AND gate's output were to become "stuck" in the high state regardless of its input conditions. What effect would this kind of failure have on the counter's operation?

file 01399

Question 9

Supposed we used J-K flip-flops with asynchronous inputs (Preset and Clear) to build a counter:

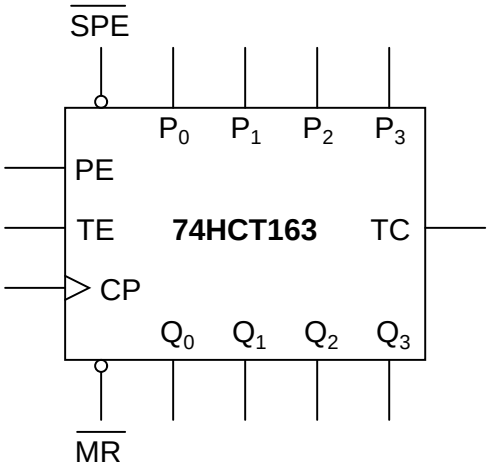


With the asynchronous lines paralleled as such, what are we able to make the counter do now that we weren't before we had asynchronous inputs available to us?

file 01401

Question 10

The part number 74HCT163 integrated circuit is a high-speed CMOS, four-bit, synchronous binary counter. It is a pre-packaged unit, will all the necessary flip-flops and selection logic enclosed to make your design work easier than if you had to build a counter circuit from individual flip-flops. Its block diagram looks something like this (power supply terminals omitted, for simplicity):

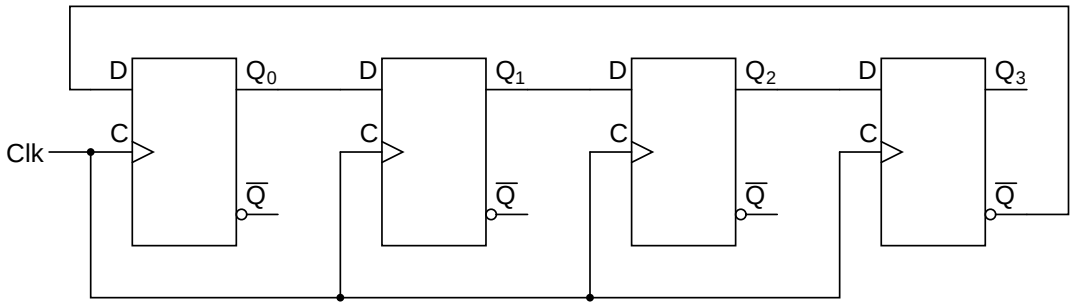


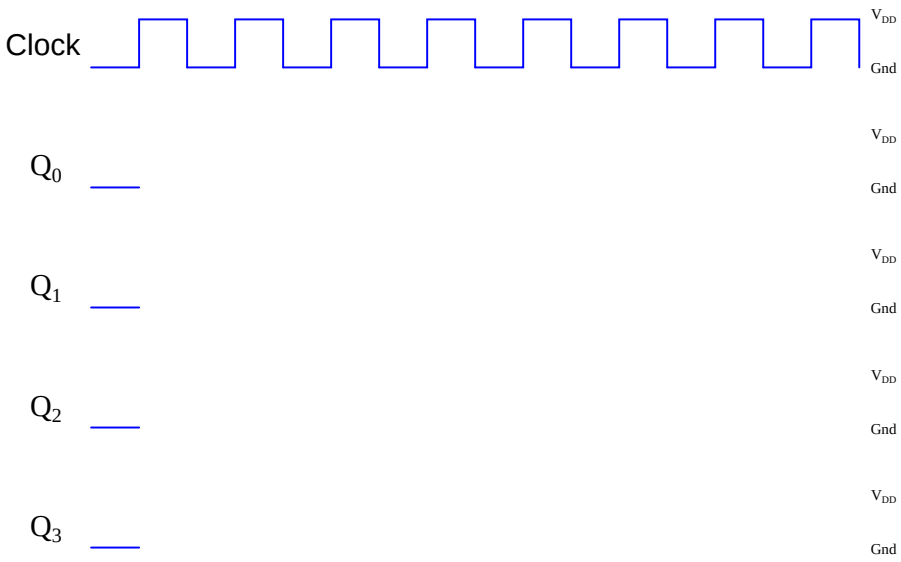
Research the function of this integrated circuit, from manufacturers' datasheets, and explain the function of each input and output terminal.

file 01403

Question 11

Determine the output pulses for this counter circuit, known as a *Johnson counter*, assuming that all Q outputs begin in the low state:

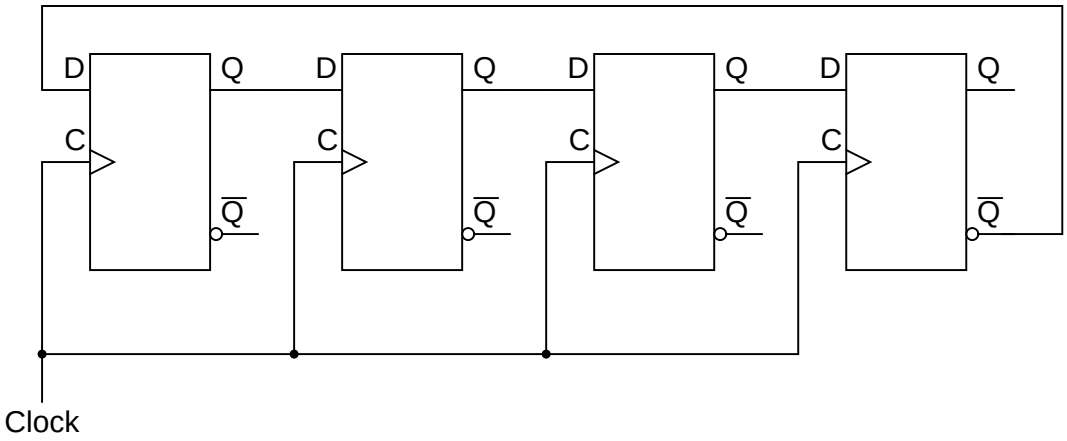




file 01427

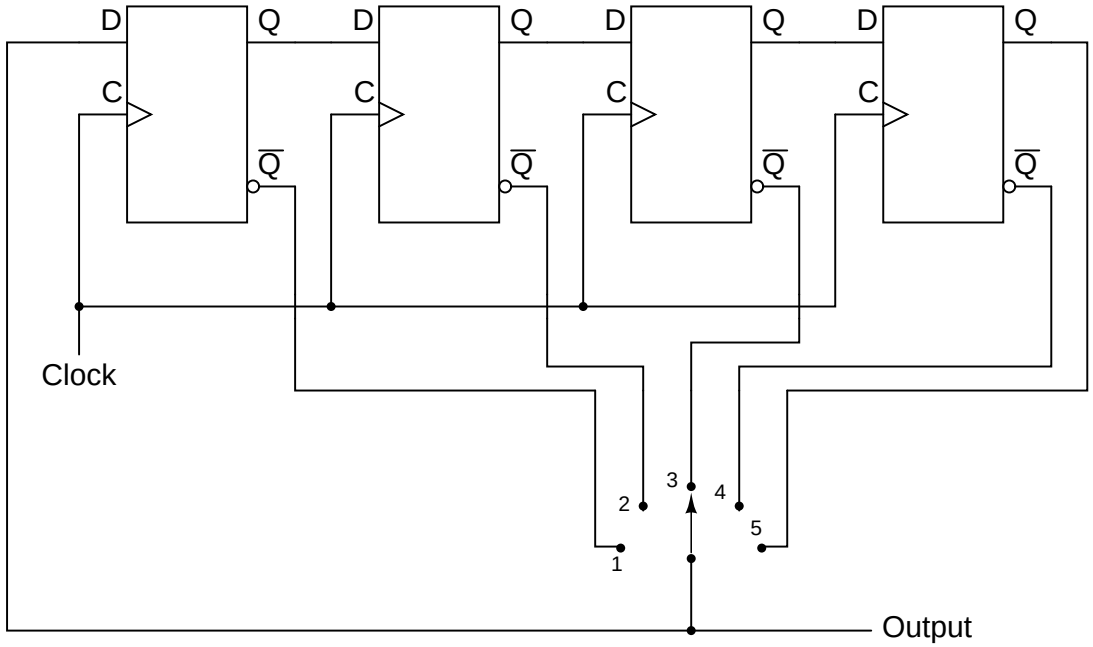
Question 12

The following circuit is known as a *Johnson counter*:



Describe the output of this circuit, as measured from the Q output of the far right flip-flop, assuming that all flip-flops power up in the reset condition.

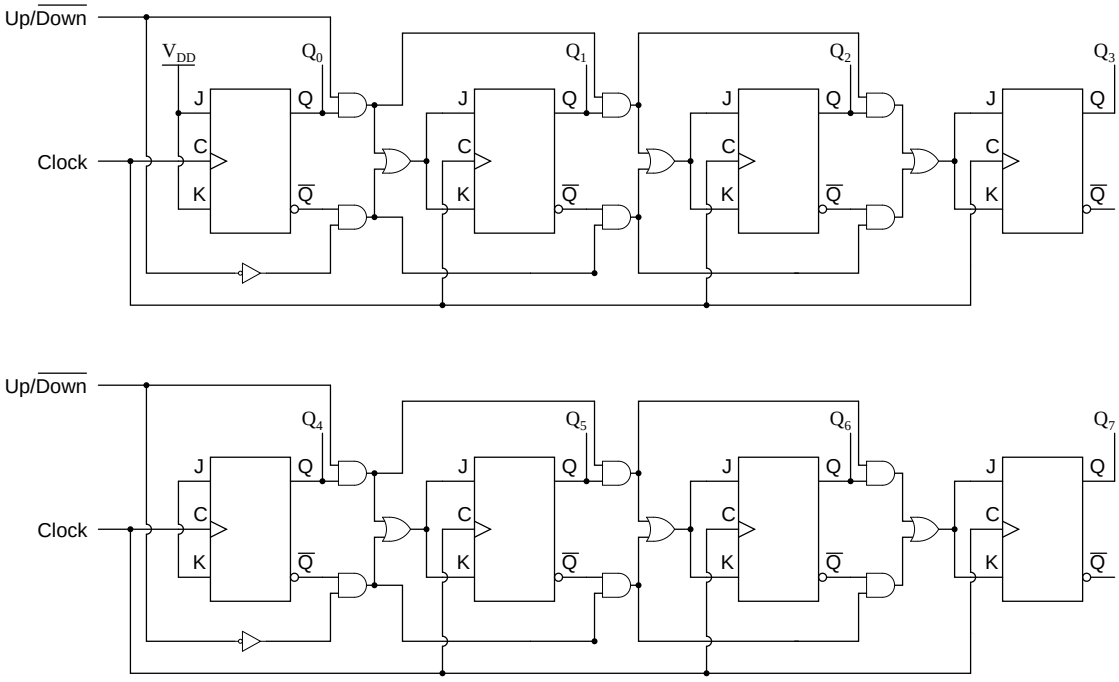
Also, explain what this modified version of the above Johnson counter circuit will do, in each of the five selector switch positions:



file 01475

Question 13

Suppose we had two four-bit synchronous up/down counter circuits, which we wished to *cascade* to make one eight-bit counter. Draw the necessary connecting wires (and any extra gates) between the two four-bit counters to make this possible:

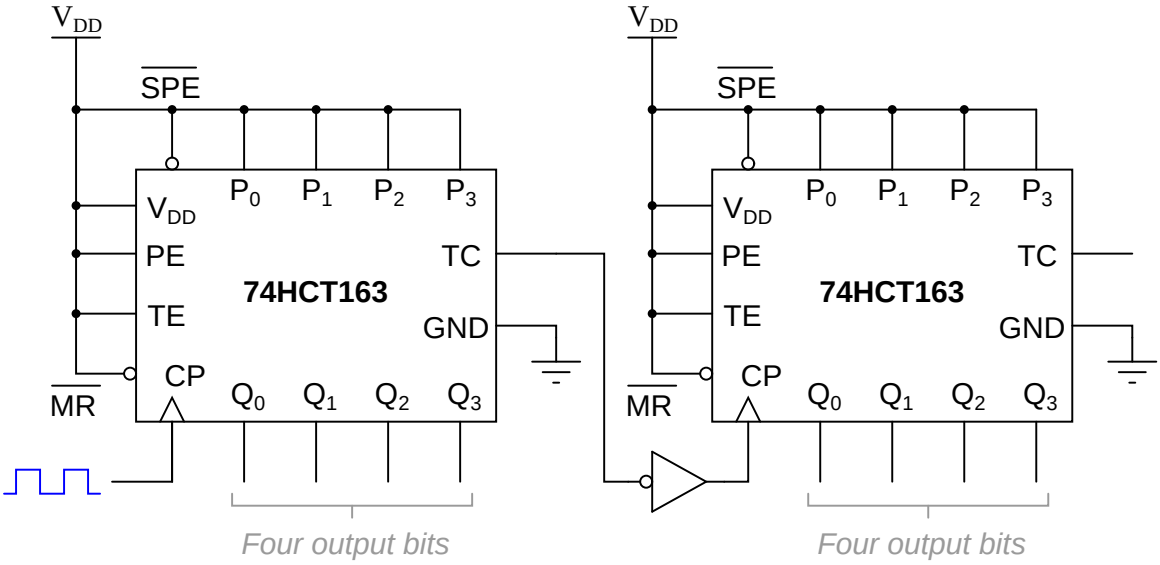


After deciding how to cascade these counters, imagine that you are in charge of building and packaging four-bit counter circuits. The customers who buy your counters might wish to cascade them as you did here, but they won't have the ability to "go inside" the packaging as you did to connect to any of the lines between the various flip-flops. This means you will have to provide any necessary cascading lines as inputs and outputs on your pre-packaged counters. Think carefully about how you would choose to build and package your four-bit "cascadable" counters, and then draw a schematic diagram.

file 01402

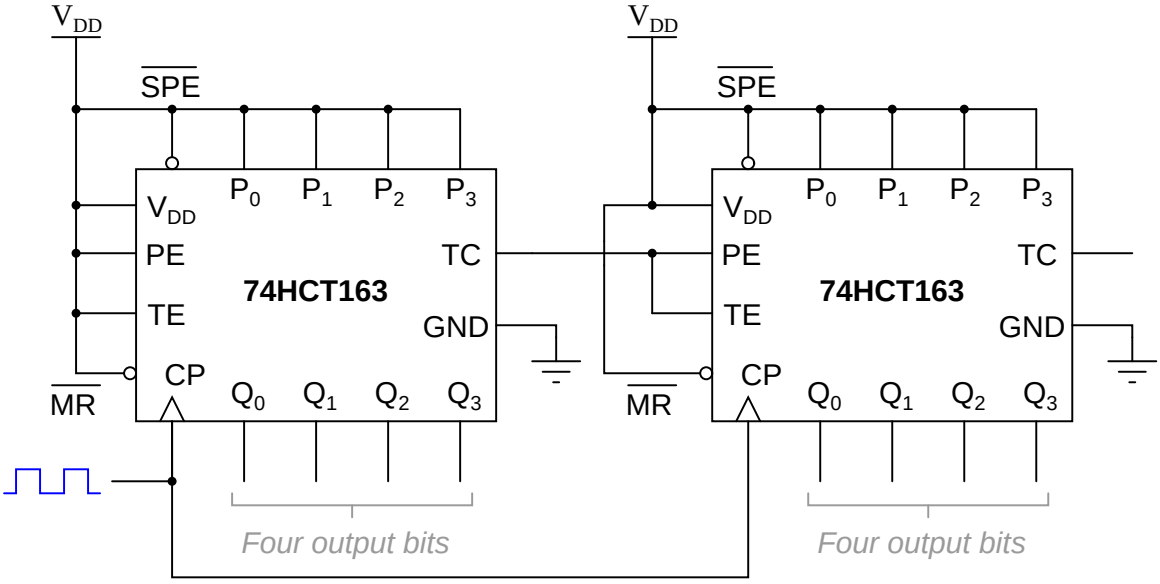
Question 14

Here is an eight-bit counter comprised of two four-bit 74HCT163 synchronous binary counters cascaded together:



Explain how this counter circuit works, and also determine which output bit is the LSB and which is the MSB.

Now, examine this eight-bit counter comprised of the same two ICs:

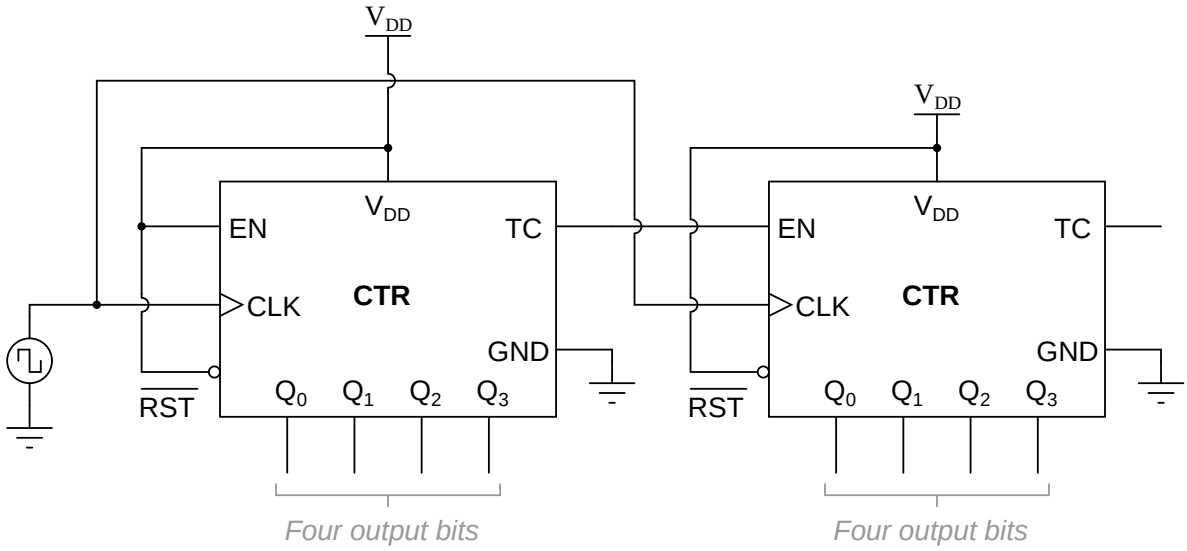


Explain how this counter circuit works, and how its operation differs from the previous eight-bit counter circuit.

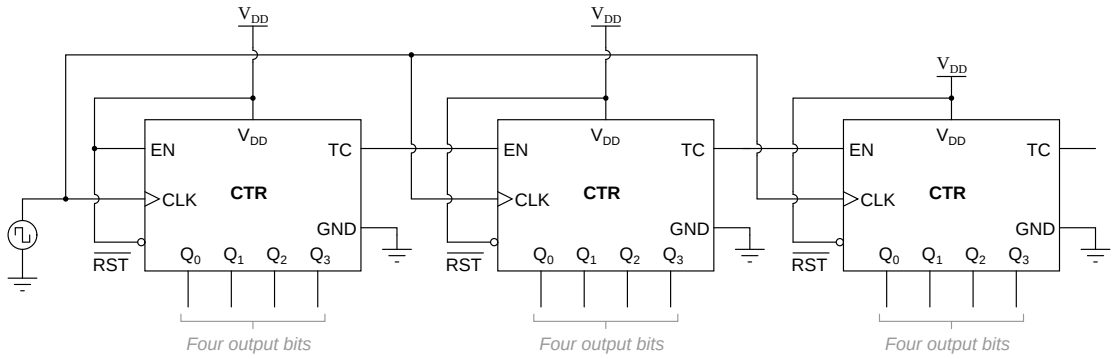
file 02952

Question 15

A student wishes to cascade multiple four-bit synchronous counters together. His first effort looks like this, and it works well as an eight-bit counter:



Encouraged by this success, the student decides to add another four-bit counter to the end to make a twelve-bit counter circuit:



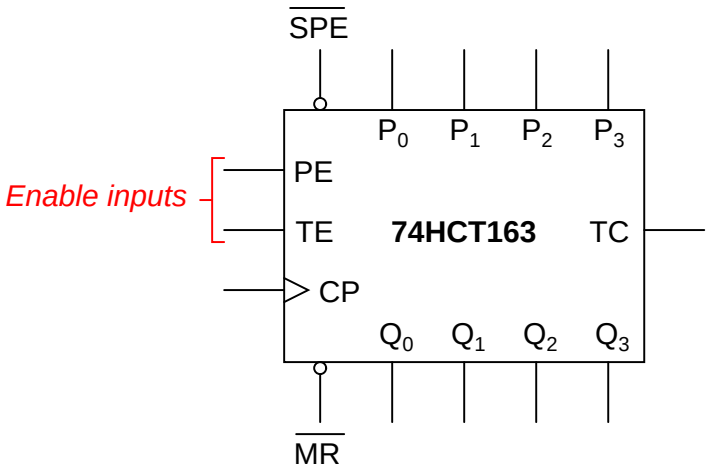
Unfortunately, this arrangement does not work so well. It seems to work good for the first 241 counts (from 000000000000 to 000011110000), but then the last four bits begin to cycle as quickly as the first four bits, while the middle four bits remain in the 1111 state for 15 additional clock pulses. Something is definitely very wrong here!

Determine what the problem is, and suggest a remedy for it. Hint: this situation is very similar to connecting more than two J-K flip-flops together to form a synchronous counter circuit.

file 02954

Question 16

Some integrated circuit counters come equipped with multiple enable inputs. A good example of this is the 74HCT163:



In this case, as in others, the two enable inputs are not identical. Although both must be active for the counter to count, one of the enable inputs does something extra that the other one does not. This additional function is often referred to as a *look-ahead carry*, provided to simplify cascading of counters.

Explain what "look-ahead carry" means in the context of digital counter circuits, and why it is a useful feature.

file 02955

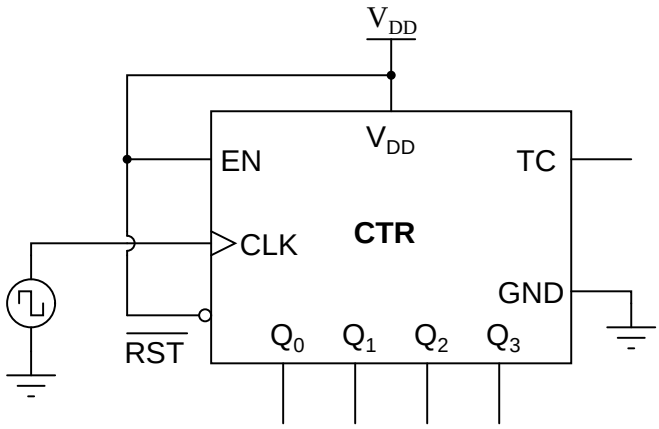
Question 17

Determine the *modulus* (MOD) of a four-bit binary counter. Determine the modulus of two four-bit binary counters cascaded to make an eight-bit binary counter.

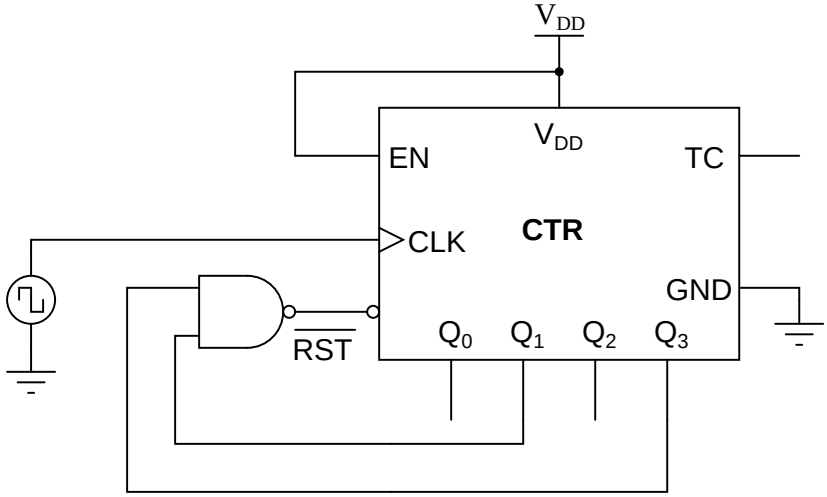
file 01404

Question 18

Consider the following four-bit binary counter integrated circuit (IC). When clocked by the square wave signal generator, it counts from 0000 to 1111 in sixteen steps and then "recycles" back to 0000 again in a single step:



There are many applications, though, where we do not wish the counter circuit to count all the way up to full count (1111), but rather recycle at some lesser terminal count value. Take for instance the application of BCD counting: from 0000 to 1001 and back again. Here is one way to truncate the counting sequence of a binary counter so that it becomes a BCD counter:



Explain how the NAND gate forces this counter to recycle after an output of 1001 instead of counting all the way up to 1111. (Hint: the reset function of this IC is assumed to be *asynchronous*, meaning the counter output resets to 0000 immediately when the $\overline{RST}$ terminal goes low.)

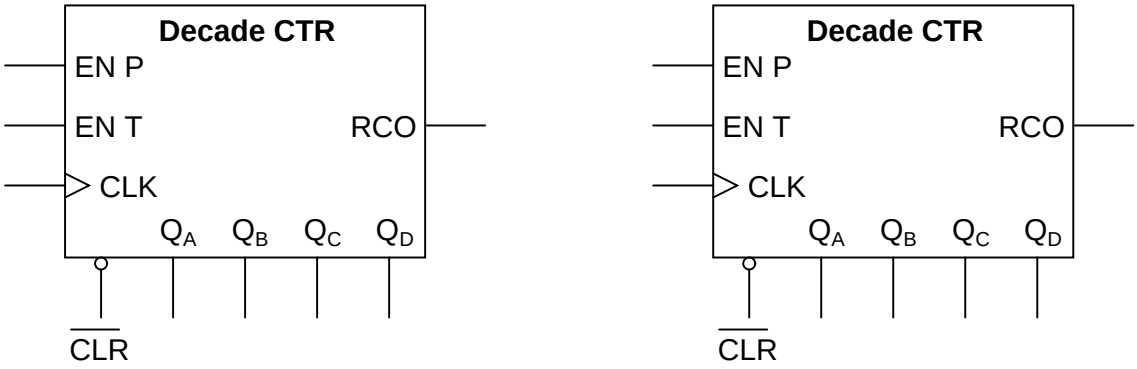
Also, show how you would modify this circuit to do the same count sequence (BCD) assuming the IC has a *synchronous* reset function, meaning the counter resets to 0000 if $\overline{RST}$ is low *and* the clock input sees a pulse.

file 02953

Question 19

Suppose you had an astable multivibrator circuit that output a very precise 1 Hz square-wave signal, but you had an application which requires a pulse once every *minute* rather than once every second. Knowing that there are 60 seconds in a minute, can you think of a way to use digital counters to act as a "frequency divider" so that every 60 multivibrator pulses equates to 1 output pulse?

You don't have a divide-by-60 counter available, but you do have several divide-by-10 ("decade") counters at your disposal. Engineer a solution using these counter units:

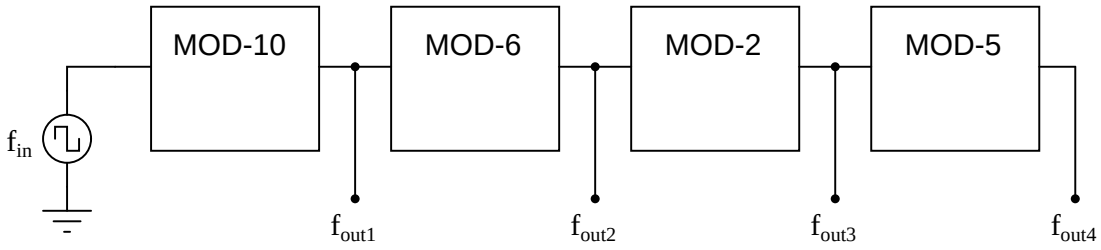


Note: assume these counter ICs have *asynchronous* resets.

file 01405

Question 20

When counters are used as frequency dividers, they are often drawn as simple boxes with one input and one output each, like this:



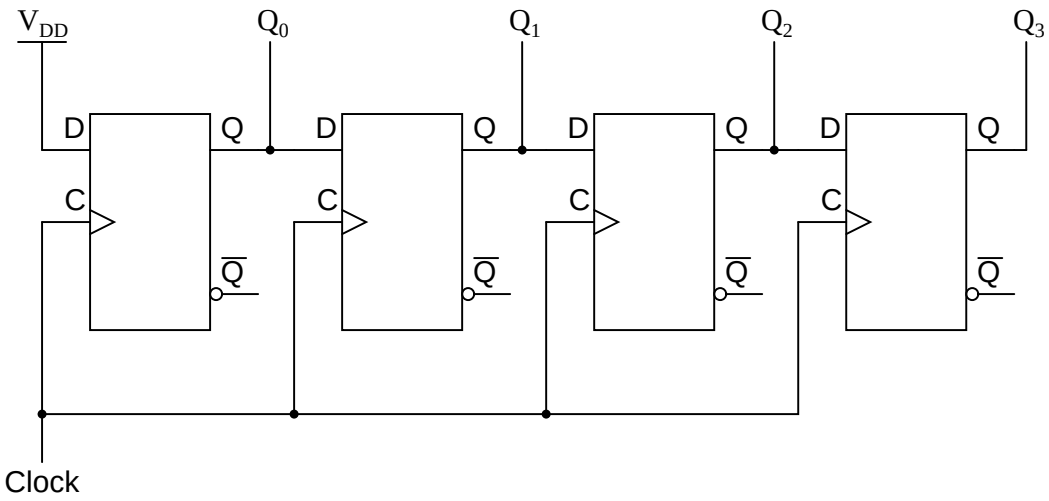
Calculate the four output frequencies (f_{out1} through f_{out4}) given an input frequency of 1.5 kHz:

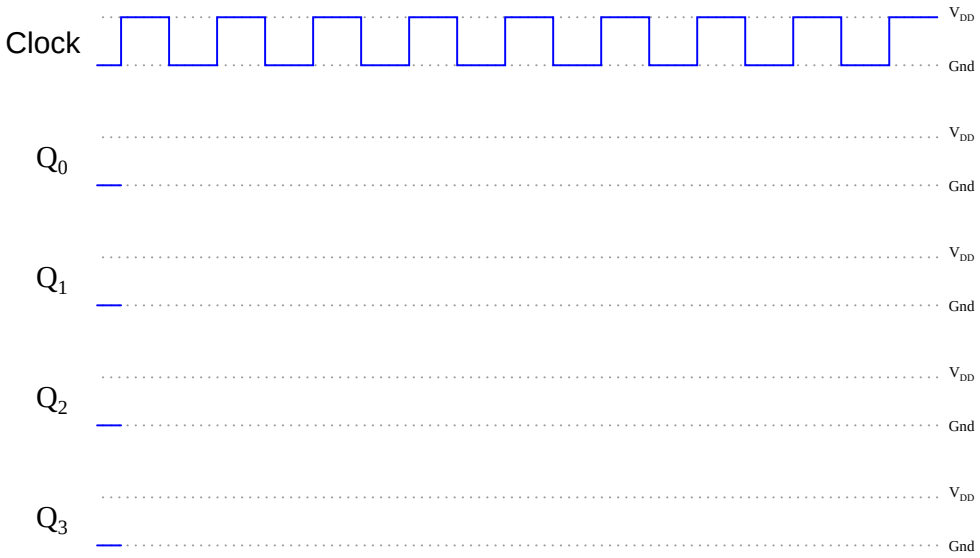
- f_{out1} =
- f_{out2} =
- f_{out3} =
- f_{out4} =

file 02956

Question 21

Complete the timing diagram for this circuit, assuming all Q outputs begin in the low state:

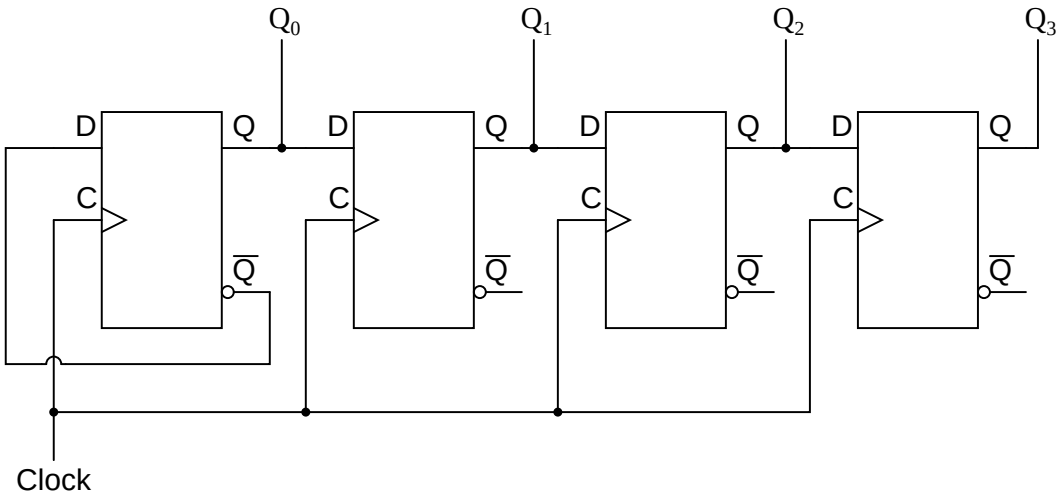


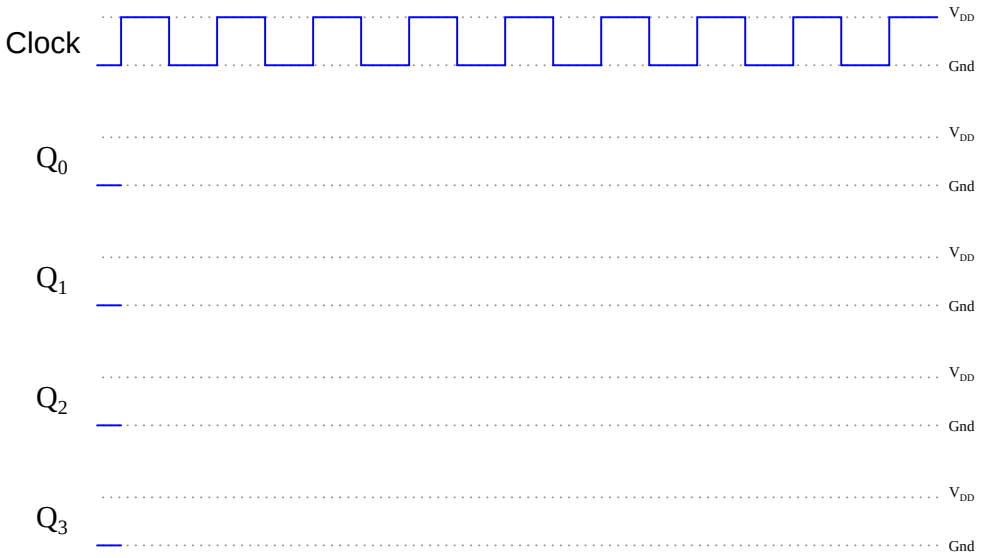


file 02986

Question 22

Complete the timing diagram for this circuit, assuming all Q outputs begin in the low state:





file 02987

Question 23

What is the definition of a *register* in the context of digital circuitry? Also, define and compare/contrast what a *shift register* is.

file 02989

Question 24

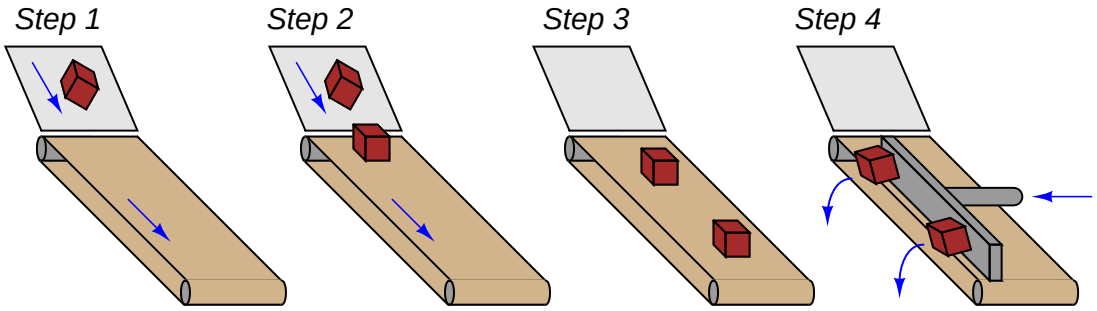
Explain the difference between *serial* digital data and *parallel* digital data.

file 01466

Question 25

A helpful analogy for a shift register is a *conveyor belt*. Examine this illustration showing a single conveyor belt at four different times, and determine which of the following shift register operations the sequence represents:

- Parallel-in, serial-out
- Parallel-in, parallel-out
- Serial-in, serial-out
- Serial-in, parallel-out

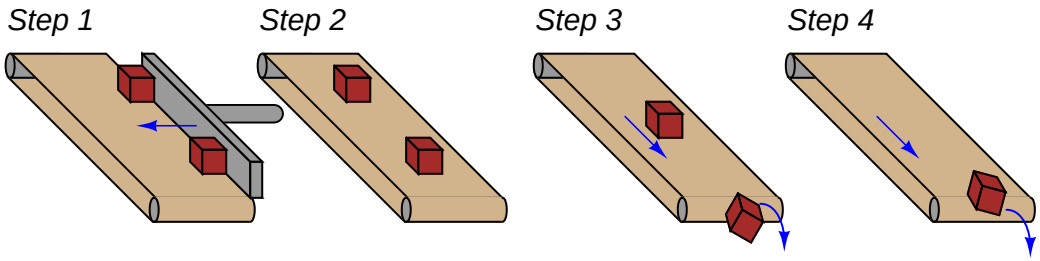


file 02961

Question 26

A helpful analogy for a shift register is a *conveyor belt*. Examine this illustration showing a single conveyor belt at four different times, and determine which of the following shift register operations the sequence represents:

- Parallel-in, serial-out
- Parallel-in, parallel-out
- Serial-in, serial-out
- Serial-in, parallel-out

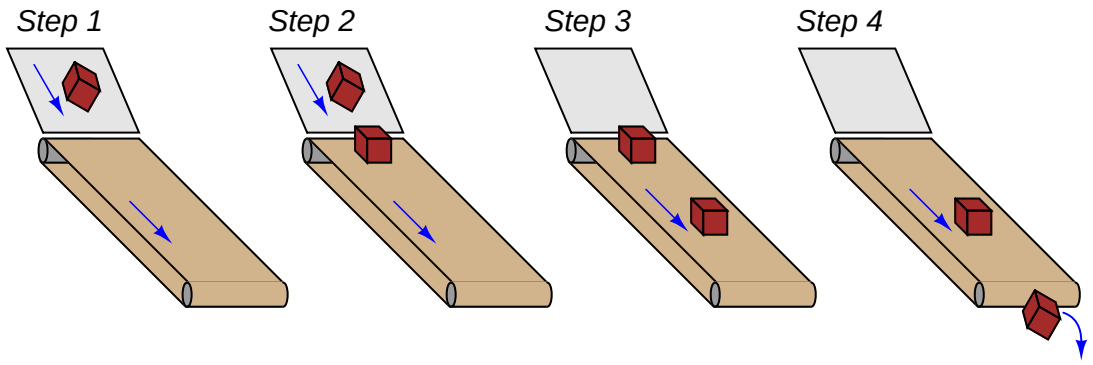


file 02985

Question 27

A helpful analogy for a shift register is a *conveyor belt*. Examine this illustration showing a single conveyor belt at four different times, and determine which of the following shift register operations the sequence represents:

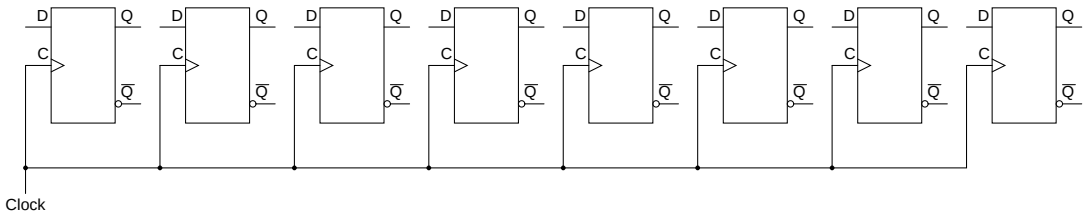
- Parallel-in, serial-out
- Parallel-in, parallel-out
- Serial-in, serial-out
- Serial-in, parallel-out



file 02960

Question 28

Draw the necessary connecting wires between flip-flops so that serial data is shifted from *right to left* instead of left to right as you may be accustomed to seeing in a shift register schematic:



Be sure to also note where data enters this shift register, and where data exits.

file 01471

Question 29

Explain how a shift register circuit could be built from D-type flip-flops with the ability to shift data either to the right or to the left, on command. I'm not necessarily asking for a schematic diagram so much as I'm looking for an *explanation* of how such a circuit might be built. Of course, if your best way of presenting your idea is to draw a schematic diagram, go ahead!

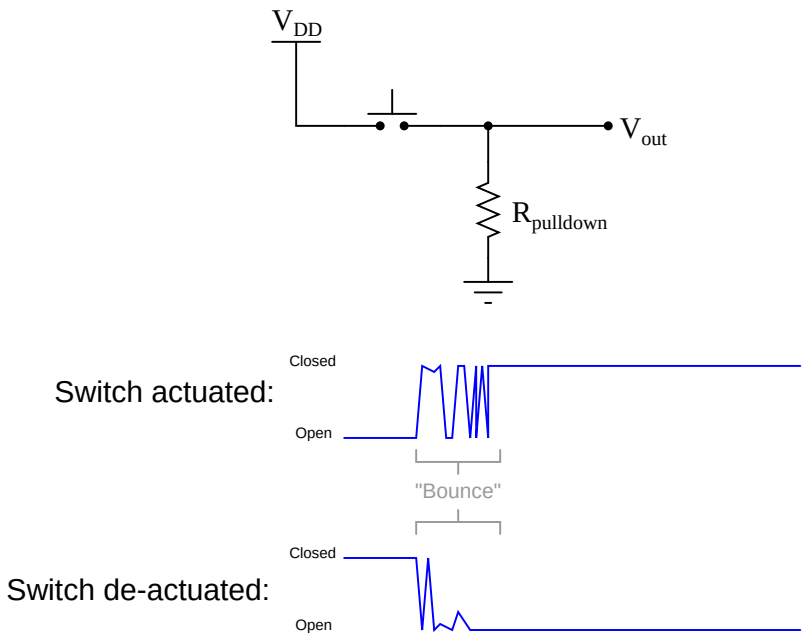
file 01472

Question 30

Explain what a *universal* shift register is. The 74194 is an example of a TTL universal shift register, so you will find that datasheet very helpful in answering this question.

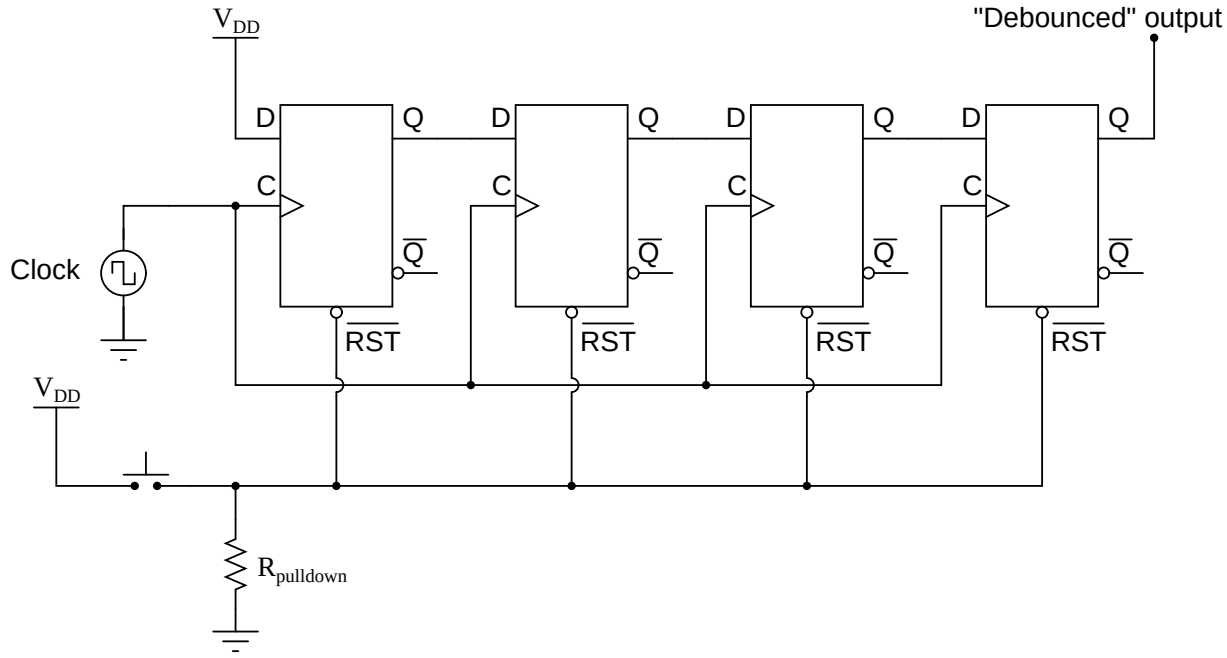
file 01470

Switch contact bounce is often a problem when connecting mechanical contact switches or relays to the inputs of digital semiconductor circuits. When a switch transitions from open to closed, or from closed to open, there is usually a burst of on/off pulses rather than a single, crisp, change of logic state:



Digital electronic circuits, of course, react to these pulses as though they were very rapid actuations/de-actuations of the switch. This may cause problems, especially in applications where a mechanical switch input causes a counter to increment or decrement!

To fix this problem we must properly condition the switch signal to eliminate the spurious on/off pulses. The process of doing this is called *debouncing*. There is more than one way to de-bounce a switch, but one of the more sophisticated ways uses a serial-in, serial-out shift register with an asynchronous reset (clear) input:

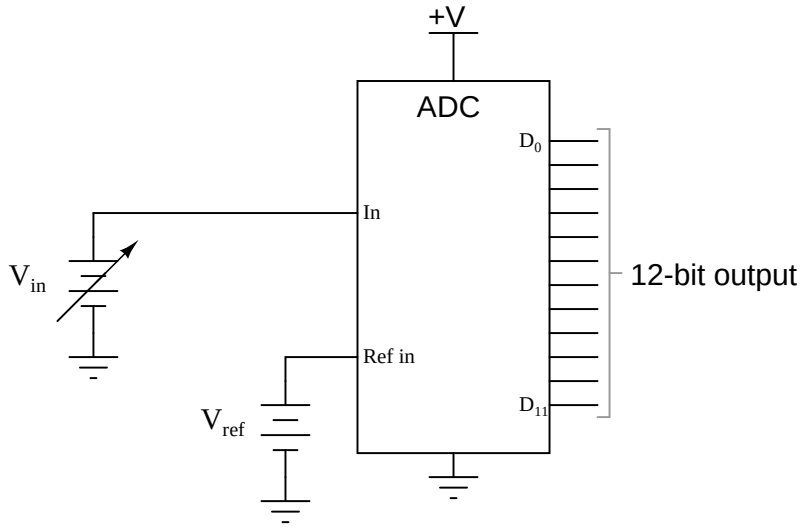


Explain how this circuit works to de-bounce the switch's "dirty" signal, producing a "clean" (de-bounced) signal for a subsequent digital circuit's input.

file 02990

Question 32

An analog-to-digital converter is a circuit that inputs an analog signal and outputs a multiple-bit binary number equivalent to that signal's amplitude:



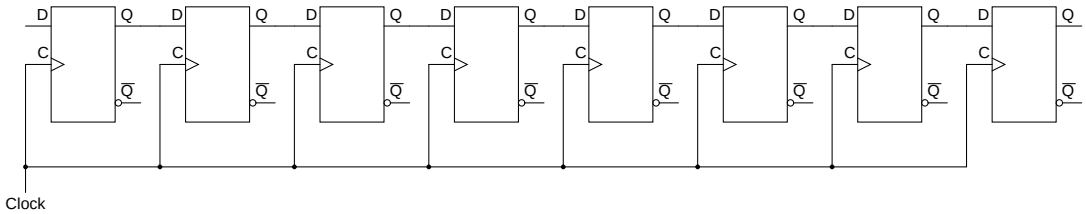
A *free-running* analog-to-digital converter is one that updates its digital output as often as it can, not waiting for any prompting from another device. If we were to connect a free-running ADC to a computer (microprocessor or microcontroller), we would need some way to sample the ADC's output at times specified by the computer, and hold that binary number long enough for the computer to register it. Otherwise, the ADC may update its output in the middle of one of the computer's "input" cycles, possibly resulting in corrupted data.

We could build such a sample-and-hold circuit out of flip-flops. What type of flip-flop would we use for this purpose, and how many would we need for the ADC circuit shown above? This circuit we would build is also known as a *shift register*. What kind of shift register inputs multiple bits of data all at once, and transfers that data to its output lines all at once, at the command of a clock pulse?

file 01465

Question 33

An important function in computer circuitry is *serial-to-parallel data conversion*, where a stream of serial data is "read" one bit at a time, then all bits output at once in parallel form. A shift register circuit is ideal for this application. Shown here is an eight-bit shift register circuit:

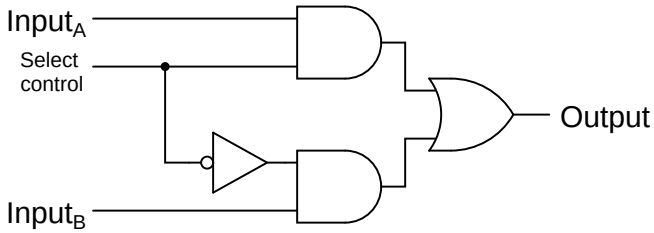


Draw any necessary wires and labels showing where serial data would enter the circuit, and where parallel data would exit.

file 01468

Question 34

The following schematic diagram is for a *two-input selector* circuit, which (as the name implies) selects one of two inputs to be sent to the output:



Determine what state the "select control" input line has to be in to select Input$_A$ to be sent to the output, and what state it has to be in to select Input$_B$ to go to the output.

file 03065

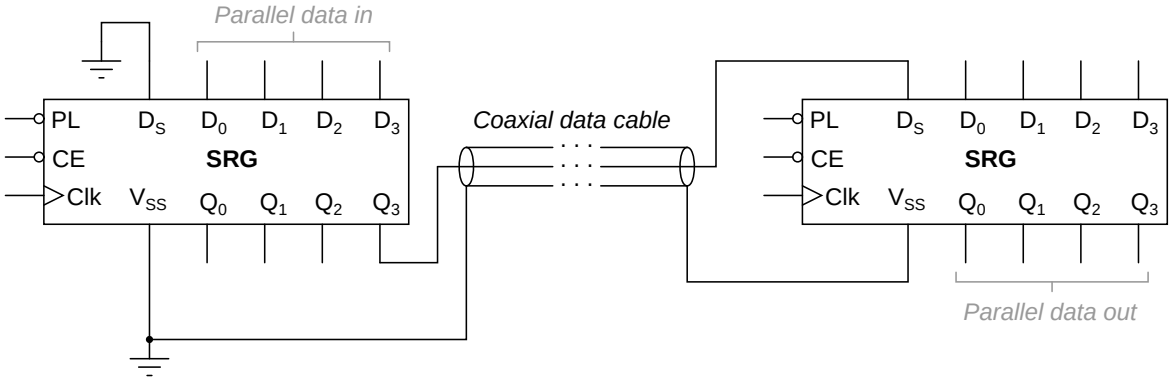
Question 35

Suppose we wished to use a shift register circuit to input several binary bits at once (*parallel* data transfer), and then output the bits one at a time over a single line (*serial* data transfer). You should be aware of how shift registers are constructed with D-type flip-flops. Now, describe how we can get parallel data entered into a shift register circuit. Note: there is more than one answer to this question!

file 01469

Question 36

The following schematic diagram shows two four-bit universal shift registers used to communicate data serially over a coaxial cable of unspecified length:



Specify what logic states would have to be input at the PL, CE, and Clk terminals of each shift register, and at what times, to successfully load four bits of parallel data, shift them serially over the coaxial data cable, and then hold them at the outputs (Q) of the receiving shift register.

file 02997

Question 37

Personal computers and peripheral devices provide a rich source of examples for both serial and parallel data transmission. Identify some common examples of both serial and parallel data transmission networks (and standards) at work in a common personal computer. Examples may include communication between computers, between computers and peripheral devices (printers, scanners, cameras, special cards), or between fundamental components of the computer (CPU, disk drive, monitor, etc.).

file 02993

Question 38

A ubiquitous example of serial data communication is the cable linking a keyboard to a personal computer: for every key switch pressed, an ASCII character is transmitted to the computer. An interesting characteristic of this particular communication protocol is the random rate at which the ASCII characters are sent. Because the characters are generated at the rate the computer user happens to type, the rate is completely unpredictable. Consequently, this form of serial data communication is known as *asynchronous*.

Compare and contrast this against *synchronous* serial data communication, giving an example of a synchronous data communications standard.

file 02995

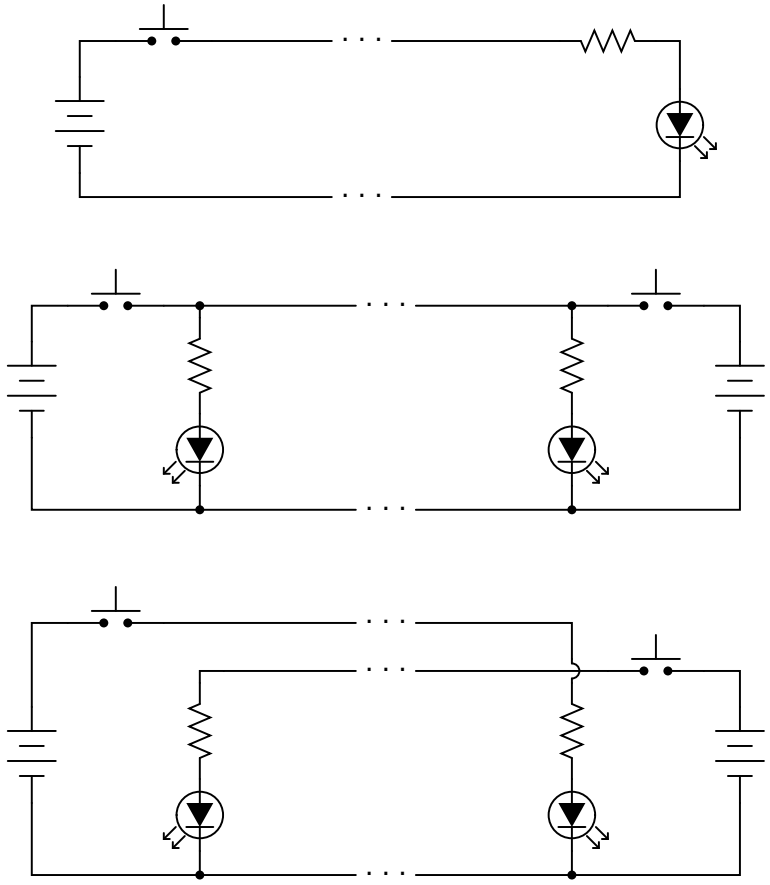
Question 39

An important integrated circuit (IC) used in digital data communication is a *UART*. Describe what this acronym stands for, and explain the purpose of this circuit.

file 02994

Question 40

Shown here are three different telegraph circuits. Determine which of these could be classified as *simplex*, *full-duplex*, and *half-duplex*, in terms of serial data transmission:



file 01284

Question 41

When Digital Audio Tape (DAT) was first introduced to the American public, it was touted as delivering superior sound quality. Most importantly, this high quality of sound was not supposed to degrade over time like standard (analog) audio cassette tape recordings.

The magnetic media from which DAT was manufactured was basically the same stuff used to make *analog* audio tape. Explain why the encoding of audio data *digitally* on the same media would provide superior resistance to degradation over analog recordings even though the recording media was the same. Also, explain how this is significant to modern digital data storage technologies such as those used to store photographic images and numerical data.

file 01441

Question 42

Define the following terms, as they relate to digital memory devices:

- RAM:
- ROM:
- Volatile:
- Nonvolatile:

In particular, explain why "RAM" is a misleading term.
file 01439

Question 43

Determine whether the following recording devices are *random access* or *sequential access*, and discuss the advantage(s) of one type of access over the other:

- DVD (disk)
- Audio tape cassette
- CD-ROM (disk)
- ROM memory chip
- Vinyl phonograph record
- Video tape cassette
- Magnetic "hard" drive
- Magnetic bubble memory
- Paper tape (a long strip of tape with holes punched in it)
- RAM memory chip

file 01440

Question 44

Define the following acronyms:

- ROM:
- PROM:
- EPROM:
- EEPROM:
- UVEPROM:

Be prepared to explain a few things about each of these memory technologies: how they work, what applications they might be found in, advantages and disadvantages of each.
file 01449

Question 45

Explain the difference between *static* RAM ("SRAM") and *dynamic* RAM ("DRAM") memory technologies. Which type of memory technology provides faster access of data, and why? Which type of memory technology provides the greatest storage density, and why?
file 01442

Question 46

Flash memory is a nonvolatile memory technology, offering greater density than either SRAM or DRAM, and faster erasure than standard EPROMs. At first, it would seem Flash memory outperforms all other memory types, but it doesn't. What are some of the *disadvantages* of Flash memory, and what kind of applications is it best suited for?
file 01452

Question 47

Two very important concepts to understand when working with digital memory devices are *address* and *data*. Define each of these terms in your own words.

file 01444

Question 48

A ROM memory chip is rated at 4k $\times$ 8 bits. What, exactly, does this designation mean? How many addresses are there inside this memory chip? How many bits of storage are there, total, in this memory chip? How many address bits are there, and how many data bits are there?

file 01443

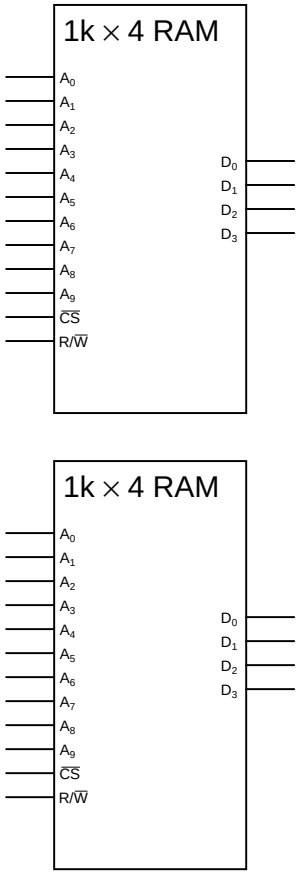
Question 49

Suppose you need to store a text message in digital memory, consisting of 7500 ASCII characters. What is the most logical memory organization (addresses $\times$ data lines) to do this? How many address bits would be needed to store these 7500 characters?

file 01445

Question 50

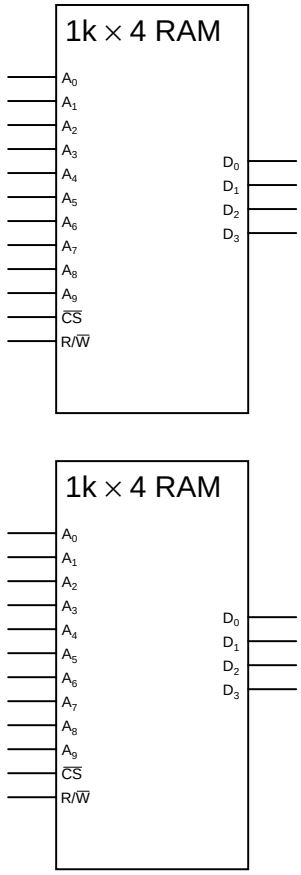
Suppose you need a memory array with 1k $\times$ 8 organization, but all you have on hand are 1k $\times$ 4 memory chips. Show how you could connect two of them to form the desired array:



file 01446

Question 51

Suppose you need a memory array with 2k × 4 organization, but all you have on hand are 1k × 4 memory chips. Show how you could connect two of them to form the desired array:



file 01447

Question 52

Dynamic RAM chips often contain more addresses than they have address lines to select them with. For example, the MCM516100 DRAM chip has an organization of 16M × 1, yet it only has twelve address lines.

Explain how it is possible to select one out of 16 *million* unique addresses while using only twelve address lines. Hint: the technique is known as *address multiplexing*. Be sure to refer to one or more dynamic RAM datasheets when doing your research!

file 01451

Question 53

After a ROM memory has been programmed with data, it is good to verify that the data now stored is okay, and not corrupted with any errors. A popular method of doing this is to calculate a *checksum* on the stored data, and compare that against the checksum for the original data. If the checksum numbers are identical, chances are there are no corruptions in the stored data.

Explain exactly what checksum is, and how it works as an error-detection strategy.

file 01450

Question 54

An important use for read-only semiconductor memories is as *look-up tables*. Describe what a "look-up table" is, and what one might be used for.

file 01477

Question 55

Research datasheets for the 74LS184 and 74LS185 integrated circuits, and then explain how read-only memory technology is used to perform the BCD/binary conversion functions.

file 02991

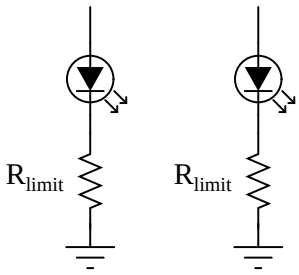
Question 56

Competency: **2-bit flip-flop counter circuit** Version:

Description

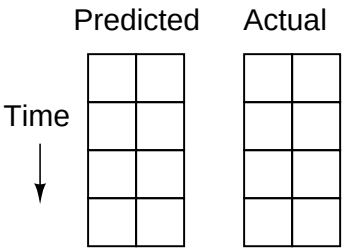
Build a 2-bit counter circuit using individual J-K flip-flops.

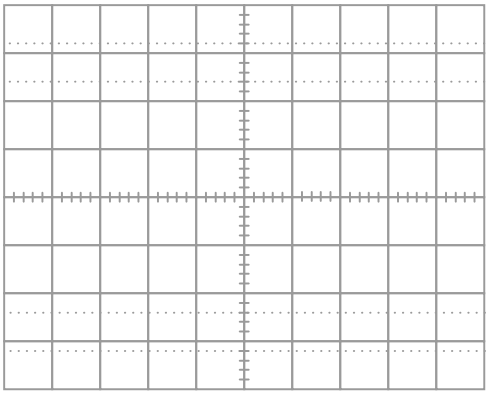
Schematic



Count sequence

Output timing diagram as shown by oscilloscope





Identify the counting states on the oscilloscope display (00, 01, 10, and 11).

file 02947

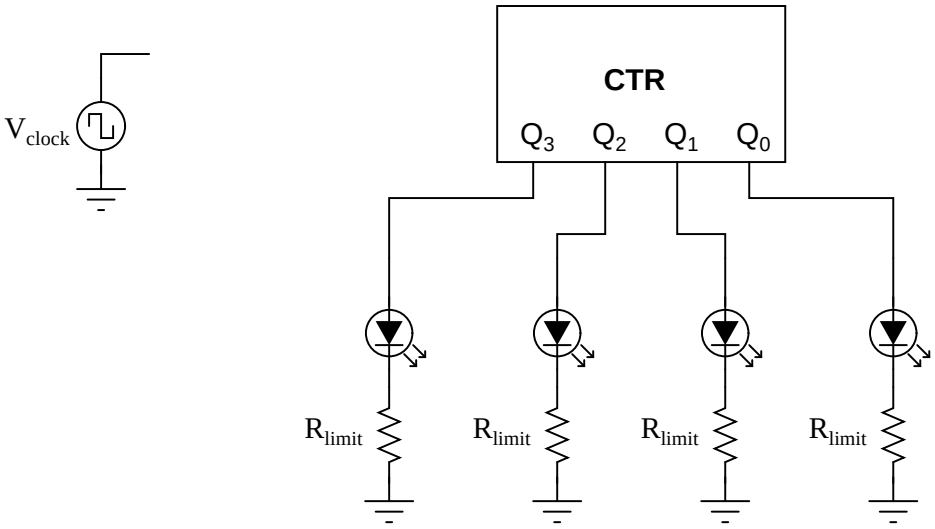
Question 57

Competency: **4-bit up/down counter IC** Version:

Description

Configure a 4-bit counter IC to count either up or down depending on the position of a selector switch. Complete the schematic diagram to show the switch and all other necessary components/connections.

Schematic



Count sequence

Counts in the "up" direction ☐

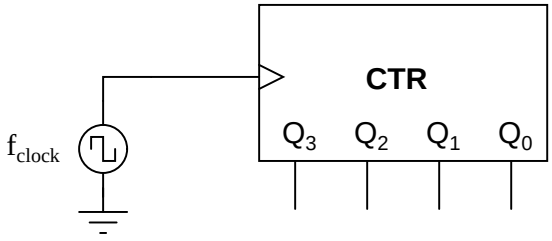
Counts in the "down" direction ☐

file 02957

Question 58

Competency: **Binary counter as frequency divider** Version:

Schematic



Given conditions

f_{clock} =

Parameters

	Predicted	Measured
f_{Q0}		
f_{Q1}		
f_{Q2}		
f_{Q3}		

file 02959

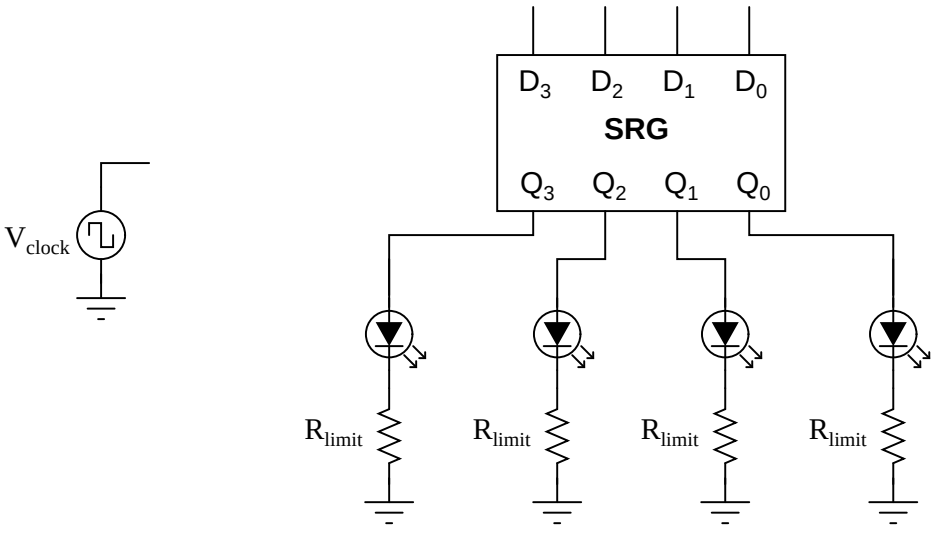
Question 59

Competency: **4-bit universal shift register IC** Version:

Description

Configure a 4-bit universal shift register IC to load parallel data, then shift in both directions. Complete the schematic diagram to show all switches and other necessary components/connections.

Schematic



Shift sequence

Loads parallel data ☐

Shifts right ☐

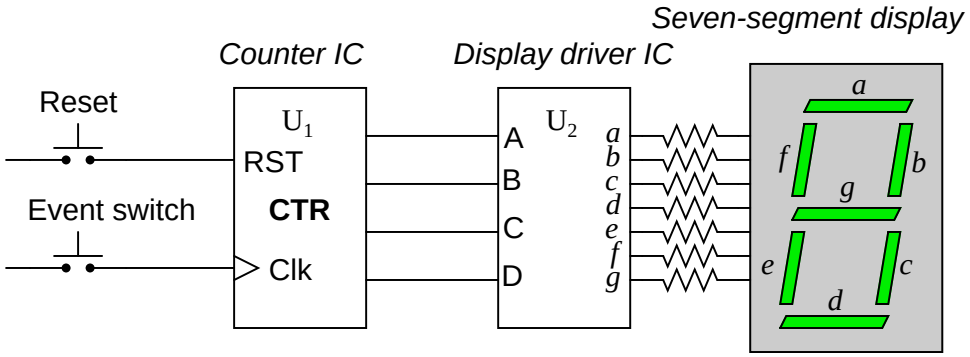
Shifts left ☐

file 02958

Question 60

Competency: **Decade counter circuit** Version:

Schematic



Details purposely omitted from schematic diagram

Given conditions

U_1 = U_2 =

Parameters

Counter increments with each physical event, counting from 0 to 9 and then resetting back to 0 again. Count sequence exhibits no skipped counts and no missed events.

☐ YES

☐ NO

file 03851

Question 61

Troubleshooting log

Actions / Measurements / Observations (i.e. *What I did and/or noticed . . .*)	**Conclusions** (i.e. *What this tells me . . .*)

file 03933

Question 62

NAME: _____ **Troubleshooting Grading Criteria**

You will receive the highest score for which *all* criteria are met.

100 % *(Must meet or exceed all criteria listed)*
A. Absolutely flawless procedure
B. No unnecessary actions or measurements taken

90 % *(Must meet or exceed these criteria in addition to all criteria for 85% and below)*
A. No reversals in procedure (i.e. changing mind without sufficient evidence)
B. Every single action, measurement, and relevant observation properly documented

80 % *(Must meet or exceed these criteria in addition to all criteria for 75% and below)*
A. No more than one unnecessary action or measurement
B. No false conclusions or conceptual errors
C. No missing conclusions (i.e. at least one documented conclusion for action / measurement / observation)

70 % *(Must meet or exceed these criteria in addition to all criteria for 65%)*
A. No more than one false conclusion or conceptual error
B. No more than one conclusion missing (i.e. an action, measurement, or relevant observation without a corresponding conclusion)

65 % *(Must meet or exceed these criteria in addition to all criteria for 60%)*
A. No more than two false conclusions or conceptual errors
B. No more than two unnecessary actions or measurements
C. No more than one undocumented action, measurement, or relevant observation
D. Proper use of all test equipment

60 % *(Must meet or exceed these criteria)*
A. Fault accurately identified
B. Safe procedures used at all times

50 % *(Only applicable where students performed significant development/design work – i.e. not a proven circuit provided with all component values)*
A. Working prototype circuit built and demonstrated

0 % *(If any of the following conditions are true)*
A. Unsafe procedure(s) used at any point

file 03932

Question 63

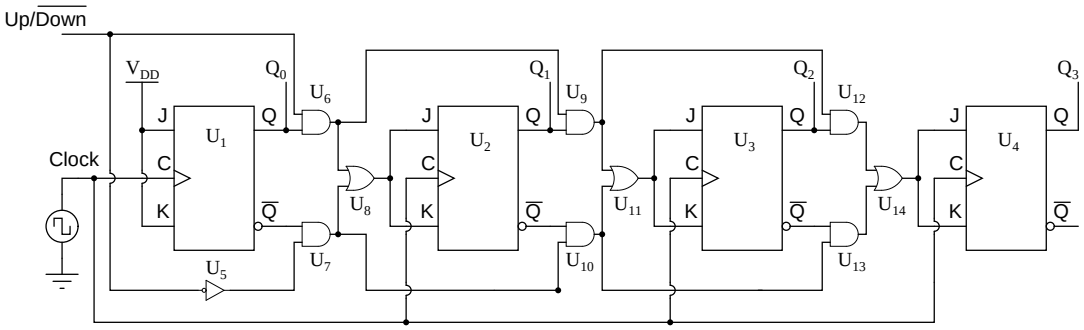
A student builds a four-bit asynchronous counter circuit using CMOS J-K flip-flops. It seems to work . . . most of the time. Every once in a while, the count suddenly and mysteriously "jumps" out of sequence, to a value that is completely wrong. Even stranger than this is the fact that it seems to happen every time the student waves their hand next to the circuit.

What do you suspect the problem to be?

file 01406

Question 64

Identify a single fault that would allow this synchronous counter circuit to count up on demand, but not down:

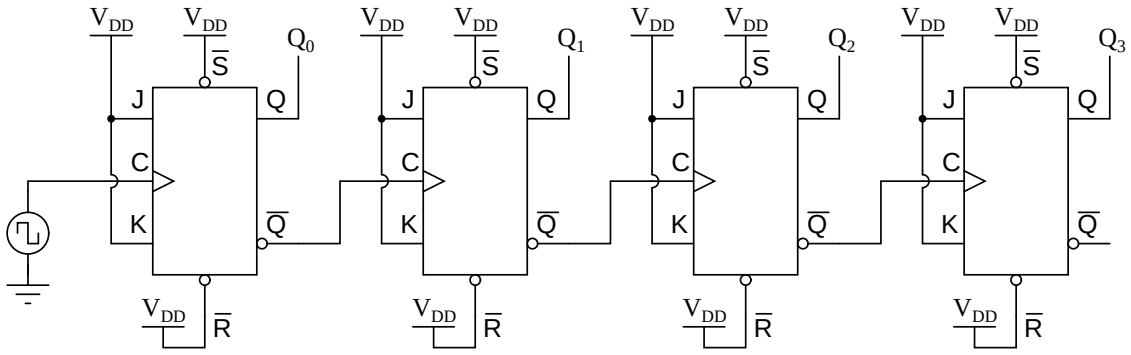


Explain *why* your proposed fault would cause the problem.

file 03897

Question 65

A student builds a four-bit asynchronous *up* counter out of individual J-K flip-flops, but is dissatisfied with its performance:

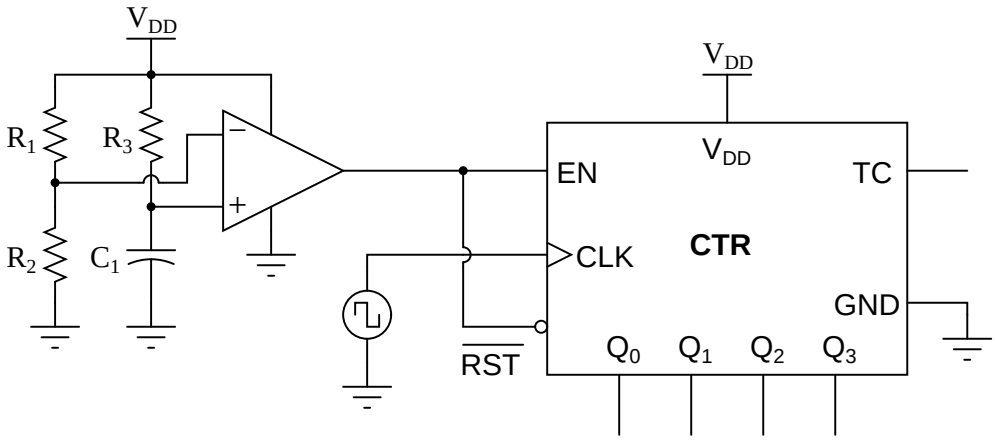


Although the counting sequence is proper, the circuit usually does not begin counting from `0000` at power-up. The fact that the circuit counts correctly suggests that there is nothing failed or mis-wired, so what could possibly be wrong?

file 03901

Question 66

The following RC circuit constitutes an *automatic reset* network for the counter. At power-up, it resets the counter to `0000`, then allows it to count normally:



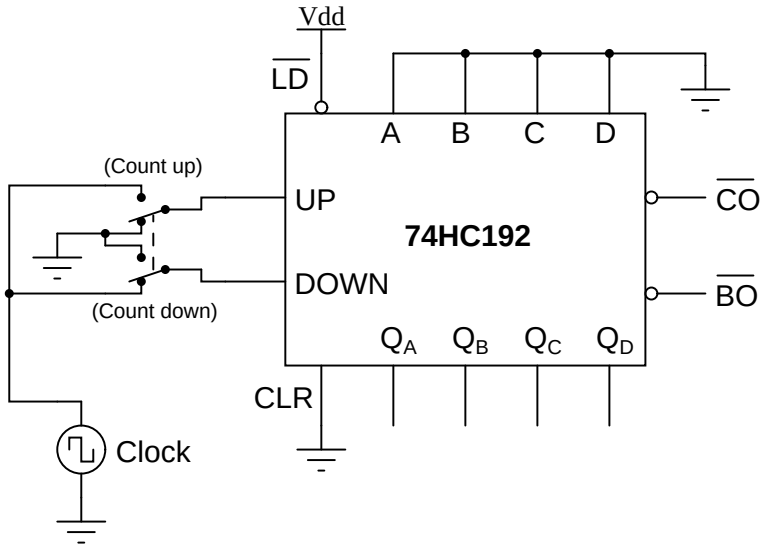
Predict how the operation of this automatic reset circuit will be affected as a result of the following faults. Consider each fault independently (i.e. one at a time, no multiple faults):

- Resistor R_1 fails open:
- Resistor R_2 fails open:
- Resistor R_3 fails open:
- Capacitor C_1 fails shorted:

For each of these conditions, explain *why* the resulting effects will occur.
file 03902

Question 67

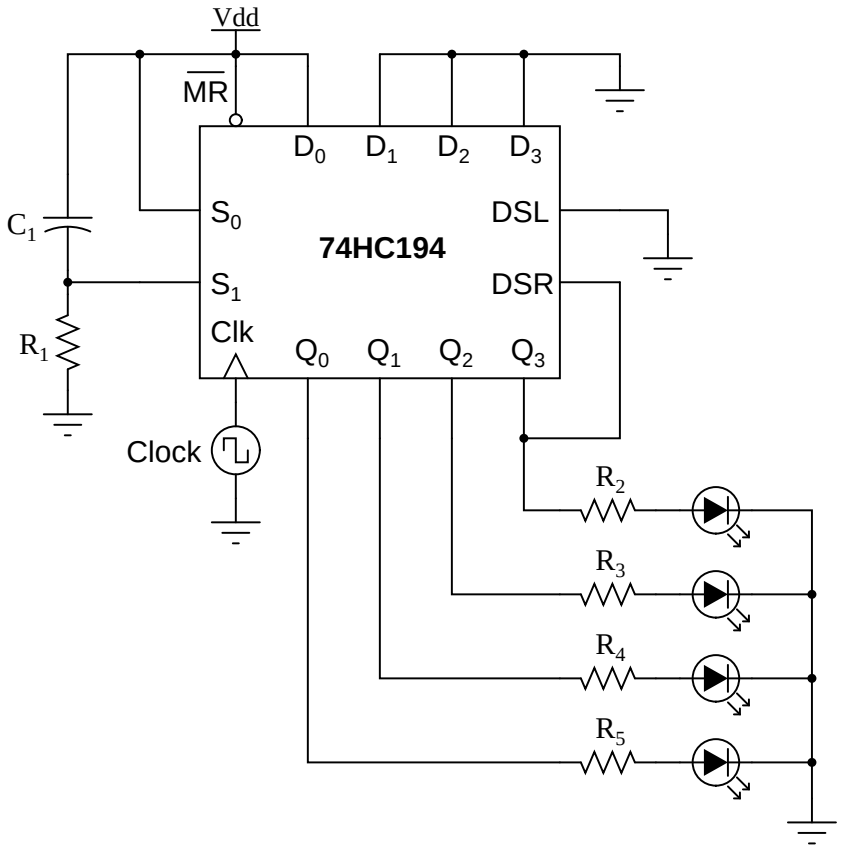
A student is trying to get a 74HC192 up/down counter to function. However, it is simply not cooperating:



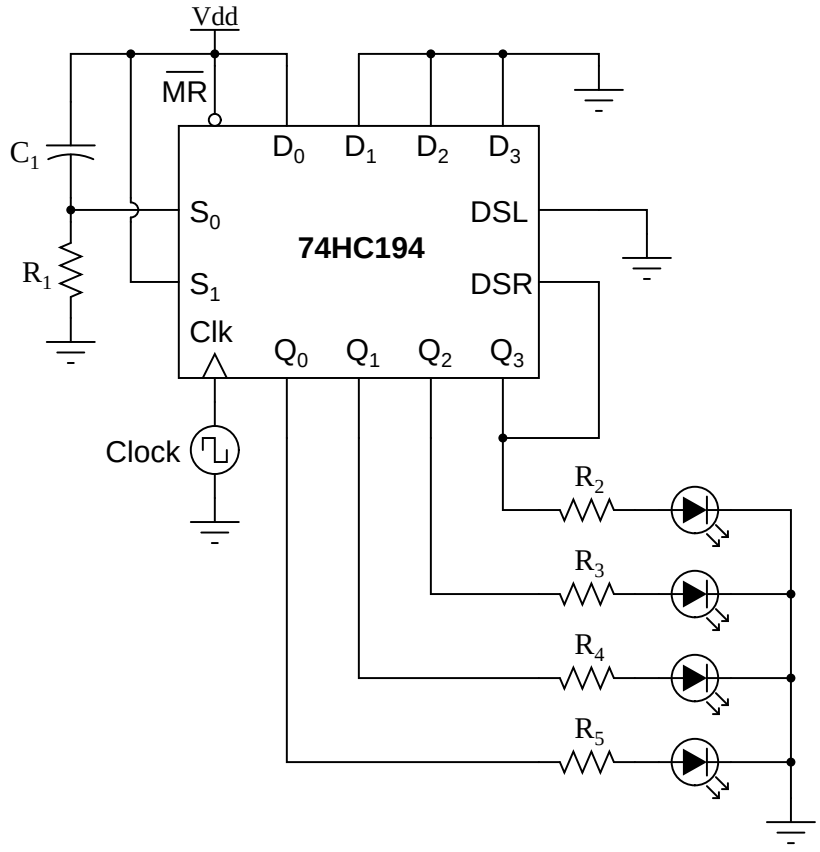
Determine what the student is doing wrong with this 74HC192, and then correct the schematic diagram.
file 03903

Question 68

This shift register circuit energizes one LED at a time (beginning with the bottom LED at power-up), in a rotating pattern that moves at the pace of the clock:



A technician decides to reverse the direction of pattern motion, and alters the circuit as such:

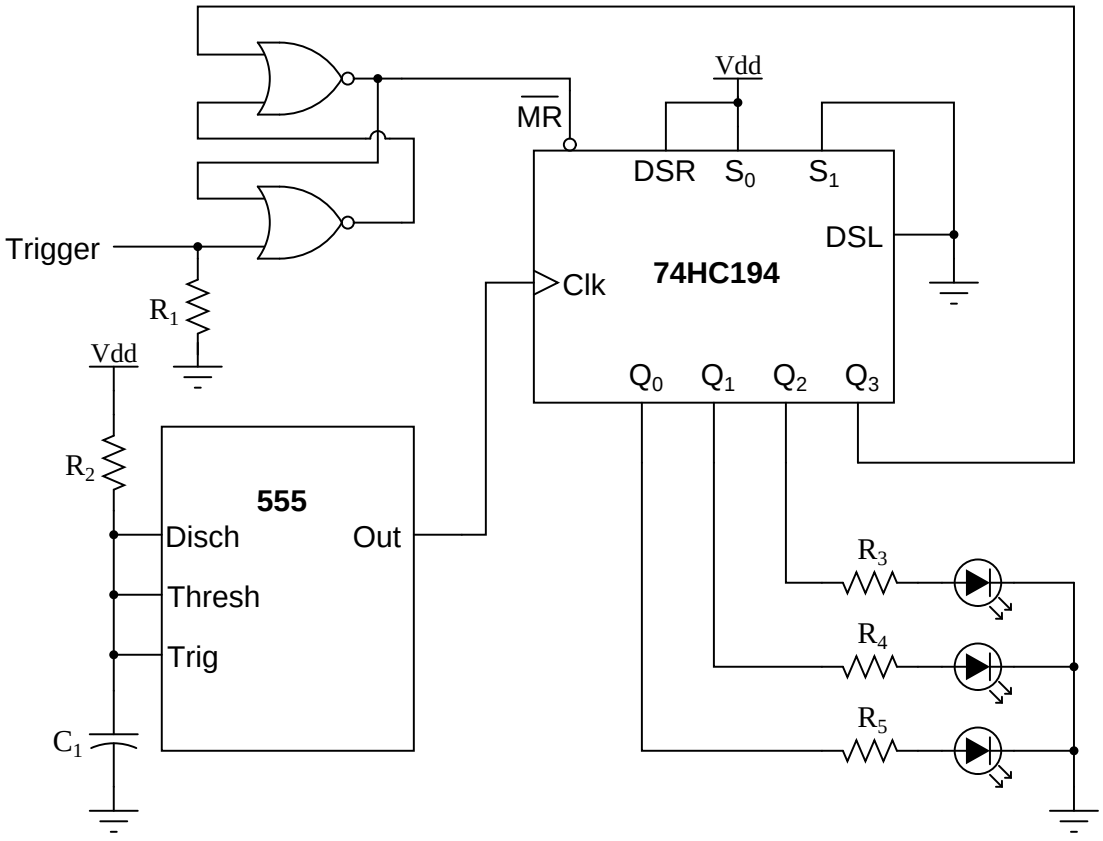


Unfortunately, this does not work as planned. Now, the bottom LED blinks once upon power-up, then all LEDs remain off. What did the technician do that was incorrect? What needs to be done to fix the problem?

file 03904

Question 69

This shift register circuit produces a sequential light pattern reminiscent of the old Mercury Cougar tail-lights: first one LED energizes, then two LEDs energize, and then all three LEDs energize before all de-energizing and repeating the sequence. The 74HC194 shift register circuit is set to always operate in the "shift right" mode with the shift-right serial input (DSR) tied high, the master reset ($\overline{MR}$) input used to set all output lines to a low state at the end of each cycle:



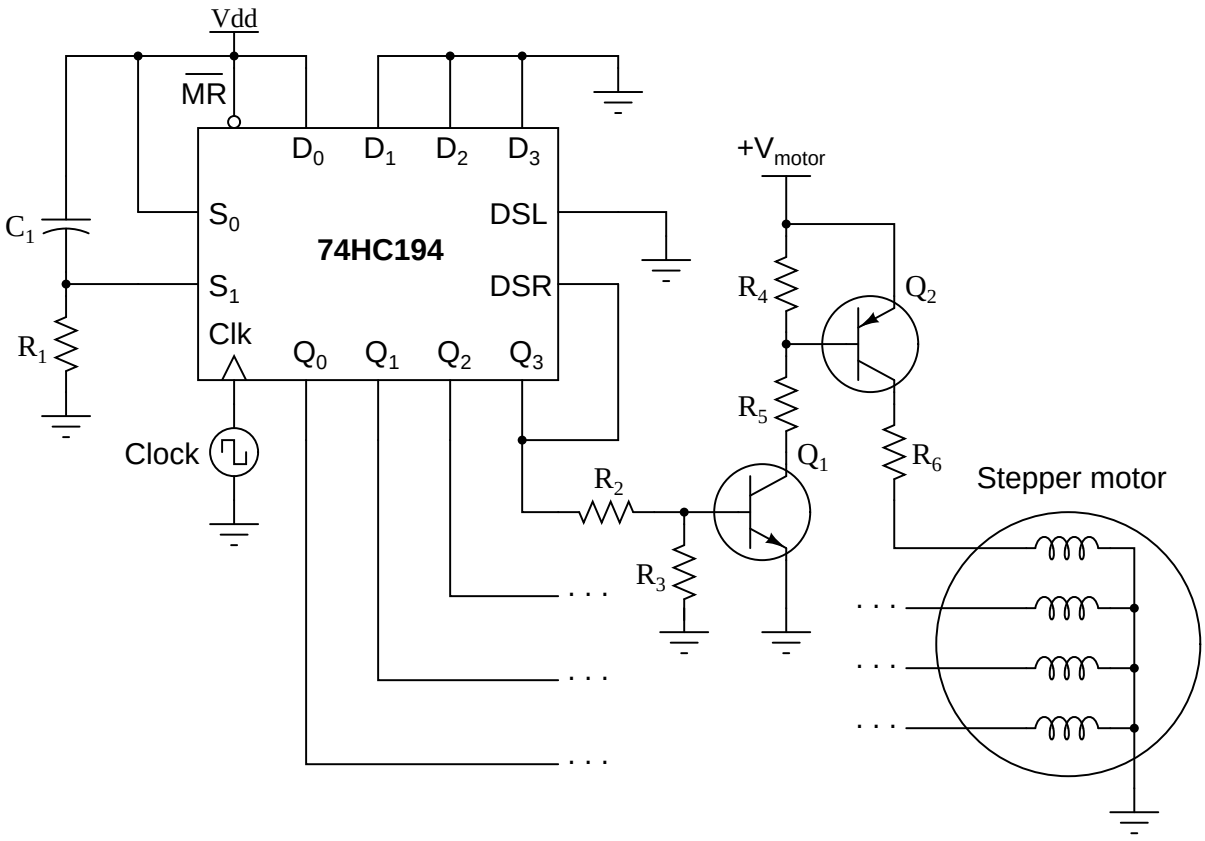
The sequential light pattern is supposed to begin whenever the "Trigger" input momentarily goes high. Unfortunately, something has failed in this circuit which is preventing any of the LEDs to come on. No blinking light sequence ensues, no matter what the state of the "Trigger" input.

Identify some likely failures in this circuit that could cause this to happen, other than a lack of power supply voltage. Explain why each of your proposed faults would cause the problem, and also identify how you would isolate each fault using test equipment.

file 03906

Question 70

This shift register circuit drives the four coils of a unipolar stepper motor, one at a time, in a rotating pattern that moves at the pace of the clock. The drive transistor circuitry (Q_1, Q_2, and resistors R_2 through R_6) are shown only for one of the four coils. The other three shift register outputs have identical drive circuits connected to the respective motor coils:

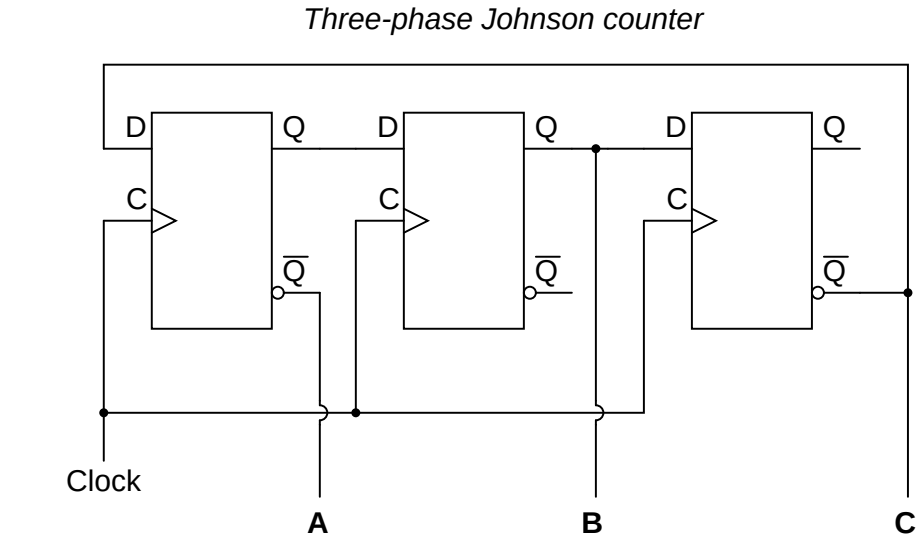


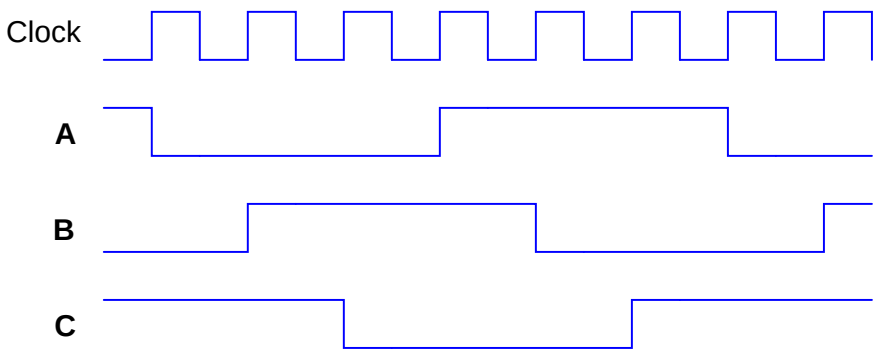
Suppose this stepper motor circuit worked just fine for several years, then suddenly stopped working. Explain where you would take your first few measurements to isolate the problem, and why you would measure there.

file 03905

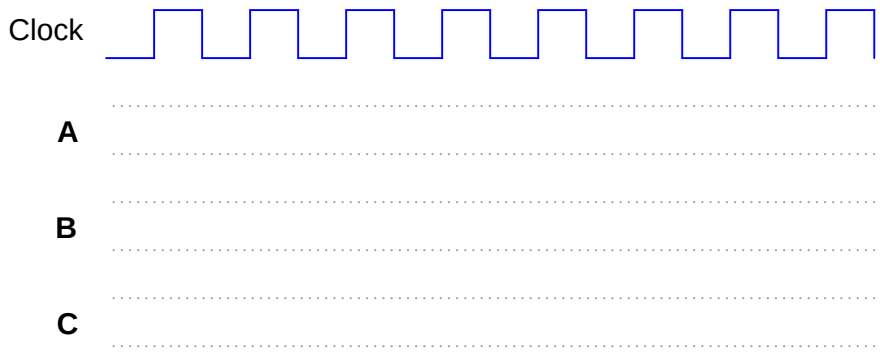
Question 71

This Johnson counter circuit is special. It outputs three square-wave signals, shifted 120^o from one another:





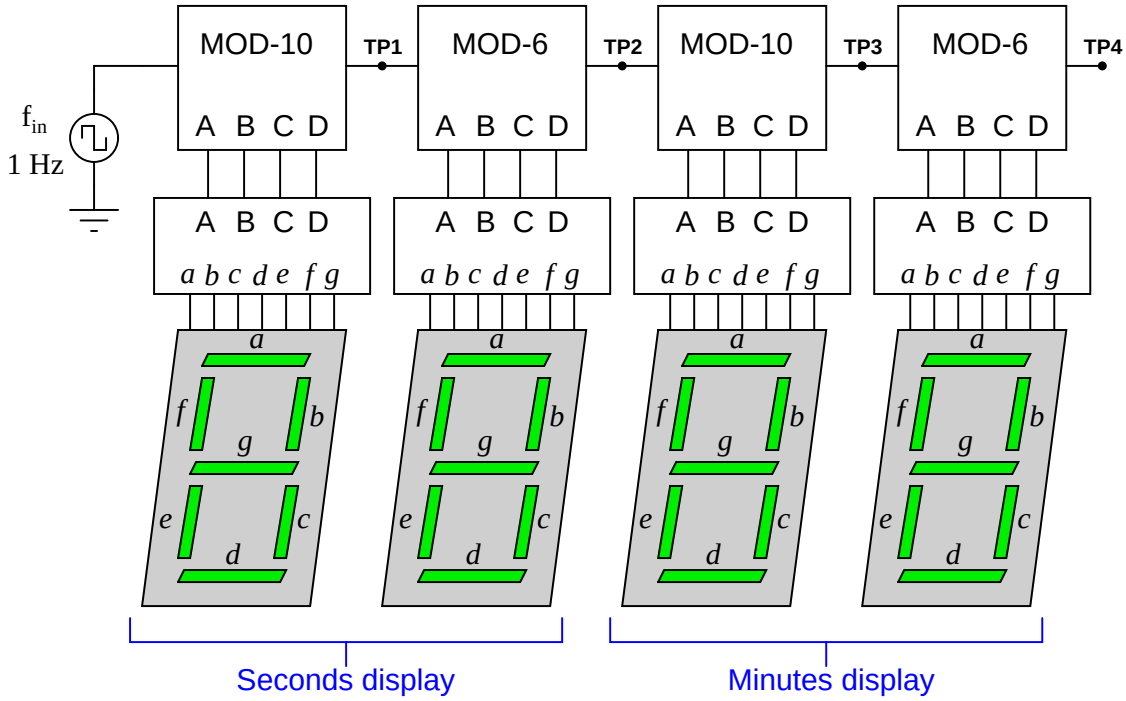
Suppose the middle flip-flop's Q output fails in the "high" state. Plot the new output waveforms for signals **A**, **B**, and **C**. Assume all Q outputs begin in the "low" state (except for the middle flip-flop, of course):



file 03907

Question 72

A technician is trying to build a timer project using a set of cascaded counters, each one connected to its own 7-segment decoder and display:



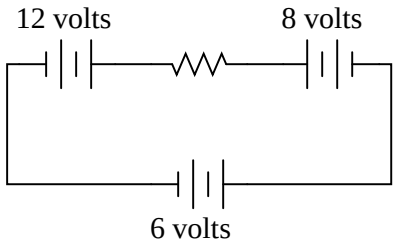
The technician was trying to troubleshoot this circuit, but left without finishing the job. You were sent to finish the work, having only been told that the timer circuit "has some sort of problem." Your first step is to start the 1 Hz clock and watch the timing sequence, and after a few minutes of time you fail to notice anything out of the ordinary.

Now, you could sit there for a whole hour and watch the count sequence, but that might take a long time before anything unusual appears for you to see. Devise a test procedure that will allow you to pinpoint problems at a much faster rate.

file 03908

Question 73

Determine both the polarity of voltage across the resistor in this circuit, and how much voltage will be dropped across the resistor:

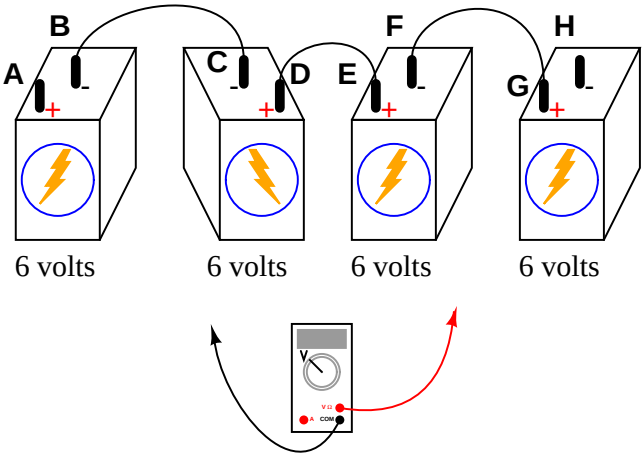


Explain the procedure(s) you used to answer both these questions.

file 01548

Question 74

Determine what a digital voltmeter (DVM) would indicate if connected between the following points in this circuit:



- Red lead on A, black lead on H
- Red lead on C, black lead on G
- Red lead on F, black lead on B
- Red lead on F, black lead on A

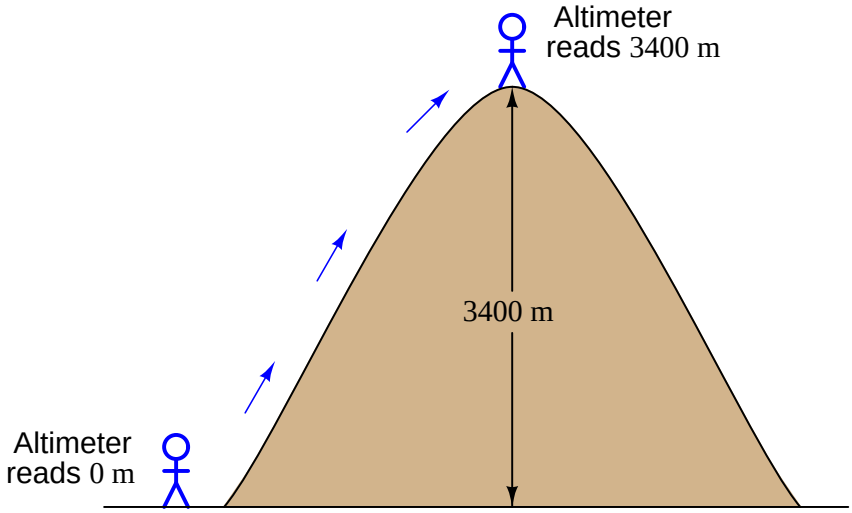
file 00347

Question 75

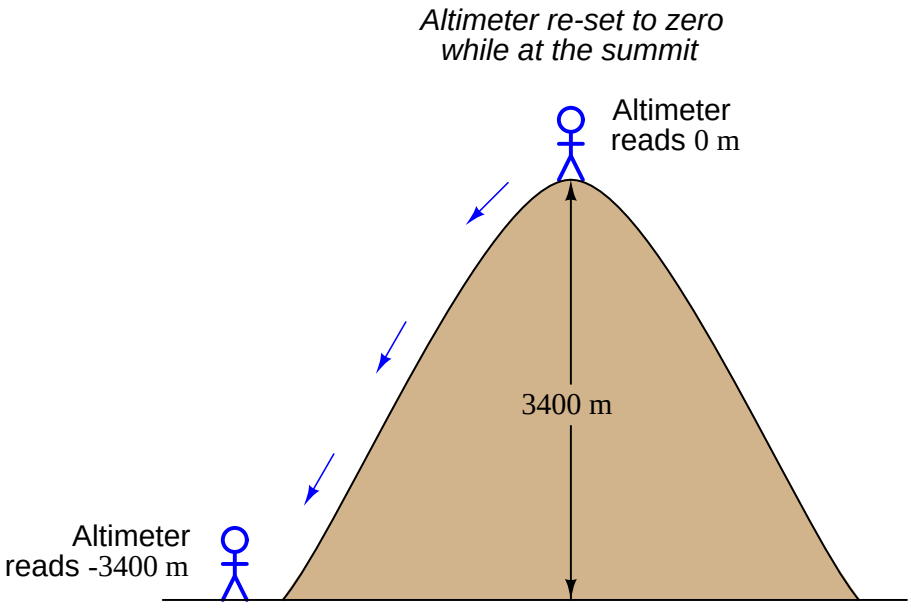
A *barometric altimeter* is a device used to measure altitude (height) by means of atmospheric pressure. The higher you go up from sea level, the less air pressure you encounter. This decrease in air pressure is closely correlated with height, and thus can be used to infer altitude.

This type of altimeter usually comes equipped with a "zero" adjustment, so that the instrument's indication may be offset to compensate for changes in air pressure resulting from different weather conditions. This same "zero" adjustment may also be used to establish the altimeter's zero indication at any arbitrary height.

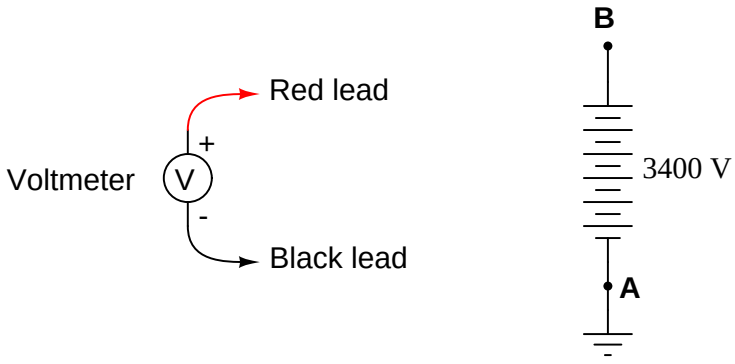
For example, if a mountain climber sets her barometric altimeter to zero meters at the base of a mountain, then climbs to the summit of that mountain (3400 meters higher than the base), the altimeter should register 3400 meters at the summit:



While at the summit, the climber may re-set the altimeter's "zero" adjustment to register 0 meters once again. If the climber then descends to the base of the mountain, the altimeter will register -3400 meters:



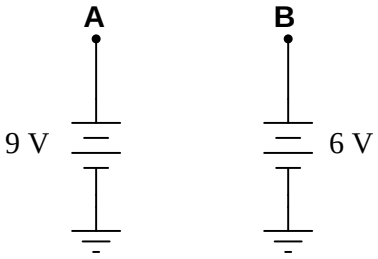
Explain how this scenario of mountain climbing and altimeter calibration relates to the measurement of voltage between points **A** and **B** in the following circuit:



file 01960

Question 76

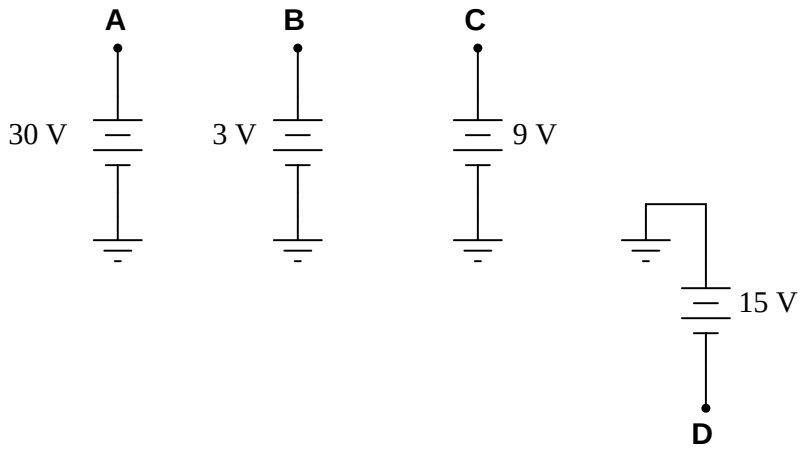
Determine the amount of voltage measured at points **A** and **B** with reference to ground, and also determine voltage V_{AB} (defined here as the voltage indicated by a voltmeter with the red test lead touching point **A** and the black test lead touching point **B**):



file 01958

Question 77

Determine the voltages registered by a voltmeter between the following points in this circuit:



V_A = _____ (red lead on **A**, black lead on ground)

V_B = _____ (red lead on **B**, black lead on ground)

V_C = _____ (red lead on **C**, black lead on ground)

V_D = _____ (red lead on **D**, black lead on ground)

V_{AC} = _____ (red lead on **A**, black lead on **C**)

V_{DB} = _____ (red lead on **D**, black lead on **B**)

V_{BA} = _____ (red lead on **B**, black lead on **A**)

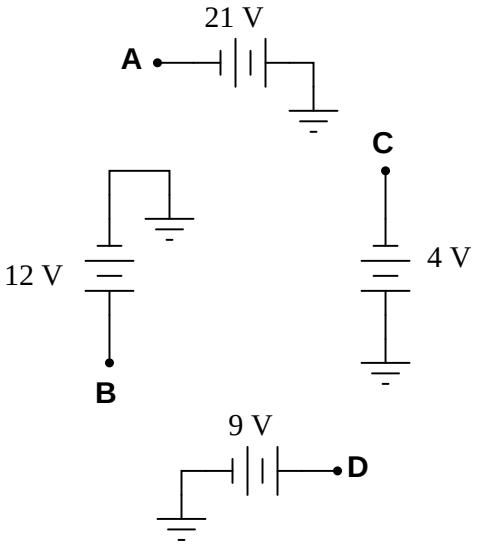
V_{BC} = _____ (red lead on **B**, black lead on **C**)

V_{CD} = _____ (red lead on **C**, black lead on **D**)

file 02750

Question 78

Determine the voltages registered by a voltmeter between the following points in this circuit:



V_A = _____ (red lead on **A**, black lead on ground)

V_B = _____ (red lead on **B**, black lead on ground)

V_C = _____ (red lead on **C**, black lead on ground)

V_D = _____ (red lead on **D**, black lead on ground)

V_{AC} = _____ (red lead on **A**, black lead on **C**)

V_{DB} = _____ (red lead on **D**, black lead on **B**)

V_{BA} = _____ (red lead on **B**, black lead on **A**)

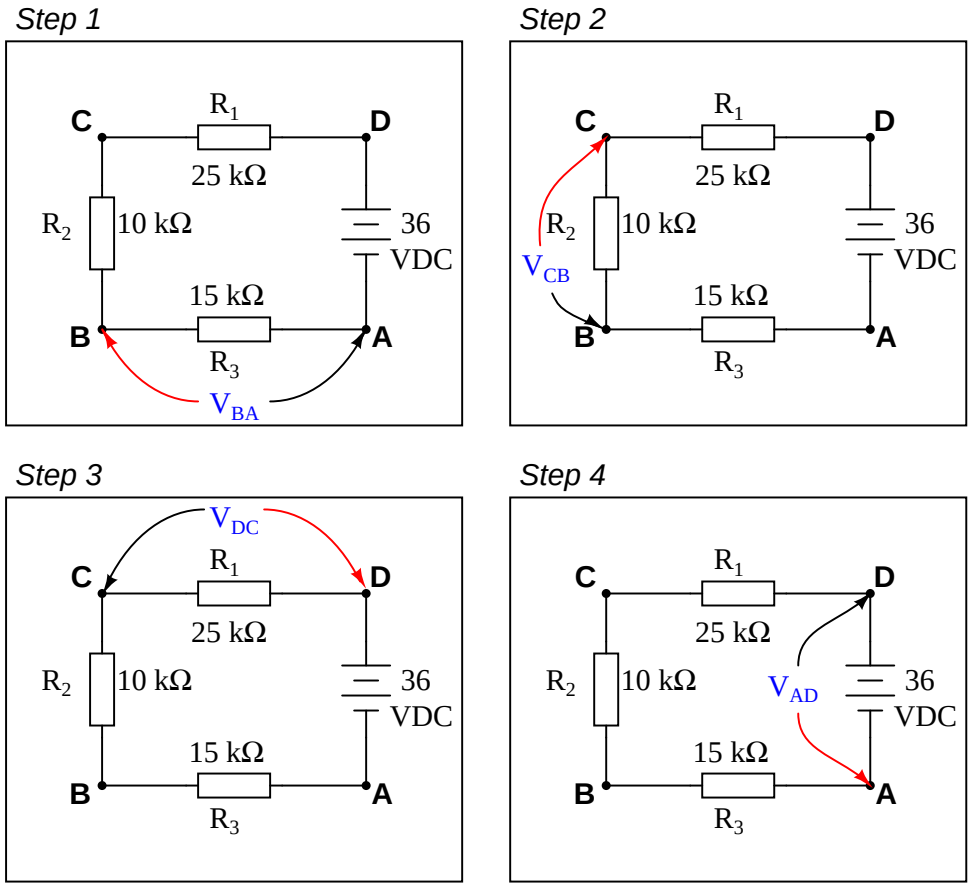
V_{BC} = _____ (red lead on **B**, black lead on **C**)

V_{CD} = _____ (red lead on **C**, black lead on **D**)

file 02752

Question 79

Imagine you are using a digital voltmeter to measure voltages between pairs of points in a circuit, following the sequence of steps shown in these diagrams:



How much voltage would be registered by the voltmeter in each of the steps? Be sure to include the sign of the DC voltage measured (note the coloring of the voltmeter leads, with the red lead always on the first point denoted in the subscript: V_{BA} = red lead on "B" and black lead on "A"):

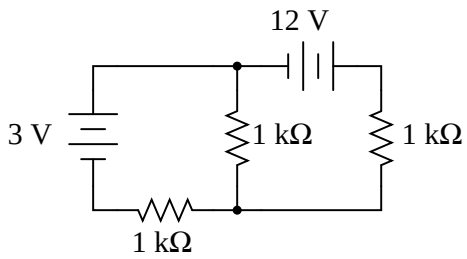
- V_{BA} =
- V_{CB} =
- V_{DC} =
- V_{AD} =

What is the algebraic sum of these voltages?

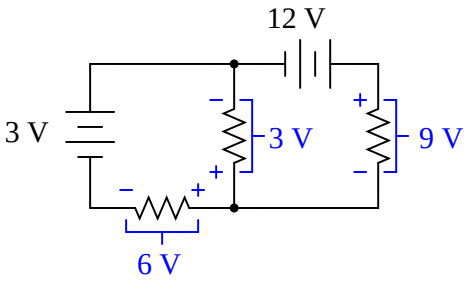
file 00345

Question 80

Note that this circuit is impossible to reduce by regular series-parallel analysis:



However, the Superposition Theorem makes it almost trivial to calculate all the voltage drops and currents:

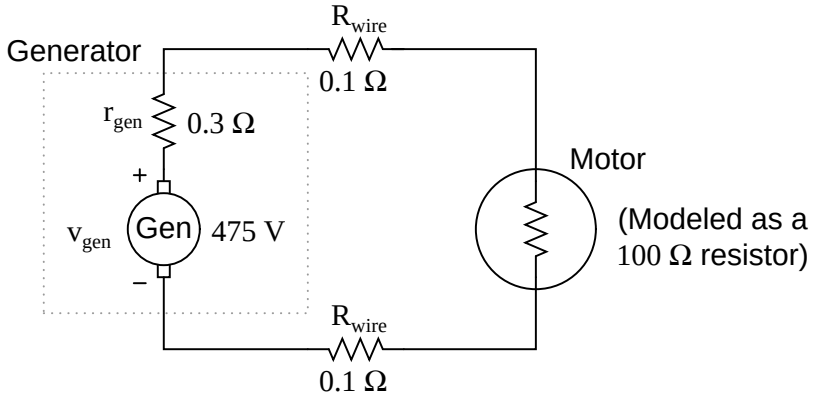


(Currents not shown for simplicity)

Explain the procedure for applying the Superposition Theorem to this circuit.
file 01855

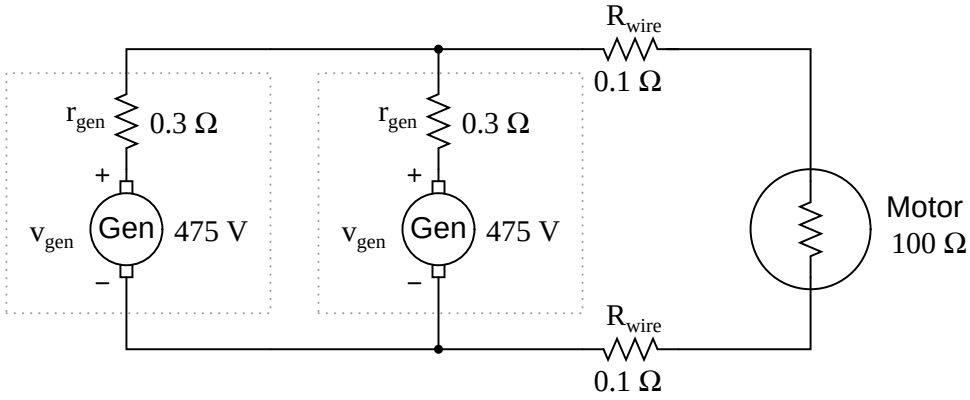
Question 81

Suppose a DC generator is powering an electric motor, which we model as a 100 Ω resistor:



Calculate the amount of current this generator will supply to the motor and the voltage measured across the motor's terminals, taking into account all the resistances shown (generator internal resistance r_{gen}, wiring resistances R_{wire}, and the motor's equivalent resistance).

Now suppose we connect an identical generator in parallel with the first, using connecting wire so short that we may safely discount its additional resistance:

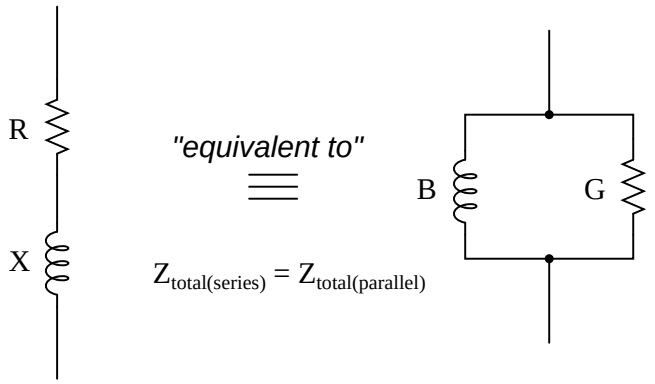


Use the Superposition Theorem to re-calculate the motor current and motor terminal voltage, commenting on how these figures compare with the first calculation (using only one generator).

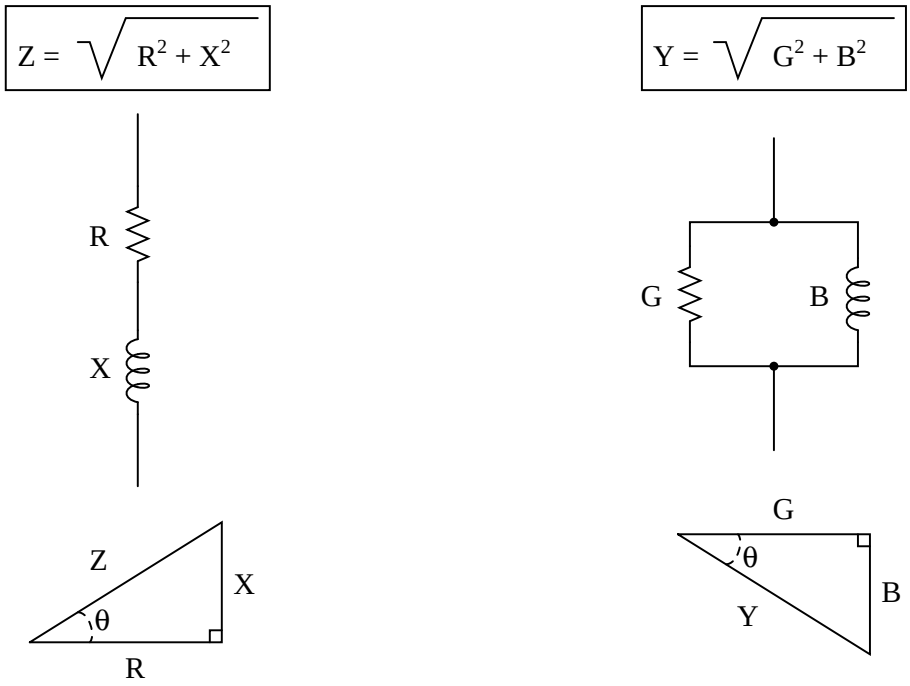
file 03130

Question 82

It is often useful in AC circuit analysis to be able to convert a series combination of resistance and reactance into an equivalent parallel combination of conductance and susceptance, or visa-versa:



We know that resistance (R), reactance (X), and impedance (Z), as scalar quantities, relate to one another trigonometrically in a series circuit. We also know that conductance (G), susceptance (B), and admittance (Y), as scalar quantities, relate to one another trigonometrically in a parallel circuit:



If these two circuits are truly equivalent to one another, having the same total impedance, then their representative triangles should be geometrically similar (identical angles, same proportions of side lengths). With equal proportions, $\frac{R}{Z}$ in the series circuit triangle should be the same ratio as $\frac{G}{Y}$ in the parallel circuit triangle, that is $\frac{R}{Z} = \frac{G}{Y}$.

Building on this proportionality, prove the following equation to be true:

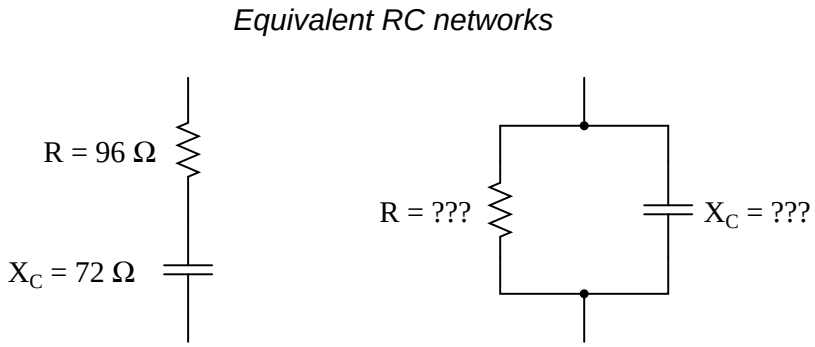
$$R_{series} R_{parallel} = {Z_{total}}^2$$

After this, derive a similar equation relating the series and parallel reactances (X_{series} and $X_{parallel}$) with total impedance (Z_{total}).

file 00856

Question 83

Determine an equivalent *parallel* RC network for the series RC network shown on the left:

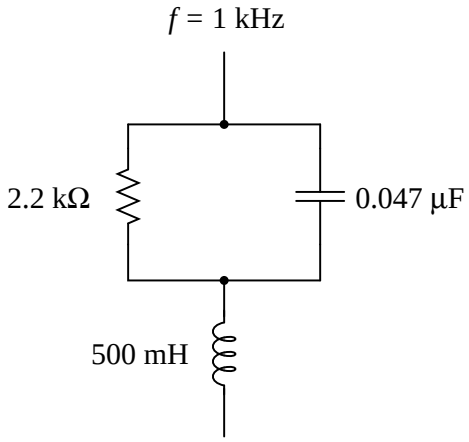


Note that I have already provided a value for the capacitor's reactance (X_C), which of course will be valid only for a particular frequency. Determine what values of resistance (R) and reactance (X_C) in the parallel network will yield the exact same total impedance (Z_T) at the same signal frequency.

file 01540

Question 84

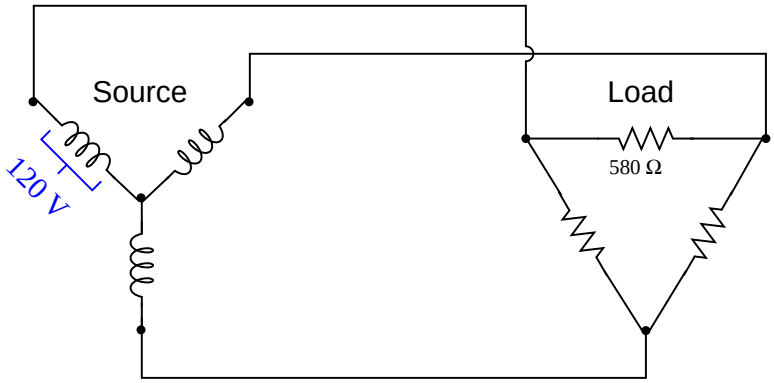
Determine the total impedance of this series-parallel network by first converting it into an equivalent network that is either all-series or all-parallel:



file 01864

Question 85

Calculate all voltages, currents, and total power in this balanced Y-Delta system:

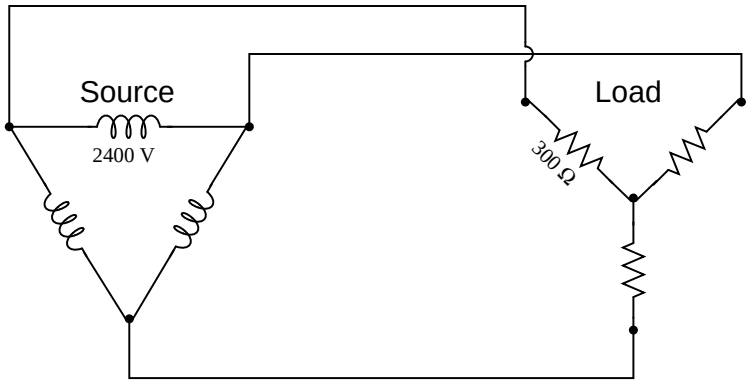


E_{line} =
I_{line} =
$E_{phase(source)}$ =
$I_{phase(source)}$ =
$E_{phase(load)}$ =
$I_{phase(load)}$ =
P_{total} =

file 02204

Question 86

Calculate all voltages, currents, and total power in this balanced Delta-Y system:

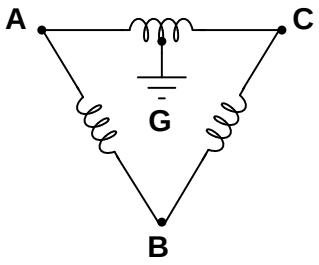


E_{line} =
I_{line} =
$E_{phase(source)}$ =
$I_{phase(source)}$ =
$E_{phase(load)}$ =
$I_{phase(load)}$ =
P_{total} =

file 00428

Question 87

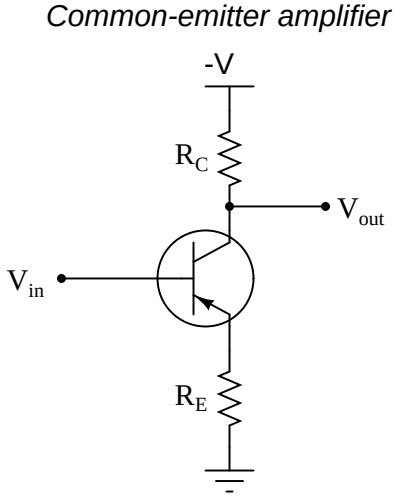
This Delta-connected three-phase power source provides three different voltage levels: 120 V, 208 V, and 240 V. Determine which points of connection provide these voltages:



file 01058

Question 88

The following schematic diagram shows a simple *common-emitter* transistor amplifier circuit:



Explain why the voltage gain (A_V) of such an amplifier is approximately $\frac{R_C}{R_E}$, using any or all of these general "rules" of transistor behavior:

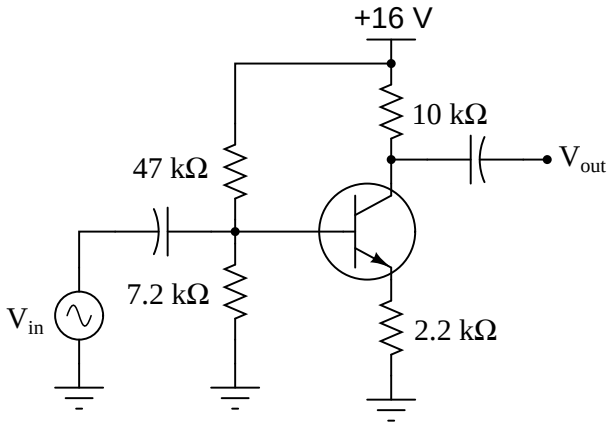
- $I_E = I_C + I_B$
- $I_E \approx I_C$
- $V_{BE} \approx 0.7$ volts
- $\beta = \frac{I_C}{I_B}$

Remember that (AC) voltage gain is defined as $\frac{\Delta V_{out}}{\Delta V_{in}}$. Hint: this question might be easier to answer if you first consider how to explain the unity-gain of a common-collector amplifier circuit (simply eliminate R_C, replacing it with a direct connection to $-V$, and consider V_E to be the output voltage).

file 01524

Question 89

Calculate the approximate voltage gain (A_V) for the following common-emitter amplifier circuit, and also calculate the quiescent DC voltages measured at the three terminals of the transistor with respect to ground (V_B, V_E, and V_C). Assume a silicon transistor:

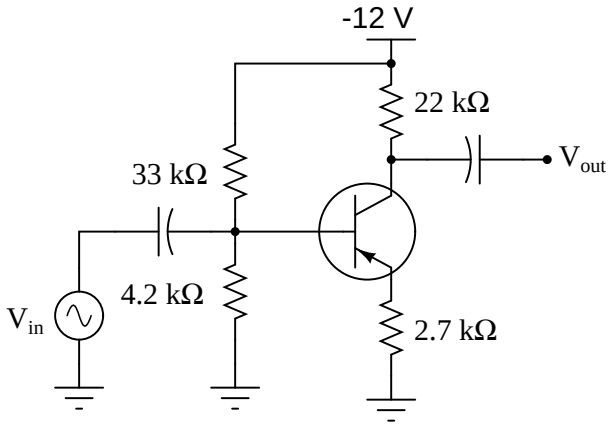


- $A_V \approx$
- $V_B \approx$
- $V_E \approx$
- $V_C \approx$

file 02442

Question 90

Calculate the approximate voltage gain (A_V) for the following common-emitter amplifier circuit, expressing it both as a ratio and as a figure in decibels. Also calculate the quiescent DC voltages measured at the three terminals of the transistor with respect to ground (V_B, V_E, and V_C). Assume a silicon transistor:

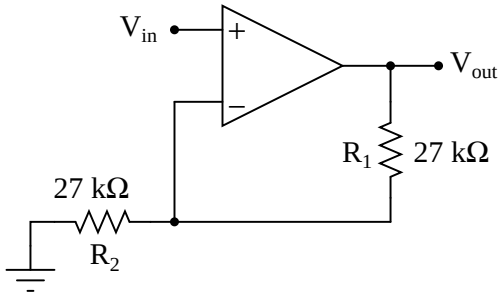


- A_V (as a ratio) $\approx$
- A_V (in decibels) $\approx$
- $V_B \approx$
- $V_E \approx$
- $V_C \approx$

file 02450

Question 91

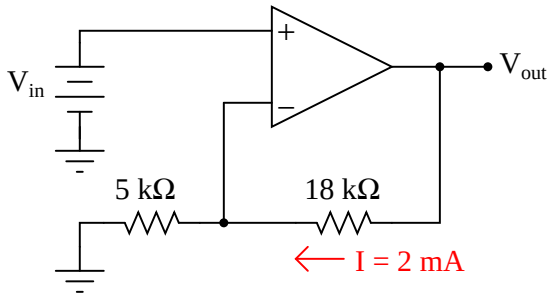
Calculate the overall voltage gain of this amplifier circuit (A_V), both as a ratio and as a figure in units of decibels (dB). Also, write a general equation for calculating the voltage gain of such an amplifier, given the resistor values of R_1 and R_2:



file 02457

Question 92

Determine both the input and output voltage in this circuit:



file 02726

Question 93

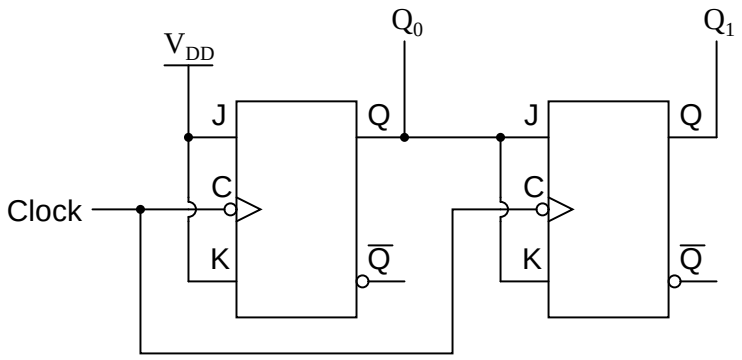
Explain the difference between a *synchronous* counter and an *asynchronous* counter circuit.
file 04048

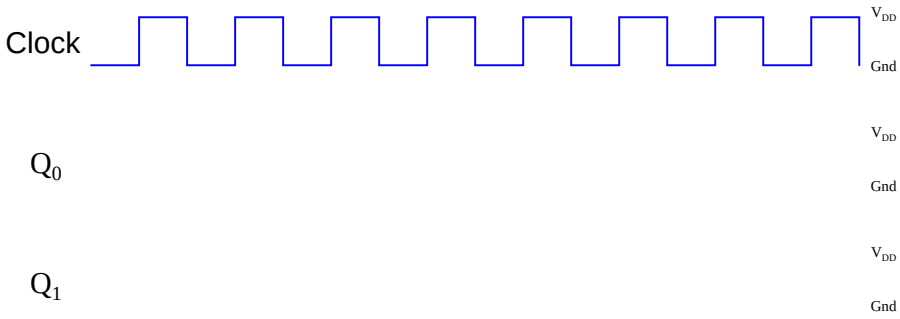
Question 94

Draw the schematic diagram for a four-bit binary "up" counter circuit, using J-K flip-flops.
file 01375

Question 95

Complete a timing diagram for this circuit, and determine its direction of count, and also whether it is a *synchronous* counter or an *asynchronous* counter:

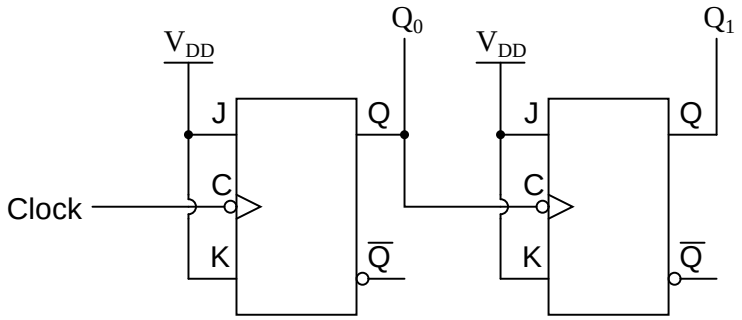


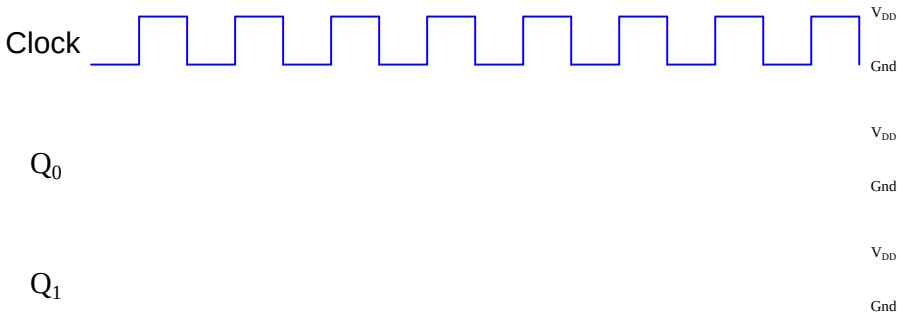


file 04050

Question 96

Complete a timing diagram for this circuit, and determine its direction of count, and also whether it is a *synchronous* counter or an *asynchronous* counter:

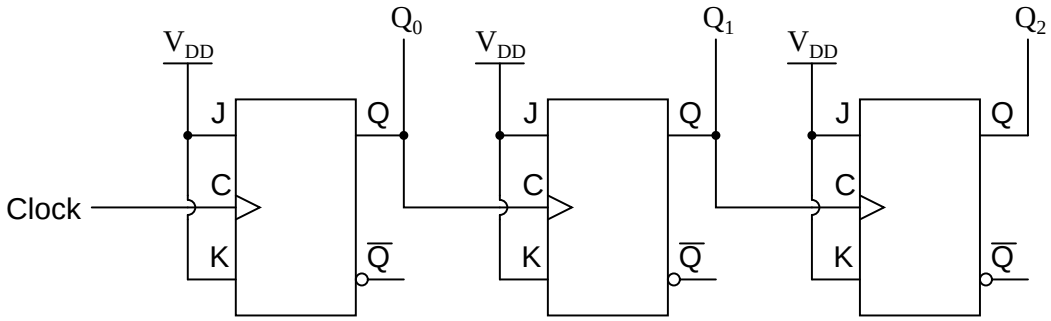


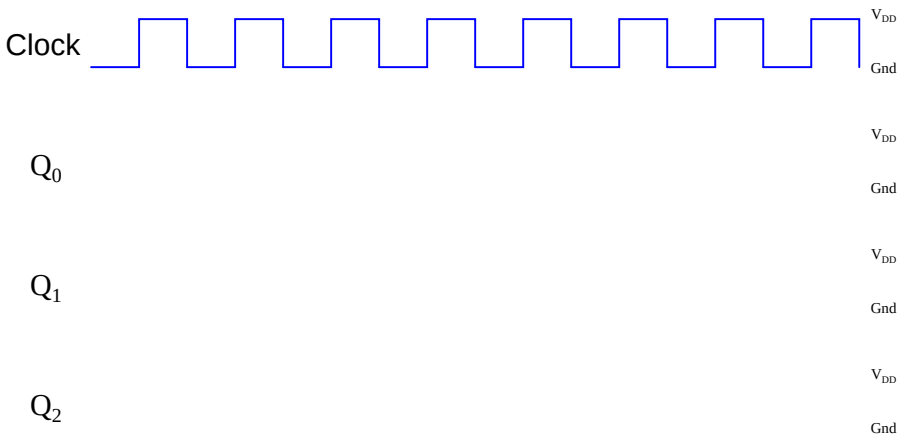


file 04051

Question 97

Complete a timing diagram for this circuit, and determine its direction of count, and also whether it is a *synchronous* counter or an *asynchronous* counter:

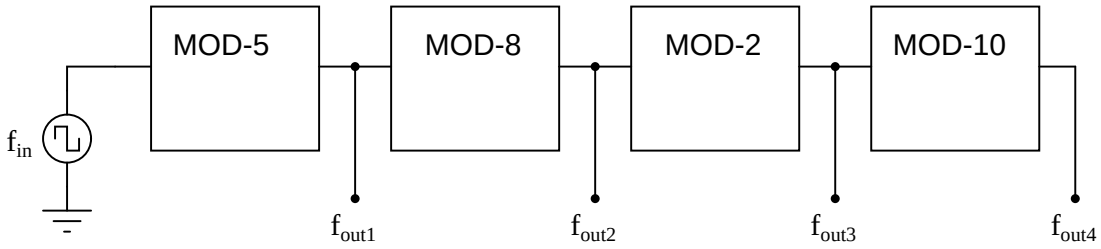




file 04052

Question 98

When counters are used as frequency dividers, they are often drawn as simple boxes with one input and one output each, like this:



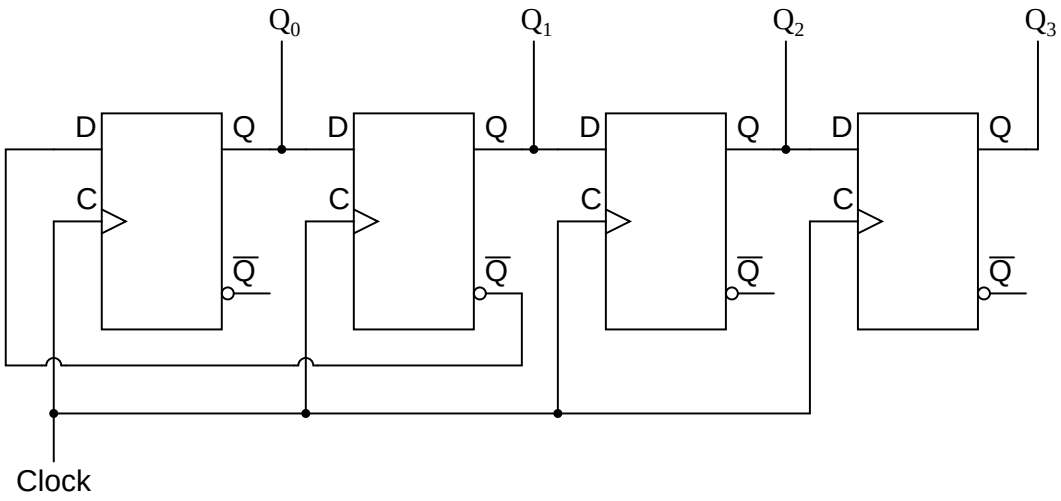
Calculate the four output frequencies (f_{out1} through f_{out4}) given an input frequency of 25 kHz:

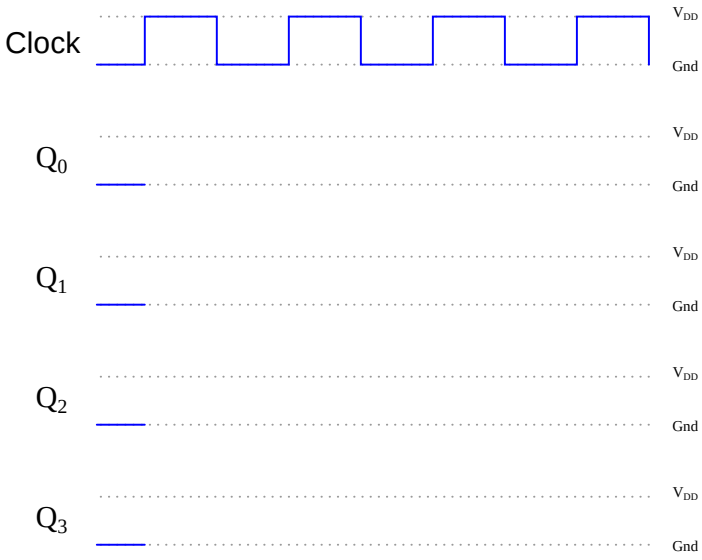
- f_{out1} =
- f_{out2} =
- f_{out3} =
- f_{out4} =

file 03073

Question 99

Complete the timing diagram for this circuit, showing propagation delays for all flip-flops (delay times much less than the width of a clock pulse), assuming all Q outputs begin in the low state:





file 02988

Question 100

Draw the schematic diagram for a five-bit serial-in/serial-out shift register circuit, and be prepared to give a brief explanation of how it functions.

file 01467

Question 101

A binary number is parallel-loaded into a shift register. The shift register is then commanded to "shift right" for one clock pulse. How does the value of the shifted binary number compare to the number originally loaded in, assuming that the MSB is on the very left flip-flop of the shift register?

file 01474

Question 102

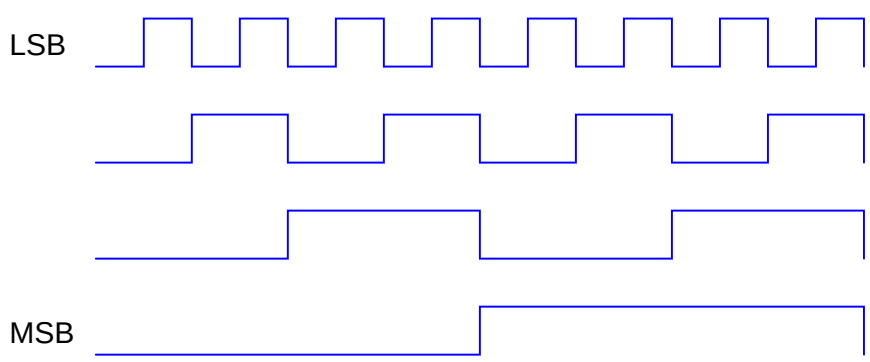
Suppose an automobile manufacturer was designing a new car engine design, and they needed a memory chip to store *look-up tables* for the engine's control computer, holding data such as optimum fuel/air ratios for different engine loads which the computer would then consult to maintain best performance, or economy, or emissions. What type of memory chip would you recommend for the task, and why? Choose from the following list:

- Static RAM (SRAM)
- Mask ROM
- PROM
- Dynamic RAM (DRAM)
- EPROM
- Magnetic core

file 04049

Answers

Answer 1



Answer 2

This counter circuit counts in the *down* direction. I'll let you figure out how to alter its direction of count!

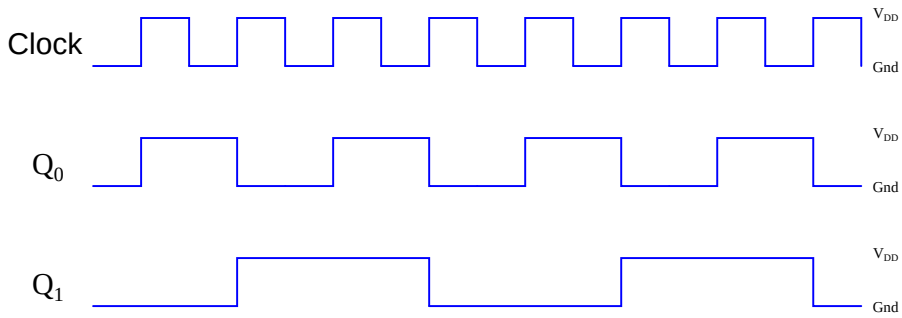
Answer 3

When these counters increment or decrement, they do so in such a way that the respective output bits change state in rapid sequence ("rippling") rather than all at the same time. This creates false count outputs for very brief moments of time.

Whether or not this constitutes a problem in a digital circuit depends on the circuit's tolerance of false counts. In many circuits, there are ways to avoid this problem without resorting to a re-design of the counter.

Answer 4

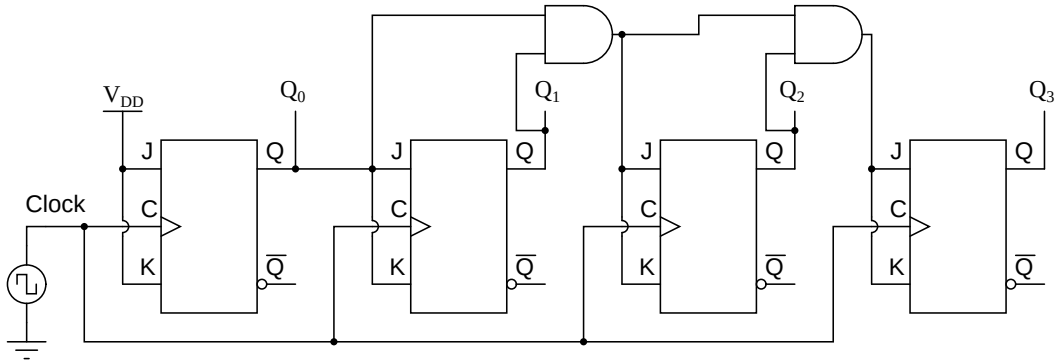
The timing diagram shown here is ideal, with no propagation delays shown:



However, even with propagation delays included (equal delays for each flip-flop), you should find there is still no "ripple" effect in the output count.

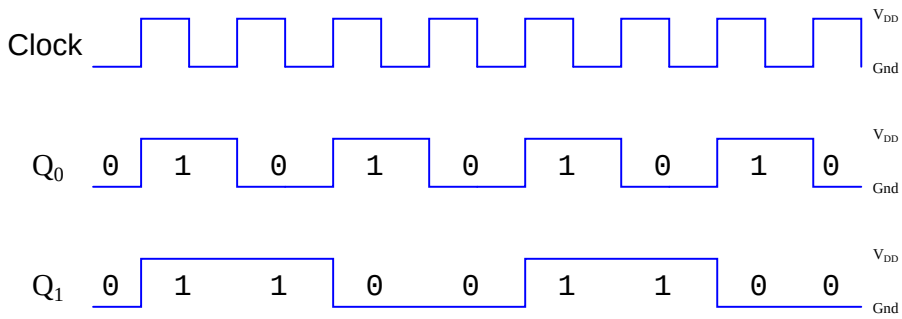
Answer 5

The errant count sequence is as such, with only eight unique states (there should be sixteen!): 0000, 0001, 0010, 0111, 1000, 1001, 1010, and 1111. A corrected up-counter circuit would look like this:



Answer 6

This circuit counts *down*:



Answer 7

The "extra" AND gates allow higher-level bits to toggle if and only if *all* preceding bits are high.

Answer 8

The counter would not be able to count in the "up" direction. When commanded to count that direction, the LSB would toggle between 0 and 1, but the MSB would not change state.

Answer 9

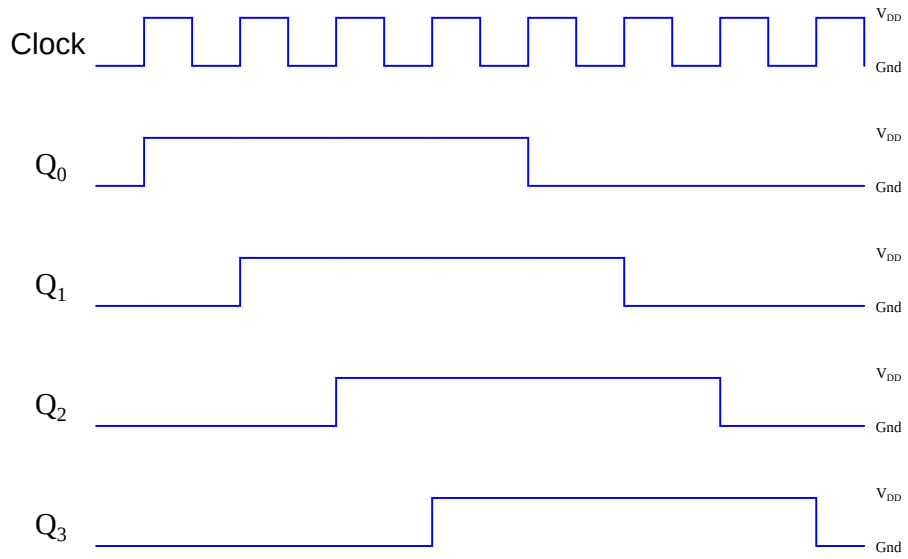
Now, we are able to force the counter to zero (0000) or full count (1111) at will.

Answer 10

- P_0, P_1, P_2, and P_3 = parallel load data inputs
- Q_0, Q_1, Q_2, and Q_3 = count outputs
- CP = Clock pulse input
- $\overline{MR}$ = Master reset input
- $\overline{SPE}$ = Synchronous parallel enable input
- PE = Enable input
- TE = Enable input
- TC = Terminal count output (sometimes called *ripple carry output*, or RCO)

Follow-up question: both the reset ($\overline{MR}$) and preset ($\overline{SPE}$) inputs are synchronous for this particular counter circuit. Explain the significance of this fact in regard to how we use this IC.

Answer 11



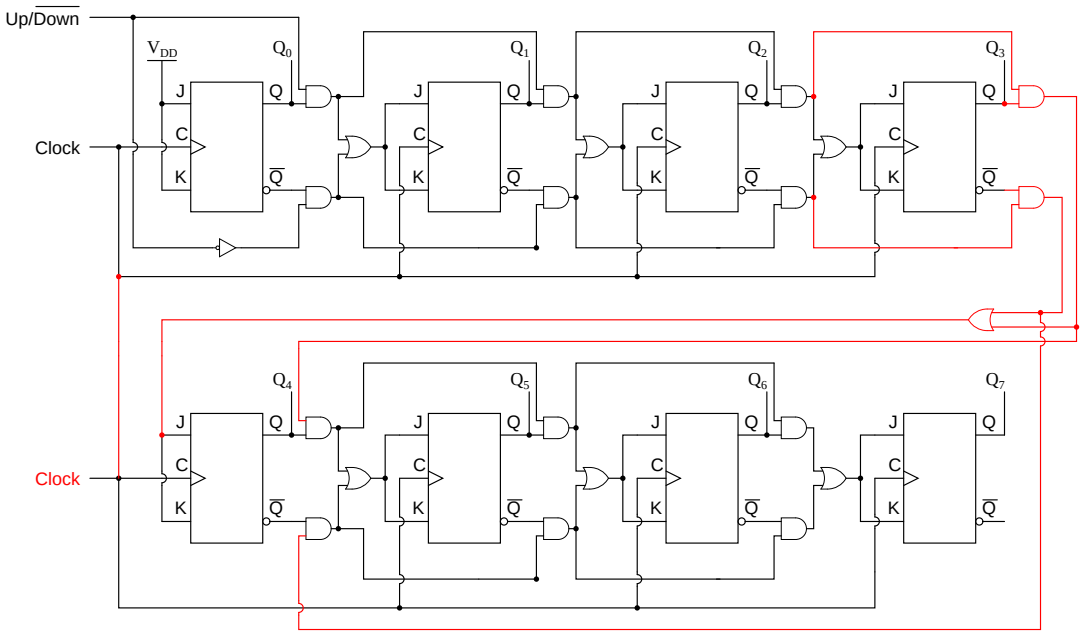
Follow-up question: if used as a frequency divider, what is the input:output ratio of this circuit? How difficult would it be to design a Johnson counter with a different division ratio?

Answer 12

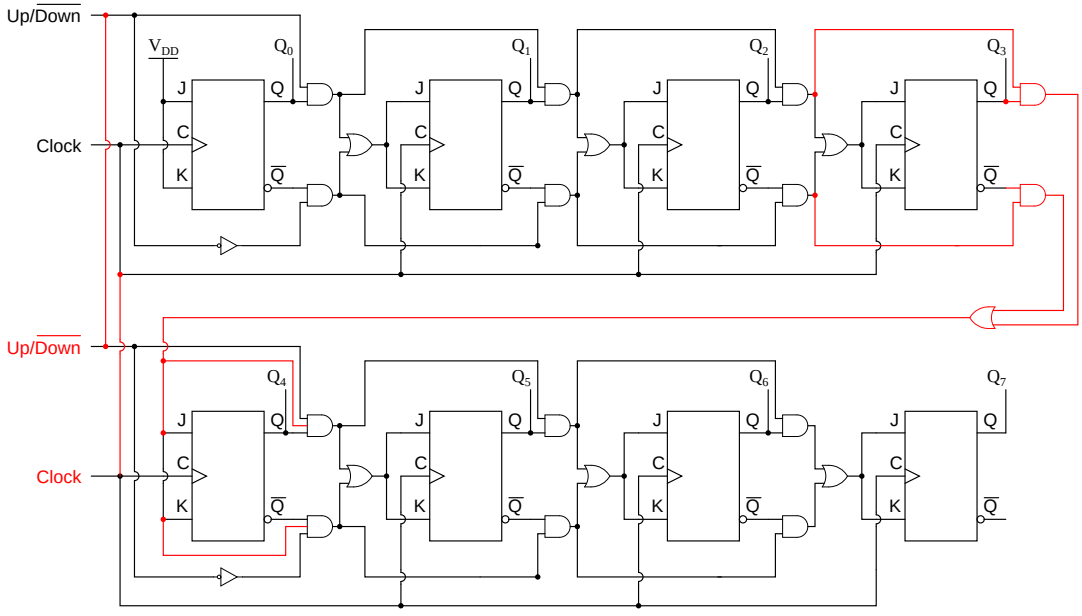
Johnson counters provide a divide-by-n frequency reduction. The second counter circuit shown has the ability to select different values for n.

Answer 13

This first solution requires some elimination of wires and one gate from the front end of the second counter . . .

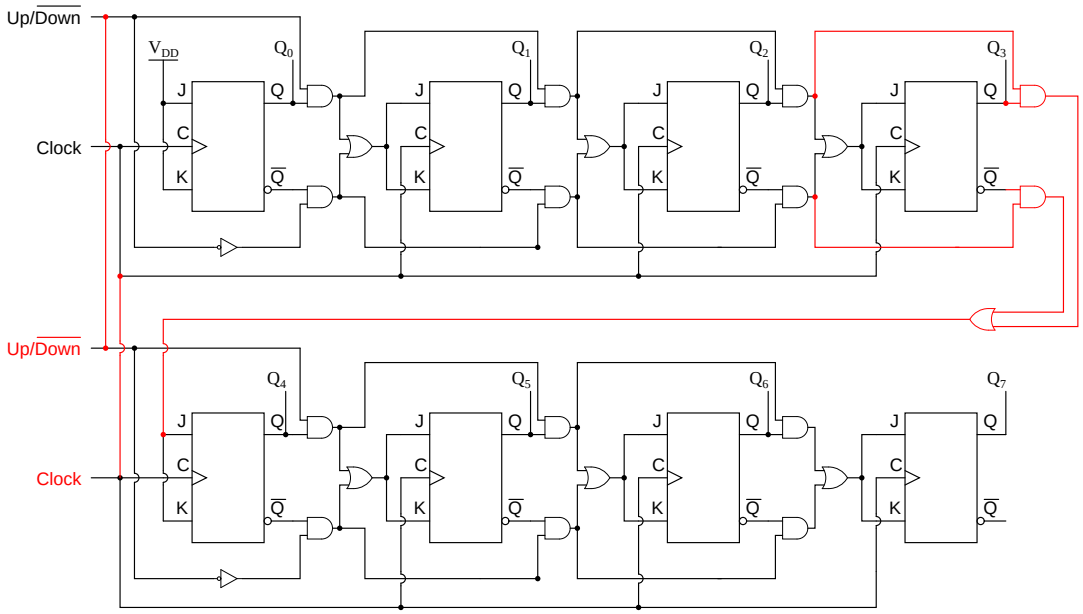


. . . while this solution does only requires different AND gates (3-input instead of 2-input) on the first flip-flop stage of the second counter:



I'll let you decide how you might wish to package your four-bit counter circuits, so as to allow easy cascading. This will be an excellent topic for classroom discussion!

Follow-up question: why isn't the following circuit an acceptable solution?



Answer 14

The first circuit shows two four-bit counters cascaded together in a *ripple* fashion. The second circuit shows the same two four-bit counters cascaded in a *synchronous* fashion. In both cases, Q_0 of the left counter is the LSB and Q_3 of the right counter is the MSB.

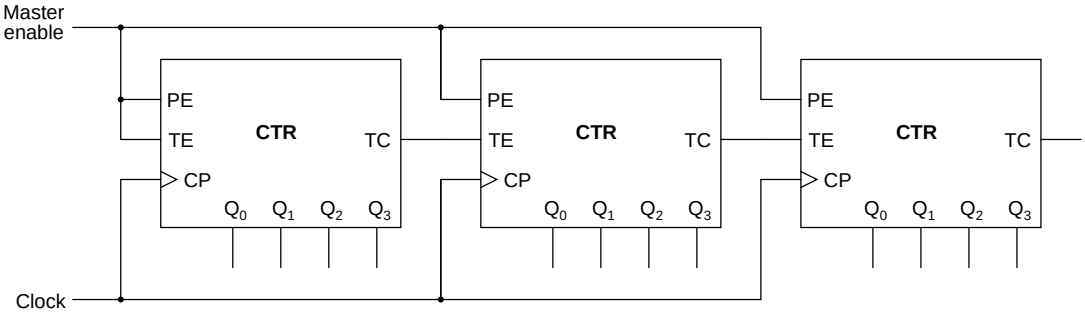
Follow-up question: comment on which method of cascading is preferred for this type of counter IC. Is the functional difference between the two circuits significant enough to warrant concern?

Answer 15

The "fix" for this problem is to enable the last (most significant) four-bit counter only when the terminal count (TC) outputs of *both* preceding counter circuits are active. I will let you figure out the details of this solution for yourself.

Answer 16

The "TE" input not only enables the count sequence, but it also enables the "terminal count" (TC) output which is used to cascade additional counter stages. This way, multiple synchronous counter stages may be connected together as simply as this:



Answer 17

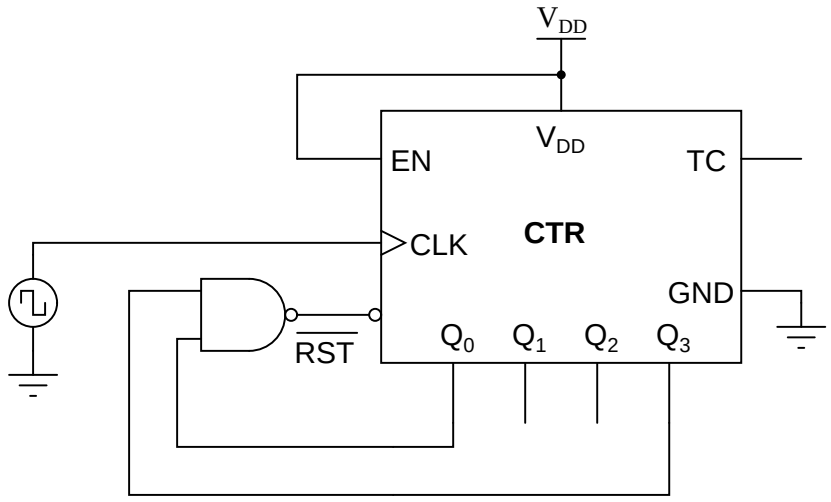
Four bit counter modulus = 16.

Eight bit counter modulus = 256.

Follow-up question: is it possible for a four-bit counter to have a modulus equal to some value other than 16? Give an example!

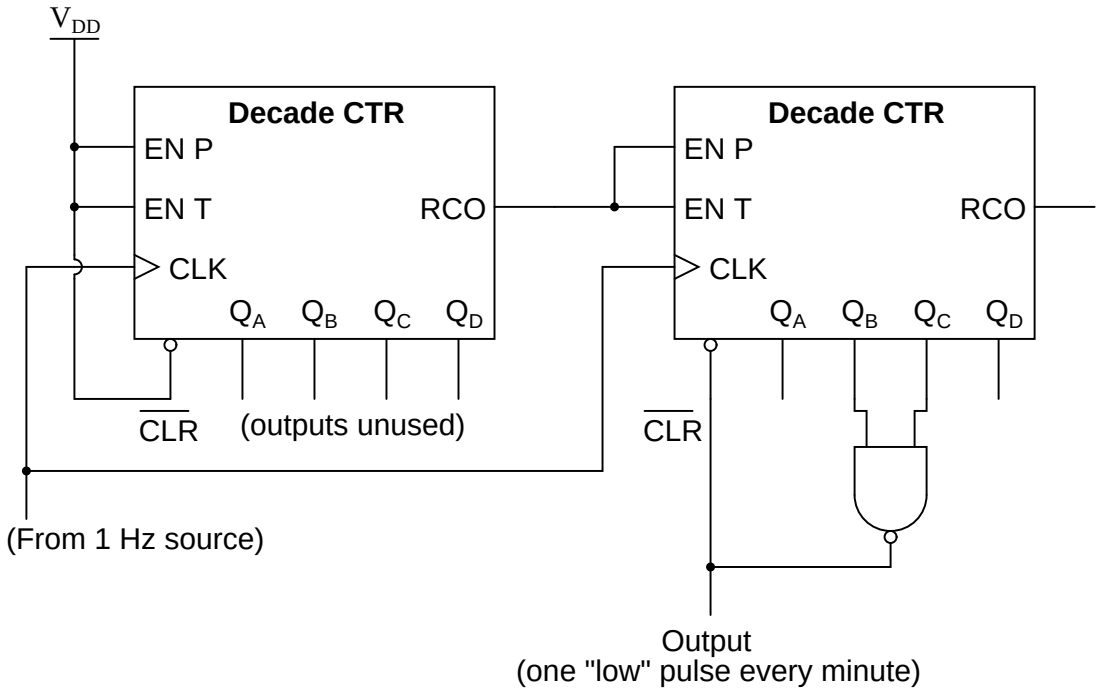
Answer 18

A timing diagram is probably the best way to answer this question! As for the synchronous-reset BCD counter circuit, the only change necessary is a simple wire move (from output Q_1 to Q_0):



Answer 19

Cascade two decade counters together, with a NAND gate to decode when the output is equal to 60:



Follow-up question: why can't we take the divide-by-60 pulse from the RCO output of the second counter, as we could with the divide-by-10 pulse from the first counter?

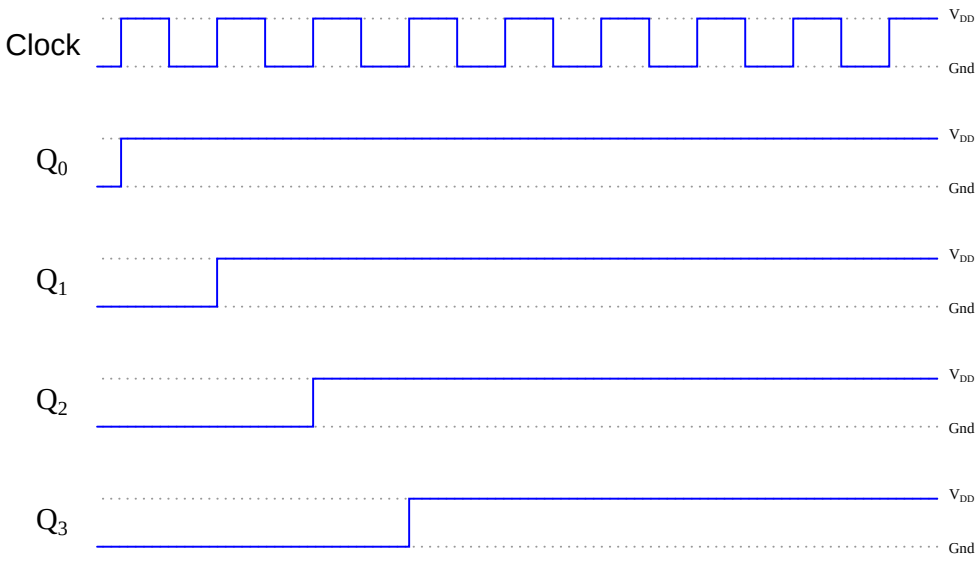
Challenge question: re-design this circuit so that the output is a square wave with a duty cycle of 50% ("high" for 30 seconds, then "low" for 30 seconds), rather than a narrow pulse every 60 seconds.

Answer 20

- $f_{out1} = 150$ Hz
- $f_{out2} = 25$ Hz
- $f_{out3} = 12.5$ Hz
- $f_{out4} = 2.5$ Hz

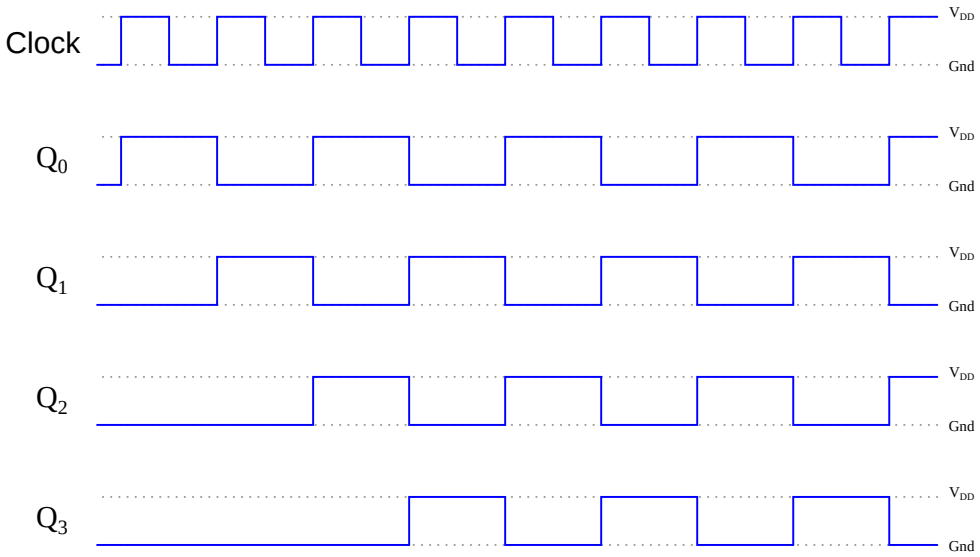
Follow-up question: if the clock frequency for this divider circuit is *exactly* 1.5 kHz, is it possible for the divided frequencies to vary from what is predicted by the modulus values (150 Hz, 25 Hz, 12.5 Hz, and 2.5 Hz)? Explain why or why not.

Answer 21



Follow-up question: explain why the "high" state at the D input of the first flip-flop does not ripple through *all* the flip-flops at the first clock pulse.

Answer 22



Answer 23

A "register" is a collection of flip-flops or latches used to store a binary number (several bits). In essence, it is a one-word *memory circuit*. A "shift register" does the same thing as a register, except that it also has the ability to *move* that binary word from one place to another.

Answer 24

Serial data is transmitted along one line, one bit at a time; *parallel* data is transmitted all at once.

Answer 25

This is a *serial-in, parallel-out* shift register analogy, with each box arriving on the conveyor belt one at a time, but leaving together as a group.

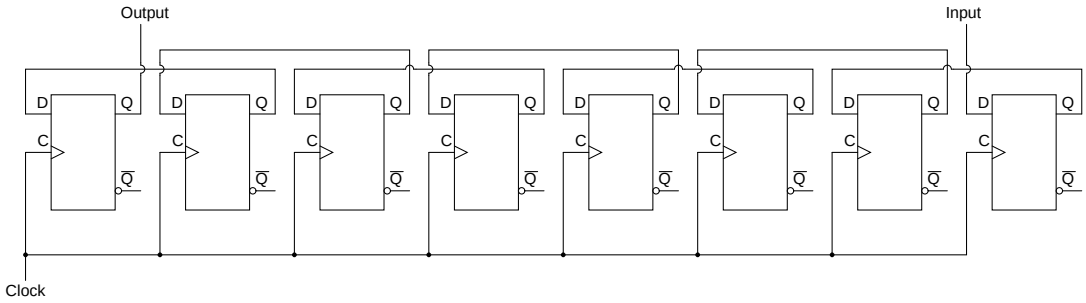
Answer 26

This is a *parallel-in, serial-out* shift register analogy, with each box arriving on the conveyor belt one at a time, but leaving together as a group.

Answer 27

This is a *serial-in, serial-out* shift register analogy, with each box arriving on the conveyor belt one at a time, and leaving one at a time as well.

Answer 28



Answer 29

In order to provide *bidirectional* shift direction ability to a shift register circuit, you will probably have to use *steering gates* to direct the flip-flop outputs to different flip-flop inputs. I'll leave the details for you to research and explain!

Answer 30

A *universal* shift register has the ability to input data in either serial or parallel form, as well as output data in either serial or parallel form.

Note: this answer is purposely minimal. I expect you to provide a more detailed answer during discussion, based on research of universal shift registers!

Answer 31

The "de-bounced" output line will go high only when the switch signal has been continuously high for at least four clock pulses.

Follow-up question #1: which switch (input) transition is seen *immediately* at the output, a low-to-high transition or a high-to-low transition?

Follow-up question #2: does this circuit de-bounce a noisy low-to-high switch (input) transition, a noisy high-to-low switch transition, or both?

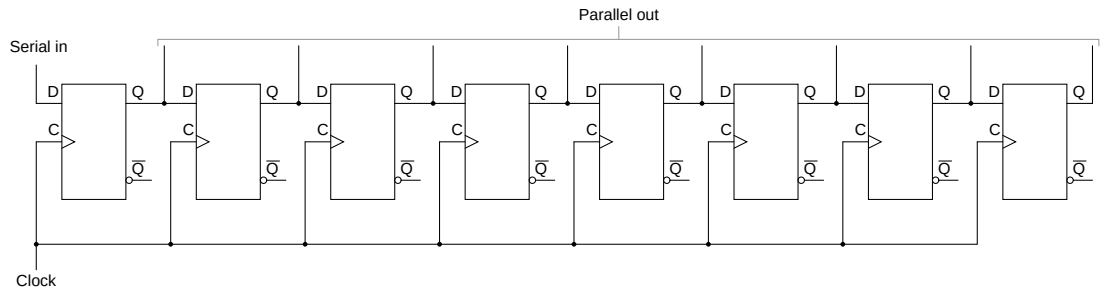
Follow-up question #3: does the pushbutton switch *source* or *sink* current in this circuit?

Challenge question: how would you go about selecting an appropriate clock frequency for this circuit?

Answer 32

Use twelve D-type flip-flops to build a parallel-in/parallel-out shift register.

Answer 33



Follow-up question: if we were to actually use this circuit for serial-to-parallel data conversion, we would have to be careful how fast we clocked the shift register. Explain why.

Answer 34

A high signal on the "select control" line selects Input_A, while a low signal on that same line selects Input_B.

Answer 35

Perhaps the most direct way to provide parallel data entry is to make use of the flip-flops' asynchronous inputs.

Answer 36

I won't give you all the details here, but I will get you started with a few steps:

- De-activate the clock enable (CE) inputs of both shift registers.
- Apply the four desired bits (logic levels) to the D_0 through D_3 inputs of the left-hand shift register.
- Briefly activate the parallel load (PL) input of the left-hand shift register.
- Activate the clock enable (CE) inputs of both shift registers simultaneously for four clock pulses.
- etc.
- etc. . . .

Answer 37

Examples of serial data communication include the 9-pin and/or 25 pin "serial" connectors for RS-232C communication, Ethernet communication, USB ports, and most "mice." Examples of parallel data communication include 25-pin "parallel" connectors to printer and scanner devices, and cables between motherboard and disk drives (legacy IDE technology).

Answer 38

One widespread synchronous data communications standard is SONET, used in long-distance data communication applications. I'll let you do the research to compare and contrast synchronous against asynchronous.

Challenge question: the data sent between computers along serial-format networks such as RS-232C and Ethernet is "clocked" by precise oscillators at both the transmitting and receiving ends, yet is not considered "synchronous," even if each byte of data is sent at regular (non-random) intervals. Explain why.

Answer 39

"UART" stands for *Universal Asynchronous Receiver Transmitter*, and its job is to act as an interface between two parallel-data devices, managing communications in serial format along a communication line of some sort.

Follow-up question: give an example of a UART IC available for purchase today.

Answer 40

- Simplex: one-way communication
- Half-duplex: two-way communication, one way at a time.
- Full-duplex: two-way communication, both ways simultaneously.

Follow-up question: trace all currents in these circuits using conventional flow, and then electron flow.

Answer 41

The answer to why digital recordings retain their quality longer lies in the bivalent nature of digital data, being comprised of either "high" or "low" states, with nothing in between. Consider a sine wave, directly recorded in analog form on magnetic tape, versus a *digitized* representation of a sine wave, recorded as a series of 1's and 0's on the same type of tape. Now introduce some "noise" to each of the signals, and consider the results upon playback.

Answer 42

ROM stands for Read-Only Memory, which means it can only be written to once. *Volatile* and *Nonvolatile* refer to whether or not stored data is lost when the device is powered down.

Technically, *RAM* means Random-Access Memory, where data stored in memory may be accessed without having to "sift through" all the other bits of data in sequential order. In practice, however, the term RAM is used to designate the volatile electronic memory inside a computer, which just happens to be randomly accessible.

Answer 43

- DVD (disk) – *random access*
- Audio tape cassette – *sequential access*
- CD-ROM (disk) – *random access*
- ROM memory chip – *random access*
- Vinyl phonograph record – *random access*
- Video tape cassette – *sequential access*
- Magnetic "hard" drive – *random access*
- Magnetic bubble memory – *sequential access*
- Paper tape (a long strip of tape with holes punched in it) – *sequential access*
- RAM memory chip – *random access*

Be prepared to discuss how each of these recording technologies works, and *why* each one is either random or sequential access.

Answer 44

- ROM: *Read-Only Memory*
- PROM: *Programmable Read-Only Memory*
- EPROM: *Erasable Programmable Read-Only Memory*
- EEPROM: *Electrically Erasable Programmable Read-Only Memory*
- UVEPROM: *UltraViolet Erasable Programmable Read-Only Memory*

Answer 45

Static RAM provides the fastest access, while dynamic RAM provides the greatest amount of memory per physical volume (storage density).

Follow-up question: how is *refreshing* provided for dynamic RAM chips? Is this something taken care of internal to the chip, or must the circuit designer provide external circuitry to refresh the dynamic RAM chip's memory cells?

Answer 46

Flash memories can only be erased or re-programmed in *blocks*, rather than single words at a time. Also, their cycle life is quite a bit less than either SRAM or DRAM technology.

Answer 47

I'll let you research these terms on your own! There are many technical references available on digital memory technology, so finding definitions for "address" and "data" should not be difficult.

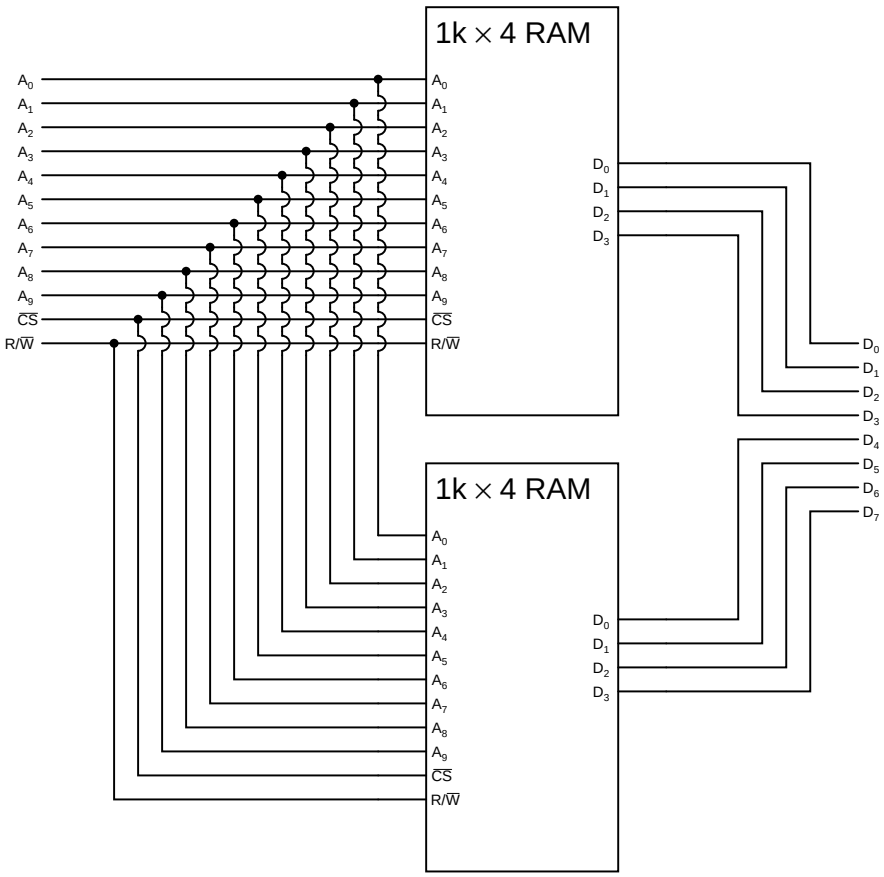
Answer 48

There are 4096 addresses inside this ROM chip, for a total of 32768 bits of data storage. This chip will have twelve address bits and eight data bits.

Answer 49

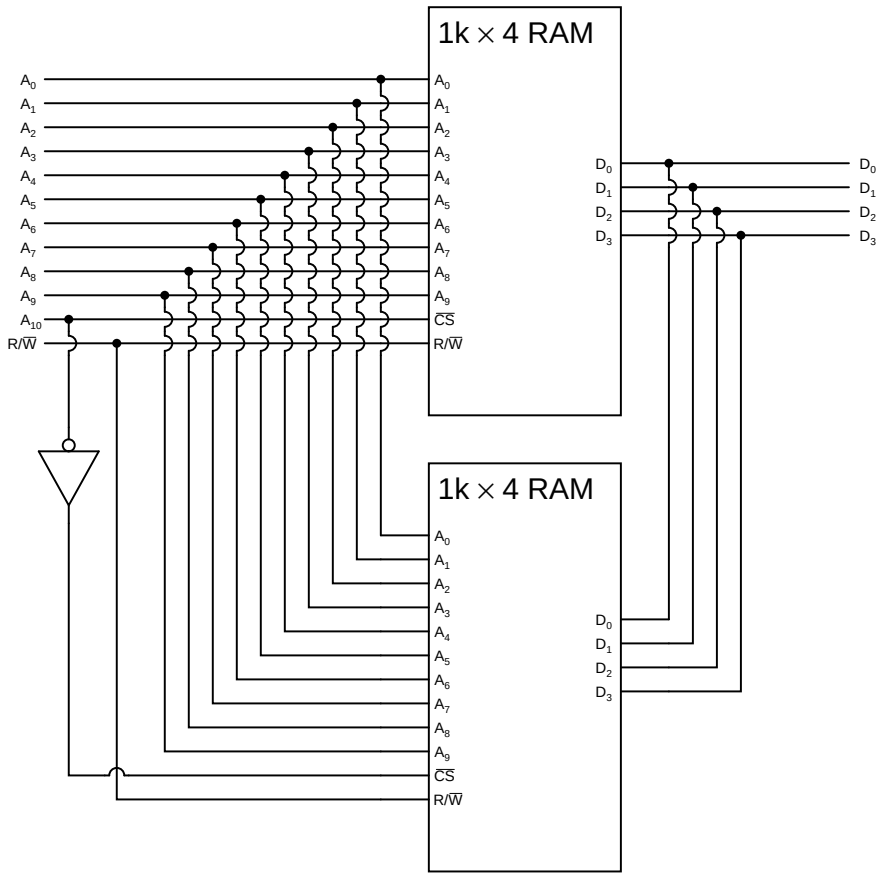
Ideal memory organization: 8k $\times$ 8, thirteen address bits required.

Answer 50



Follow-up question: a common mistake made by students when they "expand" the data bus width of a memory array is to parallel the output lines (in the same way that the address lines are shown paralleled here). Why would this be wrong to do? What might happen to the memory chip(s) if their data lines were paralleled?

Answer 51



Follow-up question: which of the two memory chips shown here stores the first 1024 addresses, and which one stores the next 1024 addresses? How can you tell?

Challenge question: as you can see, the expansion in addresses comes at the expense of losing the ability to simultaneously disable *both* memory chips. Add whatever logic gates are necessary to this circuit to provide a "global" $\overline{CS}$ line for the 2k $\times$ 4 memory array.

Answer 52

With address multiplexing, the address lines going in to the memory chip are used *twice* to select any arbitrary address, bringing in 12 bits worth of the 24-bit address at a time.

Follow-up question: explain how the memory chip "knows" which 12 bits of the address are being read at any given time.

Answer 53

One way to think about checksum is to recall the error-detection strategy of *parity bits*. At root, the two processes are very similar. As for the details of what checksum is and how it is calculated, I leave that for you to research!

Answer 54

A *look-up table* is a set of data programmed into a memory device, used to map a function of some kind: for each unique input (address), there is an output (data) that means something to the system in which it is installed.

An example of a look-up table is an EBCDIC-to-ASCII code converter, where an EBCDIC code input to the address lines of a ROM chip "looks up" the equivalent ASCII character value from memory, and outputs it as the result through the ROM chip's data lines.

Answer 55

These integrated circuits are really just read-only memory chips programmed with *look-up tables* for converting BCD to binary (74LS184) and binary to BCD (74LS185).

Answer 56

Use circuit simulation software to verify your predicted and actual truth tables.

Answer 57

Use circuit simulation software to verify your predicted and actual truth tables.

Answer 58

Use circuit simulation software to verify your predicted and actual truth tables.

Answer 59

Use circuit simulation software to verify your predicted and actual truth tables.

Answer 60

Use circuit simulation software to verify your predicted and measured parameter values.

Answer 61

I do not provide a grading rubric here, but elsewhere.

Answer 62

Be sure to document all steps taken and conclusions made in your troubleshooting!

Answer 63

This is a mistake I see students making all the time. The fact that the circuit is built with CMOS components, and fails whenever an object comes near it, is a strong hint that the problem is related to stray static electric charges. It is an easily corrected problem, caused by the student not taking time to connect *all* the pins of their flip-flops properly.

Answer 64

Two possibilities are immediately apparent: inverter U_5 has a failed-low output, or flip-flop U_1 has a failed-low $\overline{Q}$ output.

Answer 65

The flip-flops' initial states at power-up are essentially random because they are subject to internal *race conditions* between the constituent gates. What is needed is some form of *automatic reset* to force all flip-flops to the reset state at power-up.

Answer 66

- Resistor R_1 fails open: *Counter may not reset at power-up.*
- Resistor R_2 fails open: *Counter will not count, output stuck at* `0000`.
- Resistor R_3 fails open: *Counter will not count, output stuck at* `0000`.
- Capacitor C_1 fails shorted: *Counter will not count, output stuck at* `0000`.

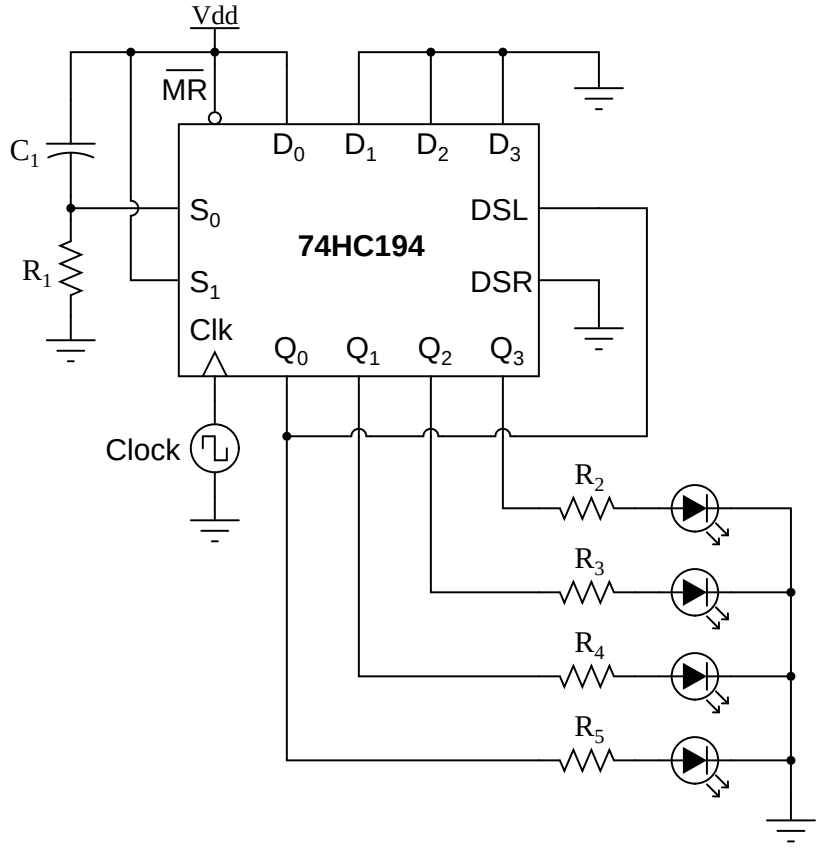
Follow-up question: suggest some reasonable values for the three resistors and the capacitor.

Answer 67

Did you think I was just going to give the answer away here? Consult a datasheet for the 74HC192 to see for yourself!

Answer 68

This will fix the problem:



I will leave it to you to explain *why* this modification works!

Answer 69

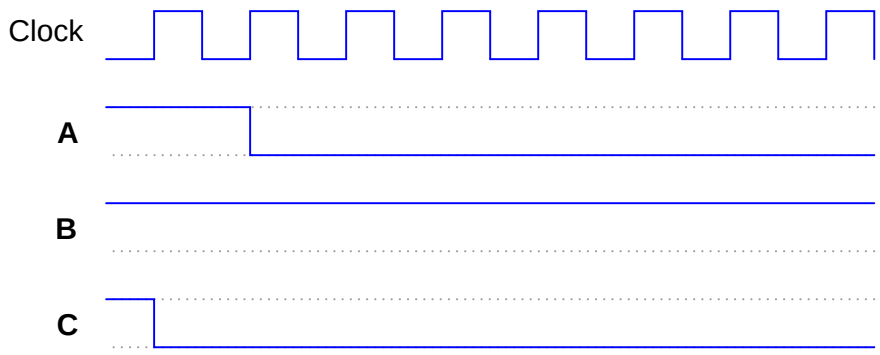
Lack of a clock signal could cause this to happen (check the output of the 555 oscillator with a logic probe or voltmeter). If the upper NOR gate output was failed low, it would also create the problem (check $\overline{MR}$ input of the shift register for a "low" state, and compare with the NOR gate input states).

These are not the only possible failures. Identify a few more on your own!

Answer 70

My first step would be to check for the presence of adequate DC power to both the shift register IC and the motor (transistor drive circuitry). Then, I would use a voltmeter or logic probe to check for pulsing at any one of the shift register's Q outputs. That would tell me whether the problem was with the shift register or with the power circuitry.

Answer 71

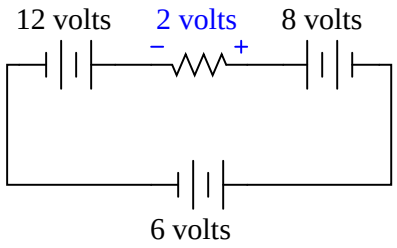


Answer 72

Disconnect the 1 Hz clock pulse generator and re-connect the counter input to a square-wave signal generator of variable frequency. This will speed up the counting sequence and allow you to see what the problem is much faster!

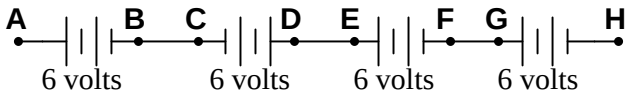
Follow-up question: suppose you did this and found no problem at all. What would you suspect next as a possible source of trouble that could cause the timer circuit to time incorrectly?

Answer 73



Answer 74

Here is a schematic diagram to help you:



- Red lead on A, black lead on H = +12 volts
- Red lead on C, black lead on G = 0 volts
- Red lead on F, black lead on B = 0 volts
- Red lead on F, black lead on A = -6 volts

Answer 75

The voltmeter's black lead is analogous to the "zero reference" level in the mountain-climbing altimeter scenario: the point at which the altimeter is calibrated to register 0 meters height.

Answer 76

V_A = +9 volts
V_B = +6 volts
V_{AB} = +3 volts

Follow-up question: explain why the mathematical signs ("+") are important in these answers.

Answer 77

V_A = +30 volts (red lead on **A**, black lead on ground)

V_B = +3 volts (red lead on **B**, black lead on ground)

V_C = +9 volts (red lead on **C**, black lead on ground)

V_D = -15 volts (red lead on **D**, black lead on ground)

V_{AC} = +21 volts (red lead on **A**, black lead on **C**)

V_{DB} = -18 volts (red lead on **D**, black lead on **B**)

V_{BA} = -27 volts (red lead on **B**, black lead on **A**)

V_{BC} = -6 volts (red lead on **B**, black lead on **C**)

V_{CD} = +24 volts (red lead on **C**, black lead on **D**)

Answer 78

$V_A =$ -21 volts (red lead on **A**, black lead on ground)

$V_B =$ +12 volts (red lead on **B**, black lead on ground)

$V_C =$ -4 volts (red lead on **C**, black lead on ground)

$V_D =$ +9 volts (red lead on **D**, black lead on ground)

$V_{AC} =$ -17 volts (red lead on **A**, black lead on **C**)

$V_{DB} =$ -3 volts (red lead on **D**, black lead on **B**)

$V_{BA} =$ +33 volts (red lead on **B**, black lead on **A**)

$V_{BC} =$ +16 volts (red lead on **B**, black lead on **C**)

$V_{CD} =$ -13 volts (red lead on **C**, black lead on **D**)

Answer 79

- $V_{BA} = +10.8$ volts
- $V_{CB} = +7.2$ volts
- $V_{DC} = +18$ volts
- $V_{AD} = -36$ volts

Answer 80

This is easy enough for you to research on your own!

Answer 81

With only one generator connected:

$I_{motor} = 4.726$ amps $\qquad V_{motor} = 472.6$ volts

With two generators connected:

$I_{motor} = 4.733$ amps $\qquad V_{motor} = 473.3$ volts

Challenge question: how much current does *each* generator supply to the circuit when there are two generators connected in parallel?

Answer 82

I'll let you figure out how to turn $\frac{R}{Z} = \frac{G}{Y}$ into $R_{series}R_{parallel} = {Z_{total}}^2$ on your own!

As for the reactance relation equation, here it is:

$$X_{series}X_{parallel} = {Z_{total}}^2$$

Answer 83

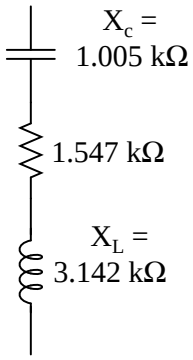
$R = 150\ \Omega$

$X_C = 200\ \Omega$

Follow-up question: explain how you could check your conversion calculations, to ensure both networks are truly equivalent to each other.

Answer 84

Equivalent series resistance and reactances:



$Z_{total} = 2.638$ kΩ

Answer 85

$E_{line} = 207.8$ V
$I_{line} = 0.621$ A
$E_{phase(source)} = 120$ V
$I_{phase(source)} = 0.621$ A
$E_{phase(load)} = 207.8$ V
$I_{phase(load)} = 0.358$ A
$P_{total} = 223.4$ W

Answer 86

$E_{line} = 2400$ V
$I_{line} = 4.619$ A
$E_{phase(source)} = 2400$ V
$I_{phase(source)} = 2.667$ A
$E_{phase(load)} = 1385.6$ V
$I_{phase(load)} = 4.619$ A
$P_{total} = 19.2$ kW

Answer 87

$V_{AB} = V_{BC} = V_{AC} = 240$ volts

$V_{AG} = V_{CG} = 120$ volts

$V_{BG} = 208$ volts

Answer 88

Since V_{BE} is relatively constant, $\Delta V_{in} \approx \Delta V_E$. The next essential step in the explanation for the voltage gain formula is to couple this fact with $I_E \approx I_C$. The rest I'll leave for you to explain.

For your discussion response, be prepared to explain everything in mathematical terms. You will have to use Kirchhoff's Voltage Law at least once to be able to do this completely.

Answer 89

- $A_V \approx 4.55$
- $V_B \approx 2.125$ volts
- $V_E \approx 1.425$ volts
- $V_C \approx 9.521$ volts

Answer 90

- A_V (as a ratio) ≈ 8.148
- A_V (in decibels) ≈ 18.22 dB
- $V_B \approx$ -1.355 volts
- $V_E \approx$ -0.655 volts
- $V_C \approx$ -6.664 volts

Answer 91

$A_V = 2 = 6.02$ dB

$$A_V = \frac{R_1}{R_2} + 1 \qquad \text{(expressed as a ratio, not dB)}$$

Follow-up question: explain how you could modify this particular circuit to have a voltage gain (ratio) of 3 instead of 2.

Answer 92

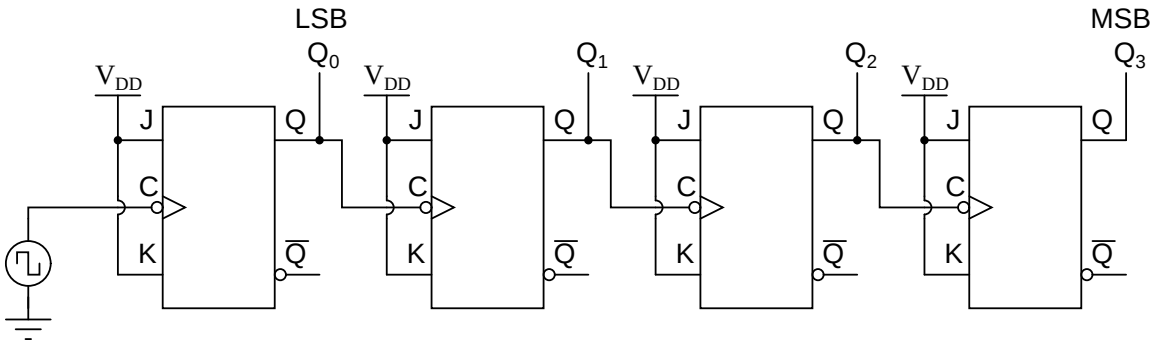
$V_{in} = 10$ V $\qquad$ $V_{out} = 46$ V

Answer 93

A "synchronous" counter circuit's flip-flops are clocked simultaneously, while each of the "asynchronous" counter circuit's flip-flops is clocked by the output of the preceding flip-flop.

Answer 94

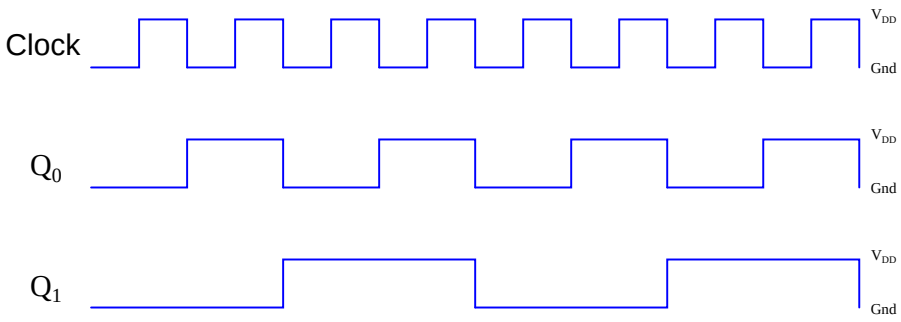
The circuit shown here is not the only valid solution!



Follow-up question: what *other* configuration of J-K flip-flops could be used to make a four bit binary "up" counter?

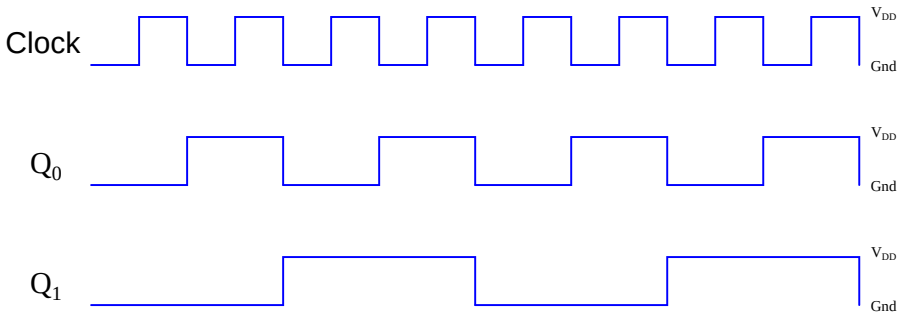
Answer 95

This is a *synchronous* "up" counter.



Answer 96

This is an *asynchronous* "up" counter.



Answer 97

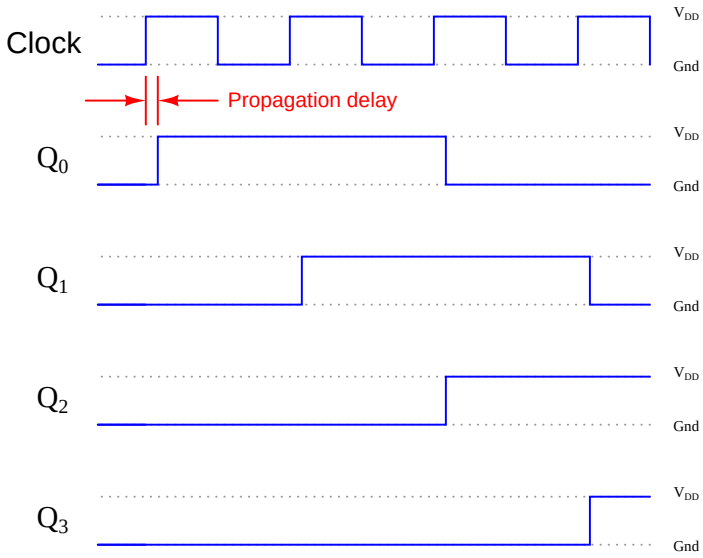
This is an *asynchronous* "down" counter.

Answer 98

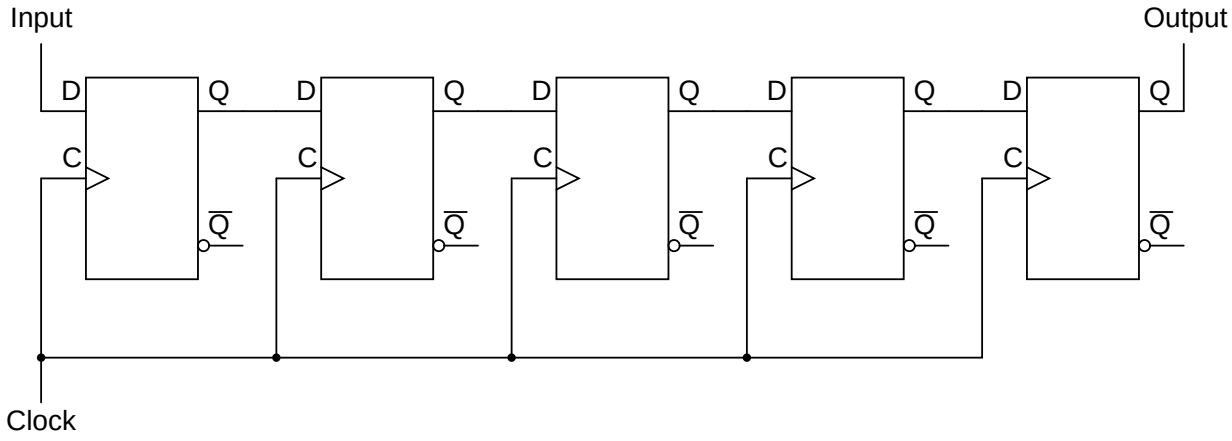
- $f_{out1} = 5$ kHz
- $f_{out2} = 625$ Hz
- $f_{out3} = 312.5$ Hz
- $f_{out4} = 31.25$ Hz

Follow-up question: if the clock frequency for this divider circuit is *exactly* 25 kHz, is it possible for the divided frequencies to vary from what is predicted by the modulus values (5 kHz, 625 Hz, 312.5 Hz, and 31.25 Hz)? Explain why or why not.

Answer 99



Answer 100



Follow-up question: if we wished to output data from this shift register circuit in parallel form, where would we make the connections?

Answer 101

The new binary number value will be one-half (or approximately one-half) the value that it was before.

Follow-up question: how could we use the shift register to *double* the value of a binary number?

Challenge question: when we divide a binary number in two by shifting its bit positions, the resulting answer may or may not be exactly one-half the original value. Explain why this is so. Also, analyze what happens when when we *multiply* a binary number by two through a process of bit-shifting. Is the resulting answer exactly twice the original value, or may it also be *approximate* as it sometimes is with division? Explain why or why not.

Answer 102

EPROM would probably be the best choice. I'll let you discuss this with your classmates and with your instructor, though!

Notes

Notes 1

The purpose of this question is to get students to relate the well-known binary counting sequence to electrical events: in this case, square-wave signals of different frequency.

Notes 2

Actually, the counting sequence may be determined simply by analyzing the flip-flops' actions after the first clock pulse. Writing a whole timing diagram for the count sequence may help some students to understand how the circuit works, but the more insightful students will be able to determine its counting direction without having to draw any timing diagram at all.

Notes 3

If your students have studied binary adder circuits, they should recognize the term "ripple" in a slightly different context. Different circuit, same problem.

Notes 4

"Walk" through the timing diagram given in the answer, and have students explain how the logic states correspond to a two-bit binary counting sequence.

Notes 5

I like to introduce students to synchronous counter circuitry by first having them examine a circuit that doesn't work. After seeing a two-bit synchronous counter circuit, it makes intuitive sense to most people that the same cascaded flip-flop strategy should work for synchronous counters with more bits, but it doesn't. When students understand why the simple scheme doesn't work, they are prepared to understand why the correct scheme does.

Notes 6

Discuss with your students how to relate timing diagrams to binary counts (as shown in the answer).

Notes 7

Although the up/down counter circuit may look overwhelmingly complex at first, it is actually quite simple once students recognize the intent of the AND and OR gates: to "select" either the Q or $\overline{Q}$ signal to control subsequent flip-flops.

Notes 8

The purpose of this question is to get students to understand how a synchronous up/down counter works, in the context of analyzing the effects of a component failure.

Notes 9

Ask your students why this feature might be useful. Can they think of any applications involving a counter circuit where it would be practical to force its output to either zero or full count regardless of the clock's action?

Notes 10

Ultimately, your students will most likely be working with pre-packaged counters more often than counters made up of individual flip-flops. Thus, they need to understand the nomenclature of counters, their common pin functions, etc. If possible, allow for the group presentation of datasheets by having a computer projector available, so students may show the datasheets they've downloaded from the internet to the rest of the class.

Something your students may notice when researching datasheets is how different manufacturers give the same IC pins different names. This may make the interpretation of inputs and outputs on the given symbol more difficult, if the particular datasheet researched by the student does not use the same labels as I do! This is a great illustration of datasheet variability, covered in a way that students are not likely to forget.

Notes 11

Discuss with your students how Johnson counters are quite different from binary-sequence counters, and how this uniqueness allows certain counting functions to be implemented much easier (using fewer gates) than other types of counter circuits.

Notes 12

Strictly speaking, this circuit is a *divide-by-*$2n$ counter, because the frequency division ratio is equal to twice the number of flip-flops.

The final (#5) switch position is interesting, and should be discussed among you and your students.

Notes 13

Figuring out how to cascade the two four-bit counters is the easy part. The challenge is to "think ahead" in designing a four-bit counter with all the necessary connections to make cascading easy for the end-user. Make this the center of discussion on this particular question.

Notes 14

It is important for students to consult the datasheet for the 74HCT163 counter circuit in order to fully understand what is going on in these two cascaded counter circuits.

Notes 15

The "hint" in this question may give away too much, as the problem is *precisely* identical to the problem encountered with overly simplistic synchronous J-K flip-flop cascades. What new students tend to overlook is the necessity to enable successive stages only when *all* preceding stages are at their terminal counts. When you only have two stages (two J-K flip-flops or two IC counters) to deal with, there is only one TC output to be concerned with, and the problem never reveals itself.

Be sure to give your students time and opportunity to present their solutions to this dilemma. Ask them how they arrived at their solutions, whether by textbook, prior example (with J-K flip-flops), or perhaps sheer brain power.

Notes 16

The important lesson in this question is that synchronous counter circuits with more than two stages need to be configured in such a way that *all* higher-order stages are disabled with the terminal count of the lowest-order stage is inactive. This ensures a proper binary count sequence throughout the overall counter circuit's range. Your students should have been introduced to this concept when studying synchronous counter circuits made of individual J-K flip-flops, and it is the same concept here.

Also important here is the realization that some IC counters come equipped with the "look-ahead" feature built in, and students need to know how and why to use this feature.

Notes 17

The real purpose of this question is to get students to find out what term "modulus" means, and how it relates to counter bits.

Notes 18

Although both circuits achieve a BCD count sequence, the synchronous-reset circuit is preferred because it completely avoids spurious ("ripple-like") false outputs when recycling. Be sure to emphasize that the difference between an asynchronous and a synchronous reset function is internal to the IC, and not something the user (you) can change. For an example of two otherwise identical counters with different reset functions, compare the 74HCT161 (asynchronous) and 74HCT163 (synchronous) four-bit binary counters.

Notes 19

Tell your students that counter circuits are quite often used as frequency dividers. Discuss the challenge question with them, letting them propose and discuss multiple solutions to the problem.

The "note" in the question about the asynchronous nature of the counter reset inputs is very important, as synchronous-reset counter ICs would not behave the same. Discuss this with your students, showing them how counters with synchronous reset inputs would yield a divide-by-61 ratio.

Incidentally, a divide-by-60 counter circuit is precisely what we would need to arrive at a 1 Hz pulse waveform from a 60 Hz powerline frequency signal, which is a neat "trick" for obtaining a low-speed clock of relatively good accuracy without requiring a crystal-controlled local oscillator. (Where the "mains" power is 50 Hz instead of 60 Hz, you would need a divide-by-50 counter – I know, I know . . .) If time permits, ask your students to think of how they could condition the 60Hz sine-wave (120 volt!) standard powerline voltage into a 60 Hz square-wave pulse suitable for input into such a frequency divider/counter circuit.

Notes 20

The purpose of this question is to introduce students to the schematic convention of counter/dividers as simple boxes with "MOD" specified for each one, and to provide a bit of quantitative analysis (albeit very simple).

Notes 21

This question reviews the principles of D-type flip-flops, timing diagrams, and serves as an introduction to shift registers.

Notes 22

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Notes 23

Registers are a good way to introduce the basic concepts of solid-state (RAM) memory technology, showing how flip-flop or latch circuits may be used as data storage devices. Be sure to ask your students where they were able to find this information, as it should be very easy for them to research!

Notes 24

Ask your students of they have ever heard of "serial" and "parallel" ports on personal computers. If time permits, have them examine the two types of ports on the back of a PC, contrasting the number of pins used for each connector.

Notes 25

Some analogies can be very helpful to students as they learn new concepts. I have found that conveyor belts work very well to illustrate the different types of shift register behaviors.

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Notes 28

This is a very simple question to answer. I present it here primarily so that students start thinking about how to *change* the direction of shift in a shift register circuit: a prelude to bidirectional shift register circuits.

Notes 29

I purposely avoided asking a question about schematics for a reason: it is too easy to simply look through a textbook or research a datasheet and copy a drawing. What is most important here is that students comprehend *how* bidirectionality is achieved in shift register circuits. What, exactly, is a *steering gate*, why are they used, and what in/out flip-flop connections are needed to achieve a desired shift direction.

Notes 30

Regarding the point in the answer about student research, ask your students how a single shift register chip is able to perform all the different types of input/output combinations. Ask your students, for instance, how to make the 74194 act *only* as a parallel-in/parallel-out register.

Notes 31

Some students may need to see a pulse diagram for this circuit before they fully grasp how it functions. If so, have students come up to the board in the front of the room and work through an analysis of it rather than doing it yourself.

Not only does this question review shift register operation, but it also reviews the problem of switch contact bounce and showcases a practical solution for it. Incidentally, this question provides a good excuse for a hands-on demonstration of switch bounce using the switch/pulldown circuit first shown and a digital storage oscilloscope to capture the switching action. Students are likely to be surprised by just how "dirty" the switch signal is!

Notes 32

This type of shift register is immensely useful for sample-and-hold applications such as this.

Notes 33

The subject of serial-to-parallel data conversion is much deeper than what is suggested by this disarmingly simple circuit. Talk with your students about the need for clock synchronization (even in "asynchronous" serial data transmission).

Notes 34

Selector circuits are widely used internally in counter and shift register circuits where digital signals must be selected from multiple sources to achieve certain functions. Be sure your students understand how it works, for they will surely see it later in some application!

Notes 35

During discussion, have your students draw a picture of a parallel-in/serial-out shift register circuit, or at least cite a page number reference in their textbook, so you may be sure they understand what they're talking about (and not just repeating the given answer).

Notes 36

This question asks students to think their way through the operation of two coupled shift registers to accomplish the task of parallel-to-serial-to-parallel data conversion. Not only is this a good review of shift register operation, but it shows some (not all!) of what happens during the seemingly simple procedure of sending four bits of data in serial form over a cable.

A challenging detail to figure out in this scheme is how to keep both shift registers synchronized so that one receives the serial data bits at the same time the other sends them. There is more than one way to do this, of course, but the easiest would be to connect the two clock inputs together through another cable conductor.

Notes 37

As computer-savvy as most young students are, questions such as these tend to evoke ready responses and strong interest. You may find that little effort is required on your part to introduce these technologies to your students, as they may be more familiar with certain areas and features of it than you!

Notes 38

At first, it seems as though any communication between digital devices occurring at a pre-determined frequency (bps) and rate (characters per second) would be synchronous, because everything is happening on fixed intervals. However, the precision inherent to a true synchronous communications network is more rigorous than this. Let your students elaborate on what they have found through their research.

Notes 39

When students research what a UART is, they will invariably stumble upon terms such as *parity*, *start bit*, and *stop bit*. If they are not yet familiar with the details of asynchronous data communications, this could lead to some enlightening discoveries. Be sure to discuss these terms and details with your students if they bring them up in class, because it means they will be very receptive to your instruction (having been "primed" for learning by *wanting* to know).

Notes 40

I could have just asked for definitions here, but relating these concepts to real circuits, however simple, carries with it more educational benefit. It is also important to show students that the basic concept of digital communication is really no more complex than the old telegraph, just faster.

Notes 41

Challenge students to come up with some *disadvantages* of digital recordings, now that they understand the difference between analog and digital data storage. While digital technology certainly enjoys some advantages over analog, it is not necessarily superior in all aspects!

Notes 42

The mis-use of the acronym "RAM" is another unfortunate entry in the lexicon of electronics. Your students are sure to have questions about this term, so be prepared to discuss it with them!

Notes 43

One of the purposes of this question is to get students to realize that "RAM" memory (solid-state, volatile memory "chips" in a computer) is not the only type of data storage device capable of randomly accessing its contents, and that the term "RAM" as it is commonly used is something of a misnomer.

Notes 44

ROM designations are another set of misnomers that have crept into the electronics lexicon. I mean really, how can anything be both *erasable* and *programmable*, but still be *read-only*?

Notes 45

Ask your students where they obtained their information on static versus dynamic RAM technologies. Extra credit for consulting datasheets!

Notes 46

Discuss with your students some of the different applications of Flash memory technology. Talk about how those applications fit the capabilities (and weaknesses) of Flash technology well.

Notes 47

Analogies are often helpful to communicate the concepts of "address" and "data" to new students. I like to use the example of post office boxes (lots of addressed boxes, each containing different items) when I explain address and data.

Notes 48

Discuss with your students why there are not 4000 (exactly) addresses in a "4k" memory chip.

Notes 49

Be sure to ask your students *how* they calculated 13 bits for the address. Of course, there is the trial-and-error method of trying different powers of two, but there is a much more elegant solution involving logarithms to find the requisite number of bits.

Notes 50

Be sure to spend some time discussing the common mistake referenced in the follow-up question. This is something I've seen more than once, and it reveals a fundamental gap in understanding on the part of the mistaken student. What students are prone to do is try to *memorize* the sequence of connections rather than really understand *why* memory array expansion works, which leads to errors such as this.

Note that the answer to "what might happen" depends on whether the first operation is a *read*, or a *write*.

Notes 51

Be sure to spend some time discussing the follow-up question. Once again, I've noticed students are prone to memorizing the connection pattern rather than take the time to figure out *why* the chips are connected as they are.

Notes 52

Explain to your students that address multiplexing is not technically limited to application in *dynamic* RAM chips only, but that it is usually applied there because of the high address density afforded by dynamic RAM technology. Most static RAMS, by contrast, are not dense enough to require address lines serve double-duty!

Notes 53

Once again, there is little I can reveal in the answer without giving everything away. There are enough resources available for students to learn about checksum on their own, that you should not have to supply additional information.

Notes 54

The EBCDIC-to-ASCII code converter concept is not hypothetical! I actually designed and helped build such a circuit to allow standard personal computers to "talk" to an obsolete CNC machine tool control computer which didn't understand ASCII data, only EBCDIC. A look-up table implemented in a UVEPROM served as a neat way to implement this function, without a lot of complex circuitry.

Notes 55

Discuss with your students why someone would choose to implement these functions in a look-up table instead of using combinational logic or a microprocessor/microcontroller. What advantage(s) might be realized with the look-up table approach?

Notes 56

One lesson of digital circuits many students learn the hard way is the importance of not leaving CMOS inputs floating. In this case, the lesson is often learned in the form of leaving asynchronous inputs of the J-K flip-flops floating (preset, clear, or both). Be sure to check to see that all chip inputs are accounted for before passing students on this competency. If you see an input floating, touch the chip pin with a pen or pencil and let your students see the effect static has on their circuit!

Notes 57

Students are to research the datasheet for their particular IC and figure out from that what connections and timing sequences they need to make the circuit perform as requested. It is very important for students to learn to interpret manufacturers' datasheets!

I recommend a slow clock frequency (1 Hz or so) to allow for easy viewing of the count sequence.

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I recommend a slow clock frequency (1 Hz or so) to allow for easy viewing of the shift patterns. To conserve the number of necessary input switches, I allow students to hard-wire the data inputs (D_0 through D_3). This means they only need switches to control the mode of the shift register (parallel load, shift right, shift left, and shift inhibit).

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Notes 60

I have purposely left the details of the schematic diagram vague, so that students must do a lot of datasheet research on their own to figure out how to make an event counter circuit. You may choose to give your students part numbers for the integrated circuits, or choose not to, depending on how capable your students are. The point is, they must figure out how to make the ICs work based on what they read from the manufacturer.

Something else students will probably have to do is de-bounce the event switch. Some event switches are inherently bounceless, while others are definitely not. Switch debouncing is something your students need to learn about and integrate into this circuit.

An extension of this exercise is to incorporate troubleshooting questions. Whether using this exercise as a performance assessment or simply as a concept-building lab, you might want to follow up your students' results by asking them to predict the consequences of certain circuit faults.

Notes 61

The idea of a troubleshooting log is three-fold. First, it gets students in the habit of documenting their troubleshooting procedure and thought process. This is a valuable habit to get into, as it translates to more efficient (and easier-followed) troubleshooting on the job. Second, it provides a way to document student steps for the assessment process, making your job as an instructor easier. Third, it reinforces the notion that each and every measurement or action should be followed by reflection (conclusion), making the troubleshooting process more efficient.

Notes 62

The purpose of this assessment rubric is to act as a sort of "contract" between you (the instructor) and your student. This way, the expectations are all clearly known in advance, which goes a long way toward disarming problems later when it is time to grade.

Notes 63

I didn't exactly reveal the source of trouble in the answer, but I gave enough hints that anyone familiar with CMOS should be able to tell what it is! This truly is a problem I've seen many times with my students!

Notes 64

Discuss the merit of all faults proposed in answer to this question with your students. Ask them to explain the reasoning behind their answers, and use this as an opportunity to correct conceptual errors about the operation of this circuit.

Notes 65

This is a very practical issue for state-machine circuits: making sure the circuit begins in the desired state rather than in some random condition.

Notes 66

The purpose of this question is to approach the domain of circuit troubleshooting from a perspective of knowing what the fault is, rather than only knowing what the symptoms are. Although this is not necessarily a realistic perspective, it helps students build the foundational knowledge necessary to diagnose a faulted circuit from empirical data. Questions such as this should be followed (eventually) by other questions asking students to identify likely faults based on measurements.

Notes 67

The point of this question is to have students research a datasheet to figure out the necessary conditions for making a digital IC perform as it should. This is *extremely* important for students to get into the habit of doing, as it will save them much trouble as technicians!

Notes 68

Students will probably need to consult a datasheet for the 74HC194 in order to figure out what is going on here. If they have not taken the initiative to do so, encourage them to both now and later! Datasheets are an invaluable source of information when it comes to integrated circuit behavior and the conditions necessary to make them do what you want them to do.

Notes 69

Students will find a datasheet for the 74HC194 helpful in figuring out how this circuit is supposed to work.

Notes 70

This is a good question to discuss with your students, as it helps them understand how to "divide and conquer" a malfunctioning system.

Notes 71

The purpose of this question is to approach the domain of circuit troubleshooting from a perspective of knowing what the fault is, rather than only knowing what the symptoms are. Although this is not necessarily a realistic perspective, it helps students build the foundational knowledge necessary to diagnose a faulted circuit from empirical data. Questions such as this should be followed (eventually) by other questions asking students to identify likely faults based on measurements.

Notes 72

Connecting a faulty circuit to a different input signal than what it normally runs at is an excellent way to explore faults. However, it should be noted that some faults may go undetected using this technique, because you have altered the circuit in the process.

Notes 73

The answer to this question is fairly simple, but the real point of it is to get students thinking about how and why it is the way it is. One thing I've noticed as an instructor of electronics is that most students tend to follow the rule of proximity: the resistor's voltage drop polarity is determined by proximity to poles of the battery. The resistor terminal closest to the battery's negative terminal must be negative as well, or so the thinking goes.

In this particular circuit, though, the rule of proximity does not hold very well, and a different rule is necessary.

Notes 74

Kirchhoff's Voltage Law (KVL) is very easily explored in real life with a set of batteries and "jumper wire" connections. Encourage your students to build battery circuits like the one shown in this question, to be able to see the results for themselves!

One really nice feature of digital multimeters (DMMs) is the ability to register negative as well as positive quantities. This feature is very useful when teaching Kirchhoff's Laws, with the *algebraic* (sign-dependent) summation of voltages and currents.

Students may arrive at more than one method for determining voltmeter indications in problems like these. Encourage this type of creativity during discussion time, as it both helps students gain confidence in being able to approach problems on their own terms, as well as educates those students who might be confused with the concept. Quite often the explanation of a peer is more valuable than the explanation of an instructor. When students are given the freedom to explore problem-solving methods, and then share those methods with their classmates, substantial learning always results.

Notes 75

Physical height (and depth) is a very useful analogy for electrical potential, helping students relate this abstract thing called "voltage" to more common differential measurements.

Notes 76

Determining differential voltages is a skill that many students find frustrating to attain. There is more than one way to explain how to arrive at +3 volts as the answer for V_{AB}, and it is good for students to see more than one way presented.

Notes 77

Discuss with your students multiple techniques of solving for these voltages, asking them first for their solution strategies.

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Notes 79

Ask your students this question: "Will the algebraic sum of voltage measurements ever be other than zero in a loop?" Ask them to explain *why* this is, as best they can.

Notes 80

I really enjoy covering the Superposition Theorem in class with my students. It's one of those rare analysis techniques that is intuitively obvious and yet powerful at the same time. Because the principle is so easy to learn, I highly recommend you leave this question for your students to research, and let *them* fully present the answer in class rather than you explain any of it.

Notes 81

Some students will erroneously leap to the conclusion that another generator will send twice the current through the load (with twice the voltage drop across the motor terminals!). Such a conclusion is easy to reach if one does not fully understand the Superposition Theorem.

Notes 82

Being able to convert between series and parallel AC networks is a valuable skill for analyzing complex series-parallel combination circuits, because it means any series-parallel combination circuit may then be converted into an equivalent simple-series or simple-parallel, which is mush easier to analyze.

Some students might ask why the conductance/susceptance triangle is "upside-down" compared to the resistance/reactance triangle. The reason has to do with the sign reversal of imaginary quantities when inverted: $\frac{1}{j} = -j$. The phase angle of a pure inductance's impedance is +90 degrees, while the phase angle of the same (pure) inductance's admittance is -90 degrees, due to reciprocation. Thus, while the X leg of the resistance/reactance triangle points up, the B leg of the conductance/susceptance triangle must point down.

Notes 83

This problem just happens to work out with whole numbers. Believe it or not, I chose these numbers entirely by accident one day, when setting up an example problem to show a student how to convert between series and parallel equivalent networks!

Notes 84

Although there are other methods of solving for total impedance in a circuit such as this, I want students to become comfortable with series/parallel equivalents as an analysis tool.

Notes 85

Be sure to ask your students to describe *how* they arrived at the answers to this question. There is more than one place to start in determining the solution here, and more than one way to calculate some of the figures. No matter how your students may have approached this question, though, they should all obtain the same answers.

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Notes 87

Despite the fact that this connection scheme is quite common in industry, I have found little reference to it in textbooks. The equilateral layout of the windings in this diagram facilitates graphical (phasor) analysis of the voltages, providing students with the opportunity to exercise their knowledge of trigonometry.

Notes 88

Although the given answer seems complete, what I'm looking for here is a good analytical understanding of why the voltage gain is what it is. Placing the requirement of using KVL on the students' answers ensures that they will have to explore the concept further than the given answer does.

Notes 89

Nothing much to comment on here – just some practice on common-emitter amplifier calculations. Note that the approximations given here are based on the following assumptions:

- 0.7 volts drop (exactly) across base-emitter junction.
- Infinite DC current gain (β) for transistor ($I_B = 0\,\mu$A ; $I_C = I_E$).
- Negligible loading of bias voltage divider by the emitter resistance.
- Negligible dynamic emitter resistance ($r'_e = 0\,\Omega$)

This question lends itself well to group discussions on component failure scenarios. After discussing how to calculate the requested values, you might want to ask students to consider how these values would change given some specific component failures (open resistors, primarily, since this is perhaps the most common way that a resistor could fail).

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Notes 91

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Notes 92

Ask your students how they solved this problem, sharing techniques and strategies to help other students know where to begin and where to proceed from there.

Notes 93

Ask your students to discuss what advantages, if any, one of these counter circuit types may have over the other.

Notes 94

Be sure to discuss the follow-up question with your students. It is important that they understand how to make both "up" and "down" counters using J-K flip-flops, and that there are two basic methods to make each direction of counter.

Notes 95

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Notes 98

The purpose of this question is to introduce students to the schematic convention of counter/dividers as simple boxes with "MOD" specified for each one, and to provide a bit of quantitative analysis (albeit very simple).

Notes 99

This question reviews the principles of D-type flip-flops, timing diagrams, and serves as an introduction to shift registers.

Notes 100

One application for a serial-in/serial-out shift register is a precise time delay for serial-stream data.

Notes 101

This is a really neat trick for dividing or multiplying binary numbers by powers of two. It is often used in machine-language microprocessor programming, due to its simplicity of execution.

Notes 102

This question is multi-faceted. Students must consider volatility and ease of updating (the data), as well as simply applying the concept of a look-up table to a car's engine control computer, in order to intelligently answer this question.