

ARM Instruction Set Format

31	2827				1615				87				0				<u>Instruction type</u>										
Cond		0	0	I	Opcode			S	Rn		Rd		Operand2				Data processing / PSR Transfer										
Cond		0	0	0	0	0	0	0	A	S	Rd		Rn		Rs	1	0	0	1	Rm	Multiply						
Cond		0	0	0	0	0	1	U	A	S	RdHi		RdLo		Rs	1	0	0	1	Rm	Long Multiply (v3M / v4 only)						
Cond		0	0	0	1	0	B	0	0		Rn		Rd		0	0	0	0	1	0	0	1	Rm	Swap			
Cond		0	1	I	P	U	B	W	L		Rn		Rd		Offset						Load/Store Byte/Word						
Cond		1	0	0	P	U	S	W	L		Rn		Register List									Load/Store Multiple					
Cond		0	0	0	P	U	1	W	L		Rn		Rd		Offset1	1	S	H	1	Offset2		Halfword transfer : Immediate offset (v4 only)					
Cond		0	0	0	P	U	0	W	L		Rn		Rd		0	0	0	0	1	S	H	1	Rm	Halfword transfer: Register offset (v4 only)			
Cond		1	0	1	L	Offset															Branch						
Cond		0	0	0	1	0			0	1	0	1		1	1	1	1		1	1	1	0	0	0	1	Rn	Branch Exchange (v4T only)
Cond		1	1	0	P	U	N	W	L		Rn		CRd		CPNum		Offset				Coprocessor data transfer						
Cond		1	1	1	0	Op1						CRn		CRd		CPNum		Op2		0	CRm		Coprocessor data operation				
Cond		1	1	1	0	Op1			L		CRn		Rd		CPNum		Op2		1	CRm		Coprocessor register transfer					
Cond		1	1	1	1	SWI Number															Software interrupt						