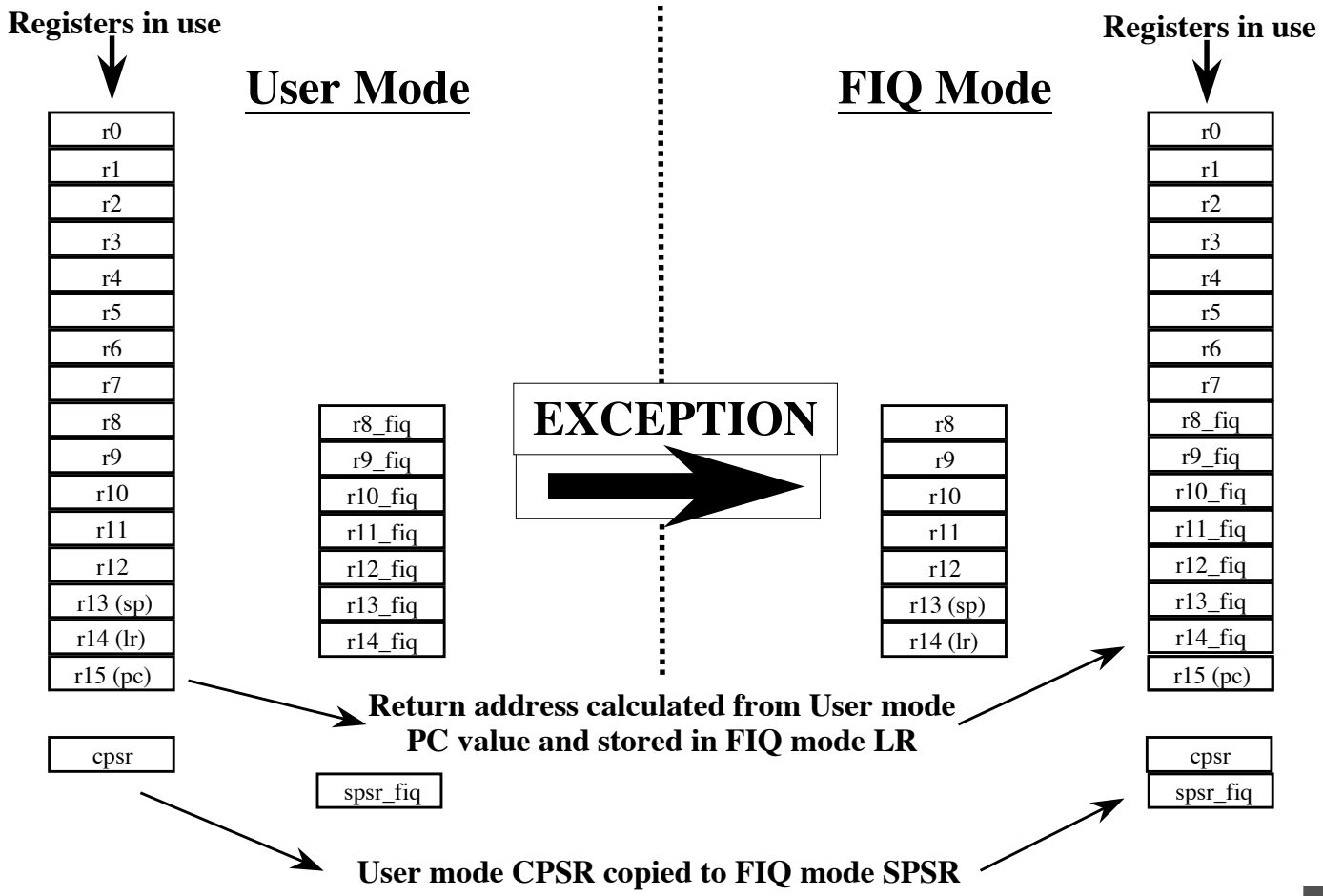
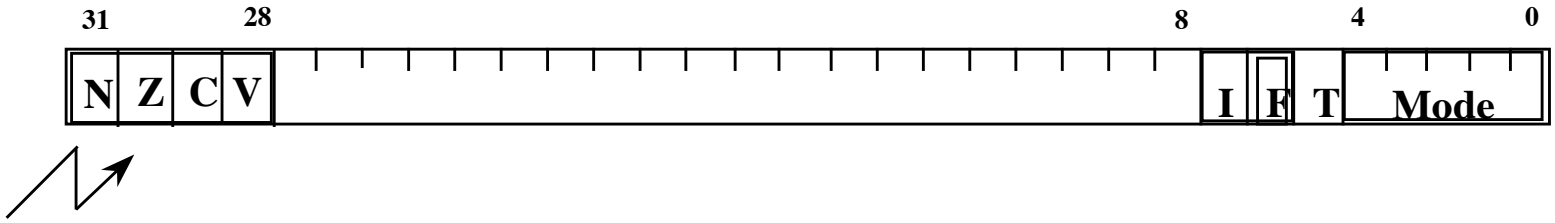
Register Example: User to FIQ Mode



Accessing Registers using ARM Instructions

* **No breakdown of currently accessible registers.**
  - All instructions can access r0-r14 directly.
  - Most instructions also allow use of the PC.
* **Specific instructions to allow access to CPSR and SPSR.**
* **Note : When in a privileged mode, it is also possible to load / store the (banked out) user mode registers to or from memory.**
  - See later for details.

The Program Status Registers (CPSR and SPSRs)



Copies of the ALU status flags (latched if the instruction has the "S" bit set).

* **Condition Code Flags**

  N = **N**egative result from ALU flag.
  Z = **Z**ero result from ALU flag.
  C = ALU operation **C**arried out
  V = ALU operation o**V**erflowed

* **Mode Bits**

  M[4:0] define the processor mode.

* **Interrupt Disable bits.**

  I = 1, disables the IRQ.
  F = 1, disables the FIQ.

* **T Bit (Architecture v4T only)**

  T = 0, Processor in ARM state
  T = 1, Processor in Thumb state

Condition Flags

	Logical Instruction	Arithmetic Instruction
Flag		
Negative (N='1')	No meaning	Bit 31 of the result has been set Indicates a negative number in signed operations
Zero (Z='1')	Result is all zeroes	Result of operation was zero
Carry (C='1')	After Shift operation '1' was left in carry flag	Result was greater than 32 bits
oVerflow (V='1')	No meaning	Result was greater than 31 bits Indicates a possible corruption of the sign bit in signed numbers

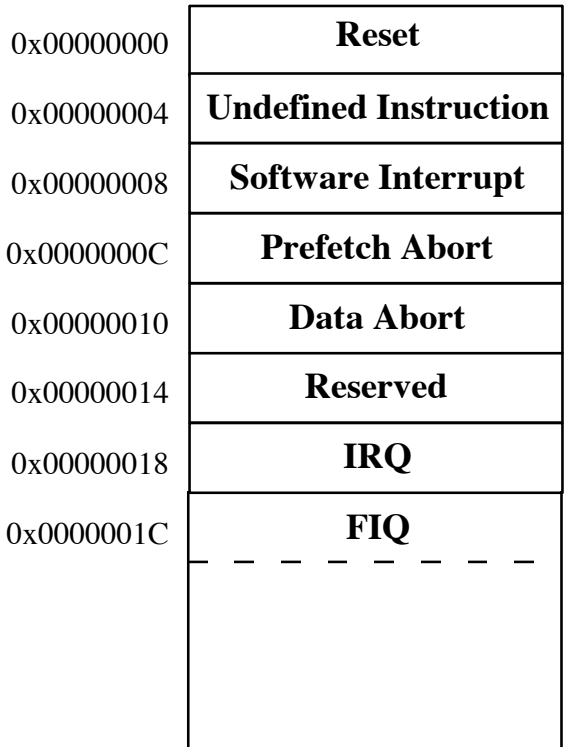
The Program Counter (R15)

* **When the processor is executing in ARM state:**
  - All instructions are 32 bits in length
  - All instructions must be word aligned
  - Therefore the PC value is stored in bits [31:2] with bits [1:0] equal to zero (as instruction cannot be halfword or byte aligned).
* **R14 is used as the subroutine link register (LR) and stores the return address when Branch with Link operations are performed, calculated from the PC.**
* **Thus to return from a linked branch**
  - `MOV r15,r14`

  or
  - `MOV pc,lr`

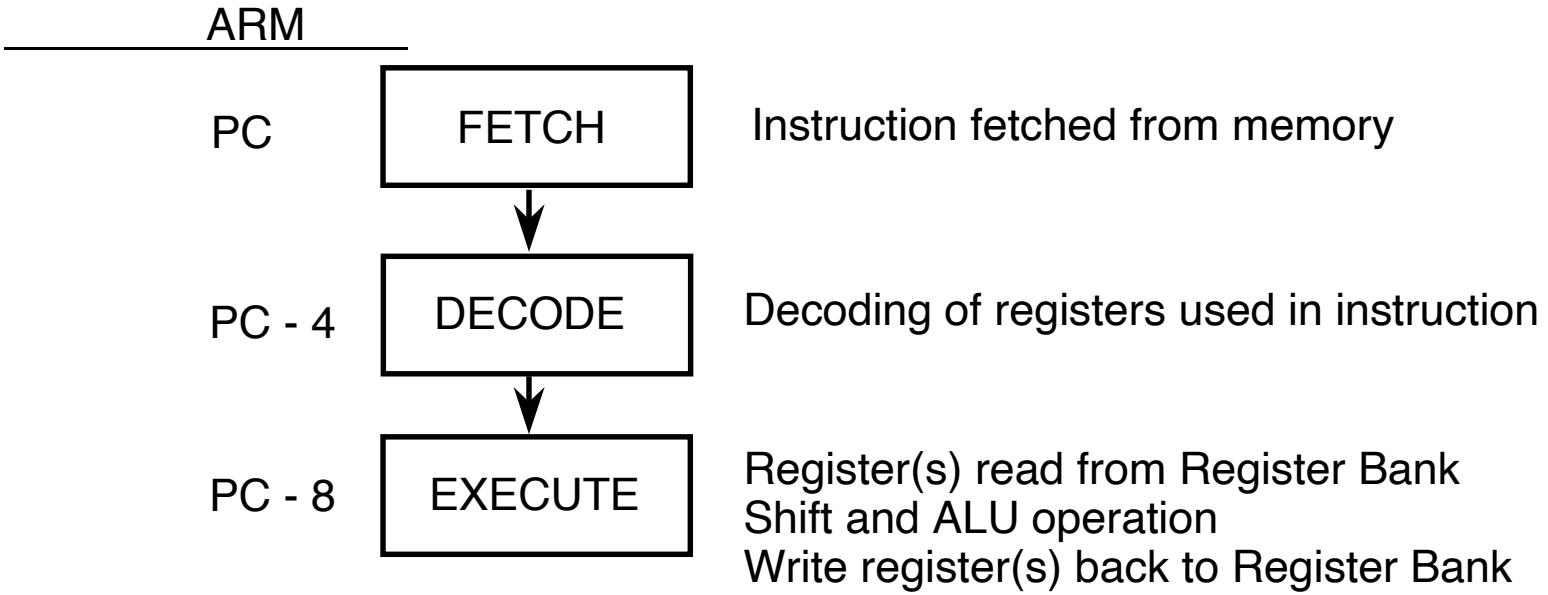
Exception Handling and the Vector Table

* **When an exception occurs, the core:**
  - Copies CPSR into SPSR_<mode>
  - Sets appropriate CPSR bits
    - If core implements ARM Architecture 4T and is currently in Thumb state, then
      - ARM state is entered.
    - Mode field bits
    - Interrupt disable flags if appropriate.
  - Maps in appropriate banked registers
  - Stores the "*return address*" in LR_<mode>
  - Sets PC to vector address
* **To return, exception handler needs to:**
  - Restore CPSR from SPSR_<mode>
  - Restore PC from LR_<mode>



The Instruction Pipeline

* **The ARM uses a pipeline in order to increase the speed of the flow of instructions to the processor.**
  - Allows several operations to be undertaken simultaneously, rather than serially.



* **Rather than pointing to the instruction being executed, the PC points to the instruction being fetched.**

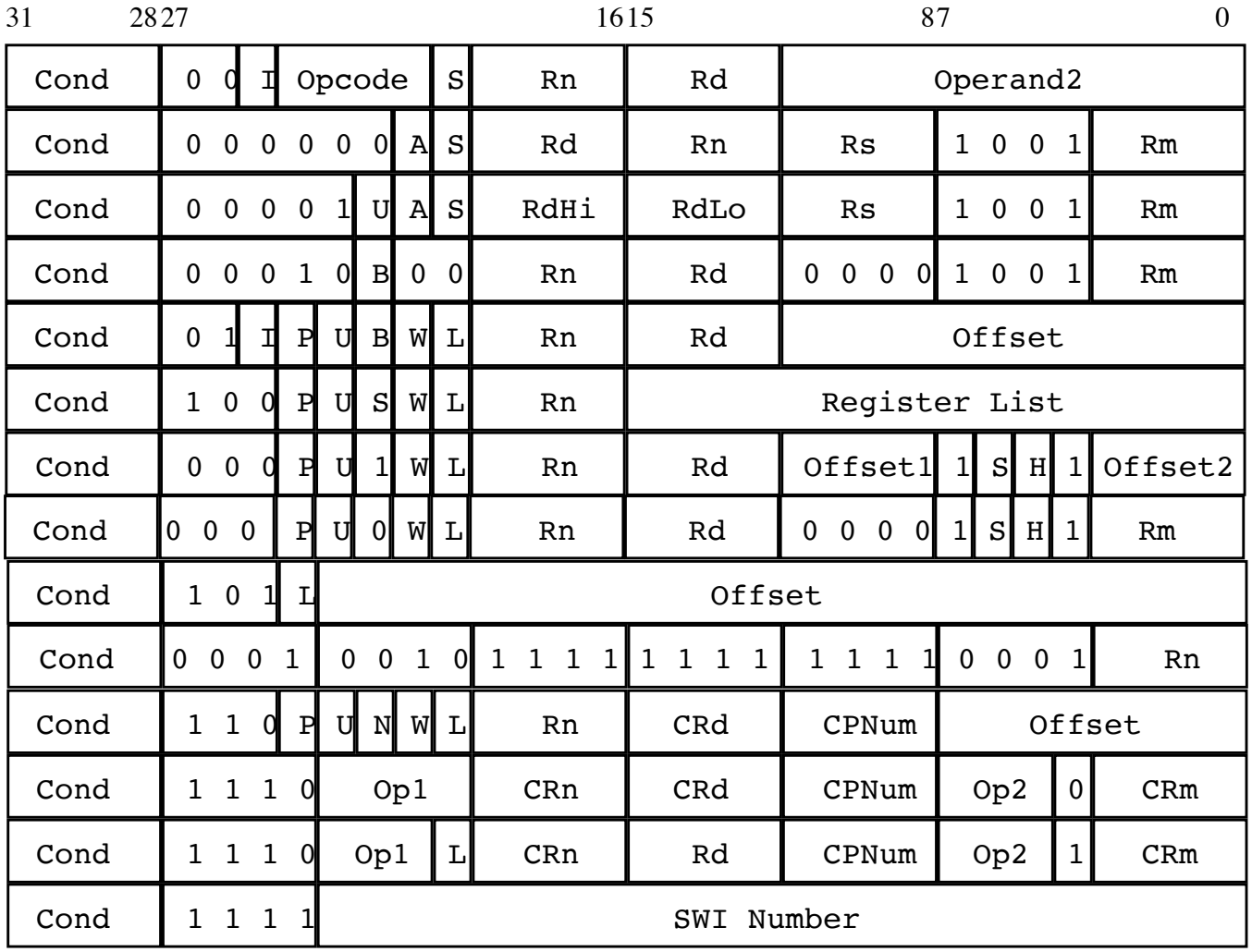
Quiz #1 - Verbal

* What registers are used to store the program counter and link register?

* What is r13 often used to store?

* Which mode, or modes has the fewest available number of registers available? How many and why?

ARM Instruction Set Format



Instruction type

Data processing / PSR Transfer

Multiply

Long Multiply **(v3M / v4 only)**

Swap

Load/Store Byte/Word

Load/Store Multiple

Halfword transfer : Immediate offset **(v4 only)**

Halfword transfer: Register offset **(v4 only)**

Branch

Branch Exchange **(v4T only)**

Coprocessor data transfer

Coprocessor data operation

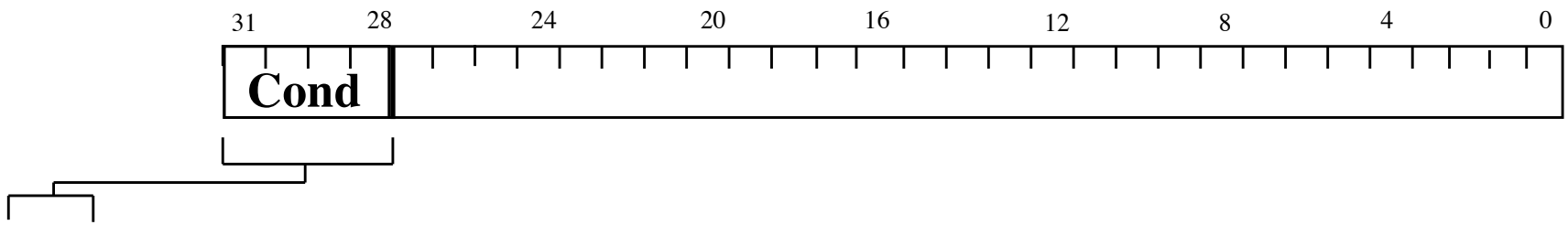
Coprocessor register transfer

Software interrupt

Conditional Execution

* **Most instruction sets only allow branches to be executed conditionally.**
* **However by reusing the condition evaluation hardware, ARM effectively increases number of instructions.**
  - All instructions contain a condition field which determines whether the CPU will execute them.
  - Non-executed instructions soak up 1 cycle.
    - Still have to complete cycle so as to allow fetching and decoding of following instructions.
* **This removes the need for many branches, which stall the pipeline (3 cycles to refill).**
  - Allows very dense in-line code, without branches.
  - The Time penalty of not executing several conditional instructions is frequently less than overhead of the branch or subroutine call that would otherwise be needed.

The Condition Field



0000 = EQ - Z set (equal)

0001 = NE - Z clear (not equal)

0010 = HS / CS - C set (unsigned higher or same)

0011 = LO / CC - C clear (unsigned lower)

0100 = MI -N set (negative)

0101 = PL - N clear (positive or zero)

0110 = VS - V set (overflow)

0111 = VC - V clear (no overflow)

1000 = HI - C set and Z clear (unsigned higher)

1001 = LS - C clear or Z (set unsigned lower or same)

1010 = GE - N set and V set, or N clear and V clear (>or =)

1011 = LT - N set and V clear, or N clear and V set (>)

1100 = GT - Z clear, and either N set and V set, or N clear and V set (>)

1101 = LE - Z set, or N set and V clear,or N clear and V set (<, or =)

1110 = AL - always

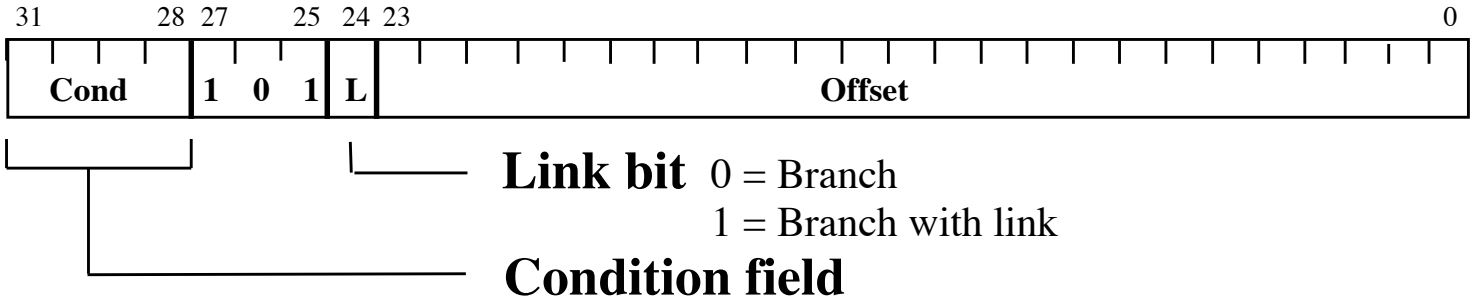
1111 = NV - reserved.

Using and updating the Condition Field

* **To execute an instruction conditionally, simply postfix it with the appropriate condition:**
  - For example an add instruction takes the form:
    - `ADD r0,r1,r2 ; r0 = r1 + r2 (ADDAL)`
  - To execute this only if the zero flag is set:
    - `ADDEQ r0,r1,r2 ; If zero flag set then...`
      `; ... r0 = r1 + r2`
* **By default, data processing operations do not affect the condition flags (apart from the comparisons where this is the only effect). To cause the condition flags to be updated, the S bit of the instruction needs to be set by postfixing the instruction (and any condition code) with an "S".**
  - For example to add two numbers and set the condition flags:
    - `ADDS r0,r1,r2 ; r0 = r1 + r2`
      `; ... and set flags`

Branch instructions (1)

* **Branch :** `B{<cond>} label`
* **Branch with Link :** `BL{<cond>} sub_routine_label`



* **The offset for branch instructions is calculated by the assembler:**
  - By taking the difference between the branch instruction and the target address minus 8 (to allow for the pipeline).
  - This gives a 26 bit offset which is right shifted 2 bits (as the bottom two bits are always zero as instructions are word – aligned) and stored into the instruction encoding.
  - This gives a range of ± 32 Mbytes.

Branch instructions (2)

* **When executing the instruction, the processor:**
  - shifts the offset left two bits, sign extends it to 32 bits, and adds it to PC.
* **Execution then continues from the new PC, once the pipeline has been refilled.**
* **The "Branch with link" instruction implements a subroutine call by writing PC-4 into the LR of the current bank.**
  - i.e. the address of the next instruction following the branch with link (allowing for the pipeline).
* **To return from subroutine, simply need to restore the PC from the LR:**
  - `MOV pc, lr`
  - Again, pipeline has to refill before execution continues.
* **The "Branch" instruction does not affect LR.**
* **Note: Architecture 4T offers a further ARM branch instruction, BX**
  - See Thumb Instruction Set Module for details.

Data processing Instructions

* **Largest family of ARM instructions, all sharing the same instruction format.**
* **Contains:**
  - Arithmetic operations
  - Comparisons (no results - just set condition codes)
  - Logical operations
  - Data movement between registers
* **Remember, this is a load / store architecture**
  - These instruction only work on registers, ***NOT*** memory.
* **They each perform a specific operation on one or two operands.**
  - First operand always a register - Rn
  - Second operand sent to the ALU via barrel shifter.
* **We will examine the barrel shifter shortly.**

Arithmetic Operations

* **Operations are:**
  - ADD operand1 + operand2
  - ADC operand1 + operand2 + carry
  - SUB operand1 - operand2
  - SBC operand1 - operand2 + carry -1
  - RSB operand2 - operand1
  - RSC operand2 - operand1 + carry - 1
* **Syntax:**
  - <Operation>{<cond>}{S} Rd, Rn, Operand2
* **Examples**
  - ADD r0, r1, r2
  - SUBGT r3, r3, #1
  - RSBLES r4, r5, #5

Comparisons

* **The only effect of the comparisons is to**
  - ***UPDATE THE CONDITION FLAGS.*** Thus no need to set S bit.
* **Operations are:**
  - CMP operand1 - operand2, but result not written
  - CMN operand1 + operand2, but result not written
  - TST operand1 AND operand2, but result not written
  - TEQ operand1 EOR operand2, but result not written
* **Syntax:**
  - <Operation>{<cond>} Rn, Operand2
* **Examples:**
  - CMP r0, r1
  - TSTEQ r2, #5

Logical Operations

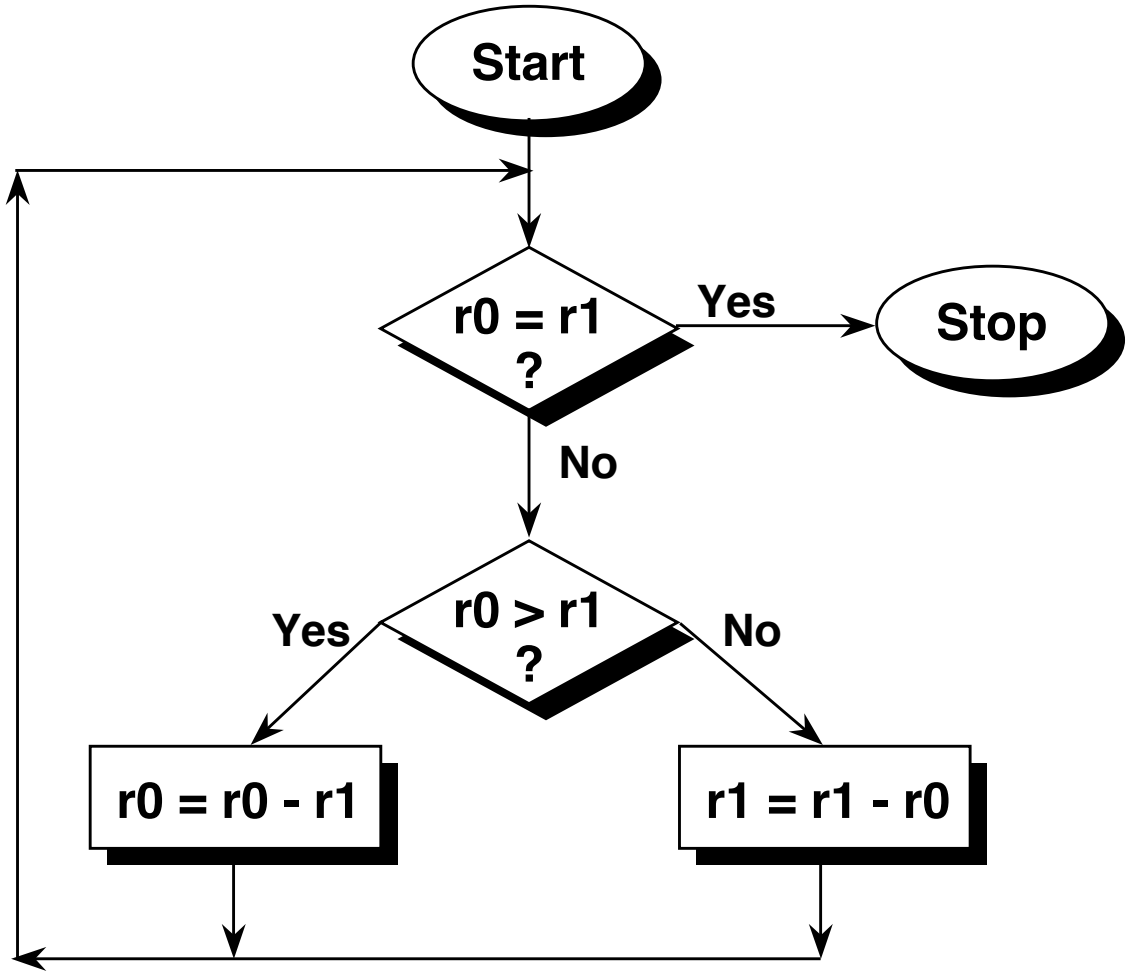
* **Operations are:**
  - AND operand1 AND operand2
  - EOR operand1 EOR operand2
  - ORR operand1 OR operand2
  - BIC operand1 AND NOT operand2 [ie bit clear]
* **Syntax:**
  - <Operation>{<cond>}{S} Rd, Rn, Operand2
* **Examples:**
  - AND r0, r1, r2
  - BICEQ r2, r3, #7
  - EORS r1,r3,r0

Data Movement

* **Operations are:**
  - MOV operand2
  - MVN NOT operand2

  Note that these make no use of operand1.
* **Syntax:**
  - <Operation>{<cond>}{S} Rd, Operand2
* **Examples:**
  - MOV r0, r1
  - MOVS r2, #10
  - MVNEQ r1,#0

Quiz #2



* **Convert the GCD algorithm given in this flowchart into**
  1) "Normal" assembler, where only branches can be conditional.
  2) ARM assembler, where all instructions are conditional, thus improving code density.

* **The only instructions you need are CMP, B and SUB.**