

Laboratory 3

Expected delivery of lab_03.zip must include:

- program_2_a.s, program_2_b.s and program_2_c.s
- this file compiled and if possible in pdf format.

Please, configure the winMIPS64 simulator with the *Base Configuration* provided in the following:

- Code address bus: 12
- Data address bus: 12
- Pipelined FP arithmetic unit (latency): 4 stages
- Pipelined multiplier unit (latency): 8 stages
- divider unit (latency): not pipelined unit, 12 clock cycles
- Forwarding is enabled
- Branch prediction is disabled
- Branch delay slot is disabled
- *Integer ALU: 1 clock cycle*
- *Data memory: 1 clock cycle*
- *Branch delay slot: 1 clock cycle.*

1) Starting from the assembly program you created in the previous lab called **program_2.s**:

```
for (i = 0; i < 40; i++){
    v5[i] = v1[i] + (v2[i] * v3[i]);
    v6[i] = v5[i] * v4[i];
    v7[i] = v6[i] / v2[i];
}
```

- a. Detect manually the different data, structural and control hazards that provoke a pipeline stall
- b. Optimize the program by re-scheduling the program instructions in order to eliminate as much hazards as possible. Compute manually the number of clock cycles the new program (**program_2_a.s**) requires to execute, and compare the obtained results with the ones obtained by the simulator.
- c. Starting from **program_2_a.s**, enable the *branch delay slot* and re-schedule some instructions in order to improve the previous program execution time. Compute manually the number of clock cycles the new program (**program_2_b.s**) requires to execute, and compare the obtained results with the ones obtained by the simulator.
- d. Unroll 4 times the program (**program_2_b.s**), if necessary re-schedule some instructions and renaming the used registers. Compute manually the number of clock cycles the new program (**program_2_c.s**) requires to

execute, and compare the obtained results with the ones obtained by the simulator.

Complete the following table with the obtained results:

Program	program_2.s	program_2_a.s	program_2_b.s	program_2_c.s
Clock cycle computation				
By hand	1647	1567	1520	1072
By simulation	1647	1567	1527	1080

Compare the results obtained in the point 1, and provide some explanation in the case the results are different.

Eventual explanation:

-program_2_a

Ho modificato l'ordine di alcune istruzioni al fine di ottimizzare le diverse fasi in pipeline.

-program_2_b

Essendo attivo il branch delay slot, spostato l'istruzione di aggiornamento dell'indice dopo l'eventuale salto, in modo che venga preparata prima indipendentemente dall'esito.

-program_2_c

Unroll x4 :

```
for (i=0;i<N;i++){
    x[i] = x[i] + y[i]
}
```

---->

```
for(i=0;i<N;i=i+4){
    x[i] = x[i] + y[i]
    x[i+1] = x[i+1] + y[i+1]
    x[i+2] = x[i+2] + y[i+2]
    x[i+3] = x[i+3] + y[i+3]
}
```