① Amplifier modeling.

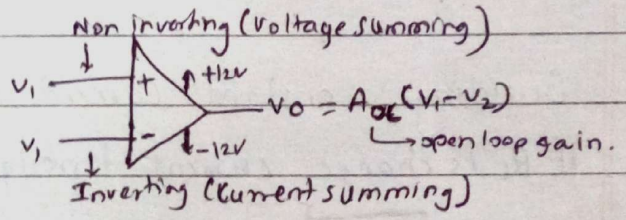
amp^r	R_{in}	R_o	voltage source / voltage controlled
Voltage	high	low	$V_o = K V_{in}$ (VS, VC)
current	low	high	$I_o = K I_{in}$ (CS, CC)
transconductance	high	high	$I_o = g_m V_{in}$ (CS, VC)
transresistance	low	low	$V_o = R_m I_{in}$ (VS, CC)

(Av) Voltage gain $= \frac{V_o}{V_s} = \frac{V_o}{V_{in}} \frac{V_{in}}{V_s}$

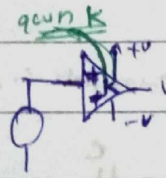
(A_I) Current gain $= \frac{I_o}{I_s} = \frac{I_o}{I_{in}} \frac{I_{in}}{I_s}$

(A_p) power gain $= A_v \cdot A_I$

Operational amp^r.



* In amp^r



to avoid cliping $\boxed{-\frac{V_o}{K} \le V_{in} \le \frac{V_o}{K}}$ condition for i/p

* -ve feedback given to inverting whereas +ve f/B to Noninverting.

* -ve f/B is stable with high slew rate, whereas +ve f/B is bistable.

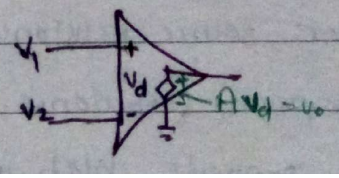
* Opamp actually amplify error signal.

for amp^r with -ve feedback & having ~~[illegible]~~ very high gain two points are imp in solving example.

① voltage at inverting = voltage at Noninverting.

② opamp draws No current.

for opamp having marginal gain (like 10, 100 ck) use ideal model of opamp



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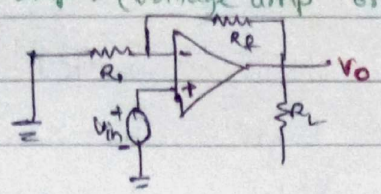
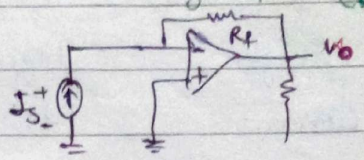
* Non Inverting N.I amp^r. (voltage amp^r or VCVS)



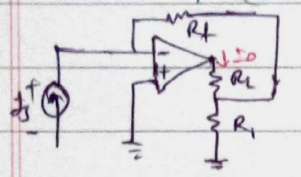
$V_o = (1+\frac{R_f}{R_1})V_{in}$

* Inverting amp^r. (transresistance CCVS)



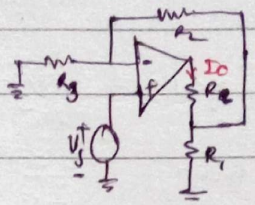
$V_o = -I_R R_f$.

* current amp^r (CCCS)



$I_o = -[1+\frac{R_F}{R_1}]$

* Transconductance amp^r VCCS transconductance

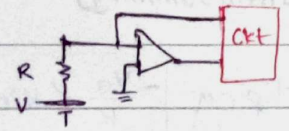


$V_s = \frac{R_1 R_3}{R_1+R_2+R_3} I_o$

$I_o = g_m V_s$.

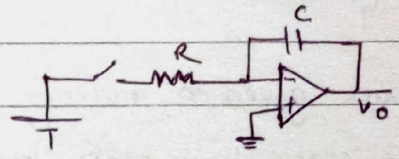
* Building constant current source

if R_L is change current through it must be same.



as opamps draw no current ∴ I is constant $= \frac{V}{R}$.

* miller integrator.

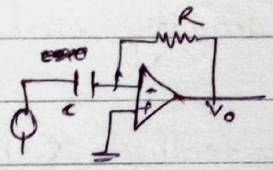


$V_o = \frac{-V}{RC}t$

$V_C = \frac{1}{C}\int I\,dt$

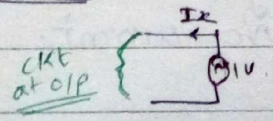
$I = C\frac{dV_c}{dt}$

* differentiator.



* i/p & o/p Resistance ⇒ $R_{in} = \frac{V_{in}}{I_{in}}$

for Ro ① O.C. R_L ② SC Vin OR OC I_s ③ connect 1V source at o/p & find $R_o = \frac{1V}{I_x}$



Ix is current at o/p

* Buffer or unity gain amp^r.

Whenever source Resistance is higher than the load Resistance to deliver power (impedance matching device) used having high power gain.

I.M.D. connects high impedance source to low impedance load.

Voltage buffer	Current buffer
high Rin, low Ro, $A_v \simeq 1$	low Rin, high Ro, $A_I \simeq 1$
high A_I, $A_p = A_I$	high A_V, $A_p = A_V$
eg common collector	eg. common base.

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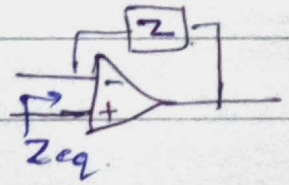
* miller effect.



$Z_{eq} = \frac{Z}{1+A}$

$R_{eq} = \frac{R}{1+A}$ $L_{eq} = \frac{L}{1+A}$ $C_{eq} = C(1+A)$

* miller effect seen only for inverting amp^r eg. common emmiter.

No. miller effect in CB, & CC. amp^r.

$\tau \propto RC$, $\tau \propto \frac{1}{B.W}$

To avoid miller effect we use impedance mismatching

* if opamp has opeloop gain 10^6 $R_{in} = R_o$ without feedback

∴ Opamp used to design buffer then $R_{in(feedback)} = R_{in}(1+A\beta)$

$R_{o(feedback)} = \frac{R_o}{(1+A\beta)}$ $A\beta \to 10^6$

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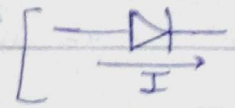
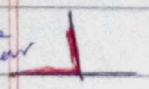
* Diode applications.

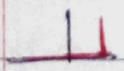
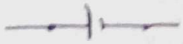
→ Diode is FB when anode is more +ve than cathod.

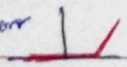
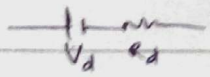
→ To find biasing find current through diode if +ve FB, if -ve RB.

→ But to find current short diodes then find currents by KCL

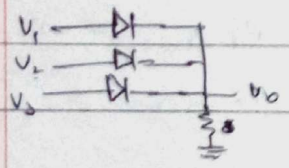
** [ I +ve FB, I -ve RB] $I_D = I_S e^{V_D/V_T}$

Piecewise linear  $I = V_{in}/R$

 $I = \frac{V_{in} - 0.7}{R}$ 

non linear  $I = \frac{V_{in} - 0.7}{R + R_d}$ 

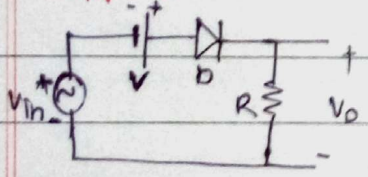
Diode is logarithmic device. $V_D = V_T \ln\left(\frac{I_D}{I_S}\right)$

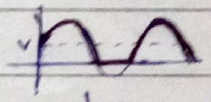
* 

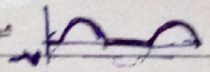
if $V_1 > V_2$ & V_3 D is FB D_2 D_3 RB & vice versa.

If Direction of diod reverse condition also reverse

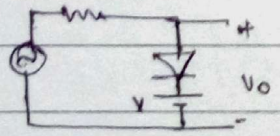
* clippers.

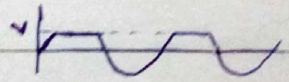


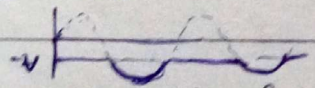
$V_o = V_{in} + V$ ⇒ 

if V is ⊣⊢ then $V_{in} - V$ 

if direction of diode change then it clips +ve cycle & retain -ve cycle

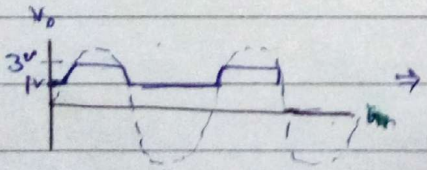


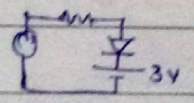
V_o ⇒ 

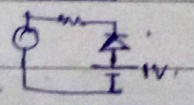
if V ⊣⊢ then 

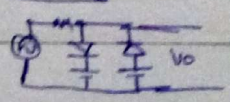
if we interchange the polarity of diode it will clip darp part & retain shaded part.

* (conclude according to current passing through diode)



① $V_{in} > 3$ ⇒ 

② $V_{in} < 1$ ⇒ 

③ $1 \le V_{in} \le 3$ ⇒ 

Double bias clipper or slicer.

* While drawing transverse characteristic taken conditions (like) ($V_{in} > 100$, $V_{in} > 25$ etc.) take care of 3 imp. points

① current through resistor 0 or not

② if not zero find condition by linear relationship.

③ $V_{in} > 50$ if $V_o = 50$

} see example

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* Clampers

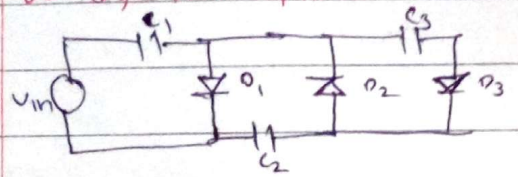
→ clampers is ckt which adds dc to the given i/p waveform.

→ It is also called DC Resistors.

To draw clamp o/p → ① find capacitor voltage in its steady state.

② Replace diode with open switch draw o/p waveform

* Voltage multiplier



$V_{C_1} = V_{in}$

$V_{C_2} = 2V_{in}$ → voltage doubler

volty tripler

$V_{C_3} = 2V_{in}$

$V_{C_n} = 2V_{in}$

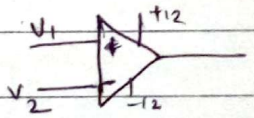
-ve f/B → linear, VCVS, VCCS, CCCS, CCVS amp, Adders, subtractors

non-linear, Rectifier, Peak detector, Log amp, Antilog etc.

openloop → comparator

+ve f/B → ~~s~~ schmitt trigger, multivibrator

* comparator

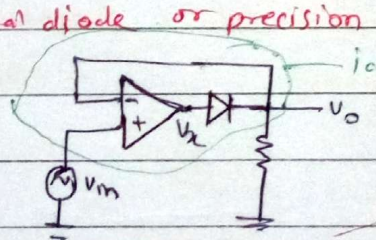


$V_0 = A[V_1 - V_2]$

$V_1 > V_2 \rightarrow V_0 = +12V.$

$V_1 < V_2 \rightarrow V_0 = -12V.$

* Ideal diode or precision diode or superdiode

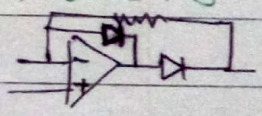


ideal diode =

$V_{in} > 0 \rightarrow V_x$ +ve ⇒ diode FB

$V_{in} < 0 \rightarrow V_x$ -ve ⇒ diode RB

but slew rate is very low ∴ modified to



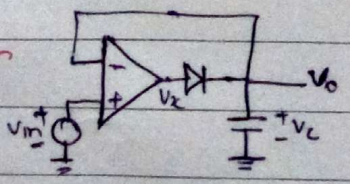
(if V_{in} applied at - terminal of opamp above conditions will. (V_{in} +ve V_x -ve reverse)

actually V_d +ve ⇒ V_x +ve

$V_d = V_1 - V_2$ (+) (-) terminals of opamp

major advantage of -ve feedback is Desensitization of forward transfer parameter

* Peak detector



① V_d +ve → V_x +ve

(i.e. $V_{in} > V_c$) ⇒ D FB

Capacitor charge to V_{in}

② V_d -ve → V_x -ve D RB.

capacitor holds the value.

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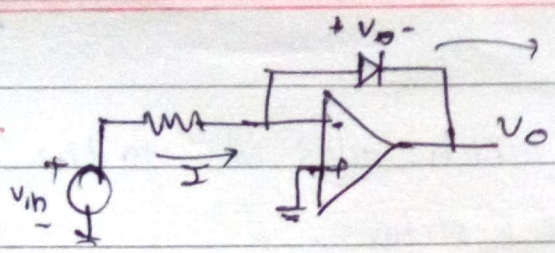
* log ampr

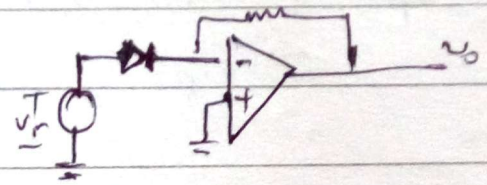


→ Diode (Logarithmic device)

(CCVS)

$V_o \propto \ln[V_{in}]$ ⇒ log ampr

* exponential ampr



(just interchanged R & D)

$V_o \propto e^{V_{in}}$ ⇒ exponential ampr or antilog ampr.

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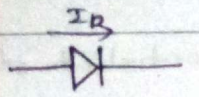
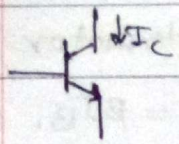
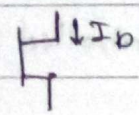
* Non linear Devices.



$$I_D = I_S e^{V_D/V_t}$$



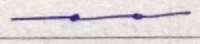
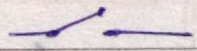
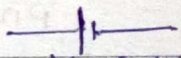
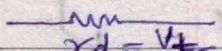
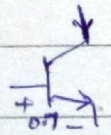
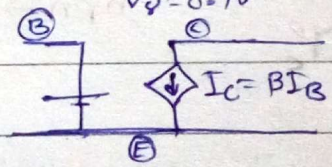
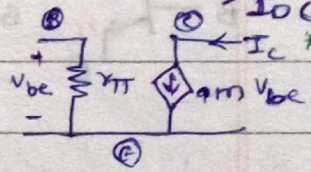
$$I_C = I_S e^{V_{be}/V_t}$$



$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

* Non linear Device can be made to be act linearly by keeping the signal sufficiently small and adding dc to the signal (i.e. operating in linear region)

$e^x = \overset{\to DC}{1} + \underset{\to \text{ sufficiently small signal}}{x}$ (approximat^n of e^x)

*	component	DC ($\omega = 0$)	AC (ω = high).
①	Resistor	R	R
②	capacitor ($\frac{1}{\omega C}$)		
③	Inductor (ωL)		
④	Diode (small signal)	 $V_\gamma = 0.7V$	 $r_d = V_t / I_D$ (DC)
⑤	BJT 	 $I_C = \beta I_B$	 $r_\pi = \frac{\beta}{g_m}$

* Diode is two terminal Non-linear passive device.
* BJT is three terminal Non-linear active device.

BJT is current controlled current source

BJT o/p does not depend upon V_{CC} or load resistor.

O/p current of BJT is controlled by i/p current I_B ∵ $I_C = \beta I_B$

If $R_{CE} = \infty$ → cutoff region if $R_{CE} = 0$ → saturation Region.

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Region of operation	Emitter Base Junction BE	Collector Base Junction BC.	
① Cutoff	($V_{BE} < 0.6$) → RB	RB	controlled off switch
② Inverse active	RB	FB	Attenuator
③ Active	($V_{BE} \geq 0.6$) → FB	RB	$I_C = \beta I_B$. (ampr)
④ Saturation	FB	FB.	controlled ON switch

$\boxed{\beta_{forced} < \beta_{active}}$ ~~→ saturation region~~

β_{forced} ↓ saturatn, β_{active} ↓ Active

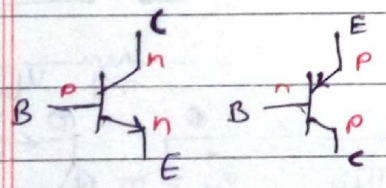
(if $V_{CE} > 0.2$ then BJT is in active region)

* Procedure :- find in order $V_E \rightarrow I_E \rightarrow I_C \rightarrow V_C \rightarrow V_{CE}$.

if $V_{CE} > 0.2 \rightarrow$ BJT in active region.

* check whether BJT is in active region or not. consider saturation region and findout the actual values without considering $I_C = \beta I_B$ relation. it is valid only for active region

*



pnp → V_{EC}

npn → V_{CE}

* $\beta = \frac{I_C}{I_B}$ → In active region. ⇒ $\beta = \frac{I_C}{I_B}$ → I_C less → R_C ↑, I_B → high → V_{bb} ↑

if R_C is ↑↑ & V_{bb} also ↑↑ the β goes on decreasing & hence BJT will go in saturatn. ∴ to avoid BJT to go in saturatn β value should greater & R_C should be around 1k & V_{bb} very less.

* diffential ampr will work as ampr only when BJT is in active region. & also small signal is applied.

* BJT wich experience higher Potential diff will ON first in diff ampr.

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* Biasing in BJT

* purpose is to switch on BJT to work in active Region such that DC collector current I_{cdc} Remains constant. It should be independent of β, temp. variation & load variat^n.

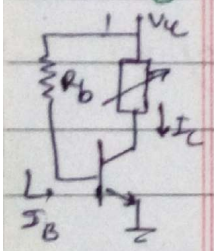
* temp change → V_{BE} will change -2.5 mV/°C called drift problem ∴ I_c changes.

* Load changes → V_{CE} changes → I_c changes called early effect.

* β changes → I_c changes can compensated by using R_E Resistor.

* ∴ summary is I_c should not depend upon β, V_{be}, V_{ce} & should provide constant current I_c called desensitizat^n of active parameters

① fixed bias.

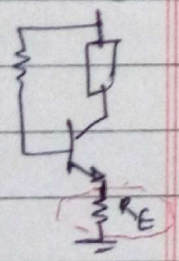


$$I_{C_{DC}} = \beta I_B = \beta\left[\frac{V_{CC}-V_{BE}}{R_b}\right] \qquad \because I_B = \frac{V_{CC}-V_{BE}}{R_b}$$

∴ I_{cdc} depends on particular Value of β

ckt which depends on β is bad ckt.

② Biasing with emitter resistor R_E:

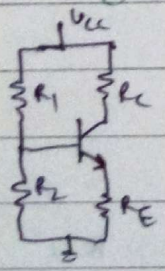


$$I_B = \frac{I_E}{\beta+1} \Rightarrow I_E = \frac{V_{CC}-V_{BE}}{R_E + \frac{R_b}{\beta+1}} \qquad R_E >> \frac{R_b}{\beta+1}$$ to densistise β variation.

then $I_E \simeq I_{cDC} = \dfrac{V_{CC}-V_{BE}}{R_E}$. $\qquad I_c = \left(\dfrac{\beta}{\beta+1}\right) I_E$

* but this ckt is practically not possible

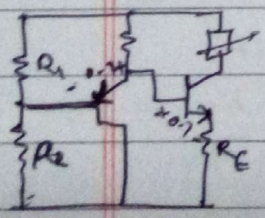
③ Self bias or universal or voltage devider bias:-



$$V_{TH} = V_{CC}\cdot\frac{R_2}{R_1+R_2} \qquad R_{th} = R_1 \| R_2 \qquad I_B = \frac{I_E}{\beta+1}$$

$$\therefore I_E = \frac{V_{th}-V_{BE}}{R_E + \frac{R_{th}}{\beta+1}} \qquad \text{choose } R_E >> R_{th}/\beta+1$$

then $I_E \simeq I_{cdc} = \dfrac{V_{th}-V_{BE}}{R_E}$



⇒ This ckt eleminate drift problem i.e. temp. dependancy. provided that two transistors should have same temp. coefficients.

$I_c \simeq I_E = \dfrac{V_{th}}{R_E}$ → independent of V_{be}

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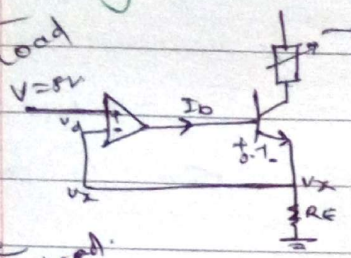
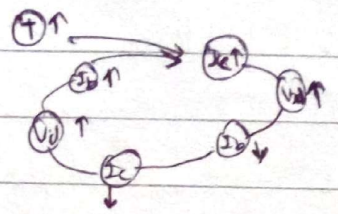
* Biasing a BJT with opamp in a negative feedback will totally eliminate the problem of drift.

* Driver stage
* Current source with floating load

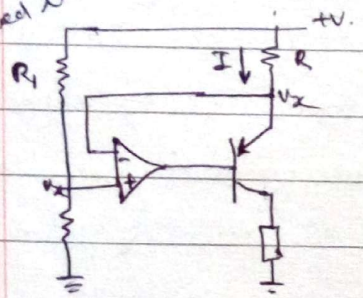


→ Floating load. * this ckt is independent of temp. variations.



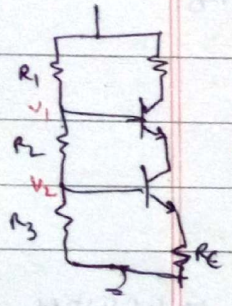
* Current source with grounded load.

Opamp driving BJT



$I_L = I = \frac{V - V_x}{R} = \frac{V - V_{th}}{R}$ → independent of V_{BE}

* Cascode current source - To improve current stability on load variation.
(i.e. to reduce early effect)



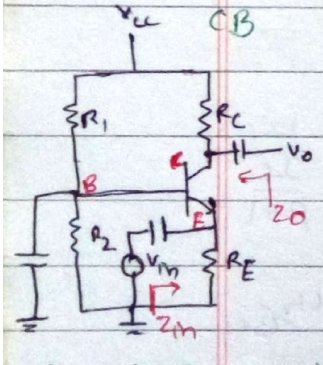
$V_1 = \frac{V_{cc}(R_2+R_3)}{R_1+R_2+R_3}$

$V_2 = \frac{V_{cc}(R_3)}{R_1+R_2+R_3}$

* Configuration of BJT

~~CB~~

CB



$Z_{in} = 30\Omega$ $Z_0 = 1m\Omega$

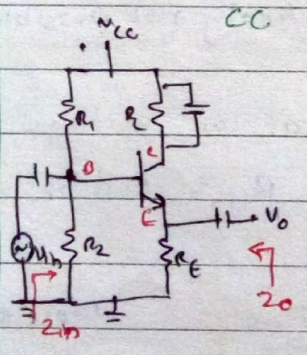
Current controll current source

$A_I \approx 1$, $A_V = 600$

$A_P = A_V A_I \approx A_V$

(Current Buffer)

CC



$Z_{in} = 9m\Omega$

$Z_0 = 8\Omega$

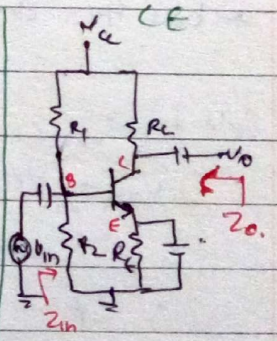
Voltage controll voltage source

$A_V \approx 1$ $A_I = 100$

$A_P = A_V A_I \approx A_I$

(Voltage Buffer)

CE



$Z_{in} = 1K\Omega$, $Z_0 = 50K\Omega$

$A_V = -200$ $A_I = -100$

$A_P = A_V A_I$.

It has high power gain.

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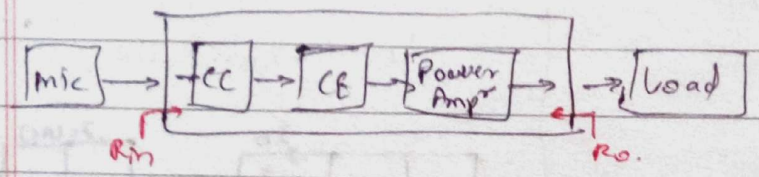
* we want dynamic resistance using BJT
* BJT characteristic is non linear but we will model BJT to work in a particular linear region by applying some dc bias.
* DC bias is used to operate BJT at its operating points or in linear region.
* Ac characteristics of BJT will totally depend on dc point i.e. operating point.
* CE amp^r is neither good source nor good driver it lies somewhere in the middle but it has large power gain.
* in CE -sign in gain indecates 180° phase shift.

*eg. public address system.



→ I/P Resistance Rin found for impedance matching where Ro found for maximum power transfer.

→ If O/P res. Ro = Load Res. R_L then maximum power transfered.

→ Rin is nothing but Rin of 1st stage CC.

→ Ro is Ro of last stage Power Amp^r.

→ overall gain is the product of gains of each stage.

* ① open ckt voltage gain → voltage source → VCVS → opamp.
② short ckt current gain → current source → CCCS → BJT.

* Small signal Analysis of BJT.
When excitat^n is dc + AC, → (i.e. Vcc + small signal)
→ Then instantaneous voltage or current at any point is (ac voltg + dc voltg) or (ac current + dc current)
i.e. given by superposition → i.e. Ac picture + DC picture.

* R_E provides stability of I_{CDC} independent of β. in DC But Ac it is gain Reducing factor to avoid gain reduce. we add bypass capacitor with short R_E in AC.

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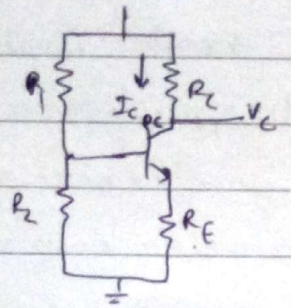
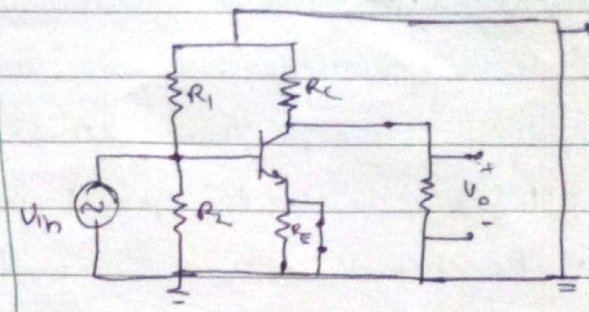
DC picture



$V_{c(DC)} = V_{cc} - I_{cDC} R_c$

$I_{cDC} = \dfrac{V_{th} - V_{BE}}{R_E + \frac{R_{th}}{\beta+1}}$

AC picture



$R_{in} = R_1 \| R_2$

$V_o = -I_{c(AC)} (R_c \| R_L)$

$V_{in} = V_{be(AC)}$

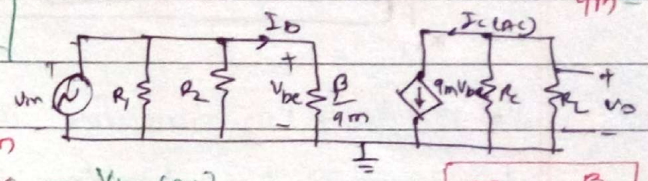
$A_v = \dfrac{-I_{c(AC)}}{V_{be(AC)}} (R_c \| R_L)$

$\boxed{V_t = V_T}$

$\therefore A_v = -g_m (R_c \| R_L)$

* $\because g_m = \dfrac{I_{cdc}}{V_t}$

* $g_m = \dfrac{-I_{c(AC)}}{V_{be(AC)}}$



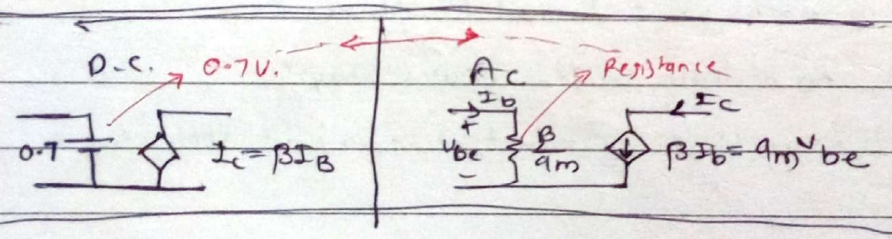
total $V_c = V_{c(DC)} + V_{c(AC)}$

$\therefore$ Total $V_c = (V_{cc} - I_c R_c) + [-g_m (R_c \| R_L)] V_{in}$

(base to emmiter resistance) $\rightarrow r_\pi = \dfrac{V_{be(AC)}}{I_{b(AC)}}$

$\boxed{r_\pi = \dfrac{\beta}{g_m}}$

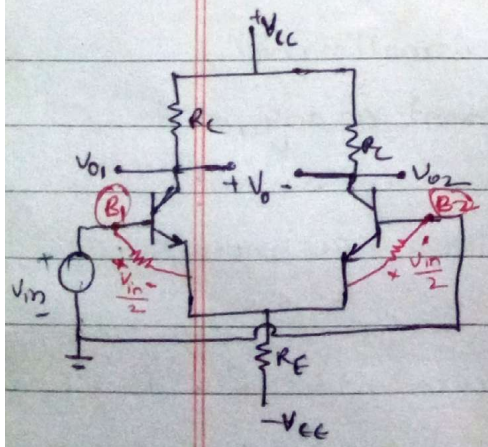
$\boxed{I_c = \beta I_b}$

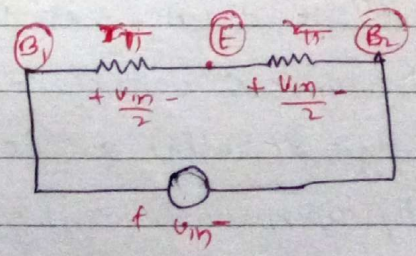


* Differential ampr

Drawback of CE ampr is it suffers from all common problems i.e. temp, drift, noise etc.

To avoid this we are using Differential ampr.



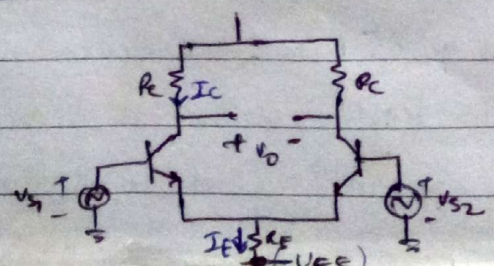


$V_{o1} = -g_m R_c \left(\dfrac{V_{in}}{2}\right)$

$V_{o2} = +g_m R_c \left(\dfrac{V_{in}}{2}\right)$

$V_o = V_{o1} - V_{o2} = -g_m R_c V_{in}$

$\therefore \boxed{\dfrac{V_o}{V_{in}} = -g_m R_c}$



$V_o = -g_m R_c (V_{s1} - V_{s2})$

$I_E = \dfrac{V_{s1} - V_{BE} + V_{EE}}{R_E}$ $\quad I_c = \dfrac{I_E}{2}$

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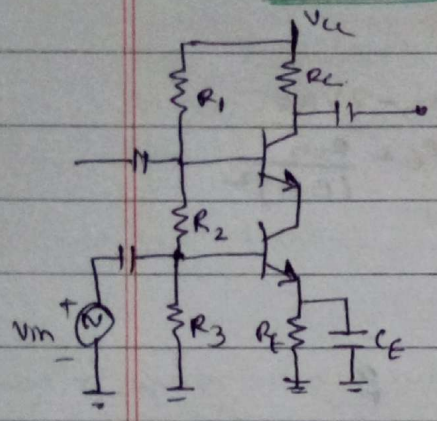
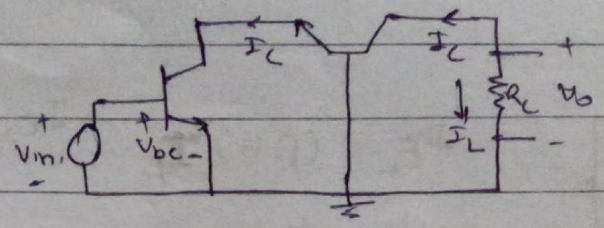
* Wideband structures.

① Cascode : [common emmitted cascaded to common base]

$\boxed{CE}_{①} \rightarrow \boxed{CB}_{②}$ or $\boxed{CS} \rightarrow \boxed{CG}$ (in FET)

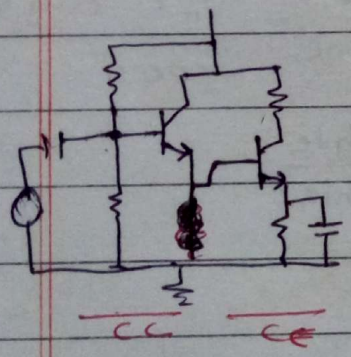


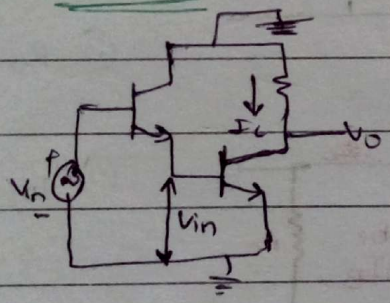


* Wider Bandwidth due to cross impedance mismatch between two impedance stages.
* Overall transconductance of cascode structure = the larger transconductance of CE amp
* large o/p impedance.

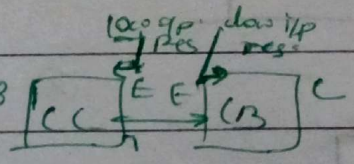
* CE amp suffers due to miller effect. to avoide this it is cascaded with amp which have themselves mismatch capability. or technique i.e. CB or CC.
* CB or CC having mismatching capacity.

② Cascode : $\overset{①}{CC}$ with $\overset{②}{CE}$.

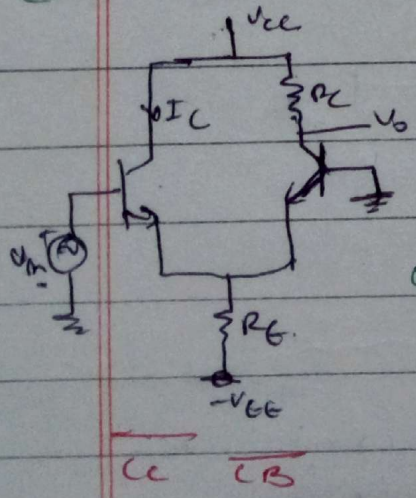




$$\frac{V_o}{V_{in}} = -g_m R_c$$



③ CC with CB.



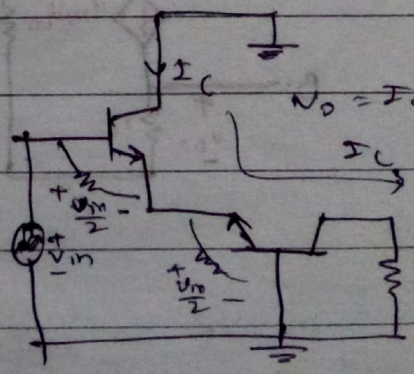
$V_o = I_c R_c$

$g_m = \frac{2 I_{CAC}}{V_{in}}$

Overall $g_m = \frac{g_m}{2} = \frac{I_{CAC}}{V_{in}}$

$A_v = +\frac{g_m}{2} R_c$

↑ no phase shift.



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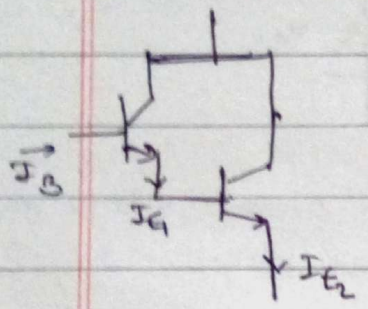
* Darlington pair:

- High current gain. High i/p Impedance.

→ Treat pair of two transistors as single transistor



$I_{E_2} = (\beta+1)^2 I_B$ $\quad I_{E_2} = \dfrac{V_{Th} - 2V_{BE}}{R_E + \dfrac{R_{Th}}{(\beta+1)^2}}$

* with darlington pair, we are going to ↑se the current range

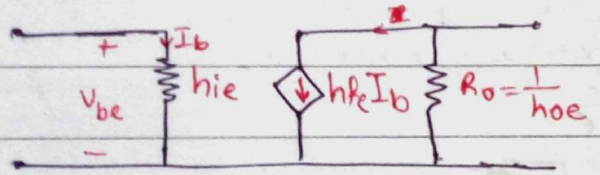
* Power transistor have low value (β) in the range of 10-15

* it is used to improve driving capacity.

* o/p is not going to ↑se ∴ we have to ↑se i/p current.

* Equivalent models for BJT.

① h-parameter model



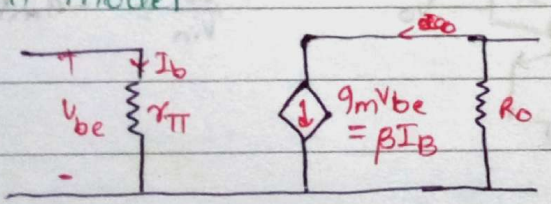
① $h_{ie} = r_\pi = \dfrac{\beta}{g_m}$

② $h_{fe} = \beta$

③ $R_o = \dfrac{1}{h_{oe}} = \dfrac{V_A}{I_{CQ}}$ ← early voltage.

④ $g_m = \dfrac{h_{fe}}{h_{ie}}$

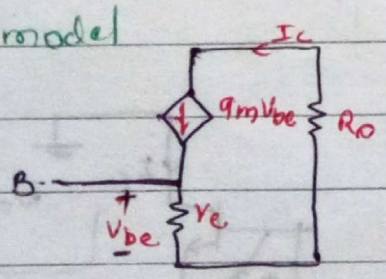
② π model



⑤ $r_e = \dfrac{V_{be}}{I_e} \simeq \dfrac{V_{be}}{I_c} = \dfrac{1}{g_m}$

⑥ $r_\pi = \beta r_e$

③ T-model



* To find i/p resistance $R_{in} = \dfrac{V_{in}}{I_{in}}$

* To find o/p resistance SC Voltg SC, OC current source.

short load give 1V supply at o/p find I_x through o/p

$Z_o = \dfrac{1}{I_x}$

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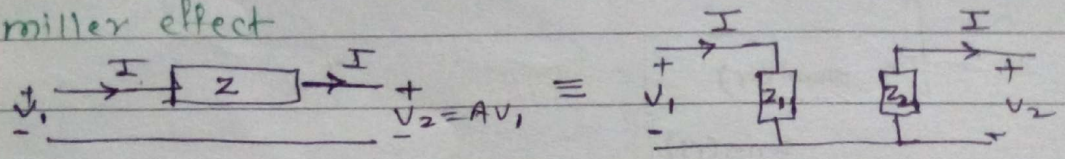
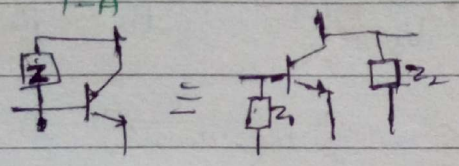
* miller effect



$Z_1 = \frac{Z}{1-A}$ $\qquad$ $Z_2 = \frac{Z}{1-1/A}$

i.e. 

⇒ splitting the ckt.

$\left(-\frac{R_f}{R_1}\right)$

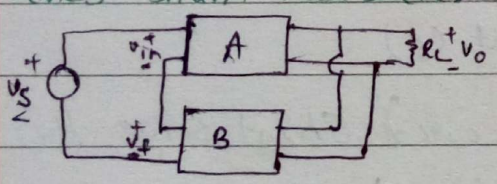
* or solve this type of problem by inspection see example in notes.

* Feedback Amp^rs.

* gain with f/B $= A_f = \frac{A}{1+AB}$ $\qquad$ if $AB >> 1$ $\quad A_f = \frac{1}{\beta}$.

* -ve f/B systems are very accurate & stable.

① Series-shunt feedback. (VCVS) 'H' feedback.

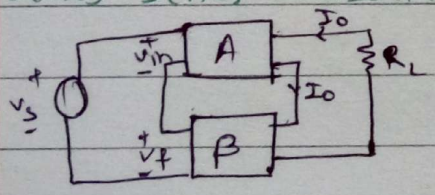


$A = \frac{V_o}{V_{in}} = \frac{V_o}{V_s - V_f}$ $\qquad$ $\because V_{in} = V_s - V_f$.

$\beta = \frac{V_f}{V_o}$; $A_f = \frac{A}{1+A\beta}$

$R_{in} = High(\infty)$ $\quad R_o = low\ (0)$

② Series series feedback. (VCCS) 'Z' feedback.

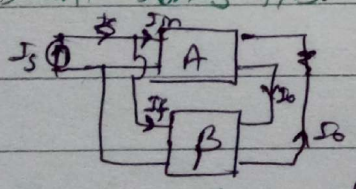


$A = \frac{I_o}{V_{in}} = \frac{I_o}{V_s - V_f}$ $\qquad$ $V_{in} = V_s - V_f$

$\beta = \frac{V_f}{I_o}$ $\qquad$ $A_f = \frac{A}{1+A\beta}$.

$R_{in} = \infty$ $\qquad$ $R_o = \infty$.

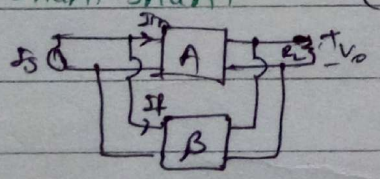
③ shunt-series f/B. (CCCS) 'G' feedback.



$A = \frac{I_o}{I_{in}} = \frac{I_o}{I_s - I_f}$ $\qquad$ $\beta = \frac{I_f}{I_o}$ $\qquad$ $A_f = \frac{A}{1+A\beta}$

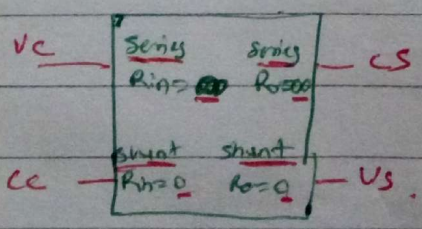
$R_{in} = 0$ $\qquad$ $R_o = \infty$

④ shunt shunt. (CCVS) 'Y' feedback.



$A = \frac{V_o}{V_{in}} = \frac{V_o}{I_s - I_f}$ $\qquad$ $\beta = \frac{I_f}{V_o}$ $\qquad$ $A_f = \frac{A}{1+A\beta}$

$R_{in} = 0$, $R_o = 0$.



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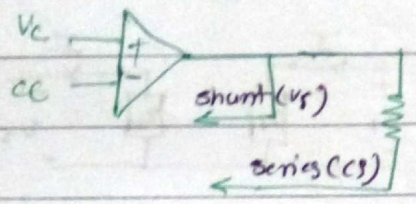

① Series shunt f/B amp^r. ① $\frac{V_o}{V_s} = A_f = 1 + \frac{R_f}{R_1} = \frac{1}{\beta}$ → Vltg gain.

② shunt shunt amp^r (Trans resistance amp^r) Inverting amp^r.

① $R_m = \frac{V_o}{I_s} = -R_f$ Trans resistance. → gain.
$= \frac{1}{\beta}$

③ Series - Series f/b amp^r (Transconductance) VCCS.

① gain (gm) $= \frac{I_o}{V_s} = \frac{R_1 + R_2 + R_3}{R_1 R_3} = \frac{1}{\beta}$

$A_V = \frac{V_o}{V_s} = -g_m R_c$ (with C_E)

$A_V = -\frac{R_c}{R_E}$ (without C_E)

④ (Current controlled current source) Shunt series f/B Amp^r.

$\frac{I_o}{I_s}$ gain $= -\left[1 + \frac{R_f}{R_1}\right] = \frac{1}{\beta}$

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* Oscillators

* Barkhausen's criterion ($A\beta=1$) is a necessary condition. for getting sine wave we have to design 2nd order system.

→ While solving quation get A & β then $A\beta=1$ comparing real parts & imaginary parts get necessary condition and frequency of oscillations

* Barkhausen's criterion.

① Magnitude of loop gain is unity. $A\beta=1$

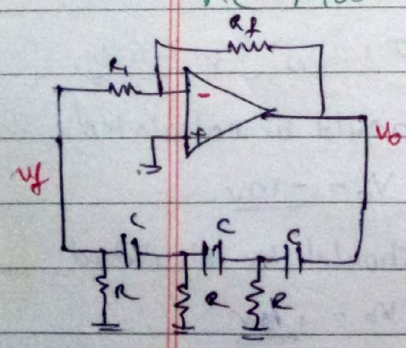
② phase angle of the loop gain is $0°$ or $360°$.

* make loop gain = 1 for sinusoidal oscillat's.

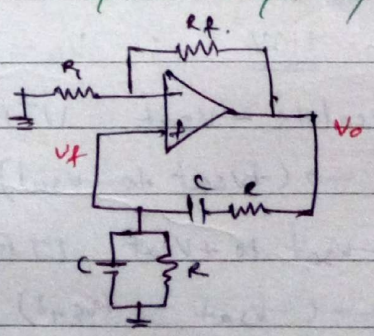
* RC phase shift oscillator is a fixed audio frequency oscillator. where weigh bridge oscillator is variable audio freq. oscillator

For high freq. oscillations go for wide band amp or LC networks.

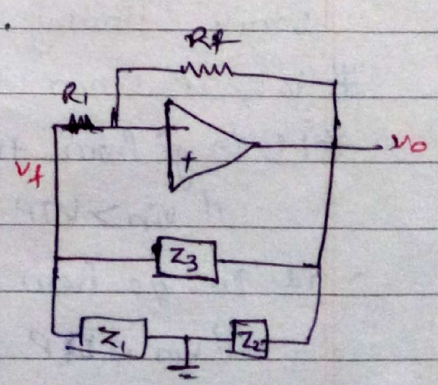
* If amp's suffers a phase lag the compensation should automatically come from RC Network to give a phase lead But RC Network have a slow variation of phase w.r.t. frequency for an ideal oscillator $\frac{d\phi}{d\omega}$ should be infinite. At lower freq. RC N/w is stable phase & freq. variations is low. At higher freq. RC N/w not stable there will be large variation in freq. Hence we should not use RC N/w at higher frequency.



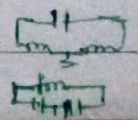
RC phase oscillator



wein Bridge



LC oscillator.



2 Inductor 1 capacitor - Hartley osc.

2 capa. & 1 inductor - Colpitts oscillator

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* Hartley Oscilat^r $\omega = \frac{1}{\sqrt{L_{eq}C}}$ $L_{eq} = L_1 + L_2$

$$\frac{R_f}{R_1} = \frac{L_2}{L_1}$$

* Colpitt's oscilat^r $\omega = \frac{1}{\sqrt{LC_{eq}}}$ $C_{eq} = \frac{C_1C_2}{C_1+C_2}$

$$\frac{R_f}{R_1} = \frac{C_1}{C_2}$$

* Duty Cycle $= \frac{T_{on}}{T_{total}}$

* Schitt trigger

* schmitt trigger has two thresholds UTP & LTP

1) The o/p switches from +Vsat to -Vsat when Vin is greater than UTP i.e. $V_{in} > UTP$.

2) o/p switches from -Vsat to +Vsat when $V_{in} < LTP$

3) o/p does not change when Vin is bet^n UTP & LTP
$LTP < V_{in} < UTP$

* opamp tracks the i/p vtg i.e. $V_{in} = V_f$.

* Phase locked loop (PLL) tracks the i/p freq. i.e. f_{in} = feedback.

* In a positive feedback system if i/p is fixed then o/p is either +Vsat OR -Vsat.

While finding UTP & LTP

* V_t = UTP when $V_o = +10V$. ; V_t = LTP when $V_o = -10V$.

* i.e. To go from +Vsat to -Vsat UTP should be calculated.
if $V_{in} > UTP$ → (+Vsat to -Vsat) $V_o = -10V$.

* i.e. To go from -Vsat to +Vsat LTP should be calculated
if $V_{in} < LTP$ → (-Vsat → +Vsat) $V_o = +10V$.

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* Non-inverting schmitt trigger. = $V_{in} = \left(-\frac{R_2}{R_1}\right) V_o$.

$V_o = +V_{sat}$ $\quad V_{in} < -\frac{R_2}{R_1} V_{sat}$ to switch V_o from $+V_{sat}$ to $-V_{sat}$

$V_o = -V_{sat}$ $\quad V_{in} > +\frac{R_2}{R_1} V_{sat}$ to switch V_o from $-V_{sat}$ to $+V_{sat}$.

* Triangular Wave generator

= schmitt trigger + miller Integrator.

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* opamp. specificat^n

* Skew Rate :- It is max. rate of change of o/p voltage for all possible i/p signals.

$$SR = \left|\frac{dV_o}{dt}\right|_{max}$$

SR of signal $= 2\pi f_{max} V_{o\,max}$ (if signal is having band of frequencies then max. freq is considered)

$|SR|_{signal} \leq |SR|_{opamp}$. (– for distortion less o/p)

* CMRR :- (common mode Rejection Ratio)

It is ratio of differential gain to the common mode gain. i.e. how much deviation will be there from amplifying the noise. it gives how much error is generated.

$$CMRR = \left|\frac{A_d}{A_{cm}}\right|$$ (CMRR is an AC quantity ∵ Noise is an AC or varying quantity)

$$CMRR_{dB} = 20\log\left|\frac{A_d}{A_{cm}}\right|$$

$$V_o = A_d V_d + \underbrace{A_{cm} V_{cm}}_{error}$$ → Practically it should be less than 0.1%.

common mode signal → generally Noise signal.

A_{cm} → gain due to Noise.

Ideally → $A_{cm} = 0$ ∴ $CMRR = \infty$.

$CMRR_{dB}$ = 40dB error = 1%.

60dB error = 0.1%

∴ practically opamp having CMRR above 60dB are preferred ∵ gives error which is always less than 0.1%

$V_1 = \frac{V_d}{2} + V_{cm}$ $\quad V_{cm} = \frac{V_1 + V_2}{2}$ $\quad V_o = A_d V_d + A_{cm} V_{cm}$

$V_2 = -\frac{V_d}{2} + V_{cm}$ $\quad V_d = V_1 - V_2$.

$A_d = \frac{A_1 - A_2}{2}$ $\quad A_1 = \frac{V_o}{V_1}\Big|_{V_2=0}$

$A_{cm} = A_1 + A_2$ $\quad A_2 = \frac{V_o}{V_2}\Big|_{V_1=0}$

Calculate A_1 & A_2 by using superposition theorem.

$$|CMRR| = \frac{A_1 - A_2}{2(A_1 + A_2)}$$

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* CMRR should always calculated only for half ckt.
Rejection should be done individually not collectively.

* For diff ampr $V_o = -g_m R_C (V_1 - V_2)$ considering half ckt

$A_{cm\,(half\,ckt)} = \frac{-R_C}{2R_E}$ $\therefore CMRR_{(half\,ckt)} = g_m R_E$

$A_{d\,(half\,ckt)} = \frac{-g_m R_C}{2}$

* Dont bias diff ampr with R_E
* CMRR can be improved by increasing R_E hence
Replace R_E with constant current source or current mirror

~~* Current mirror~~

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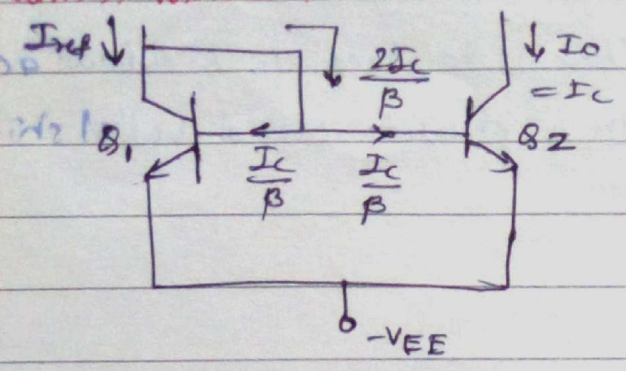
* Current mirror:

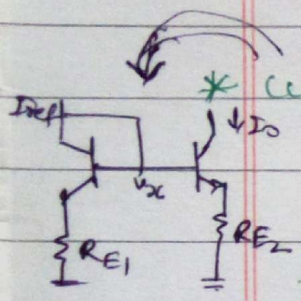


$I_{ref} = I_o\left[1+\frac{2}{\beta}\right] \cong I_o$

i.e. $\beta >> 1$

* if diode is connected to BJT is a current mirror.

$I \rightarrow \boxed{\text{Log}}_{\text{Diode}} \boxed{\text{exp.}}_{\text{BJT}} \rightarrow I$

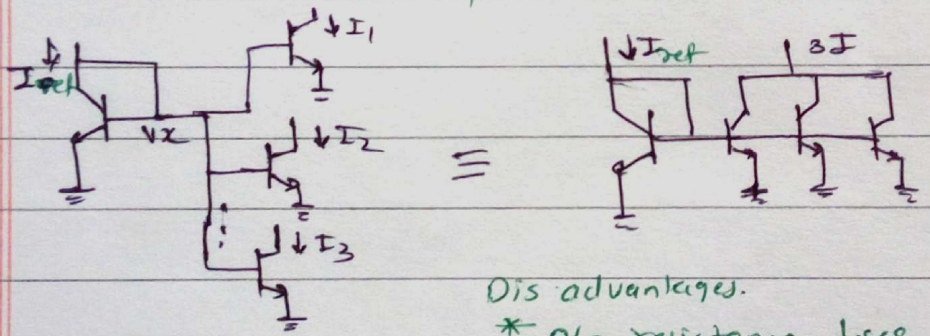


* Current mirror with emmitter generation $\frac{I_o}{I_{ref}} = \frac{R_{E_1}}{R_{E_2}}$

* If R_{E_1} & R_{E_2} are not given then $I_{ref} = I_o$.

* The ratio of Resistances is equal to emmitter areas

* Current source in IIe | → All BJT's have same V_{be}



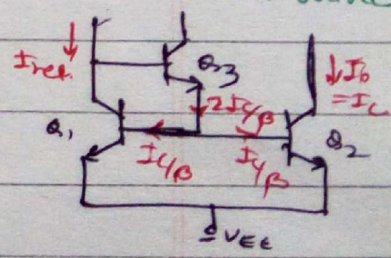
$I_1 = I_2 = I_3 = I$

$I_{ref} = 3I$

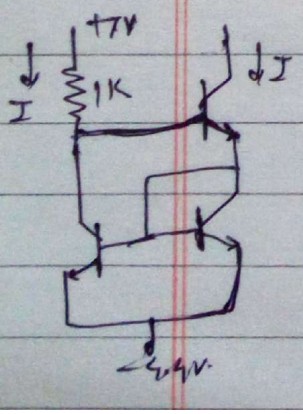
Dis advantages.

* o/p resistance tises. undesirable for constant current source

* Q_3 is used to decrease load on Iref.



* Wilson's current source.



This ckt does not undergo early effect i.e. load variations will not change the V_{CE} ~~always~~.

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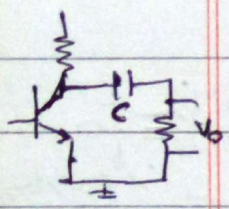
* Level shifter *



purpose of o/p capacitor is to block dc & allow ac.
DC can be blocked with a circuit called level shifter.

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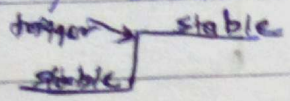
* Multivibrator's :-

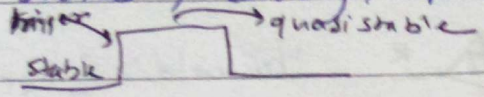
It is Regenerative ckt where transistors are cross coupled to work eigther in cutoff (OR) in saturation. Opamps in saturation limits.

① Bistable multivibrator



two stable states ; Binary / flip-flops. ; Eccles Jordan ckt.

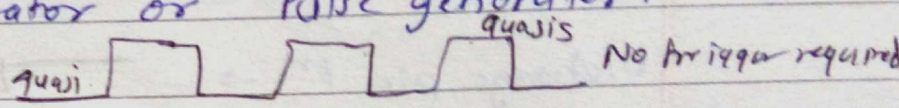
② monostable



one stable & one temporary states (i.e. quasistate)

Oneshot ~~vib~~ multivibrator or Pulse generator.

③ astable multivibrator



two quasi state , square wave generator

Free running multivibrator

* ∞ → cross coupled connection ⟶ +ve feedback

Two ways of triggering a bistable ckt

① asymmetrical triggering → trigger given to both BJT seperately.

② symmetrical triggering → If trigger given to both BJTs is same

$$V_c(t) = [V_{c\,initial} - V_{c\,final}]\, e^{-t/RC} + V_{c\,final}$$

for monostable $V_c(t) = -2V_{cc}\, e^{-t/RC} + V_{cc}$ ⟹ (if $V_{c\,initial} = -V_{cc}$, $V_{c\,final} = +V_{cc}$)

$T = 0.69RC$

for Bi-stable $T = T_1 + T_2 = 0.69R_1C_1 + 0.69R_2C_2$.

Bistable multivibrator is same as schimitt trigger ckt

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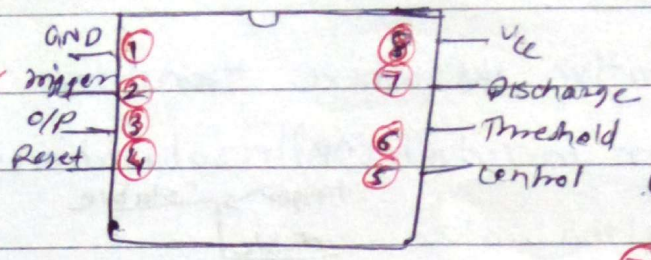
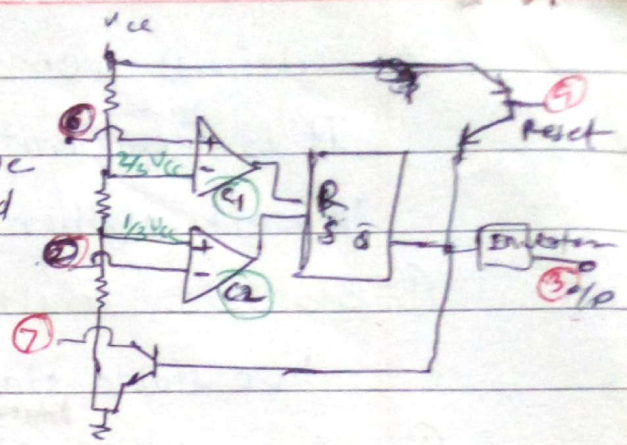
* 555 Timer





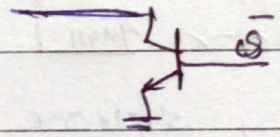
C1 - comparator 1

threshold > $\frac{2}{3}V_{cc}$ → R = logic 1

threshold < $\frac{2}{3}V_{cc}$ → R = logic 0.

Illy for C2

Discharge pin pin →



Q̄ = logic 0 ⇒ transistor OFF

Q = logic 1 ⇒ transistor ON.

* ~~In schmitt trigger using 555~~

* 555 timer changes its states only when threshold > $\frac{2}{3}V_{cc}$ (UTP) or trigger < $\frac{1}{3}V_{cc}$ (LTP). in schmitt trigger

* In RC ntwork current has to be calculate twice taking $V_c = \frac{1}{3}V_{cc}$ & $V_c = \frac{2}{3}V_{cc}$ ∵ current nature is exponential through capacitor.

* we can make schmitt trigger, bistable, monostable & astable multivibrator using 555 timer IC.

* To find T put t = T in equation of $V_c(t)$.

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