

* Chap 1 (Basics)

① 17 10 points on gates (Logic gates)

1) let analyse problems - 1 tick

② 4 conversion of betⁿ Number system (Number system)

4) finding base in operation

5) binary signed unsigned Numbers

6) 2's complement method

7) sign bit extension

8) Range of Numbers $2^{n-1} - 1$ 2^{n-1}

9) multiplicatⁿ & ÷ in 2's complement No.

10) complement of numbers.

11) advantage of 2's complement

③ 12) Binary codes. (Binary codes)

13) code conversions.

14) Addition of codes & carry?

15) Hamming code $p_1, p_2, m_1, p_3, m_2, m_3, m_4$ $2^p \geq m + p + 1$

④ 16) boolean algebra (Boolean Algebra)

17) imp laws, properties & expressions (consensus, shannon, Transposition)

18) NAND gate & NOR gate (min. nos) $2n-2$ - NAND $2n-3$ - AND 4 - S. NOR

⑤ 19) min terms, max terms its properties. (SOP & POS)

20) Various forms of $2^n - 1$ min terms in Exor, 2^n boolean fn.

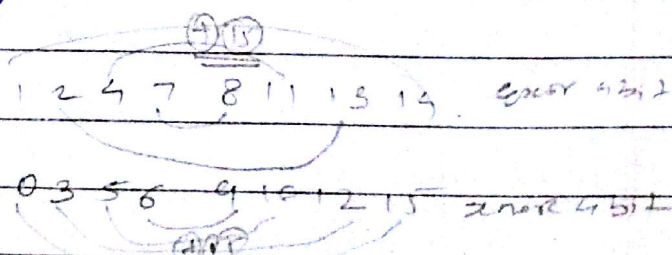
21) how to convert to canonical form trick $SOP \rightarrow AND-OR \equiv NAND-NAND$ $POS \rightarrow OR-AND \equiv NOR-NOR$

⑥ 22) k-map (k-map)

23) implicant & its types

24) dont care, & finding ^{ham 1's, 2's etc} to ~~find 1's, 2's etc~~

25) wave forms with delay.



* combinational ckt

- 1) Code converters (BC9 - to 9's compl. BCD to excess 3 etc.)
 - 2) Half adder & full adder half subtractor full subtractor.
 - 3) HA, FA, HS, FS using NAND NOR mini gates in HA, HS, & FS eqns
 - 4) Binary adders
 - a) Parallel $\rightarrow T = (N-1)t_c + \max(t_c, t_s)$ Adv. & Disadv.
 - b) Carry look ahead $\rightarrow C_{i+1} = C_i(A \oplus B) + AB \rightarrow (C_i)$ ckt, advantage-disadv., time, eqns, implementation etc.
 - c) Serial
 - 5) 4 bit adder & subtractor. $X=1$ subtractor $X=0$ adder.
 - 6) How to identify which adder (eg. excess-3, 9's complement ckt etc.)
 - 7) BCD adder, excess 3 adder.
 - 8) 2 bit comparator
 - 9) Decoder
 - 10) Encoder
 - 11) mux
 - 12) demux
- ckt. / imp. eqns / various ckt like FA, FS, etc.
 various functions implementations,
 no. of min. decoder or mux etc. to make big decoder or mux
 min. gate requires, min. levels.
 mux reduction, brick method.
- 2^{xy} = size
- 13) ROM as memory, size eqn., application
 - 14) PLA, PAL, GAL?
 - 15) overflow concept.

$$FA = 1247 - S$$

$$3557 - C$$

$$1FA = 2HA + 1OP gate$$

Active low $\rightarrow \nabla$

Active high $\rightarrow \nabla$

No. of o/p required

No. of o/p given

go on doing optore

* Sequential ckt

- 1) Memory concept, latch.
- 2) Latch operations, o/p sequences, how to start?
- 3) $\{S, R, J, K, T, D\}$ 1) T.T. 2) Excitation table 3) eqn's ckt.
- 4) Race around condition, Mrs. Alf. remedy.
- 5) Asynchronous & synchronous?
- 6) Hold time, ~~set~~ setup time, R.d.
- 7) Triggering
- 8) o/p frequencies, duty cycle of ckt?
- 9) Application of FF counters, shift register etc.
- 10) shift register.

1) PISO

2) SISO

3) SIPO

4) PISO

ckt, o/p frequency, delay, properties

11) shift register applications

Conv. g.d. seq. generator
① ② ③ ④ - counter

⑤ counters → ⑥ Ring counter

⑦ Johnson counter

ckt, operation, properties, o/p freq.

12) 3 bit Asynchronous counter (Ripple counter)

13) 2 bit Asynchr. up/down counter.

14) Up-down counter identification various combinations

15) mod counter; how to use p & c to make mod counter

16) ~~How~~ method to find ckt for ^{mod} counter, up/down?

o/p. frequency, cascading of counter.

& draw back of Asynchronous counter.

17) Excitation table, concept how to make it

18) how to make synchronous counter using excitation table

19) steps to follow, Designing, frequency of operation

20) Self start counter concepts, identification of mod

21) Identification of mod of counter?

22) State diagram, how to make state diagram table?

23) sequence detector

① mealy, o/p, properties,

② moore