

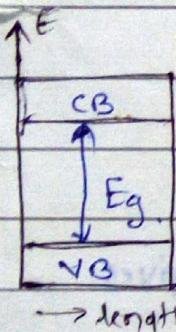
- * if charge carrier moves through a unit cross sectional area, then unit time current produced

$$i = \frac{dq}{dt}$$

- * If external force applied to an e^- more than the e^- force applied by the nucleus then e^- comes out of attraction of nucleus such free are mobile e^- can support current.

- * move away from nucleus Force of attraction reduces
for conductivity valence shell e^- are considered since it is farthest shell from the nucleus.

* Intrinsic Semiconductor



when e^- gets energy in VB it moves to CB & becomes free. $Eg = E_c - E_v$

Eg increases material becomes more and more insulator.

$Eg \approx 6\text{ eV}$ (insulator) $Eg \approx 0\text{ eV}$ conductor $Eg \approx 1\text{ eV}$ semicond.

At 300°K e^- break covalent bond becomes free can be drifted by providing external voltage to produce electron drift current I_n to make the material conductor.



e^- current (I_n)

Hole current (I_p)

	1) A free e^- is moving	1) An e^- is moving from one bound state to other.
	2) An e^- is moving in conduct. Band	2) An e^- is moving in valence band
	3) An e^- is moving at higher energy level	3) An e^- is moving at lower energy level
	4) An e^- is moving through inter atomic gap.	4) An e^- is moving from one covalent bond to other.

- * Non existence of e^- in covalent bond is space hole effects proved that Hole is existing true charge particle, not imaginary.
- * if one e^- goes to conduction band it leaves a hole in valence band hence called Electron hole pair generation (EHP).
- * In an intrinsic semiconductor free e^- concentration (n) is equal to the hole concentration (p) i.e. $(n=p)$
- * But in intrinsic semiconductor e^- current I_n is greater than hole current I_p bcoz. mobility of e^- is greater than mobility of hole
- * (drift current) $\rightarrow I = I_n + I_p$. $\frac{\text{hole conc.}}{\text{charge}} \frac{\text{mobility}}{\text{Electric field}} \times \text{Area}$
 $= nqU_n EA + pqU_p EA \rightarrow \text{Area}$
- * electrons & holes move in opposite direction but gives current in same direction.

$$\sigma = nqU_n + pqU_p$$

$$R = \frac{l}{\sigma A} = \frac{S l}{A}$$

$$\sigma = \frac{1}{S}$$

* Extrinsic Semiconductor:

All EDC devices are made up of extrinsic semiconductor

* Extrinsic -ve type, n type semiconductor.

Pentavalent impurities Phosphorous, Arsenic, Antimony
bismuth (Donors) $No \rightarrow$ Donor conc.

one pentavalent atom replace one tetravalent atom of silicon or germanium four covalent bond & $1 e^-$ excess.

All such excess e^- occupy in energy level E_D below conduction band. 0.01 eV for germanium
0.05 eV for silicon.

* Pentavalent impurities loses excess e^- becomes +ve ion called impurity ionisation. (I-I)

* e^- moves from E_D to C_B. not create hole since they are excess e^- Not covalent bond e^-
but at 300°C. EHP or BB starts. & σ increases, R_t, I_{PSS}

$$\text{II} \quad I = I_n(I\cdot I\cdot) + I_n(B\cdot B) + I_p(B\cdot B)$$

$$\therefore n \neq p \quad I_n > I_p \quad \underline{n > p}$$

majority carriers $\rightarrow e^-$ minority carriers \rightarrow Hole
Majority current $\rightarrow 2n$ minority current $\rightarrow I_p$.

* We can't say majority current is always greater than minority current.

* Extrinsic +ve type or P-type semiconductor.

Trivalent impurities like boron, Aluminium, gallium or Indium (Acceptors) $N_A \rightarrow$ Acceptor conc.

3 valence e^- are supplied but one excess hole created.

all such excess hole occupy at 0K a new energy level above VB. at 0.01eV for Ge. 0.05eV for silicon.

called EA

P>n

majority carriers - holes

minority carriers - e^-

majority current - I_p

minority current - I_n .

At very high temperature all extrinsic semiconductor becomes intrinsic because Band to band transition i.e. EHP dominates over impurity ionisation & at this temperature usefulness of device will get terminated.

* Mass action law:-

product of n & P at given temp. is constant

$$NP = n_i^2 \quad (n_i \text{ intrinsic conc.})$$

$$\boxed{n_i^2 = A_0 T^3 e^{-E_{go}/RT}}$$

E_{go} - energy band gap at 0°K .
 A_0 - constant.

$$N_D + P = N_A + n \quad N_D, N_A - \text{donor or acceptor conc.} \\ P, n - \text{hole, free-conc.}$$

$$\textcircled{1} \rightarrow \text{for intrinsic } N_D = 0, N_A = 0 \therefore \underline{\underline{P = n}}$$

$$\therefore \boxed{n = P = n_i}$$

$$\textcircled{2} \rightarrow \text{for n-type } N_D > 0, N_A = 0 \quad P_n \ll \ll \\ \therefore \boxed{n_n \approx N_D} \Rightarrow P_n = \frac{n_i^2}{n_n} = \frac{n_i^2}{N_D}$$

$$\textcircled{3} \rightarrow \text{for P-type } N_D = 0, N_A > 0 \quad n_p \ll \ll \\ \boxed{P_p \approx N_A} \Rightarrow n_p = \frac{n_i^2}{P_p} \approx \frac{n_i^2}{N_A}$$

* Diffusion :-

from higher concentration to lower concentration.

$$\text{for P-type} \rightarrow J_p(x) = \frac{I_p}{A} = -q D_p \frac{dp}{dx} \quad D_{pp} - \text{diff. const.} \\ J \rightarrow \text{current density.}$$

$$\text{for N-type} \rightarrow J_n(x) = \frac{I_n}{A} = +q D_n \frac{dn}{dx}$$

$$* J = \frac{I}{A} = \sigma E = (n q u_n + p q u_p) E$$

A charge carriers moves due to difference in concentration
 is diffusing & charge carriers moves due to attractn
 & repulsion is drifting

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = \frac{V_F}{1} = \frac{kT}{1} = \frac{q}{k} = \frac{T^0 K}{11600} = 0.026 \quad (\text{at } 300^\circ\text{K})$$

Thermal | Bolt. | Boltzmann
 vltg cont. cont. in J/ok
 in eV/K

* generation and Recombination of charge carriers.

during EHP Generation e^- becomes free & hole is created while in Recombination ~~area~~ free e^- becomes bound and hole disappears hence current decreases.

τ_n, τ_p duration of time for which e^- & hole support current

$L_n & L_p$ is distance traveled by e^- & hole then

$$L_n = \sqrt{D_n \tau_n} \quad \& \quad L_p = \sqrt{D_p \tau_p}$$

* Variation in minority carrier concentration (for n type).

with time: $\rightarrow P_n(t) = P_{n0} + P'_n(0) e^{-t/\tau_p}$ $\rightarrow P'_n(t)$

. total hole concentration at any time $t \rightarrow P_n(t)$

excess hole concentration at $t=0 \rightarrow P'_n(t)$

Initially thermally generated minority carriers $\rightarrow P_{n0}$

$$\text{at } t=0 \quad P_n(0) = P_{n0} + P'_n(0)$$

$$\text{at } t=\infty \quad P_n(\infty) = P_{n0}.$$

% Increase in minority carrier conc. due to

Illumination is very much greater than percentage increase in majority carrier conc.

with Distance: $\rightarrow P_n(x) = P_{n0} + P'_n(0) e^{-x/L_p} \rightarrow P'_n(x)$

$$\ast P_{n0} \cdot n_{n0} = \frac{q^2}{2} P_{n0} - \text{hole conc.}$$

$n_{n0} = e^- \text{ conc.}$

* Current in diode \rightarrow voltage across diode (or diode voltage).
 (Forward current) $F.I.C \leftarrow + I = I_0 (e^{\frac{V}{nN_T}} - 1)$

R.I.C
(Reverse current)

* Fermilevel

existing e^- in CB & Non-existing e^- in VB both can support current. To comment on conductivity we should know the existing or non-existing of e^- at a given energy level. To comment this Fermi-Dirac distribution function or Fermi-Dirac probability function is defined

$$\textcircled{1} \quad F(E) = \frac{1}{1 + e^{(E-E_F)/kT}}$$

$F(E)$ probability of existence of e^- at an allowed energy level $0 < F(E) \leq 1$

E_F Fermi energy Level (Imaginary)

Comments on 50% occupancy.

Fermilevel in intrinsic Semiconductor

free e^- conc. $\rightarrow \textcircled{2} \quad n = N_c e^{-(E_C - E_F)/kT}$

$$\begin{aligned} \textcircled{3} \quad N_c &= 2(2\pi m_n \bar{R} T / h^2)^{3/2} \\ &= 4.82 (m_n T / m)^{3/2} \text{ cm}^{-3} \end{aligned}$$

$1 - F(E) \rightarrow$ Non-existence of e^- in CB or VB

\Rightarrow Existence of hole in valence band only

hole conc. $\rightarrow \textcircled{4} \quad p = N_v e^{-(E_F - E_V)/kT}$

$$\begin{aligned} \textcircled{5} \quad N_v &= 2(2\pi m_p \bar{R} T / h^2)^{3/2} \\ &= 4.82 \times 10^{15} (m_p T / m)^{3/2} \text{ cm}^{-3} \end{aligned}$$

N_c, N_v densities of energy states at CB & VB. (constant at const temp)

m_n, m_p effective mass of e^- & hole.

m - mass of e^-

k - Boltzmann constant in eV/K $\bar{R} = \text{B. const. J}/\text{K}$

h - Planck's constant.

For intrinsic semiconductor $n = p \therefore$ equate eqn $\textcircled{2}$ & $\textcircled{4}$

$$\textcircled{6} \quad E_F = \frac{E_C + E_V}{2} - \frac{kT}{2} \ln \left(\frac{N_c}{N_v} \right)$$

* if $m_n = m_p$ then $\textcircled{7} E_{F_i} = (E_c + E_v)/2$

\Rightarrow intrinsic Fermilevel lies at the centre of forbidden band if $m_n = m_p$.

Substituting $\textcircled{5}$ & $\textcircled{6}$ into $n \cdot p = n_i^2$ we get

$$\textcircled{8} E_g = kT \ln(N_c N_v / n_i^2)$$

Fermilevel in extrinsic semiconductor.

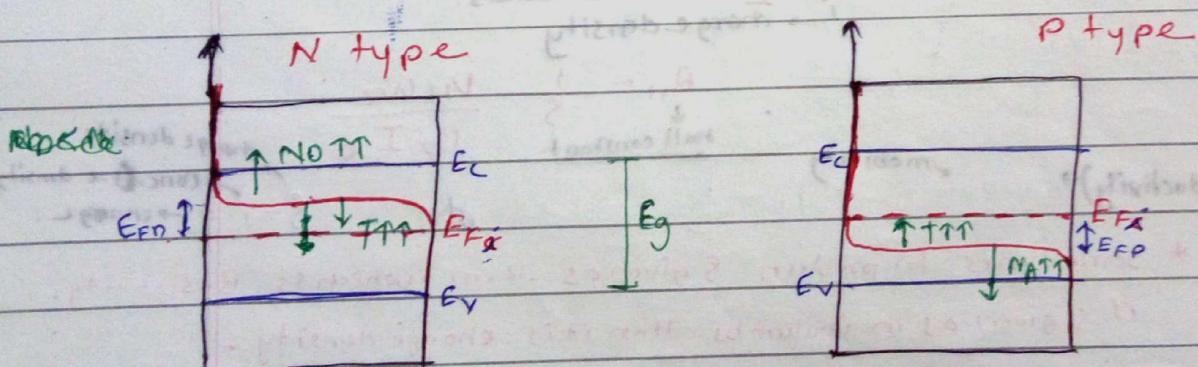
At room temp. probability of existence of e^- in CB. of N-type semicon. is greater than the probability of existence of e^- in CB. of intrinsic semicon.

Hence Fermilevel moves closer to CB in N-type than intrinsic.
for N type $n_n \approx N_c$ \therefore by eqn 2 we get.

$$\textcircled{9} E_{F_n} = E_c - kT \ln(N_c / N_n)$$

for P type $p_p \approx N_A$ \therefore by eqn 4 we get

$$\textcircled{10} E_{F_p} = E_v - kT \ln(N_v / N_A)$$



\rightarrow NOTT: Fermilevel move closer to E_c

\rightarrow TTT: Fermilevel go closer to E_F

\rightarrow NA TTT: Fermilevel move closer to E_v

\rightarrow NATT: Fermilevel going toward E_F

$$\textcircled{11} E_{F_n} - E_{F_i} = kT \ln(N_c / n_i)$$

$$N_D: N_D < N_c \rightarrow E_{F_n} < E_c$$

$$N_D: N_D = N_c \rightarrow E_{F_n} = E_c$$

$$N_D: N_D > N_c \rightarrow E_{F_n} > E_c$$

$$\textcircled{12} E_{F_p} - E_{F_i} = kT \ln(N_A / n_i)$$

$$N_A: N_A < N_v \rightarrow E_{F_p} > E_v$$

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* Fermilevel in open circuited PN Diode.

using eqn ⑪ & ⑫.

$$E_1 = KT \ln \left(\frac{N_A}{n_i} \right)$$

$$E_2 = KT \ln \left(\frac{N_D}{n_i} \right)$$

$$E_0(\text{ev}) = E_C - E_N = E_{Cp} - E_{Np}$$

$$E_1 + E_2 = KT \ln \left(\frac{N_A N_D}{n_i^2} \right)$$

$E_0(\text{ev}) = V_0(\text{Vats})$
contact potential

$E_0(\text{ev})$ shift between V_B or V_B in PN diode.

* Fermilevel is constant throughout the length in open circuited PN diode whereas not constant in FB or RB, p-n.

* Hall Effect.

If a semiconductor carrying current I_x is placed in transverse magnetic field B_z then electric field E_y is induced in y direction \perp to I_x & B_z .

$$V_H = B_z I_x$$

\downarrow w_z \rightarrow width on z axis.
 \downarrow charge density

$$E_y = \frac{V_H}{w_z}, \quad E_x = \frac{V_x}{L_x} \quad R_H = \frac{1}{S} = \frac{V_H w_z}{B_z I_x}$$

$$(\text{conductivity}) \rightarrow \sigma = S \mu \quad \xrightarrow{\text{mobility}} \mu = \frac{S}{\sigma} \quad \rightarrow \mu = \frac{R_H}{B_z} \quad S = n q \rightarrow \text{charge density}$$

* sometimes in problem S given as Ωcm which is Resistivity.

if S given as in coulombs then it is charge density.

$$\text{for } S \text{ as resistivity} \rightarrow \mu = \frac{R_H}{S}$$

Applications

- ① used to find type of semiconductor (n or p type) by V_H polarities.
- ② used to find charge density & hence carrier concentration
- ③ given mobility conductivity can calculate & vice versa.
- ④ can be use to multiply two signals (Hall effect multiplier)

$$* J_x = \frac{I_x}{A} = \frac{I_x}{w_z dy} = S v_e = S \mu n E_x \Rightarrow \frac{I_x}{B_z w_z} = S \mu n E_x dy$$

\downarrow drift velocity. \downarrow electric field
 \downarrow mobility. \downarrow charge density

$$* V_H = E_y dy.$$

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Fermilevel in extrinsic semiconductor.

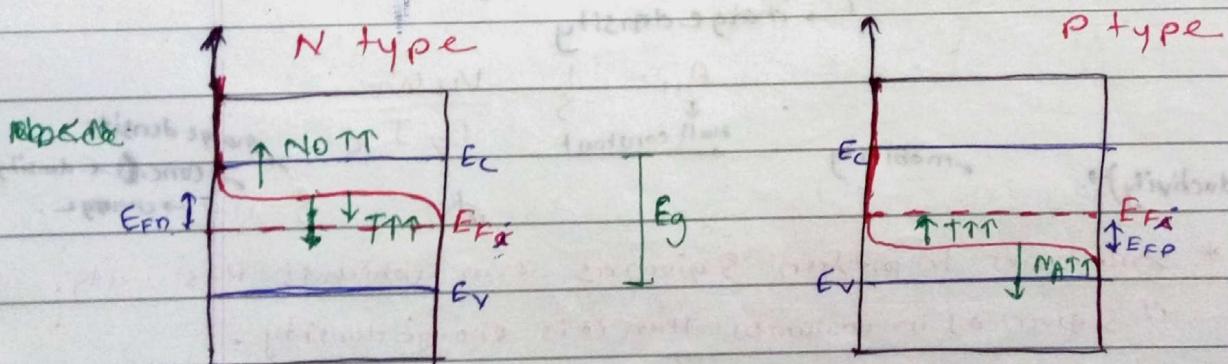
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\rightarrow NDT↑es Fermilevel move closer to E_c

\rightarrow T↑se Fermilevel going closer to E_c

\rightarrow NAT↑es Fermilevel move closer to E_v .

\rightarrow T↑se Fermilevel going toward E_v .

$$\textcircled{11} E_{F_n} - E_{F_i} = KT \ln (N_D / n_i)$$

N_D: $N_D < N_c \rightarrow E_{F_n} < E_c$

NDT↑: $N_D = N_c \rightarrow E_{F_n} = E_c$

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$$\textcircled{12} E_{F_p} - E_{F_i} = KT \ln (N_A / n_i)$$

by P=NA

N_A: $N_A < N_v \rightarrow E_{F_p} > E_v$

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NAT↑↑: $N_A > N_v \rightarrow E_{F_p} < E_v$.

* Fermilevel in open circuited PN Diode.

using eqn ⑪ & ⑫.

$$E_1 = RT \ln(\frac{N_A}{n_i})$$

$$E_2 = RT \ln(\frac{N_D}{n_i})$$

$$E_{0(\text{ev})} = E_C - E_N = E_C - E_{V_N}$$

$$E_1 + E_2 = RT \ln(\frac{N_A N_D}{n_i^2})$$

$$E_{0(\text{ev})} = V_0 (W_{\text{eff}})$$

(contact potential)

$E_{0(\text{ev})}$ shift between CB or VB in PN diode.

* Fermilevel is constant throughout the length in open circuited PN diode whereas not constant in FB or RB, PN.

* Hall Effect.

If a semiconductor carrying current I_x is placed in transverse magnetic field B_z then electric field E_y is induced in \perp direction to I_x & B_z .

$$V_H = B_z I_x$$

$\begin{matrix} \hookrightarrow \\ W_z \end{matrix}$ → width on z-axis.
 $\begin{matrix} \downarrow \\ \text{charge density} \end{matrix}$

$$E_y = \frac{V_H}{d}, \quad E_x = \frac{V_x}{L_x}, \quad R_H = \frac{1}{S} = \frac{V_H W_z}{B_z I_x}$$

$$(\text{conductivity})^{\sigma} = S \mu \xrightarrow{\text{mobility}} \mu = \frac{\sigma}{S} \rightarrow \mu = \frac{R_H}{B_z} \quad S = n q \xrightarrow{\text{charge density}}$$

* sometimes in problem S given as Ωcm which is Resistivity.

if S given as in coulombs then it is charge density.

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Applications

- ① used to find type of semiconductor (n or P type) by V_H polarities.
- ② used to find charge density & hence carrier concentration
- ③ Given mobility conductivity can calculate & vice versa.
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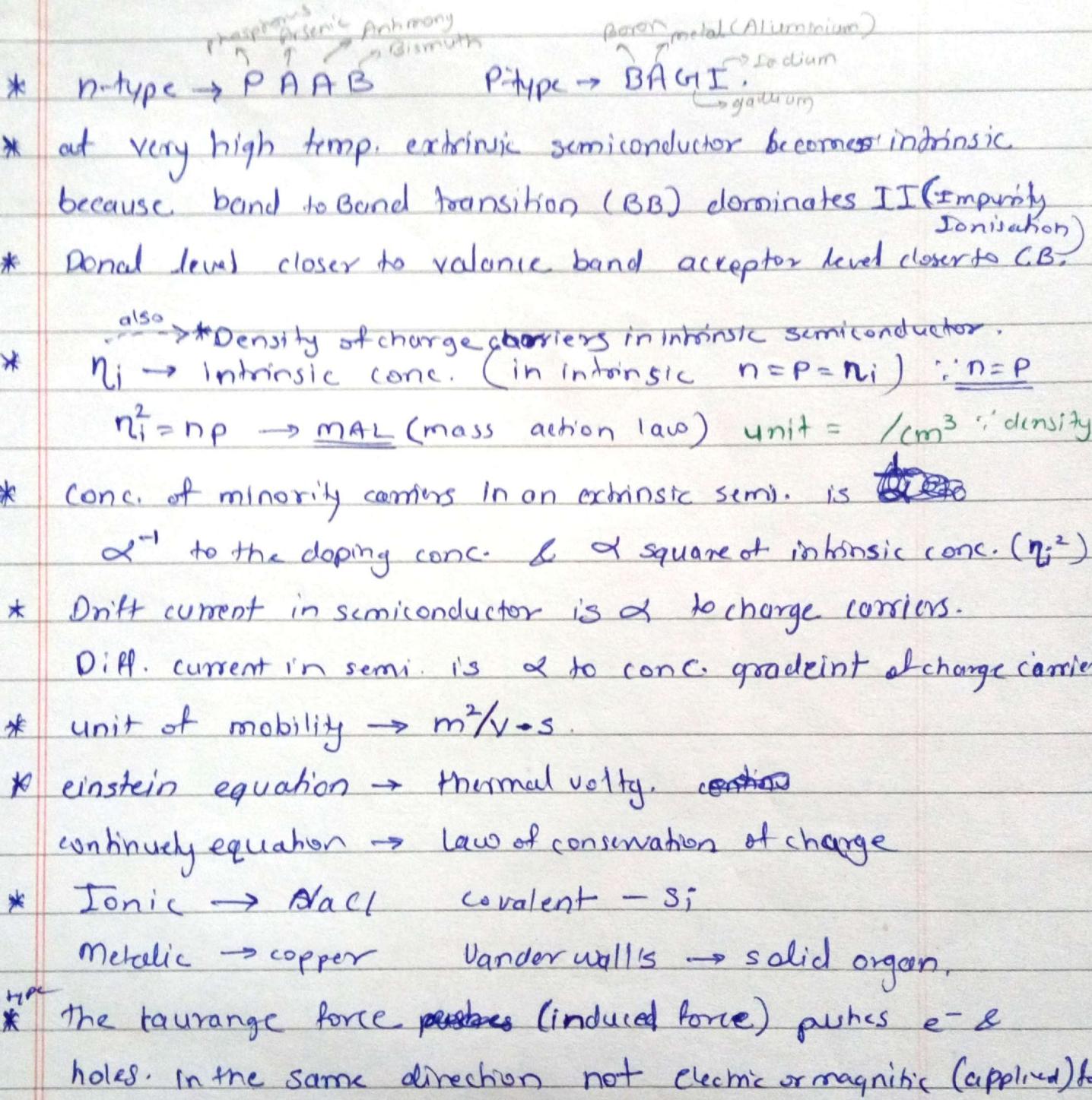
$$* I_x = \frac{I_x}{A} = \frac{I_x}{W_z d} = S V_e = S \mu n E_x \Rightarrow \frac{I_x}{B_z} = S d n E_x d y$$

\downarrow drift velocity
 \downarrow electric field
 \downarrow mobility
 \downarrow charge density

$$* V_H = E_y d y.$$



Date : / /



* Diodes

* P-N Junction diode

|| Open circuit at PN diode.

→ A barrier form due to EHP Recombination at the center.

→ barrier or depletion Region having ions hence called space charge region

Applications:- It switch or Voltage variable capacitor.

→ Barrier opposes the flow of majority carriers but supports flow of minority carriers.

→ majority carrier gives diffusion current minority carrier give drift current.

* open ckt contact potential $V_0 = kT \ln \left(\frac{N_D N_A}{n_i^2} \right)$ Volts.

* open ckt electric field intensity $E_0 = \frac{-q N_D x_{n_0}}{\epsilon} = \frac{-q N_A x_{p_0}}{\epsilon}$ V/m.

* Depletion width $w = x_{n_0} + x_{p_0}$

Total -ve charges lost in the depletion Region of n side is equal to total positive charge lost in depletion region of p side. $\therefore N_D x_{n_0} = N_A x_{p_0}$

$$x_{n_0} = \frac{w}{N_D + N_A} \quad x_{p_0} = \frac{w}{N_D + N_A} N_A$$

$$w = \sqrt{\frac{2eV_0}{q} \left[\frac{1}{N_D} + \frac{1}{N_A} \right]}$$

V_0 = built in potential if no bias

$V_0 = V_j$ when bias

$(V_d = -ve value if RB i.e. V_0 + V_B)$ $V_g = V_0 - V_d$ \rightarrow built in potential
 $\{ ve value if FB i.e. V_0 - V_B \}$ $0.8V$

* Penetration of depletion Region in to n side (x_{n_0}) is proportional to doping of p side (N_A) & vice versa

$$\text{if } N_D = N_A \rightarrow x_{n_0} = x_{p_0}$$

$$x_{n_0} \propto N_A$$

$$N_D \neq N_A \rightarrow x_{n_0} \neq x_{p_0}$$

$$x_{p_0} \propto N_D$$

* Depletion Region penetrates more in to lightly doped side. $N_D > N_A \rightarrow x_{p_0} > x_{n_0}$

* if one side is heavily doped that side penetration can be neglected.

- * forward bias:- (P side more +ve than n side)
- * Cut in voltage / offset voltage / breakpoint voltage / threshold voltage (V₀) is minimum FB for current to exist width of depletion Region decreases.

- * Reversed bias:- (P side less +ve (or more -ve) than n side)

- width of depletion Region increases.
- minority carriers drift supports current from n to P.
- very small 11 amp in germanium nAmp in silicon
- Reverse current is independent of Reverse voltage.

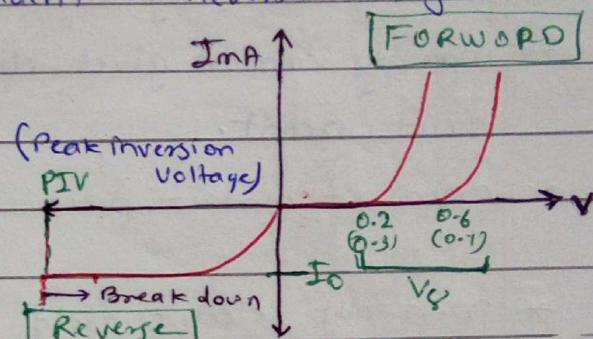
* Voltamp characteristics

$$I = I_0 (e^{\frac{V}{nV_T}} - 1)$$

$$\begin{aligned} n &= 1 \text{ Ge} \\ &= 2 \text{ Si} \end{aligned}$$

F.B.: V = +ve if $e^{\frac{V}{nV_T}} \gg 1$ then $I = I_0 e^{\frac{V}{nV_T}}$

R.B.: V = -ve if $e^{\frac{V}{nV_T}} \ll 1$ then $I = -I_0$



* Silicon over Germanium

- I_0 of Ge > I_0 of Si hence Si acts as better switch
- PIV of Ge < PIV of Si gives better operable range.
- Eg of Ge < Eg of Si gives better thermal range.
- Si available abundant Raw material.

* Diode Resistance

* DC or static Resistance $R_{DC} = \frac{V}{I}$

at operating point find voltage & current & take ratio

* AC or Dynamic Resistance $R_{AC} = \frac{dV}{dI} = \frac{1}{\tan \phi} = \frac{1}{\text{slope}}$

take slope in VI characteristics

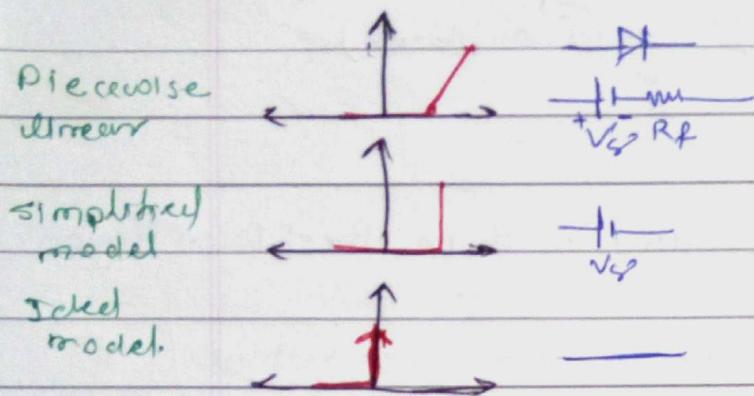
$$r_{AC} = nV_T/I \rightarrow \text{for FB only.}$$

$$= \frac{nV_T}{I_0} e^{-\frac{V}{nV_T}} \rightarrow \text{for FB \& RB}$$

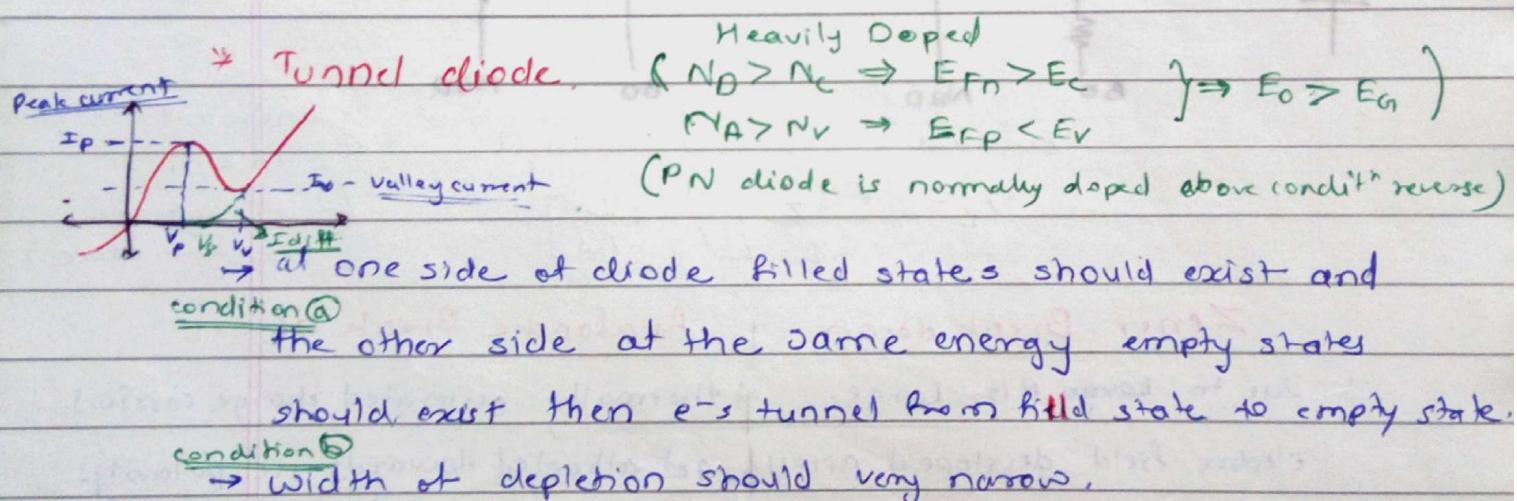
* $V_T = 0.026$ is valid only at 27°C i.e. 300K.

$$\text{at different Temp } T \text{ find } V_T = \frac{T^\circ\text{K}}{11,603}$$

* Diode Equivalent ckt. (Valid for FB) (in RB is o.c)



* Q point is defined as intersection of load line with VI characteristic



* open circuit \rightarrow condition @ not satisfied \therefore No tunneling
 \therefore current is 0.

* Reverse bias :- tunneling of e^- from filled state to empty state in RB from P to N side. hence reverse current exists. as RB uses tunneling & hence Reverse current uses. \therefore Excellent conduction is possible in RB.

* Forward bias:- (tunneling of e^- from N to P. current from P to N)

$$I_{net} = I_{tunnel} + I_{diffusion}$$

between $V_P & V_V$ as $V < V_{tse}$ $I < 0$ hence called (Negative Resistance betn $I_P & I_V$ V_1, V_2, V_3 can apply). Tripple value region (TVR) Region

NRR

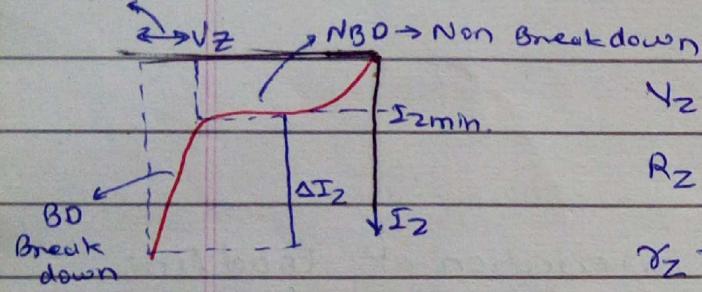
* Application :

- 1) High speed switching characteristics
- 2) High freq. oscillators. 3) Digital Design.

(VJT also exhibit NRR & used in oscillator)

* Zener Diode.

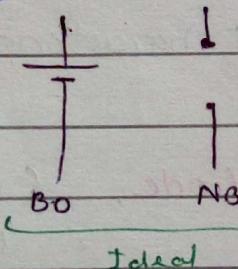
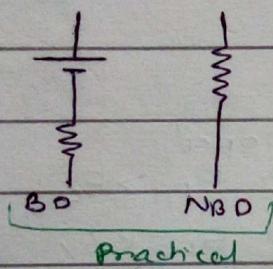
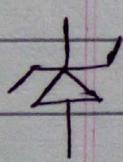
Zener diode can be operated in Reverse Breakdown Region.



$V_z \rightarrow$ knee or breakdown voltage.

$R_z \rightarrow$ Dynamic Reverse Breakdown Resistance

$$r_z = \frac{\Delta V_z}{\Delta I_z}$$



} equivalent ckt.
in R.B.

$$V_z = \frac{E_z^2}{2q} \left[\frac{1}{N_D} + \frac{1}{N_A} \right] \quad (\text{for FB eq. ckt same as diode})$$

Zener Breakdown

* Due to ~~large~~ RB Large electric field developed across zener diode pulls out charge carriers by rupturing covalent bond. & making atoms as ions.

Avalanche Breakdown

* thermally generated charge carriers get attracted towards the polarity. of applied RB. KE \Rightarrow Velocity or momentum transfer to the e^- at valence shell atom which collides & becomes two charge carriers in this way multiplication is done. Atom becomes Ion.

* Field Ionisation

* occurs in relatively more doped Step junction diode.

* occurs in relatively light doped linear junction diode

$V_z < 6V \text{ & } \frac{dV_z}{dt} = (-0.1\%) / \tau$

$* V_z > 6V \quad \frac{dV_z}{dt} = +0.1\% / \tau$

* Zener diode as voltage regulator (VR)

→ VR maintains constant voltage across terminals of load irrespective of fluctuation in load or supply.

→ Zener diod as VR in two condition satisfied.

conditions

① Current through Z.D. should be greater than or equal to $I_{z\min}$

② Voltage across terminals of zener diode, should be V_Z

while solving Numericals

P.e. Breakdown voltage

1 → Identify diode Ideal or practical.

2 → If FB. replace eq. ckt of PN diode in FB. any of the three

3 → If RB verify Break down status & replace eq. ckt. of Z.D.

4 → apply KVL, KCL

$$(F_i x e d \ i_R \ v a r i a b l e \ R_L) I_S(fix) = \frac{I_{Z(\max)} \text{ when } R_L \max}{I_{Z(\max)} + I_{L(\min)}} = \frac{I_{Z(\min)} \text{ when } R_L \ min.}{I_{Z(\min)} + I_{L(\max)}} \quad V_L \text{ constant}$$

$$(V a r i a b l e \ i_R \ R_f x R_L) I_S(fix) = \frac{I_{S(\max)} \text{ when } V_L \ max}{I_{S(\max)} - I_{Z(\max)}} = \frac{I_{S(\min)} \text{ when } V_L \ min.}{I_{S(\min)} - I_{Z(\min)}} \quad V_L \text{ constant}$$

* if I_Z, V_Z, r_Z not given the consider Ideal zener diode

& take $I_{Z(\min)}=0, r_Z=0, V_Z=10V$

* while solving taking zener in ~~RB~~ & BD region verify the condition ② by physically removing ZD & finding voltage.

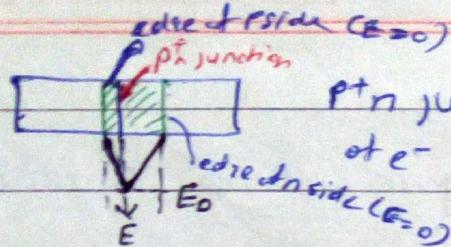
V_{AB} . if $V_{AB} < 10$ NO Not in BD replace by O.C.

if $V_{AB} \geq 10$: in BD ∴, replace by 10V. i.e. V_Z .

* max rating of zenerdiode $P_Z(\max) = V_Z \times I_{Z(\max)}$

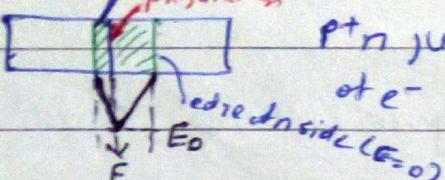
* ZTCVR (zero temperature coefficient voltage Reference)

If D_1 are $N^+ D_2$ -ve Temp. volt. to maintain constant voltage.



p⁺n junction diode under reverse bias magnitude

of e⁻ field max at p⁺n junction

- *  p⁺n junction diode under reverse bias magnitude of e⁻ field max at p⁺n junction
- * ideality factor or nonideality coefficient (m) $\approx \eta$ in some problems
- * in diode the value of currents depends exponentially on the voltage apply
- * static resistance of diode $= \frac{V}{I}$ dynamic $= \frac{dV}{dI}$
- & dynamic conductance $g = \frac{1}{V} = \frac{I}{AV_T}$ directly \propto to current.
- * $I_{D2} = I_{D1} 2^{(T_2 - T_1)/10}$
- * change in barrier potential of si p+n diode with temperature is $-2.5 \times 10^{-3} \text{ V}/^\circ\text{C}$.
- * tunnel diode is made of Ge or GaAs.; an abrupt junction with both sides heavily doped.
- * Schottky diode contains metal-semiconductor junction.

* BJT \rightarrow early effect, High current gain, Amp^r, current control device



* JFET \rightarrow Pinch off voltage, voltage control device, pinch off effect
high i/p impedance, low gain bandwidth

* MOSFET \rightarrow High i/p impedance

* LASER diode \rightarrow Population inversion, forward Bias, coherent Radiation.

* MOS capacitance \rightarrow Flat band voltage,

* Silicon diode \rightarrow Very low reverse bias saturation current, Rectifier.

* Variable capacitance diode \rightarrow used under RB condition

* germanium diode \rightarrow low FB votg drop.

* direct bandgap material \rightarrow GaAs

* LED \rightarrow cut off wavelength, direct bandgap semicon. material.

used under F.B., spontaneous emmission, injection electro-luminescence

* Photodiode \rightarrow working on photoelectric effect.

PIN-Diode

* ~~Varactor~~ \rightarrow High freq. Applicatⁿ, photo detection, High speed switching device, current control attenuator.

~~Varactor~~ \rightarrow Varactor diode \rightarrow Tuned ckt.

~~Tunnel~~ \rightarrow Tunnel diode \rightarrow microwave amplificatⁿ, -ve resistance characteristics, F.B.,
~~Schottky~~ voltage control -ve Resistance oscillator, Heavy clapping, high speed switching, multi-vibrator ckt,

~~Zener~~ \rightarrow Zener diode - voltage regulatⁿ, RB, Vtg stabilizer or reference.

* Solar cell \rightarrow R.B, $\delta\gamma$, optical energy into electrical energy.

* Avalanche photodiode \rightarrow R.B - to cause Impact ionisation, current gain.

* Schottky diode \rightarrow High speed switching. Use majority carriers for high freq. ^{high sensitivity}

* VJT \rightarrow -ve conductance device, -ve resistance for oscillator. ^{operation}

* SCR \rightarrow controlled rectification

* Gunn diode \rightarrow microwave oscillator. ^{# IMPATT diode} \rightarrow conductivity modulatⁿ device.

* Opto Electronic Devices.

- * LED & LASER convert electrical energy to light energy and are used as optical sources.
- * PIN & APD convert light energy to electrical energy & are used as optical detectors. in fiberoptic comm.
Dissipative Recombination
- * EHP Recombination by two steps i.e. Indirect Recombination,
Eg convert to heat. Indirect bandgap semiconductors are, Si.
Radiative recombination.
- * EHP Recombination by single step i.e. direct Recombination
Eg converts to radiation. direct bandgap semi-conductors gallium arsenide.
- * the wavelength & color emitted depends on Eg.
- $$\lambda(\text{nm}) = \frac{1.24}{E_g(\text{eV})}$$
- * If pN diode designed by direct bandgap semiconductor then work as LED.
- * To produce required colour two or more direct B.G. semi. used to form compound having Eg which is required to get certain color d.
- * LED (Light emitting diode) (emission occurs after life time) (spontaneous emission)
Adv. \rightarrow small size, less wt., low cost, long life, low power consumptn.
temp-dependence is less
- disadv. \rightarrow Not highly directional, Not highly chromatic.

* LASER. (Light Amplification By stimulated Emission of Radiation) (stimulated emission) (emission occurs before life time)

- * A photon injected in to cavity disturbs e⁻ during recombintn. generate another photon & process repeats & due to internal light amplification luminescent photons generated
- Adv. \rightarrow ^{invert} dis adv. of LED / Disadv. \rightarrow ^{invert} adv. of LED (e.g. Large size)

* PIN (photodiode)

- \rightarrow A photon incident on semiconductor having energy greater or equal to Eg of semi. carrier are generated leads to photo current (I_P).
- \rightarrow In absence of light thermally generated minority carriers support current I₀ called dark current.

Energy of photon \propto Planck's constant \propto speed of light.

$$E_\lambda = hf = \left(\frac{hc}{\lambda} \right) \quad \rightarrow \lambda_{(\max)} (\mu m) = \frac{1.24}{E_g (eV)}$$

$E_\lambda \geq E_g$

Quantum efficiency $\eta = \frac{\text{No. of EHP's generated}}{\text{No. of photons Incident}} = \frac{IP/q}{P_0/hf}$

Responsivity $R = \frac{IP}{P_0} = \frac{nq}{hf}$ Amp/Watt.

* Avalanche photo diode (APD)

Incident photon generates photo carriers pass through $N^+ P$ junction. Hence avalanche breakdown occurs. & avalanche multiplication starts $m = \frac{I_m}{I_p} \rightarrow$ current generated in APD due to P_0 . Current in PNP diode due to P_0 .

$$R_{APD} = \frac{nq}{hf} \cdot m. \quad * (I_m \rightarrow \text{multiplied photo current})$$

* Transition Region or Depletion Region or space charge region or barrier capacitance. (C_T) (due to change in RB)

$$C_T = \frac{EA}{W} \rightarrow \text{cross sectional area.} \quad W \propto V_j^{1/2} \text{ for step or abrupt junction}$$

$W \rightarrow \text{width of depletion Region}$

$V_j \rightarrow \text{open circuit contact potential}$

$V_j = V_0 - V_d \rightarrow \text{voltage across diode.}$

$$W \propto V_j^{1/2} \rightarrow \text{step or abrupt junction}$$

$$W \propto V_j^{1/3} \rightarrow \text{graded or linear junction}$$

$$C_T = \sqrt{\frac{2EA^2}{2\left(\frac{1}{N_D} + \frac{1}{N_A}\right)(V_0 - V_d)}} \quad \text{at } 0 \text{ bias}$$

$$C_{T0} = C_T |_{V_d=0}$$

$$C_T = \frac{C_{T0}}{\left(1 - \frac{V_d}{V_0}\right)^{m_T}} \quad m_T = 0.5 \text{ for step junction}$$

$$= 0.33 \text{ for linear junction.}$$

can be used as voltage variable capacitor \therefore change in PB change \rightarrow capacitance.

* Diffusion Capacitance (C_D) (due to change in FB)

$$C_D = \frac{\gamma I}{\eta V_T} \quad \rightarrow \text{life time.}$$

$$\gamma = \gamma_p + \gamma_n$$

* BJT

applications \rightarrow switch, amp^r, phase shifter, oscillator.

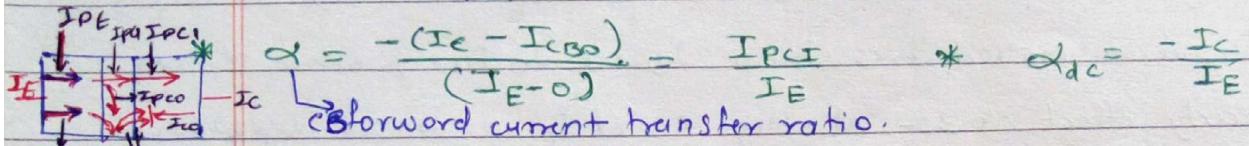
BJT works as amp^r if ① o/p is exact replica of i/o

② o/p energy greater than i/p energy.

* current component in C(B(PNP))

$$* I_E = I_{PE} + I_{NE} \approx I_{PE} * -I_{CO} = -I_{CBO} = I_{PCO} + I_{NCE}$$

$$* I_C = |I_{CEI}| + I_{CBO} * I_C = |-\alpha I_E| + I_{CBO}$$



$$* r^* = (I_{PE}/I_E) \approx 1 * \beta^* = (I_{PCO}/I_{PE}) \approx 1$$

$$* \alpha = r^* \beta^* = (I_{PCO}/I_E) \approx 1 \rightarrow \text{base transport factor.}$$

↳ Emitter efficiency or emitter injection.

$$(\alpha = \frac{\beta}{1+\beta})$$

Dopping	Heavy	less (light)	Moderate
width	moderate	thin (narrow)	Large

J _E	J _C	R _O O (Region of operation)	Application
F _B	F _B	Saturation	ON switch
R _B	R _B	cutoff	OFF switch
F _B	R _B	Normal Active	Amp ^r
R _B	F _B	Inverse Active	Attenuator

* Thermal Runaway:-

when $I_E \uparrow$ s.e., $P_c \uparrow$ s.e. $\rightarrow T_{je} \uparrow$ s.e. $\rightarrow I_{CBO} \uparrow$ s.e. $\rightarrow I_C \uparrow$ s.e. & soon

\therefore Transistor burnt away to avoid collector size is large such that I_C power P_c per unit area \uparrow s.e.

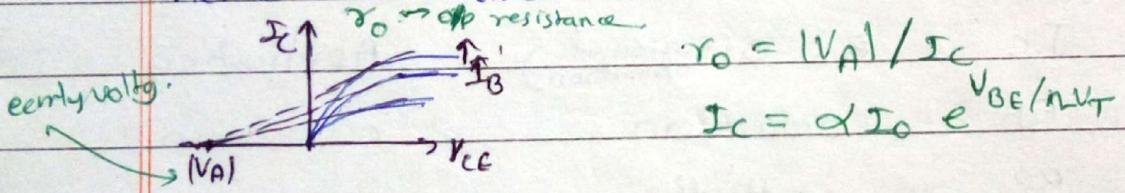
AN AT ~~as~~ * two PN diode connected back to back can not

- CB act as a transistor (amp^r) They act as attenuators
 CE
 CC

* By making base less doped & thin in size recombination of holes in base is not allowed hence large current I_E is forcedly transferred from low resistance (J_E, F_B) to high resistance (J_C, R_B) hence device exhibiting transfer resistance property.

- * Early Effect or Base width modulation or narrowing.
- * early effect no1 :- As Reverse Bias J_c Tses W_B' width decreases. concentration gradient increases. as diffusion current due to base gradient $\propto J_{diff}$ Tses hence I_E Tses.
- * early effect no.2 :- As R_B J_c Tses W_B' width & \propto width for recombination Tses hence I_B Tses $\propto I_c$ Tses & hence I_c Tses
- * early effect No.3:- at large R_B at J_c width of depletion region Tses so that W_B' becomes 0 $\therefore I_B = 0$
 \therefore transistor can not act as amp^r called punch through or reach through.

- * out of W_B only W_B' is useful for recombination hence called effective base width. change in V_{CB} (ie. R_B) changes W_B' hence called base width modulation as V_{CB} Tses W_B' Tses.



$$r_0 = |V_A| / I_C$$

$$I_C = \alpha I_0 e^{V_{BE}/nV_T}$$

* Avalanche Breakdown.

- * At large R_B to J_C collector junctⁿ undergo Avalanche Break down avalanche multiplication starts , charge carriers Tses hence I_c Tses.

$$CB: m = \frac{1}{\left[1 - \left(\frac{V_{CB}}{\beta V_{CBO}} \right)^n \right]} \quad n = 2 \text{ to } 10$$

$$CE: \beta V_{CEO} = \beta V_{CBO} \left(\frac{1}{\beta} \right)^n$$

$$\text{max Rating} = \min (\beta V_{PT}, \beta V_{AB})$$

BV_{CBO} \rightarrow Breakdown voltage in common base with Emitter open

BV_{CEO} \rightarrow Breakdown voltage in common emitter with base open

βV_{PT} \rightarrow Breakdown voltage at which punch through occurred

BV_{AB} \rightarrow Breakdown voltage at which avalanche breakdown happened

* effect of temperature on reverse saturation current I_o
 I_{scr} in Temp. \propto EHP generation and minority concentration
 hence reverse current \propto

$$a) T \uparrow \Rightarrow I_o = \frac{A_q D_p P_{no}}{L_p} + \frac{A_q D_n N_{po}}{L_n}$$

from above we get $\frac{1}{I_o} \frac{dI_o}{dT} = \frac{m}{T} + \frac{E_{no}}{\eta + V_T}$ $m=1.5 \rightarrow Si$
 $=2 \rightarrow Ge.$

$$\uparrow I_o \rightarrow = 8\% / {}^\circ C \rightarrow Si \quad] \text{ at } T=300{}^\circ K,$$

$$\uparrow I_o \rightarrow = 11\% / {}^\circ C \rightarrow Ge. \quad]$$

Practically $7\% / {}^\circ C$ in both diodes.

I_o get doubled for every $10{}^\circ C$ rise in temp.

$$I_{o2} = I_{o1} 2^{(T_2 - T_1)/10}$$

* Effect of temperature on voltage.

for $1{}^\circ C$ rise in temp to maintain constant current through diode decrease voltg across diode by $2.5mV$

$$i.e. \frac{dv}{dt} = -2.5mV / {}^\circ C$$

* JFET.

* JFET is unipolar Device bcz current due to only one carrier either e^- or holes. in BJT - majority & minority both (e^-) & (holes)

	V_{GS}	I_D
pinch off }	1 T_{Ses} constant	constant (Pinch off Region)
	2 constant T_{Ses}	0

- JFET is }
 ① voltage variable resistor in pinch off region (POR) in OR ohmic region
 ② constant current source in saturation region (CSR)
 ③ Buffer ④ Digital-analog switch
 ⑤ Voltage control device ⑥ Input Resistance high ⑦ No offset voltage

* If a is half channel height, bie half effective channel height

r_{DOn} - Drain on resistance, $I_{DSS} = I_D$ when $V_{GS} = 0$

$$* V_p = -q N_D a^2 / 2\epsilon \rightarrow N \text{ channel}$$

$$V_{DS} = V_{GS} - V_p$$

$$* V_p = +q N_A a^2 / 2\epsilon \rightarrow P \text{ channel}$$

$$* V_{GS} = \left(1 - \frac{b}{a}\right)^2 V_p \quad * I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$* I_D = \frac{2awqN_Dm_n}{L} \left[1 - \left(\frac{V_{GS}}{V_p}\right)^2\right] V_{DS}$$

$$* r_{DOn} = \frac{V_{DS}}{I_D} \Big|_{V_{GS}=0} = \frac{L}{2awqN_Dm_n}$$

1) Silicon is preferred than germanium

- Advantage
- Si: leakage current low, more energy gap, high resistivity
 - high thermal stability, high voltage carrying capacity.
 - Ge: - high mobility of electrons, used at higher frequency applications

2) IC is better than discrete component

small size, $\frac{P_{\text{consumed}}}{P_{\text{consumed}}}$, speed ↑, cost ↓

3) Scaling is very important it reduces the size.

length of the channel is reduced to reduce size of transistor.

constant field scaling -

$$L' = \frac{L}{S} \quad W' = \frac{W}{S}$$

constant voltage scaling $V_T \propto V_{DD}$ constant $t_{ox'} = \frac{t_{ox}}{S}$ etc

But $N_A' = S N_A$ $N_D' = S N_D$ bcs. to ~~not~~ increase channel length

we have to decrease depletion width for that increase doping conc. N_A, N_D

4) VLSI History

Small scale IC's (SSI) - 10 Transistors or gate, inverter, AND, logic gates.

Medium S.I. (MSI) - 1000T or gate, counter, mux, Adders.

Large S-I (LSI) - 10000T or gate, 8 bit up, ROM, RAM

Very-L-S-I (VLSI) - > 100000 gates, 16 bit up, 32 bit up.

4004 1st up in 1971 by intel 10 μm channel length.

5) FET over BJT

Unipolar - current due to majority carrier only. ($\text{BJT} \rightarrow \text{Bipolar}$)

high I/V impedance

No thermal runaway, thermally stable

voltage control device

fabrication is easy, low cost, small size, low power

No offset voltage at 0 drain current

simple biasing.

but gain is low than BJT.



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(Answer) (Part 1)

6) FET \rightarrow voltage control current source $I_D = g_m V_{GS}$ BJT \rightarrow current I_c (control) current source $I_c = h_f e I_b$ 7) $\begin{cases} \text{JFET} \\ \text{IGFET} \end{cases} \rightarrow$ Junction Field Effect transistor (JFET) \rightarrow Insulated gate FET or Metal oxide semi. FET
(MOSFET)

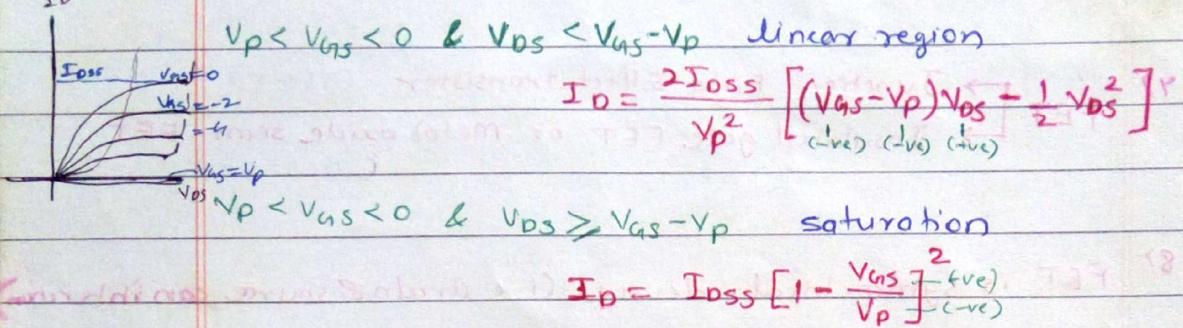
8) FET is symmetrical device (i.e. drain & source can interchange)

negative resistance in saturation of JFET
positive resistance in inversion mode
negative resistance & resistance in saturation
resistance in negative resistance region

conducting at peak (breakdown)

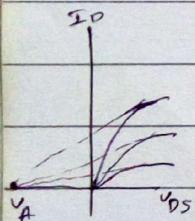
Conduction

- * for JFET (n channel) ($V_{GS} & V_P$ are -ve) (V_{DS} is +ve)
- * $V_{DS} = V_{GS} - V_P$ ← TEE ↗
- $V_{GS} \leq V_P$ cut off region $I_D = 0$ ← TEE



- * JFET is used as An Amplifier in saturation region
- * & also current source in saturation region.
- switch in linear & cut off region
- voltage variable register in linear region

* Channel length modulation:



As V_G varies length of the channel varies.

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2 (1 + \lambda V_{DS})$$

$\lambda = \frac{1}{V_A} \rightarrow$ early voltage
channel length modulation parameter

* Transconductance :

It gives how effectively JFET converts voltage changes at the input to the corresponding current change at the o/p in the saturation region. i.e. $g_m = \frac{dI_D}{dV_{GS}}$ | _{V_{DS}}

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2 \quad (\text{diff } I_D \text{ w.r.t. } V_{GS})$$

$$* \frac{dI_D}{dV_{GS}} = g_m = \underbrace{\frac{2I_{DSS}}{-V_P}}_{\text{---}} \left| \left[1 - \frac{V_{GS}}{V_P} \right] \right|$$

g_{m0} = maximum transconductance.

$$* g_m = \frac{2}{|V_P|} \sqrt{I_D \cdot I_{DSS}}$$

* Effect of temperature

1) $V_P \rightarrow T \uparrow \rightarrow V_P \uparrow \Rightarrow I_D \uparrow$ (PTC)

2) $Mofc^-$: $T \uparrow \Rightarrow N \downarrow \Rightarrow I_D \downarrow$ ($\because I = n \mu n q E A$) (NTC) } NTC dominates PTC.

* If we manage $NTC = PTC$ I_D will constant zero temp coefficient
(Condition for ZTC) $\Rightarrow |V_{GS}| = |V_P| - 0.63 \times I_D$ independent Temp $\propto ZTC$

* Amplification

ratio of change in drain to source voltage to the change in gate to source voltage i.e. $A = \frac{\Delta V_{DS}}{\Delta V_{GS}}$

$$A = g_m \cdot r_d$$

r_d = drain resistance or op resistance
 $= \frac{\Delta V_{DS}}{\Delta I_{DS}}$ (in saturation region)

* V_p (Pinch off voltage)

$$V_p = \frac{8 N_D a^2}{2e} \quad \text{half channel thickness}$$

$$V_p = \frac{8 N_A a^2}{2e} \quad (\text{P-JFET})$$

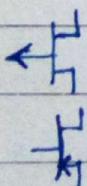
$$\begin{aligned} 2V - 0V &= 2V \\ 2V - 10V &= -8V \\ 2V - 10V &= -8V \end{aligned}$$

* drain ON resistance, $r_{d(on)}$ or ON resistance, $r_{d(on)}$; R_{on}

$$(2a + 2) \cdot R_{on} = \frac{\Delta V_{DS}}{\Delta I_{DS}} \quad (\text{in linear region})$$

$$= \left(\frac{L}{2a \omega N_D a^2} \right) \left[1 - \sqrt{\frac{V_{GS}}{V_p}} \right] \quad r_{d(on)} = \text{drain resistance at } V_{GS} = 0$$

* Pinch off voltage depends on temperature η_{SCS} by $2.2 \text{ mV/}^\circ\text{C}$



* For JFET (P-channel)

same as n channel but complementary.

V_{GS} & V_{DS} are +ve in P-channel. (V_{DS} is -ve)

$$V_{GS} - V_{DS} = V_{GS} - V_p$$

$V_{GS} \geq V_p$ cut-off region $\rightarrow I_D = 0$ initially *

$0 < V_{GS} < V_p \& V_{DS} > V_{GS} - V_p$ linear region

$$I_D = \frac{2I_{DSS}}{V_p^2} \left[(V_{GS} - V_p)V_{DS} - \frac{1}{2}V_{DS}^2 \right]$$

$0 < V_{GS} < V_p \& V_{DS} \leq V_{GS} - V_p$ saturation region

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2$$

** mobility of holes is less than mobility of e-
 $\therefore I_{DSS}$ in n-JFET is less than I_{DSS} in P-JFET.

* JFET biasing.

points

→ in BJT the biasing is required for thermal stability i.e. to avoid thermal runaway and to make Q point at the middle of the load line to avoid the half or negative or both wave distortion i.e. to keep in active region

→ In JFET biasing is required for Q point.

$$V_{DS} = V_D - V_S$$

$$V_{GS} = V_G - V_S$$

$$V_S = I_{DRS}$$

$$V_{GS} =$$

fixed bias

, Self bias

, Voltage divider bias.

$$V_G = -V_{GS}$$

$$V_G = 0$$

$$V_G = \frac{V_{DD} R_{G2}}{R_{G1} + R_{G2}}$$

$$I_D = I_{DSS} \left[1 - \frac{-V_{GS}}{V_P} \right]^2$$

$$I_{DSS} \left[1 - \frac{-I_{DRS}}{V_P} \right]^2$$

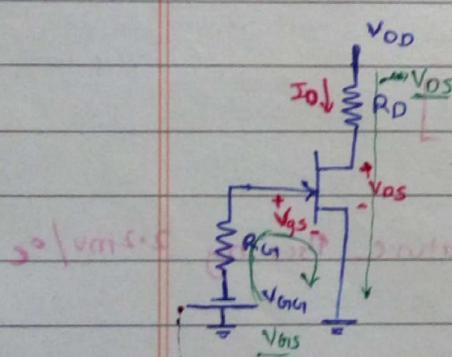
$$I_{DSS} \left[1 - \frac{V_G - I_{DRS}}{V_P} \right]^2$$

$$V_{DS} =$$

$$V_{DD} - I_D R_D$$

$$V_{DD} - I_D (R_D + R_S)$$

$$V_{DD} - I_D (R_D + R_S)$$

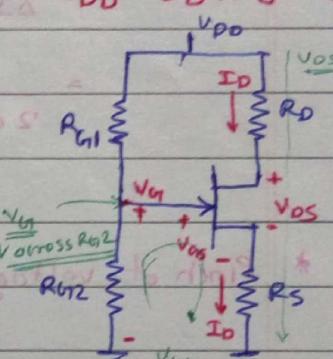


extra power supply
for V_G too fixed bias

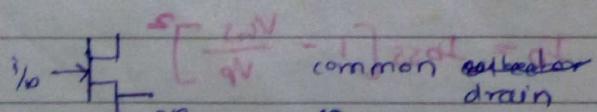
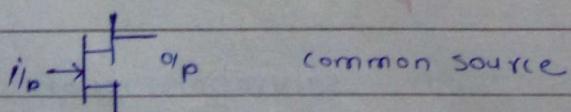
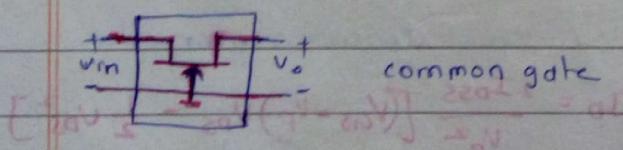
R_S provides -ve feedback
to avoid we use capacitor

use capacitor

to avoid we use capacitor



* Amplifier Analysis or Ac analysis.



→ to get common collector (source follower)

→ to get common drain (source follower)

→ to get common emitter (source follower)

- ① short DC Power supply to ground
- ② Identify terminals of JFET
- ③ Replace JFET

3 steps of Ac eqn

common source: (cs)

$$R_{in} = R_{G1} \parallel R_{G2}$$

* or R_{G1} (in fix bias & self bias)

$$R_o = R_o \parallel [r_d + (1 + g_m r_d) R_S]$$

* if without R_S put $R_S = 0$ i.e. with c

* if $r_d \gg R_o$ neglect r_d

$$A_v = -\frac{g_m (r_d \parallel R_o)}{1 + g_m R_S}$$

* it with c_s i.e. without R_S put $R_S = 0$

~~Untab~~ (CD) common drain:-

~~2nd planar process~~

~~1st result~~
~~2nd~~
~~3rd~~
~~4th~~
~~5th~~

$$R_i = R_{G1} \parallel R_{G2}$$

* or R_{G1}

$$R_o = r_d \parallel R_S \parallel \frac{1}{g_m}$$

* if R_L is there then consider

$R_S \parallel R_L$ instead R_S

$$A_v = \frac{g_m (r_d \parallel R_S)}{1 + g_m (r_d \parallel R_S)}$$

~~2nd planar~~ ~~3rd~~ ~~4th~~ ~~5th~~

common gate (cg):-

$$R_i = R_S \parallel \frac{1}{g_m}$$

$$R_o = r_d \parallel R_o$$

~~2nd planar~~ ~~3rd~~ ~~4th~~ ~~5th~~

$$A_v = g_m (r_d \parallel R_o)$$

BJT

(+ve) FET

Phase shift in i/p & o/p \Rightarrow CB $\rightarrow 0$

* CE $\rightarrow 180^\circ$

CC $\rightarrow 0^\circ$

CG $\rightarrow 0^\circ$

* CS $\rightarrow 180^\circ$

CD $\rightarrow 0^\circ$

in BJT \rightarrow Voltage gains & current gains.

in BJT \rightarrow $A_{VCC} < A_{VCE} < A_{VCB}$ $A_{ICB} < A_{ICE} < A_{ICC}$

in FET \rightarrow $A_{VCO} < A_{VCS} < A_{VCG}$ $A_{VCO} \approx 1, A_{VCG} = 1$

multistage Amplifier :-

\rightarrow provided series resistance should not there bet stages

$A_v(\text{total}) = A_{v1} \cdot A_{v2} \cdot A_{v3} \cdots A_{vn}$

$A_I(\text{total}) = A_{I1} \cdot A_{I2} \cdot A_{I3} \cdots A_{In}$

\rightarrow provided shunt resistance not them stages.

$\phi_{eq} = \phi_1 + \phi_2 + \phi_3 \cdots + \phi_n$
(phase shift)

cascade Amplifier :- To get high voltage gain

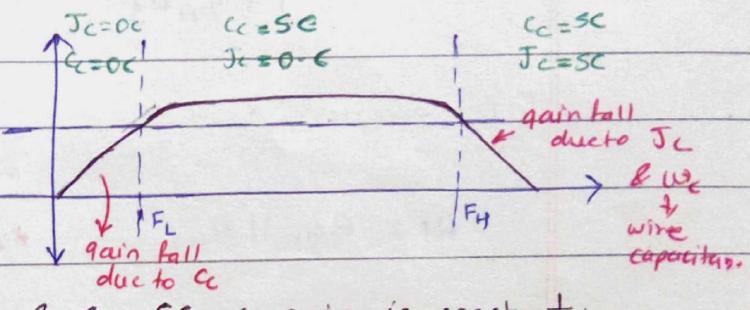
($CE-CE$) or ($CS-CS$)

cascode Amp :- To get high bandwidth & i/p impedance

$CE-CB$ or $CS-CC$

Darlington :- High current gain

$CC-CC$ or $CD-CD$



* Frequency Analysis.

for DC capacitor g_e

but for AC
it is depend upon frequency
and capacitor value

J_c - Junction capacitors
 C_c - coupling & bypass capacitors

* we preferred J_c-OC & C_c-SC ∵ gain is constant.

frequency analysis done in $\text{low frequency} \rightarrow F_L$ & F_H above where gain falls.

low frequency high frequency .

- Low frequency Analysis :- behaves as high pass filter

$$\text{at i/p ckt} \Rightarrow F_{Ld} = \frac{1}{2\pi C_d (R_o + R_{sig})} \quad F_{Ld} = \frac{1}{2\pi C_d (R_o + R_L)}$$

$$F_{Ls} = \frac{1}{2\pi C_s R_{eq}} \quad R_{eq} = R_s \parallel \frac{1}{g_m}$$

F_L, F_{Ld}, F_{Ls}

Highest among F_{Ld} , F_{Ls} taken as F_L (mostly F_{Ld})

- High frequency Analysis :- behaves as low pass filter.

$$\text{at o/p ckt} \Rightarrow F_{Hd} = \frac{1}{2\pi R_i C_i} \quad F_{Ho} = \frac{1}{2\pi R_o C_o}$$

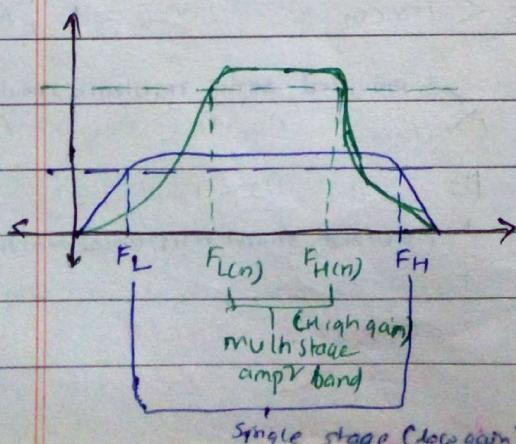
$$\begin{aligned} \text{Miller capacitance } C_{mi} &= C_{gd} (1 - A_v) & R_i &= R_g \parallel R_{sig} \\ \text{Capacitance } C_{mo} &= C_{gd} (1 - \frac{1}{A_v}) & C_i &= C_{gs} + C_{wi} + C_{mi} \\ \text{for } C_{gi} & & C_o &= C_{ds} \parallel C_{wo} \parallel C_{mo} \end{aligned}$$

Lowest among F_{Hd} & F_{Ho} taken as F_H (mostly F_{Hd})

- at low freq. high pass at high freq. low pass

⇒ Amp is bandpass filter. (\therefore increasing gain, B.W & f_{cav})

$$\therefore \text{gain} \propto B.W \cdot f_c^{n-1} = K^n$$



$$- \therefore r_{out}, F_{2(n)} \Rightarrow \frac{F_L}{\sqrt{2^{n-1}}}$$

$$F_{H(n)} = F_H \sqrt{(2^{n-1})}$$

$$B.W(n) = B.W \sqrt{(2^{n-1})}$$

* MOSFET

Depletion MOSFET \rightarrow n-channel
Enhancement MOSFET \rightarrow p-channel.

$$\rightarrow R_{BJT} < R_{JFET} < R_{MOSFET}$$

* Depletion MOSFET.

* N-channel 

* $V_{GS} \Rightarrow +ve$ or $-ve$, $V_{DS} \Rightarrow +ve$, $V_P \Rightarrow -ve$.

\rightarrow operates in depletion mode for $-V_{GS}$ & enhancement mode for $+V_{GS}$

\rightarrow \therefore operates in both depletion & enhancement mode.

\rightarrow bulk should connected ground or most -ve voltage node.

\rightarrow condition for pinchoff $V_{DS} = V_{GS} - V_p$

\rightarrow transfer characteristic of D-MOSFET gives $[V_p, I_{DSS}, \alpha_m]$

for $V_{DS} \leq V_p$ cut off region $I_D = 0$

for $V_{DS} \leq V_{GS} - V_p$ linear region

$$I_D = \frac{2I_{DSS}}{V_p^2} [(V_{GS} - V_p)V_{DS} - \frac{1}{2}V_{DS}^2]$$

$$\Rightarrow K_n (A/\sqrt{2})$$

for $V_{DS} \geq V_{GS} - V_p$ saturation Region

$V_{GS} = 1$
 $V_{GS} = 2$
 $V_{GS} = 0$
 $V_{GS} = -2$
 $V_{GS} = -4$
 $V_{GS} = -6$

$$I_D = K_n [V_{GS} - V_p]^2 \quad \therefore K_n = \frac{2I_{DSS}}{V_p^2}$$

$$I_D = I_{DSS} \left[1 - \frac{V_{DS}}{V_p} \right]^2$$

+ve or -ve

$\therefore -V_{GS} \Rightarrow$ depletion mode $\Rightarrow I_D < I_{DSS}$

$\therefore +V_{GS} \Rightarrow$ Enhancement mode $\Rightarrow I_D > I_{DSS}$

* V_{GS} +ve attracts e^- so I_D increases $\therefore V_{GS}$ +ve I_D more

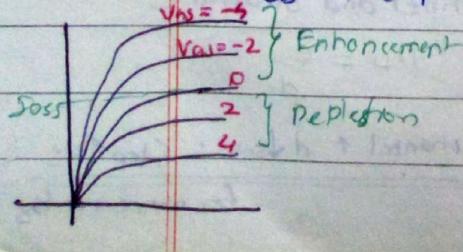
* P-channel

\rightarrow same as N-MOSFET by complement of it and I_{DSS} in NMOS is greater than I_{DSS} in PMOS since mobility of e^- is high.

\rightarrow holes are majority carrier \therefore when V_{GS} is -ve attract holes $\therefore I_D$ increases while for +ve V_{GS} attract e^- $\therefore I_D$ decreases oppo. to NMOS

$\rightarrow -V_{GS} \Rightarrow$ enhancement mode $\Rightarrow I_D > I_{DSS}$

$\rightarrow +V_{GS} \Rightarrow$ depletion mode $\Rightarrow I_D < I_{DSS}$.



* $V_{GS} \Rightarrow +ve$ or $-ve$, $V_{DS} \Rightarrow -ve$, $V_p \Rightarrow +ve$.

operational Regions & corresponding I_D is same as N-channel $K_n \Leftrightarrow K_o$
 $V_{GS} = -ve$ & $V_p = +ve$.

* Drawback of DMOS.

- Default it is in ON state
- It requires gate voltage more than V_{DD} to switch off
- It requires two power supply
- To overcome this Enhancement MOSFET are used
- Now a days all mos devices are EMOS only.

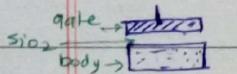
* Enhancement MOSFET.

~~enhancement mode & depletion mode~~

- Initially channel is not there in ~~existing~~ EMOS

During operation channel is form

- ∵ Default $V_{GS} = 0$ No I_D flows ∴ OFF state



forms a capacitance between gate & body.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \cdot \frac{W \cdot L}{cm^2} \quad \epsilon = \frac{\epsilon A}{d} \quad \underline{\text{A - common Area}}$$

$$C_o = C_{ox} \cdot W \cdot L$$

(see notes for detailed concept)

- EMOS operates in 3 imp. mode.

- ① $V_{GS} = -ve$ (Accumulation mode) (∴ Accumulating holes)

more no. of holes concentrate near SiO_2 in body & No channel form

- ② $V_{GS} = +ve$ ($0 < V_{GS} < V_T$) (Depletion mode) Depletion layer formed

→ Since +ve V_{GS} , attracts ~~holes~~ e^- & Repels holes near SiO_2 in body

but not sufficient V_{GS} to attract e^- from body so only holes repels

& depletion layer forms

→ so the distance between gate and body increases ∴ C_{ox} decreases

- ③ $V_{GS} = +ve$ ($V_{GS} > V_T$) (Inversion mode)

now electrons move towards gate and accumulate near SiO_2

and channel is formed as V_{GS} using channel thickness d using.

∴ Now two capacitance form

- ① between gate and channel
- ② between channel and substrate

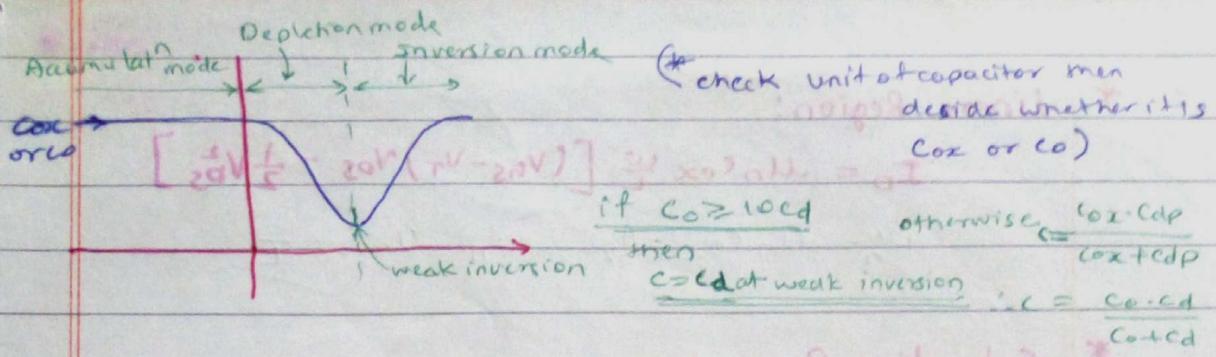
$$C_{ox} = C_o \cdot W \cdot L$$

$$C_{dep} = \frac{\epsilon_s}{d} \cdot \frac{W \cdot L}{depletion layer thickness}$$

total capacitance = $C_{ox} || C_{dep}$

$$\therefore C_{eq} = \frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}} = \frac{C_o \cdot L d}{C_o + C_d}$$

as channel $\uparrow d \downarrow C_{dep}$ ∴ C_{dep} \uparrow uses for more +ve V_{GS}



* Threshold voltage (V_T)

- minimum voltage (V_{GS}) Required to accumulate sufficient number of carriers & to form channel betⁿ source & Drain region.
- $V_T \propto f(t_{ox}, V_{SB}, N_A \text{ or } N_D)$ (V_{SB} → source to body voltage)
- ⇒ $\uparrow V_T \propto t_{ox} \uparrow, \uparrow V_T \propto V_{SB} \uparrow, \uparrow V_T \propto N_A \text{ or } N_D \uparrow$ (directly proportional)

→ V_T is +ve in n-channel & -ve in P-channel.

* n-channel MOSFET. (V_{DS} +ve, V_{GS} +ve, V_T +ve)

(Graph V_{DS} (→ A) $V_{GS} > V_T$ n-channel) is formed between source & drain.

channel offers Resistance which is 1/s between source end to

drain end. voltage at source end ($V_{DS} - V_{TH}$) low &

voltage at drain end ($V_{DS} - V_{TH} - V_{OS}$)

- +ve $V_{DS} > V_T$ - ON state ⇒ apply V_{DD} to V_{DS} - ON state
- $V_{DS} < V_T$ - OFF state ⇒ apply ground to V_{DS} - OFF state

(tiristoric region → saturation (lattice) : saturation region)

→ Substrate, body or built to ground or most -ve voltage

→ MOSFET used as an amplifier in saturation region

& switch in linear & cutoff region.

→ also used as voltage variable register in linear region

current source in saturation region

$V_{DS} < V_T$ cutoff region $I_D = 0$

→ $V_{DS} > V_T$ & $V_{DS} < V_{DS} - V_T$ linear region

$$I_D = \mu_n C_{ox} \frac{W}{L} [(V_{DS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2]$$

mobility of e⁻ $\frac{W}{L}$ V_{DS}

→ $V_{DS} > V_T$ & $V_{DS} \geq V_{DS} - V_T$ saturation region

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{DS} - V_T]^2$$

the the

* Linear Region:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2]$$

$K_n' = \mu_n C_{ox} \frac{W}{L}$ $\beta_n = \mu_n C_{ox} \frac{W}{L}$

* Saturation Region:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T]^2$$

K_n K_n' β_n

Saturation breakdown

* Deep triode Region:

it is linear region but small values of V_{DS}

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

K_n' β_n

$\therefore V_{DS} \ll \frac{1}{2} V_{DS}^2$ neglected.

TRANSISTOR (continued)

* Drain ON Resistance or ON Resistance (R_{ON}) or ($r_{ds(on)}$) or ($r_{d(on)}$)

Resistance offered by MOSFET in linear Region

$$r_{ds(on)} = R_{ON} = \frac{dV_{DS}}{dI_D} \quad \text{diff eqn of } I_D \text{ in linear Region w.r.t } V_{DS}$$

$$r_{ds(on)} = \frac{1}{\mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T]} \Rightarrow R_{ON} \propto \frac{1}{W} \quad \text{resistive due to } \frac{V_{DS}}{L}$$

* Transconductance: (mutual conductance or figure of merit)

how efficiently MOSFET converts voltage changes at the IP to the corresponding current change at the O/P

is saturation region. $g_m = \frac{dI_D}{dV_{DS}} \Big|_{V_{DS}}$ (from transverse characteristics)

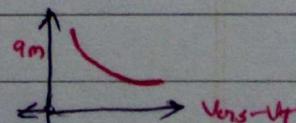
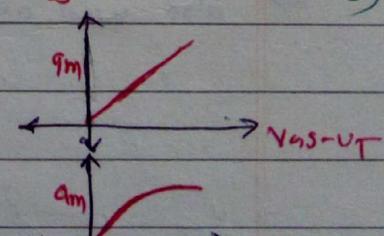
Dif I_D in saturation to get g_m

$$\therefore g_m = \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T] \Rightarrow$$

$$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} \cdot I_D} \Rightarrow$$

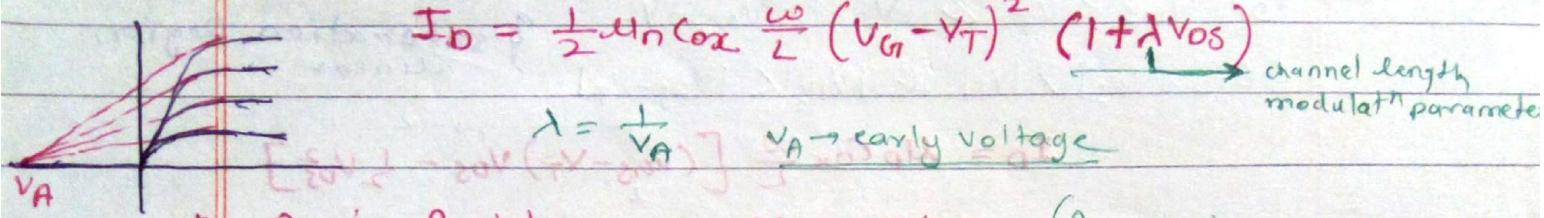
$$g_m = \frac{2 I_D}{V_{GS} - V_T} \Rightarrow$$

$$-s[\mu - s_0 V] \frac{1}{s_0 m L} = s_0 L$$



* channel width modulation

→ increase in V_{OS} decrease in effective length of the channel



* Drain Resistance or o/p resistance (A resistance or small signal resistor)

Resistance offered by MOSFET in saturation Region

$$[\sigma_d \text{ or } r_o = \frac{dV_{DS}}{dI_{DS}}] \quad \sigma_d = r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$

* Body Effect

source to body voltage $V_{SB} = V_S - V_B$

body acts like a one more gate to avoid it in NMOS
it should connected to drain or source terminal in PMOS it
should connected to V_{DD} or source terminal

V_{SB} affects threshold voltage. If V_{SB} is there (Body not connected)

$$\text{Thermal voltage.} \quad \text{acceptor conc. } V_T = V_{TO} + \gamma [\sqrt{V_{SB}} + \phi_s - \sqrt{\phi_s}]$$

$$\phi = 2kT \ln \left(\frac{N_A}{n_i} \right)$$

$$\gamma = \frac{\sqrt{2qN_A\epsilon_{Si}}}{C_{ox}} = \frac{\epsilon_{ox}}{t_{ox}} \sqrt{2qN_A\epsilon_{Si}}$$

V_{TO} - threshold voltage of MOSFET at $V_{SB}=0$.

ϕ_s - surface potential

γ = Body effect coefficient

∴ V_T is function of (V_{SB} , C_{ox} & N_A or N_D) ~~& proportionality~~

Due to body effect V_T varies hence I_D also varies.

see I_D eqn as $V_T T_{scst} I_D + I_{DSS}$

* Temperature effect

case 1) V_T depends on temperature. V_T decreases by $2mV/^\circ C$.

$T \uparrow \rightarrow V_T \downarrow \Rightarrow I_D \uparrow$ (PTC) +ve temp. coeff.

case 2) as $K' = \mu C_{ox}$ $\mu \propto \frac{1}{T^m} \Rightarrow \mu \propto T^{-m}$

$\mu (W/cm) = V_T \uparrow \rightarrow \mu \downarrow \rightarrow I_D \downarrow$ (NTC) -ve temp. coeff

combining both cases NTC dominates PTC & hence

V_T has NTC. i.e. $T \uparrow \rightarrow I_D \downarrow$

db) vol 11

* Pchannel - EMOSFET. V_{GS} or V_D $\geq V_T$ $\Rightarrow V_{DS} \geq V_T$ $\Rightarrow I_D = 0$

→ for $V_{GS} > V_T$ or $|V_{ds}| < |V_T|$ cut off $I_D = 0$.

→ for $V_{GS} < V_T$ & $V_{DS} > V_{GS} - V_T$ } saturation region
OR $|V_{ds}| > |V_T|$ & $|V_{DS}| < |V_{GS} - V_T|$ linear

$$I_D = \mu_0 C_{ox} \frac{W}{L} [(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2]$$

→ for $V_{GS} < V_T$ & $V_{DS} \leq V_{GS} - V_T$ } saturation region
OR $|V_{ds}| > |V_T|$ & $|V_{DS}| \geq |V_{GS} - V_T|$

$$I_D = \pm \mu_0 C_{ox} \frac{W}{L} [(V_{GS} - V_T)^2]$$

→ Drain characteristic & transfer characteristic is in 3rd quadrant

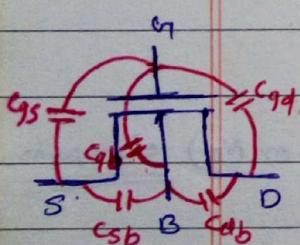
*

	Nmos	Pmos
$V_{GS} = 0$	OFF	OFF
$V_{GS} = +ve \& > V_T$	ON	OFF
$V_{GS} = -ve \& < V_T$	OFF	ON
Digital i/p '0' i.e. $V_i = 0$	OFF	ON
Digital i/o '1' i.e. $V_i = 1$	ON	OFF

see Notes
for explanation

*

mos capacitance



① gate capacitor

gate to source cap. C_{GS}

gate to drain cap. C_{GD}

gate to body cap. C_{GB}

$$\therefore C_g = C_{GS} + C_{GD} + C_{GB}$$

* presence depend upon
region of operation

② Junction capacitors

source to body junction cap. C_{SB}

drain to body junction cap. C_{DB}

* present all the time

cutoff Unctrl Saturation

$$C_{GS} \quad 0 \quad \frac{1}{2} C_0 \quad \frac{2}{3} C_0$$

$$C_{GD} \quad 0 \quad \frac{1}{2} C_0 \quad 0$$

$$C_{GB} \quad C_0 \quad 0 \quad 0$$

$$\rightarrow C_g \quad C_0 \quad C_0 \quad \frac{2}{3} C_0$$

Cov. - Cap. overlap exist
due to small overlap of S & D area with gate plate.

$$C_{OV} = C_{OX} W \cdot L_{OV}$$

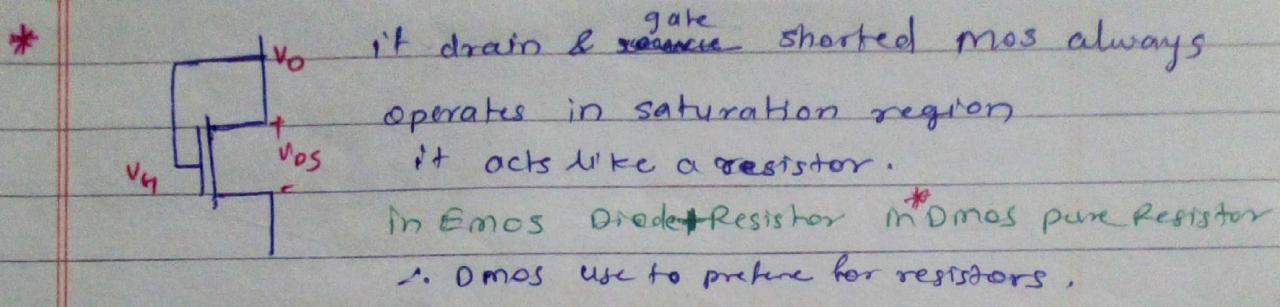
Overlap length.

$$C_{SBO} = \frac{\epsilon_s A}{d} \text{ common area} \quad C_{SB} = \frac{C_{SBO}}{\sqrt{1 + \frac{V_{SB}}{V_0}}} \text{ when } V_{SB} \text{ at } 0$$

\downarrow depletion layer thickness

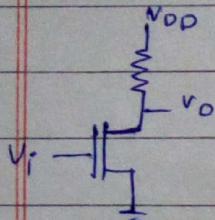
Hence for C_{DB}

$$C_{DBO} = \frac{\epsilon_s A}{d} \quad C_{DB} = \frac{C_{DBO}}{\sqrt{1 + \frac{V_{SB}}{V_0}}}$$

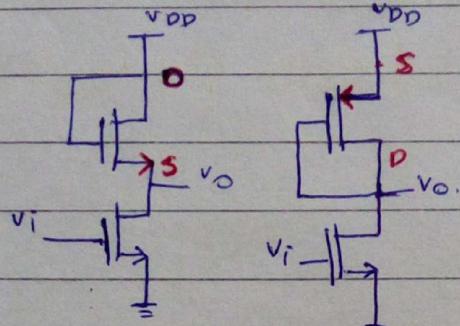


* Types of load

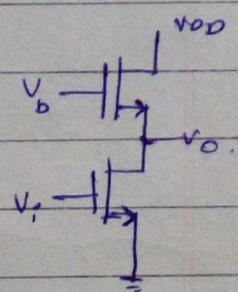
Resistive load



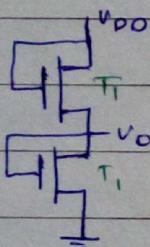
Diode connected load



current source load



*



if T_1, R_{T_2} have same $(\frac{W}{L})$ ratio same alln same parameters
if both are in saturation then they
acts like series resistance (same series resistance)
 $\therefore V_o = \frac{V_{DD}}{2}$

* MOSFET Biasing.

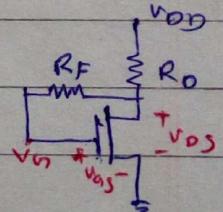
$$\begin{aligned} V_{GS} &= V_G - V_S \\ V_{DS} &= V_D - V_S \\ V_{GS} &= V_G - I_{DRS} \end{aligned}$$

Voltage divider bias
(ckt same as JFET)

$$V_{GS} = V_G - I_{DRS}$$

Drain to gate bias.

$$V_{DS}$$



$$I_D = k_n [V_G - I_{DRS} - V_T]^2 \quad k_n [V_{DS} - V_T]^2$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S) \quad V_{DD} - I_D R_D$$

* MOSFET amplifier Analysis.

* Voltage divider bias without CS

$$R_i = R_{G1} \parallel R_{G2}$$

$$R_o = R_{D1} \parallel [r_d + (1 + g_m r_a) R_S]$$

$$A_v = -\frac{g_m R_o}{1 + g_m R_S}$$

(with CS keep $R_S = 0$)

Drain to gate FB bias amp.

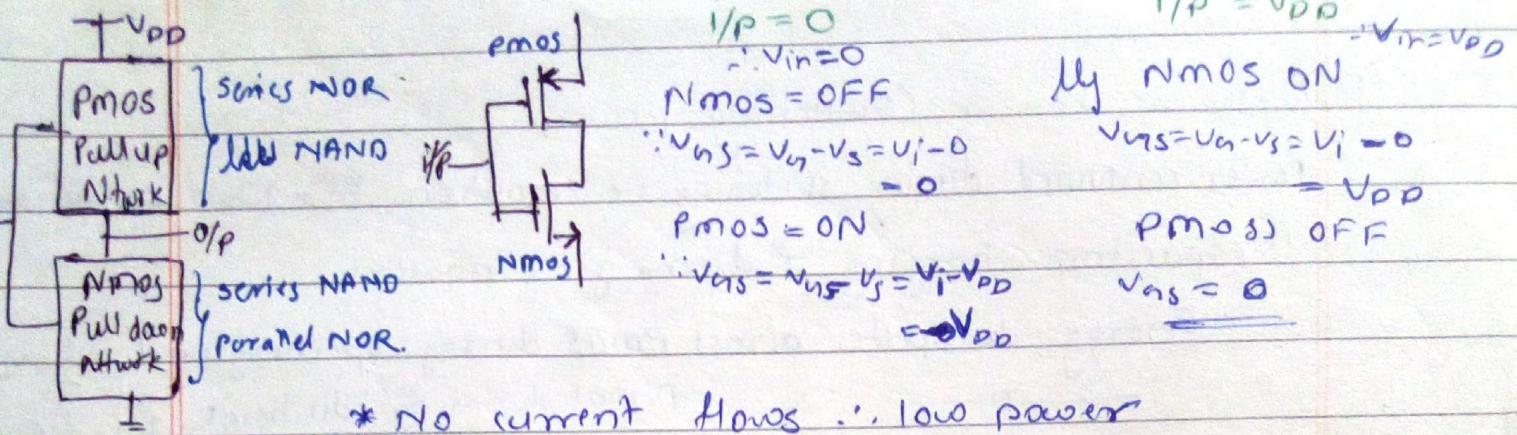
$$R_i = \frac{R_F}{1 + g_m (r_d \parallel R_o)}$$

$$R_o = r_d \parallel R_{D1} \parallel R_F$$

$$A_v = -g_m (r_d \parallel R_{D1} \parallel R_F)$$

$$A_v \approx -g_m R_o$$

* CMOS



* No current flows \therefore low power

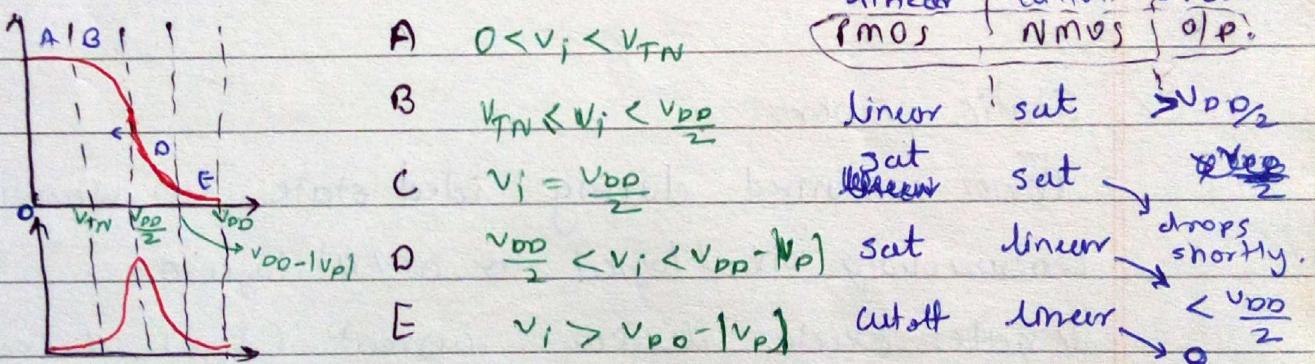
* PMOS \rightarrow logic 0 distorted \rightarrow logic 1 without distortion.

\therefore connected V_{DD} & pulled up to pass logic 1.

* NMOS \rightarrow logic 1 distorted \rightarrow logic 0 without distortion

\therefore connected ground & pull down to pass logic 0.

* Transfer characteristics of an inverter



* at C both NMOS & PMOS are ON.

* Transistor Sizing.

We know $\alpha_n \approx 2\alpha_p$ in silicon &

$$R_p = 2R_n \quad \therefore \left(\frac{w}{L}\right)_{PMOS} = 2 \quad \left(\frac{w}{L}\right)_{NMOS} = 1.$$

Rise time : time taken to rise from 20% to 80%

Fall time : time taken to fall from 80% to 20%

Propagation Delay : t_{prop}^{max} time from 50% crossing i/p to 50% crossing o/p.

Contamination Delay : min time from -11 -----.

* Power:

(1) Dynamic Power (switching power)

Power consumed during switching i.e. transition from 1 to 0 & vice versa.

① capacitor charging & discharging power.

Energy dissipate across PMOS during cap. charging $E_c = \frac{1}{2} C V_{DD}^2$

n _____ NMOS during cap. discharge $E_d = \frac{1}{2} C V_{DD}^2$

$$(E)_{\text{Total}} = E_c + E_d = C V_{DD}^2$$

$$P = \frac{E}{T} = \frac{C V_{DD}^2}{T} = C V_{DD}^2 f \rightarrow \text{switching frequency.}$$

(2) short ckt power. (when PMOS & NMOS both on)

$$\text{Req} \rightarrow C \text{ conditn} \rightarrow \frac{V_{DD}}{2} = V_i \quad \text{PMOS} \rightarrow \text{sat} \quad \text{NMOS-sat.}$$

$$\therefore P_{\text{dynamic}} = C V_{DD}^2 f + P_{\text{short}} \approx C V_{DD}^2 f \quad \therefore P_{\text{short}} \ll$$

(3) Static power.

Power consumed during ideal state i.e. when mos continuously on at logic 1 or off at logic 0.

1) gate oxide leakage current ($I_{\text{gate leak}}$)

2) junction leakage current ($I_{\text{junction leak}}$)

3) sub threshold leakage current ($I_{\text{sub leak}}$)

$$\therefore I_{\text{stat}} = I_{\text{(gate L)}} + I_{\text{(junction L)}} + I_{\text{(sub L)}}$$

* Power = $P_{\text{dynamic}} + P_{\text{static}}$

* Dynamic power is $>$ than static power. but below 90nm static power $>$ dynamic \because size \downarrow es leakage current \uparrow ses.

* Noise Margin

gives allowable noise voltages at IP without disturbing OP

① High Noise margin (HNM)

$$NM_H = V_{OH} - V_{IH}$$

— Do — Do —

② Low noise margin (LNM)

$$NM_L = V_{IL} - V_{OL}$$



* $f_o = \frac{1}{2Nn}$ (applicable for odd no. of inverters)

N - no. of inverter n - delay of each inverter.

2) IC fabrication technique:

1) Crystal growth & wafer preparation:

Czochralski process is used in crystal growth. Substrate is fabricated.

2) Oxidation:

Forming SiO_2 layer. Does not allow impurities to substrate, dissolves only in hydrofluoric acid. It is isolator.

① Dry oxidation: 1200°C , slow process, thin layer formed, better electrical properties.

② Wet oxidation: 900°C to 1000°C , fast process, thick layer formed.

3) Photolithography:

To remove SiO_2 at drain or source.

① Photoresist ② Photo mask ③ UV rays ④ Developing ⑤ Etching ⑥ Stripping

SiO_2 exposed to UV rays is removed \rightarrow +ve photoresist

SiO_2 ^{NOT} exposed to UV rays is removed \rightarrow -ve photoresist.

Now X-rays used having high resolution, small scattering effect, high accuracy.

4) Diffusion:

Diffusing source & drain region. More diffusion more depth.

① Isotropic diffusion: \rightarrow diffuse in all the direction

② Anisotropic diffusion \rightarrow diffuse in vertical direction.

5) Ion implantation:

It is also used for diffusion source & drain.

~~similar~~ similar to diffusion but takes place at low temp.

For heating strong electron beam is used. But slow process

\therefore diffusion is preferred over ion implantation.

6) Metallisation:

Process of forming metallic contacts. Old \rightarrow Al used $\text{Na}_2\text{O} \rightarrow \text{Cu}$.

7) Passivation:

Process of forming glass type epoxy coating. To protect from environmental conditions.

8) Packaging:

Occupies large area. die area 20-20%, remaining 80-80% for packaging.

DIP package: only one side mounting & other side soldering.

SMD - surface mounting devices. - both side soldering.

PGA - High power IC's

* n-channel MOSFET process

- above step wise procedure
- can make different type of MOSFET ~~at~~ simultaneously.
- All IC's have same threshold voltage.

* N-well cmos Process

- N-well is diffused in P-type substrate.
- in this we have made two mosfets in one process.

* P-well N-well cmos Process.

- similar to N-well process but complementary. P-well in N-substrate

* Triple well cmos Process.

- in P substrate. N-well on one side deep N-well on other side then in deep N-well P-well is diffused, isolated to deep N-well
- 3 mosfets designed. 1PMOS & 2NMOS with different V_T .
- change in doping concentration threshold voltage is different.

* Double well

- Isolation is due to SiO_2 .
- in this also V_T is different due to difference in concentration.