* Chap 1 (Basics)

① 1) 10 points on gates (Logic gates)

2) ckt analyse problems. 1 trick.

② 3) conversion b/w Number system (Number system)

4) finding base in operation

5) binary signed unsigned Numbers

6) 2's complement method

7) sign bit extension

8) Range of Numbers $2^{n-1}-1$ 2^{n-1}

9) multiplication & ÷ in 2's complement No.

10) compliment of numbers.

11) advantage of 2's complement

③ 12) Binary codes. (Binary codes)

13) code conversions.

14) Additions of codes & carry?

15) Hamming code $P_1 P_2 m_1 P_3 m_2 m_3 m_4$ $2^P \geq m+P+1$.

④ 16) boolean algebra (Boolean Algebra)

17) imp laws, properties & expressions consensus, shannons, Transposition.

18) NAND gate & Nor gates (min. nos.) 2n-2 - NAND 2n-3 - AND exor - 4 NAND 5 - NOR

⑤ 19) Min terms, max terms its properties. (SOP & POS)

20) Various forms of $\frac{2^n}{2}-1$ min terms in Exor. , 2^{2^n} boolean fn.

21) how to convert to canonical form trick. SOP → AND-OR ≡ NAND-NAND. POS → OR-AND ≡ NOR-NOR.

⑥ 22) K-map. (K-map)

23) implicant & its types

24) dont care, & finding f_1 from f_2, f_3 etc

25) waveforms with delay.

④ ⑮

1 2 4 7 8 11 13 14. Exor 4 bit

0 3 5 6 9 10 12 15 Xnor 4 bit

④ ⑮

* combinational ckt

1) Code converters (BCD - to 9's compl. BCD to excess 3 etc.)
2) Half adder & full adder Half subtracter full subtracter.
3) HA, FA, HS, FS using NAND NOR mini gates min HA, HS. & its eqns
4) Binary adders
   a) Parallel → $T = (N-1)t_c + \max(t_c, t_s)$ Adder
   b) carry look ahead → $C_{i+1} = C_i(A \oplus B) + AB$ (Gi) (Pi)
   c) Serial
   → ckt, advantage-disadv., time, eqns, implementation etc.
5) 4 bit adder + subtracter. $x = 1$ subtracter, $x = 0$ adder.
6) How to identify which adder (eg. excess-3, 9's complement ckt. etc)
7) BCD adder. , excess 3 adder.
8) 2 bit comparator
9) Decoder
10) Encoder
11) mux
12) Demux

→ ckts. // imp. eqns | various ckt like HA, FS, etc.
various functions implementations,
no. of min. decoder or mux etc to make big decoder or mux
min. gate requires., min. levels.
mux reduction, brick method.

$2^x \times y$ = size

13) ROM as memory, size eqn., application
14) PLA, PAL, GAL?
15) overflow concept.

FA = 1249 - 5
3567 - C
1 FA = 2 HA + 1 OR gate

Active low → $\overline{D_0}$ } decoder.
Active high → D_0

No. of o/p required
No of o/p given → go on doing operation

* Sequential ckt

1) Memory concept, latch.
2) Latch operations, o/p sequences, how to start?
3) f/f's S-R, JK, T, D } 1) T.T. 2) Excitation table 3) char. table 4) eq^n 5) ckt
4) Race around condition, M-S f/f. remedies.
5) Asynchronous & synchronous?
6) Hold time, ~~setup~~ setup time, Pd.
7) Triggering
8) o/p frequencies, duty cycle of ckt?
9) Application of f/f counters, shift register etc.
10) shift register.
    1) PIPO
    2) SISO
    3) SIPO
    4) PISO
    } ckt, o/p frequency, delay, property
11) shift register applications (conv., T.d., seq. generator) ① ② ③ ④ — counter
    ③ counters → ⓐ Ring counter
                 ⓑ Johnsons counter } ckt, operation, properties, o/p freq.
12) 3 bit Asynchronous counter (Ripple counter)
13) 2 bit Asynchro. up/down counter.
14) Up-down counter identification various combinations.
15) mod counter; how to use ~~pr~~ & Cr to make mod counter
16) ~~How~~ method to find ckt for ~~...~~ mod counter, up/down?,
    o/p. frequency, cascading of counter.
    & draw back of Asynchronous counter.
17) Excitation table, concept & how to make it
18) how to make synchronous counter using excitat^n table.
19) steps to follow, Designing, frequency of operation
20) Self start counter concepts., ~~identification of mod~~
21) Identification of mod of counter?
22) State diagram., how to make state diagram table?
23) sequence detector
    ① mealy } ckt, properties,
    ② moore