PD0 Report Document

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EECS 4201 E
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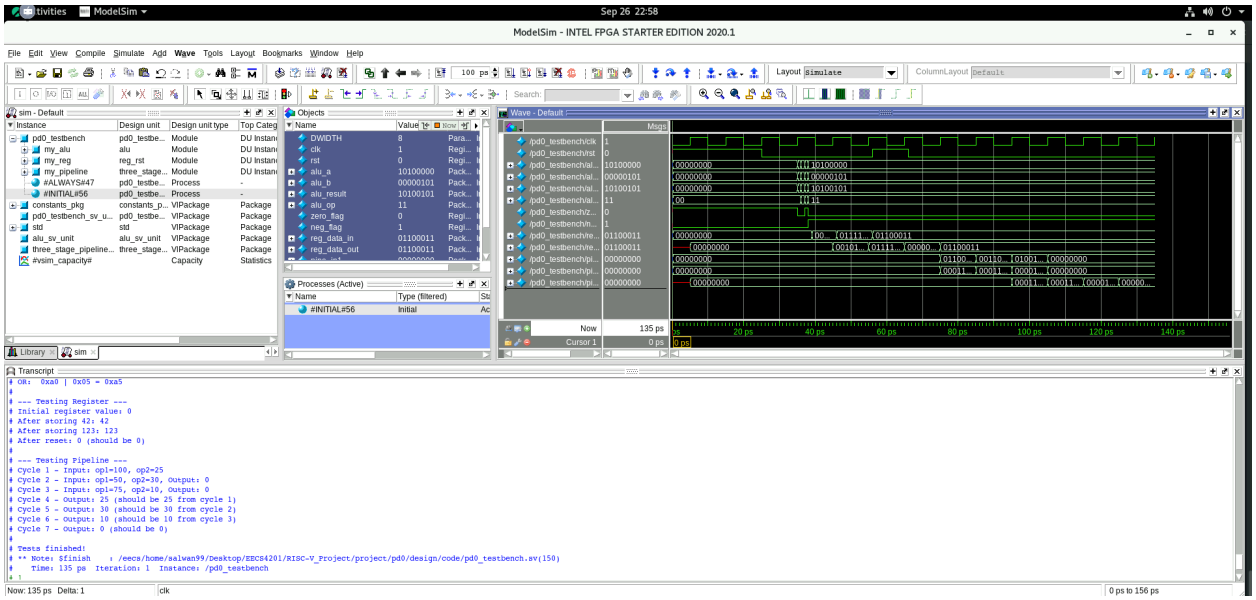
ModelSim Our Testbench Waveform Screenshots:



Simulation of pd0_testbench.sv

Challenges Faced During PD0 Deliverables:

The main challenge we faced while doing PD0 was creating the proper test benches. In the PD0 top-level is only exposed to the clk and reset signal unlike the other designs where inputs and outputs are connected directly to the top-level module. We have to access all other signals through probes which we defined in the probes.svh. Initially it confused us, then we had to learn how to map internal signals such as alu_op1, alu_op2, alu_sel, and failures so that they could be driven by the test benches. As we understood the roles of the probes, we were able to drive the inputs and observe the outputs successfully.

Another difficult part which we faced was the three-stage pipeline. At first the design did not appear immediately when we applied the input values, we believed it was a design bug. After reviewing the specifications and analyzing it carefully we realized that the design was behaving correctly, because the result from the pipeline is only visible after two clock cycles due to the registers between each stage. The stage one performs the addition and stores the value and the stage two performs the subtraction and stores the results and the last stage three registers are the final output. After recognizing the behaviour of the pipeline design helped us understand the correct behaviour of the pipelining.