

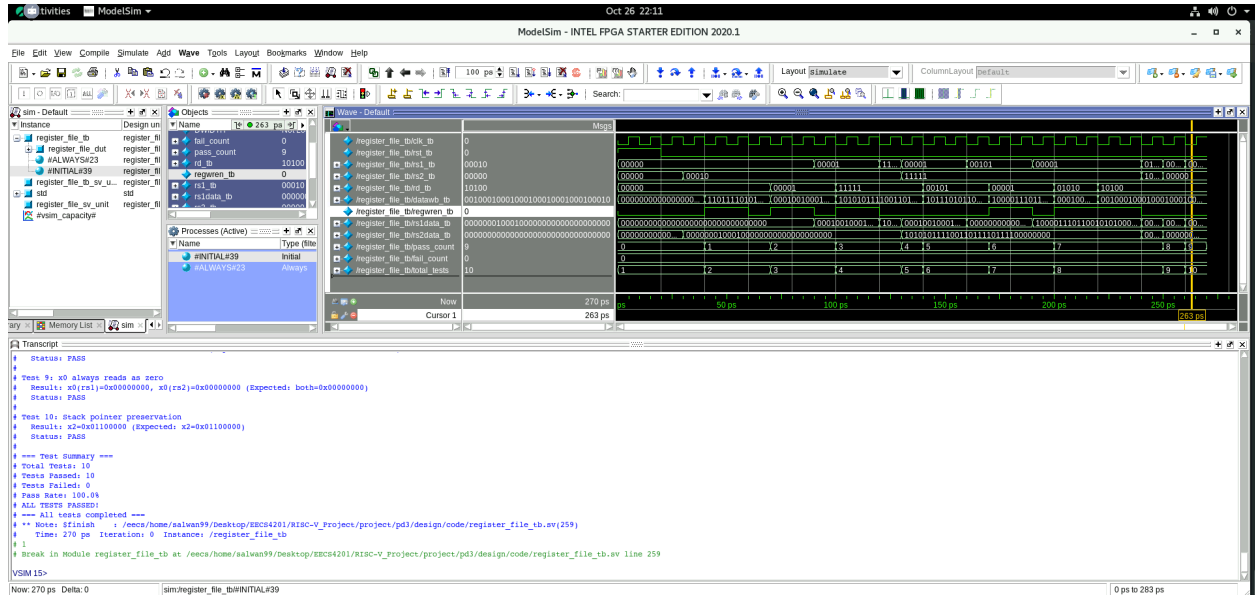
PD3 Report Document

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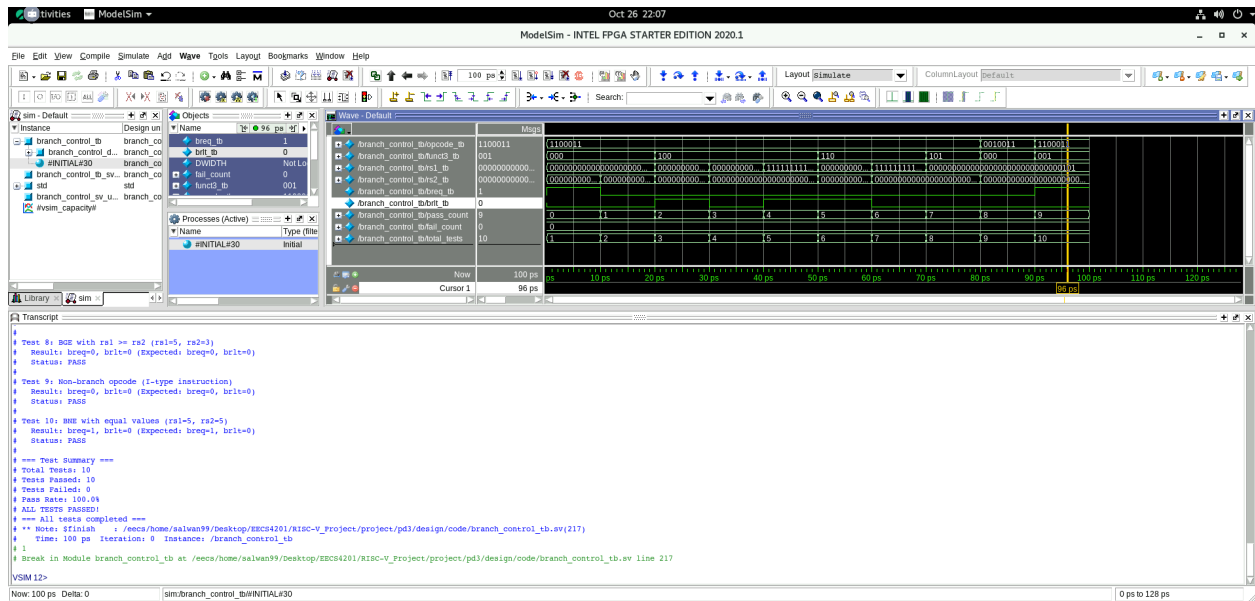
EECS 4201 E
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ModelSim Our Testbench Waveform Screenshots:

register_file_tb.sv



branch_control_tb.sv



The screenshot displays the ModelSim - INTEL FPGA STARTER EDITION 2020.1 interface during a simulation of the file `execute_tb.vv`. The top status bar indicates the date and time as Oct 26, 22:13.

The main workspace is divided into several panes:

- Objects:** Shows the design hierarchy. The selected object is `execute_tb`, which is an instance of `INITIAL40`.
- Waveform:** Displays a timing diagram for various signals. The signals listed include `execute_tb_count`, `execute_tb_func1_b`, `execute_tb_func7_b`, `execute_tb_mmm_b`, `execute_tb_opmode_b`, `execute_tb_pass_count`, `execute_tb_res_id`, `execute_tb_testen_b`, `execute_tb_bpss_count`, `execute_tb_fail_count`, and `execute_tb_fatal_tests`. The waveform shows digital logic levels over time, with a vertical yellow cursor at approximately 115 ps.
- Processes (Active):** Shows the active processes, including `INITIAL40`.
- Transcript:** Displays the simulation log. It shows the results of two test cases, both of which passed. The transcript also includes a summary of the simulation, stating "ALL TESTS PASSED!" and "Time: 120 ps Iteration: 0 Instance: /execute_tb".

The bottom status bar indicates the current time is 120 ps and the delta is 0.

While developing and testing the design our team faced challenges during PD3. One of the major issues was in the register file, specifically in setting up the stack pointer (x2) and assigning the correct initial value to it. Values were not being sorted as expected and we faced multiple errors during initialization. We finally identified the problem after several trials and debugging and assigned the correct values successfully.

Another issue we faced was in the decode because we initialized everything to 0 initially and it was giving the decode mismatch error. After spending some time on it and reviewing the code, I realized that our approach is not correct. And then we fixed it.

Another major challenge we faced was in the execution stage, where some ALU operations and control signals were not functioning properly. Due to incorrect logic connections and missing signal assignments the outputs were not matching the expected results. After reviewing the Verilog code and thoroughly analyzing the waveform we corrected the logic and made sure the proper data flow between the stages.