PD3 Report Document

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EECS 4201 E
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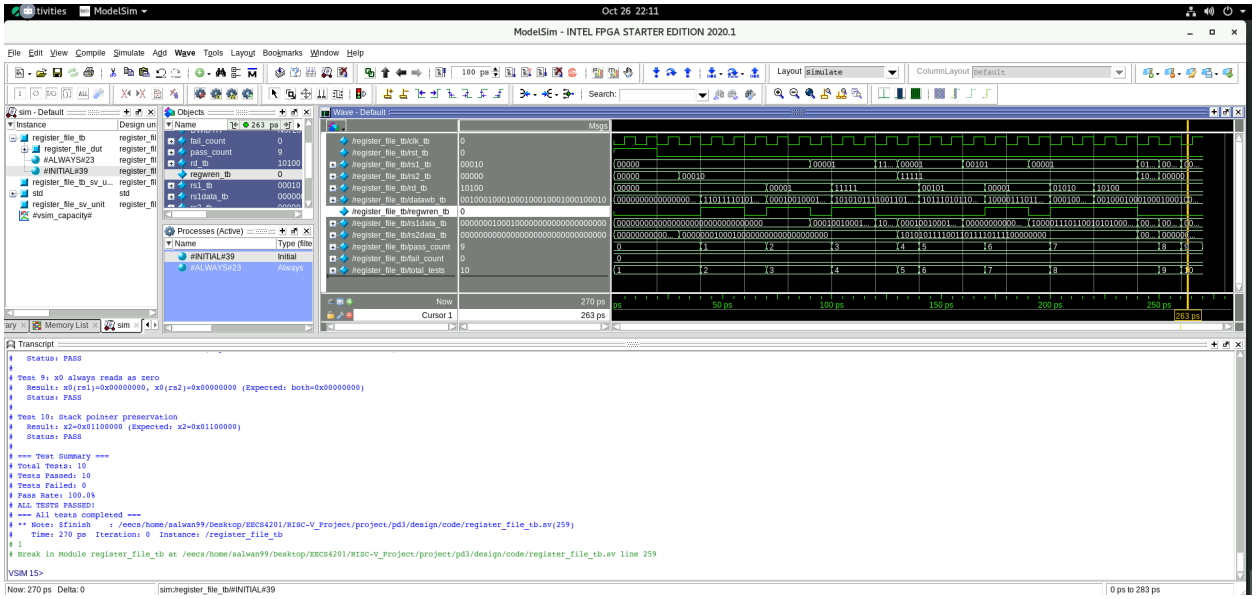
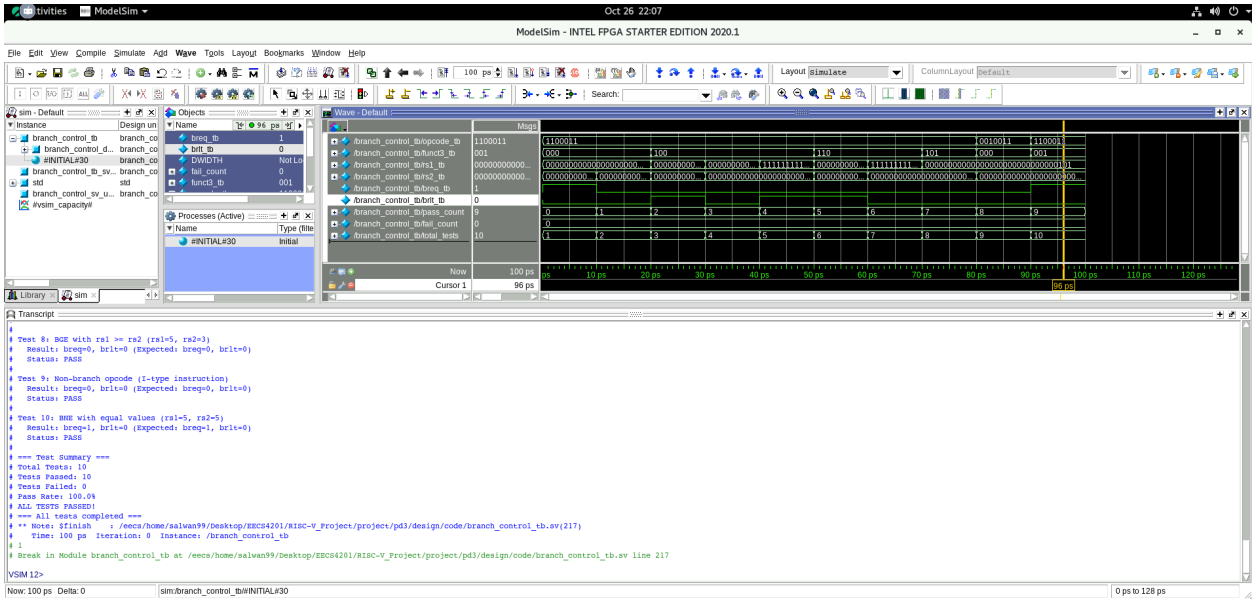
ModelSim Our Testbench Waveform Screenshots:

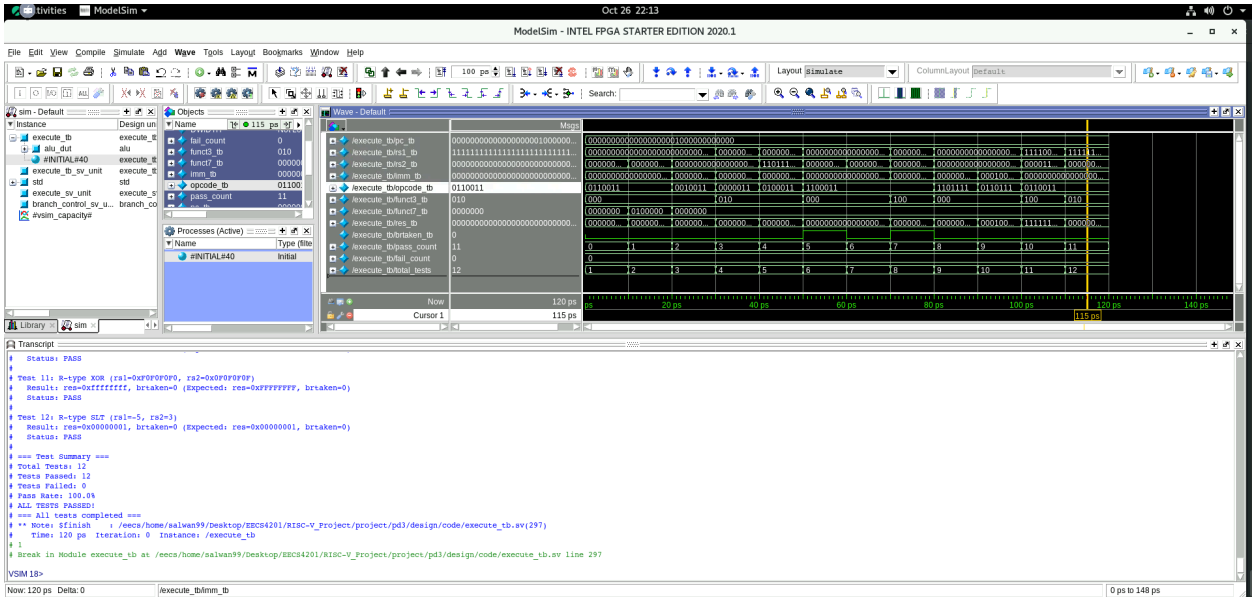
register_file_tb.sv



branch_control_tb.sv



execute_tb.sv



Challenges Faced During PD3 Deliverables:

While developing and testing the design our team faced challenges during PD3. One of the major issues was in the register file, specifically in setting up the stack pointer (x2) and assigning the correct initial value to it. Values were not being sorted as expected and we faced multiple errors during initialization. We finally identified the problem after several trials and debugging and assigned the correct values successfully.

Another issue we faced was in the decode because we initialzed everything to 0 initially and it was giving the decode mismatch error. After spending some time on it and reviewing the code, I realized that our approach is not correct. And then we fixed it.

Another major challenge we faced was in the execution stage, where some ALU operations and control signals were not functioning properly. Due to incorrect logic connections and missing signal assignments the outputs were not matching the expected results. After reviewing the Verilog code and thoroughly analyzing the waveform we corrected the logic and made sure the proper data flow between the stages.