PD1 Report Document

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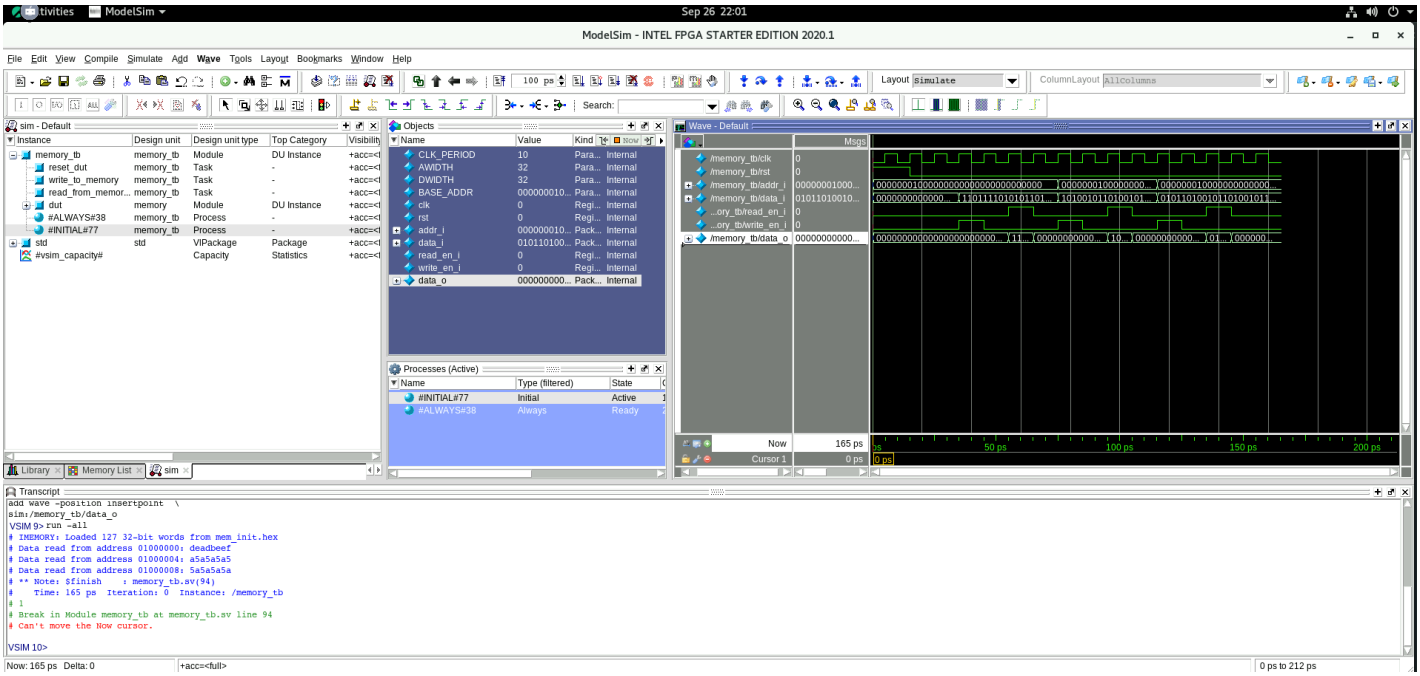
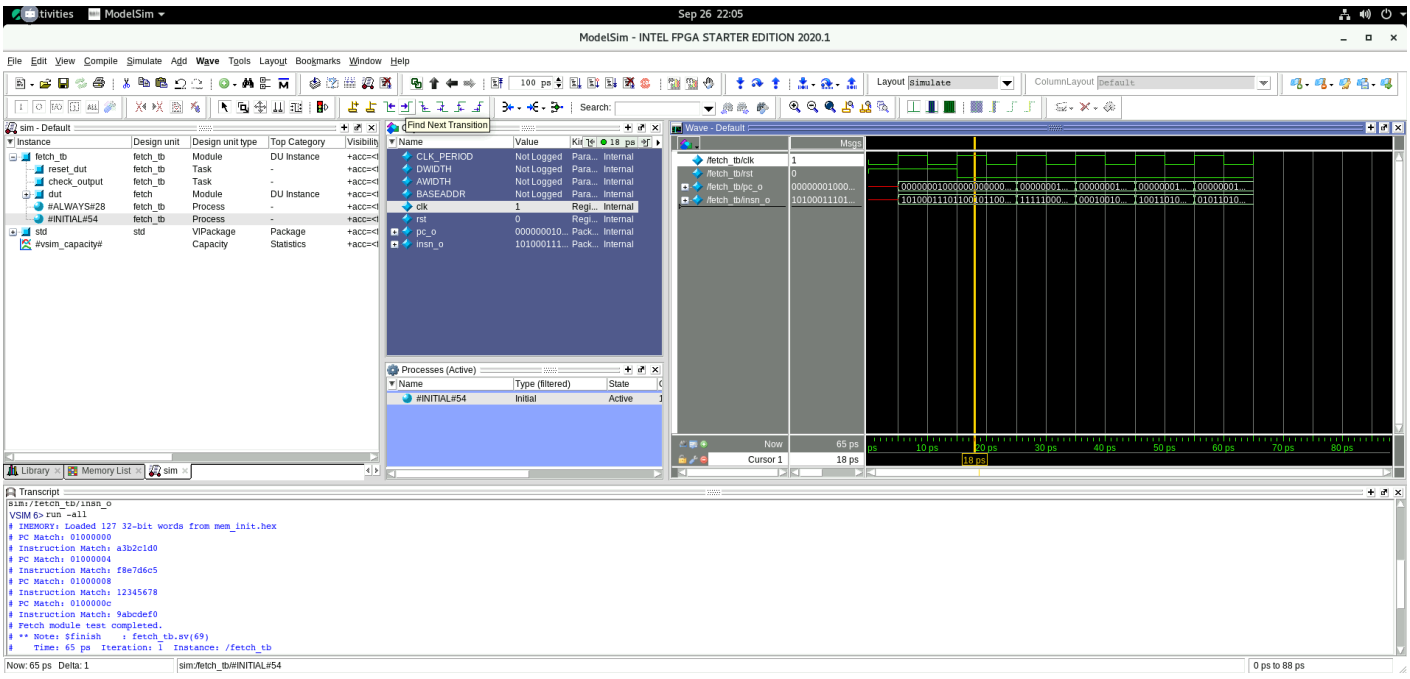
ModelSim Our Testbench Waveform Screenshots:



Simulation of memory_tb.sv



Simulation of fetch_tb.sv

Challenges Faced During PD1 Deliverables:

During the PD1 the main challenge we faced was related to the testbench integration. To observe internal signals from the design the provided testbench relies heavily on probes (design/probes.svh). At first our simulation attempts kept failing with repeated “probe signals not defined” errors. This was happening because the signal names in our top-level module (pd1.sv) did not exactly match with the macro definitions expected by the testbench. Ensuring that every required signal was explicitly declared at the top level and connected properly and tracking down the exact names that testbench checks for required carefully reading through. This taught us the value of consistency between design hierarchy, probe definitions and testbench expectations. This debugging issue took time but also gave us deeper understanding.

Another major challenge was ensuring the instruction output and synchronization of the program counter (PC). At the initial implementation stage the PC register updated correctly on each cycle but the instruction output from memory lagged behind. This misalignment caused the testbench to check the wrong instruction against the current PC, leading to repeated mismatches. The way instruction memory modeled it is the root of the problem, since the memory output was registered, the instruction available to output corresponded to the previous cycle’s PC rather than the current one. To fix the issue we reviewed the timing of the fetch stage carefully so that the PC and instruction output were visible to the test bench in the same cycle.