Project 3: RTL-to-GDSII Flow for a 16x24-Bit Multiplier

Salwan Aldhahab

218597963

EECS4612

Prof. Amir Sodagar

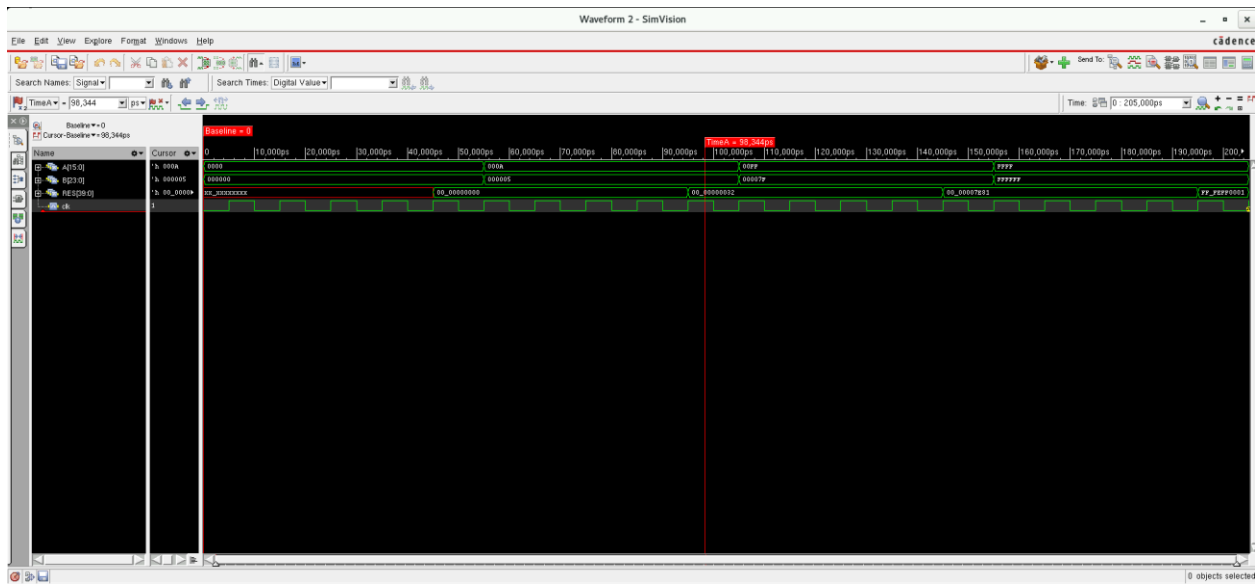**Lassonde School of Engineering**

- Simulation

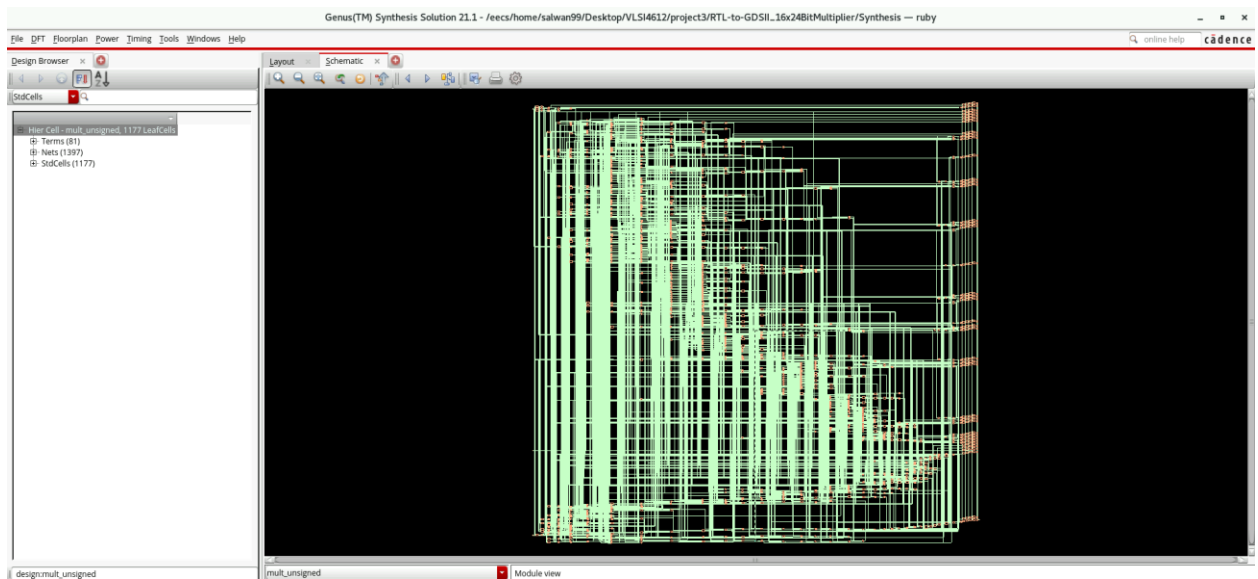*Figure 1: Waveform of mult_signed module*

- Logic Synthesis

Figure 2: Gate level netlist of mult_signed.sv

```
==========================================================
  Generated by:            Genus(TM) Synthesis Solution 21.17-s066_1
  Generated on:            Nov 06 2025   03:07:32 pm
  Module:                  mult_unsigned
  Operating conditions:    PVT_0P9V_125C (balanced_tree)
  Wireload mode:           enclosed
  Area mode:               timing library
==========================================================


    Gate      Instances    Area       Library
--------------------------------------------------
ADDFX1            177      908.010     slow_vdd1v0
AND2X1              1        1.368     slow_vdd1v0
AO22XL              1        2.736     slow_vdd1v0
AOI211XL            1        2.052     slow_vdd1v0
AOI21X1             7       11.970     slow_vdd1v0
AOI22X1           166      340.632     slow_vdd1v0
AOI22XL             3        6.156     slow_vdd1v0
AOI2BB1X1           1        2.052     slow_vdd1v0
AOI2BB1XL           2        4.104     slow_vdd1v0
AOI31X1             1        2.052     slow_vdd1v0
DFFHQX1            49      268.128     slow_vdd1v0
DFFQX2              7       45.486     slow_vdd1v0
DFFQXL            103      563.616     slow_vdd1v0
DFFRX1             40      273.600     slow_vdd1v0
DFFX1               1        7.182     slow_vdd1v0
INVX1              89       60.876     slow_vdd1v0
INVX20             40      259.920     slow_vdd1v0
INVXL               6        4.104     slow_vdd1v0
MX2X1               1        2.394     slow_vdd1v0
MX2XL               7       16.758     slow_vdd1v0
MXI2XL              2        4.788     slow_vdd1v0
NAND2BX1           21       28.728     slow_vdd1v0
NAND2X1            48       49.248     slow_vdd1v0
NAND2XL            13       13.338     slow_vdd1v0
NAND3BXL            1        1.710     slow_vdd1v0
NOR2BX1            31       42.408     slow_vdd1v0
NOR2X1             39       40.014     slow_vdd1v0
NOR2XL              4        4.104     slow_vdd1v0
NOR4X1              3        5.130     slow_vdd1v0
OA21X1              5       10.260     slow_vdd1v0
OAI211X1            3        5.130     slow_vdd1v0
OAI21X1            50       85.500     slow_vdd1v0
OAI221X1            1        2.394     slow_vdd1v0
OAI22X1           177      363.204     slow_vdd1v0
OAI22XL            18       36.936     slow_vdd1v0
OAI2BB1X1           1        1.710     slow_vdd1v0
OR2X1               7        9.576     slow_vdd1v0
OR2XL               1        1.368     slow_vdd1v0
XNOR2X1            49      117.306     slow_vdd1v0
--------------------------------------------------
total            1177     3606.048


    Type       Instances    Area     Area %
--------------------------------------------------
sequential          200   1158.012     32.1
inverter            135    324.900      9.0
logic               842   2123.136     58.9
physical_cells        0      0.000      0.0
--------------------------------------------------
total              1177   3606.048    100.0
```

Figure 3: Area utilization report of mult_signed.sv

```
1 Instance: /mult_unsigned
2 Power Unit: W
3 PDB Frames: /stim#0/frame#0
4  ------------------------------------------------------------------------
5    Category         Leakage     Internal    Switching         Total    Row%
6  ------------------------------------------------------------------------
7      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
8    register     2.08384e-08  7.69642e-05  5.83476e-06  8.28198e-05    6.18%
9       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
10      logic     6.65846e-08  6.30892e-05  1.18948e-03  1.25264e-03   93.46%
11       bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
12      clock     0.00000e+00  0.00000e+00  4.85998e-06  4.85998e-06    0.36%
13        pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
14         pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
15  ------------------------------------------------------------------------
16   Subtotal     8.74231e-08  1.40053e-04  1.20018e-03  1.34032e-03  100.00%
17 Percentage           0.01%       10.45%       89.54%      100.00% 100.00%
18  ------------------------------------------------------------------------
```

Figure 4: Power report of mult_signed.sv

```
================================================================
  Generated by:          Genus(TM) Synthesis Solution 21.17-s066_1
  Generated on:          Nov 06 2025  03:07:32 pm
  Module:                mult_unsigned
  Operating conditions:  PVT_0P9V_125C (balanced_tree)
  Wireload mode:         enclosed
  Area mode:             timing library
================================================================


Path 1: MET (1262 ps) Setup Check with Pin M_reg_0__39_/CK->D
      Startpoint: (R) rA_reg_1_/CK
           Clock: (R) clk
        Endpoint: (R) M_reg_0__39_/D
           Clock: (R) clk

                     Capture         Launch
         Clock Edge:+   6667              0
         Src Latency:+     0              0
         Net Latency:+     0 (I)          0 (I)
            Arrival:=   6667              0

             Setup:-    117
      Required Time:=   6550
       Launch Clock:-      0
          Data Path:-   5288
             Slack:=    1262

#------------------------------------------------------------------------------
#     Timing Point        Flags   Arc    Edge  Cell     Fanout Load Trans Delay Arrival Instance
#                                                               (fF)  (ps)  (ps)  (ps)  Location
#------------------------------------------------------------------------------
  rA_reg_1_/CK               -      -      R    (arrival)   200   -     0     0     0    (-,-)
  rA_reg_1_/Q               -    CK->Q    F    DFFX1        27   9.8  255   329   329    (-,-)
  mul_26_12_g10615__5526/Y  -    B->Y     R    XNOR2X1      25  10.0  224   362   691    (-,-)
  mul_26_12_g10512/Y        -    A->Y     F    INVX1         3   0.9   72   156   847    (-,-)
  mul_26_12_g10503__1881/Y  -    B->Y     F    OR2X1        24   9.5  251   243  1090    (-,-)
  mul_26_12_g10426__6260/Y  -    A1->Y    R    OAI22X1       1   0.8  121   201  1291    (-,-)
  mul_26_12_g10171__6783/S  -    B->S     R    ADDFX1        1   0.8   46   312  1603    (-,-)
  mul_26_12_g10108__5477/CO -    B->CO    R    ADDFX1        1   0.6   39   203  1806    (-,-)
  mul_26_12_g10087__6783/CO -    CI->CO   R    ADDFX1        1   0.6   39   186  1992    (-,-)
  mul_26_12_g10055__6260/CO -    CI->CO   R    ADDFX1        1   0.6   39   186  2178    (-,-)
  mul_26_12_g10030__5526/CO -    CI->CO   R    ADDFX1        3   1.2   51   193  2371    (-,-)
  mul_26_12_g10021__1666/Y  -    B->Y     F    NAND2BX1      2   0.5   66    73  2444    (-,-)
  mul_26_12_g9983__5115/Y   -    A1N->Y   F    AOI2BB1XL     1   0.2   41   104  2548    (-,-)
  mul_26_12_g9952__5115/Y   -    A1->Y    F    OA21X1        1   0.4   29   127  2675    (-,-)
  mul_26_12_g9940__5526/Y   -    A1->Y    R    OAI21X1       3   1.2   93    80  2754    (-,-)
  mul_26_12_g9937__6260/Y   -    B->Y     F    NAND2BX1      2   0.5   70    96  2850    (-,-)
  mul_26_12_g9932__7410/Y   -    A1N->Y   F    AOI2BB1XL     1   0.2   41   106  2956    (-,-)
  mul_26_12_g9927__9315/Y   -    A1->Y    F    OA21X1        1   0.4   29   127  3084    (-,-)
  mul_26_12_g9925__4733/Y   -    A1->Y    R    OAI21X1       5   1.8  119    95  3179    (-,-)
  mul_26_12_g9918__7098/Y   -    A2->Y    F    AOI31X1       2   0.7  145   178  3356    (-,-)
  mul_26_12_g9917__8246/Y   -    B->Y     R    NOR2X1        3   1.0   83   124  3480    (-,-)
  mul_26_12_g9912__3680/Y   -    C->Y     F    NAND3BXL      1   0.3  126   130  3609    (-,-)
  mul_26_12_g9907__6260/Y   -    C0->Y    R    OAI211X1      2   0.8   92    95  3704    (-,-)
  mul_26_12_g9900__2346/Y   -    B->Y     F    NAND2BX1      3   0.8   85   104  3808    (-,-)
  mul_26_12_g9897__9315/Y   -    D->Y     R    NOR4X1        1   0.2  103    99  3908    (-,-)
  mul_26_12_g9893__5115/Y   -    C0->Y    F    AOI211XL      3   1.2  194   113  4021    (-,-)
  mul_26_12_g9889__8246/Y   -    A1->Y    R    OAI221X1      1   0.6  118   174  4196    (-,-)
  mul_26_12_g9882__5526/CO  -    CI->CO   R    ADDFX1        1   0.6   39   226  4422    (-,-)
  mul_26_12_g9881__8428/CO  -    CI->CO   R    ADDFX1        1   0.6   39   186  4608    (-,-)
  mul_26_12_g9880__4319/CO  -    CI->CO   R    ADDFX1        1   0.6   39   186  4794    (-,-)
  mul_26_12_g9879__6260/CO  -    CI->CO   R    ADDFX1        1   0.6   39   186  4980    (-,-)
  mul_26_12_g9878__5107/CO  -    CI->CO   R    ADDFX1        1   0.4   35   184  5164    (-,-)
  mul_26_12_g9877__2398/Y   -    B->Y     R    XNOR2X1       1   0.3   24   124  5288    (-,-)
  M_reg_0__39_/D           <<<    -       R    DFFHQX1       1   -     -     0  5288    (-,-)
#------------------------------------------------------------------------------
```

Figure 5: Timing report of mult_signed.sv
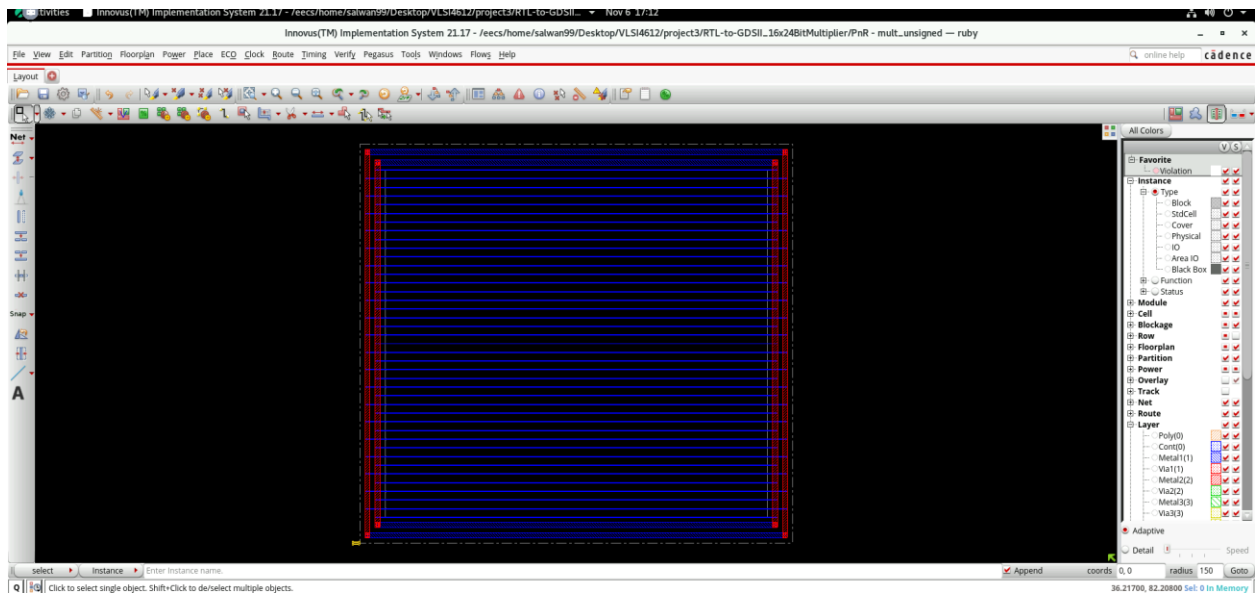
- Place and Route (PnR)

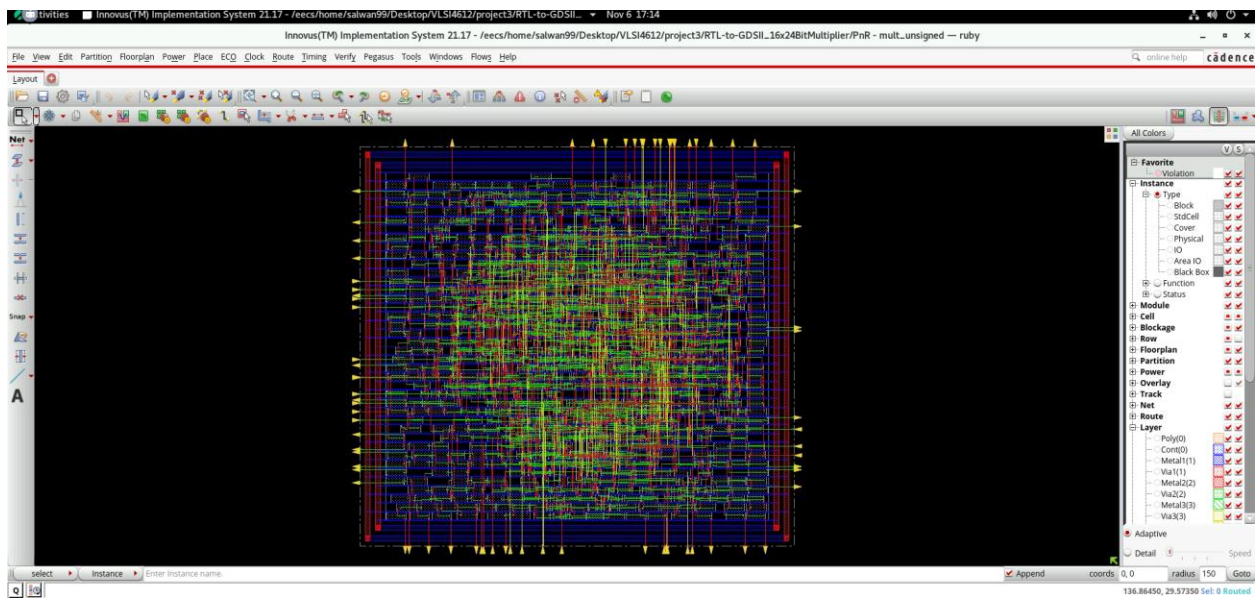
Figure 6: Power and ground routing of mult_signed.sv
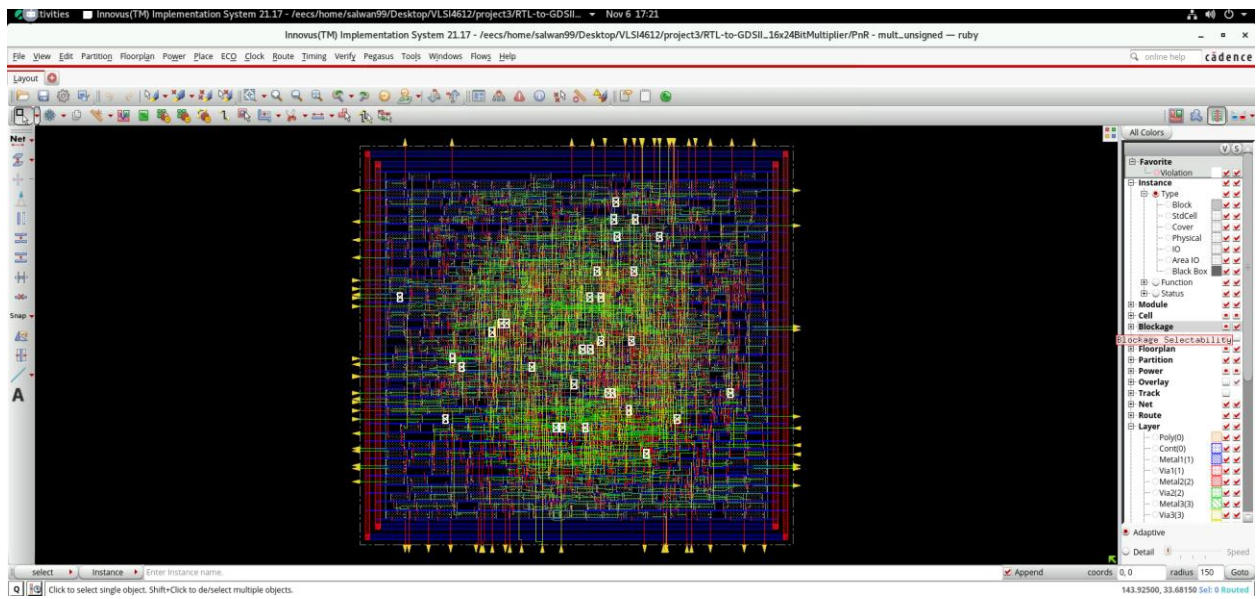

Figure 7: Placement of mult_signed.sv

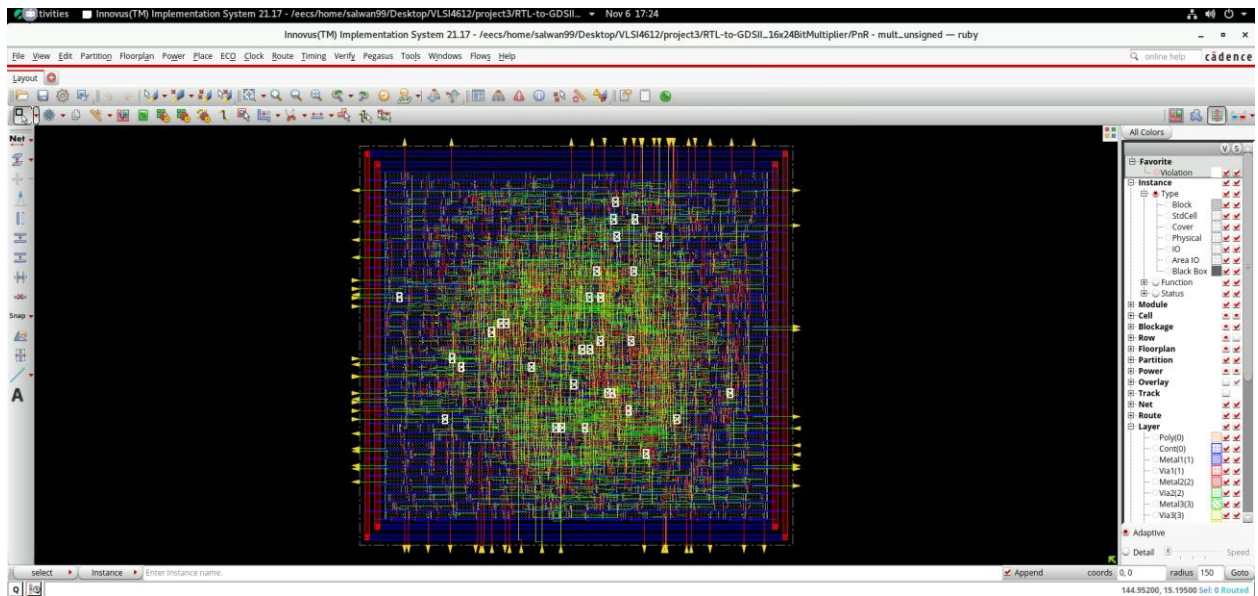*Figure 8: Final routing with NanoRoute for mult_signed.sv*

Figure 9: Filler placement for mult_signed.sv

Figure 10: DRC verification results for mult_signed.sv

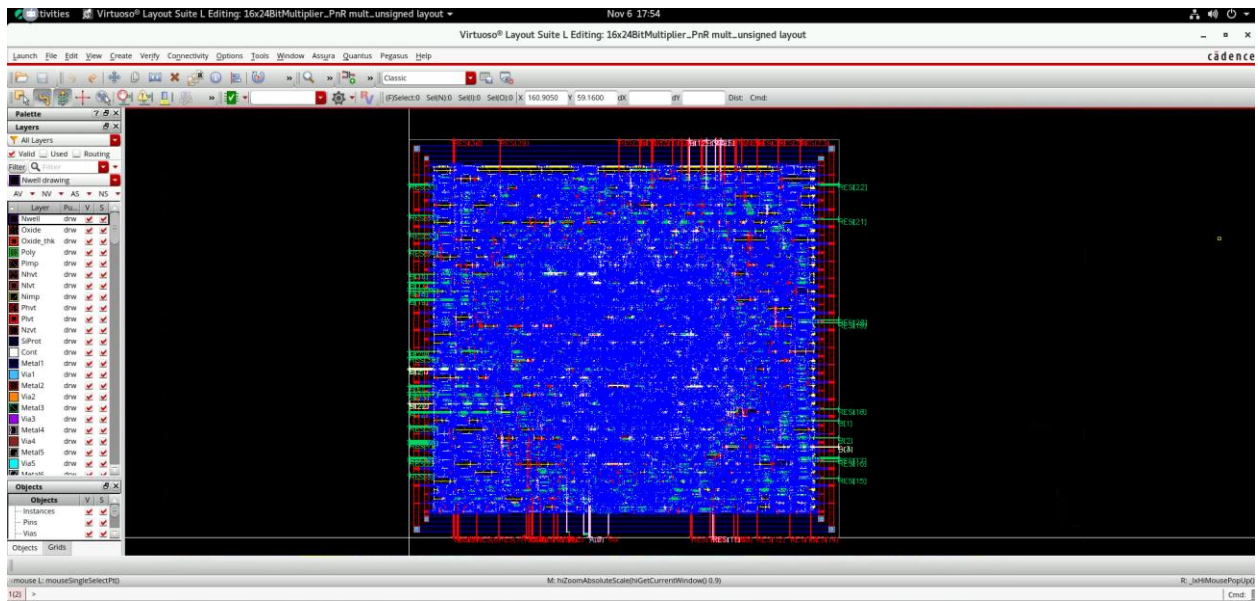
Figure 11: Connectivity verification results for mult_signed.sv

Figure 12: Layout of mult_signed.sv in Virtuoso