

Project 3: RTL-to-GDSII Flow for a 16x24-Bit Multiplier

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- Simulation

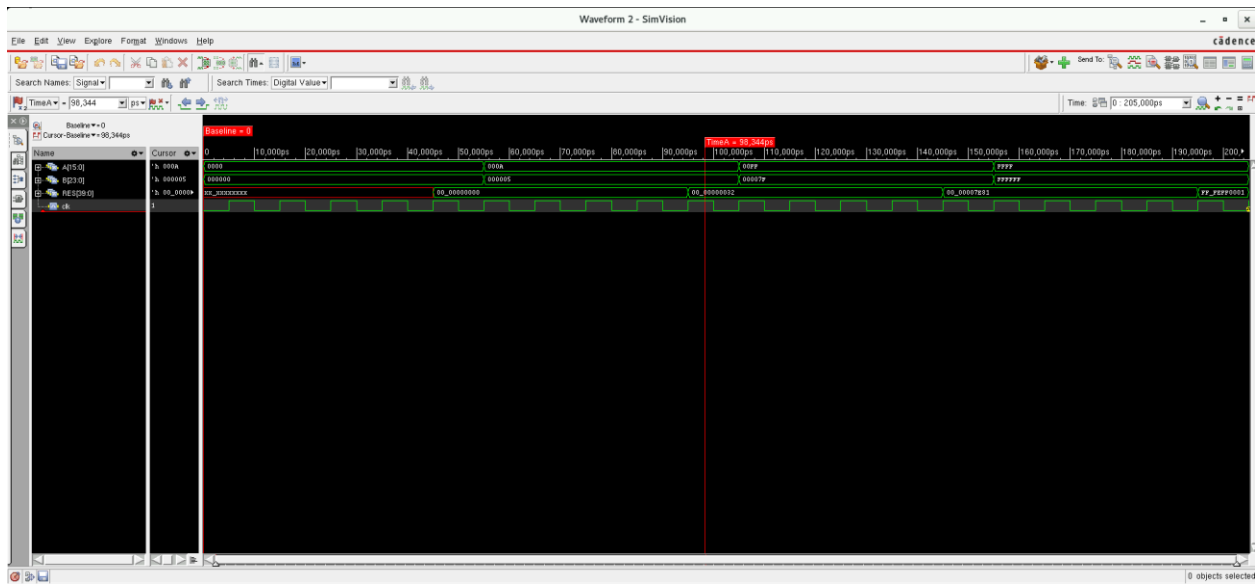


Figure 1: Waveform of mult_signed module

- Logic Synthesis

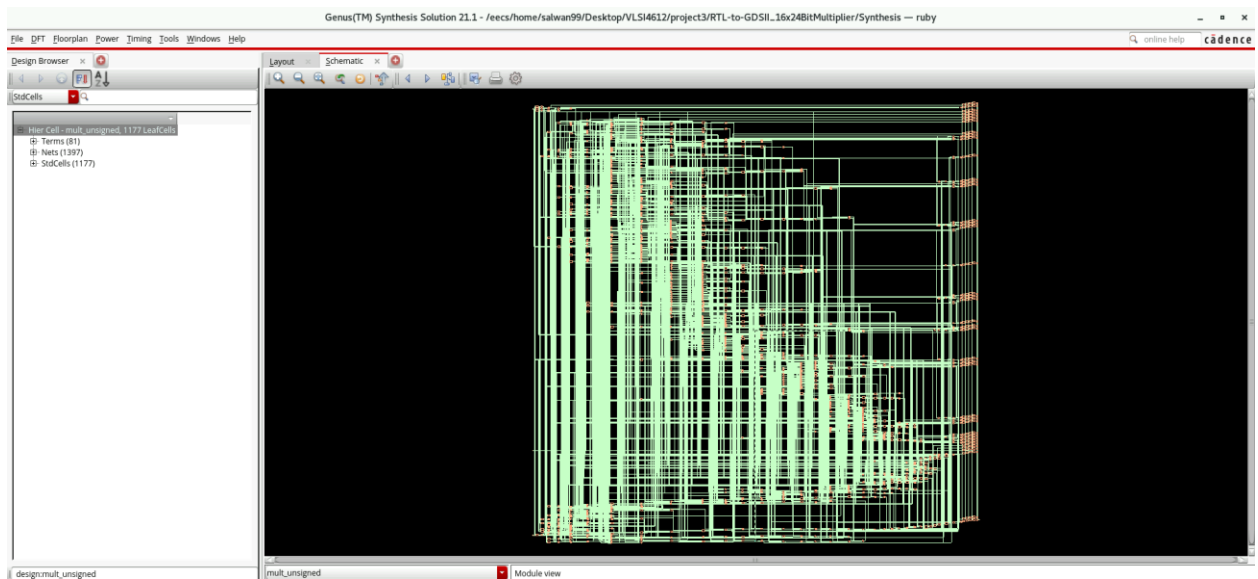


Figure 2: Gate level netlist of mult_signed.sv

```

1 =====
2 Generated by:      Genus(TM) Synthesis Solution 21.17-s066_1
3 Generated on:      Nov 06 2025 03:07:32 pm
4 Module:            mult_unsigned
5 Operating conditions: PVT_0P9V_125C (balanced_tree)
6 Wireload mode:     enclosed
7 Area mode:         timing library
8 =====
9
10
11 Gate      Instances    Area      Library
12 -----
13 ADDFX1      177    908.010    slow_vdd1v0
14 AND2X1       1     1.368    slow_vdd1v0
15 AO22XL       1     2.736    slow_vdd1v0
16 AOI211XL     1     2.052    slow_vdd1v0
17 AOI21X1      7    11.970    slow_vdd1v0
18 AOI22X1     166   340.632    slow_vdd1v0
19 AOI22XL       3     6.156    slow_vdd1v0
20 AOI2BB1X1    1     2.052    slow_vdd1v0
21 AOI2BB1XL    2     4.104    slow_vdd1v0
22 AOI31X1      1     2.052    slow_vdd1v0
23 DFFHQX1     49   268.128    slow_vdd1v0
24 DFFQX2       7    45.486    slow_vdd1v0
25 DFFQXL      103   563.616    slow_vdd1v0
26 DFFRX1       40   273.600    slow_vdd1v0
27 DFFX1        1     7.182    slow_vdd1v0
28 INVX1        89    60.876    slow_vdd1v0
29 INVX20       40   259.920    slow_vdd1v0
30 INVXL        6     4.104    slow_vdd1v0
31 MX2X1        1     2.394    slow_vdd1v0
32 MX2XL        7    16.758    slow_vdd1v0
33 MXI2XL       2     4.788    slow_vdd1v0
34 NAND2BX1     21    28.728    slow_vdd1v0
35 NAND2X1     48    49.248    slow_vdd1v0
36 NAND2XL     13    13.338    slow_vdd1v0
37 NAND3BX1     1     1.710    slow_vdd1v0
38 NOR2BX1     31    42.408    slow_vdd1v0
39 NOR2X1      39    40.014    slow_vdd1v0
40 NOR2XL       4     4.104    slow_vdd1v0
41 NOR4X1       3     5.130    slow_vdd1v0
42 OA21X1       5    10.260    slow_vdd1v0
43 OAI211X1     3     5.130    slow_vdd1v0
44 OAI21X1     50    85.500    slow_vdd1v0
45 OAI221X1     1     2.394    slow_vdd1v0
46 OAI22X1     177   363.204    slow_vdd1v0
47 OAI22XL     18    36.936    slow_vdd1v0
48 OAI2BB1X1    1     1.710    slow_vdd1v0
49 OR2X1        7     9.576    slow_vdd1v0
50 OR2XL        1     1.368    slow_vdd1v0
51 XNOR2X1     49   117.306    slow_vdd1v0
52 -----
53 total        1177  3606.048
54
55
56
57 Type      Instances    Area    Area %
58 -----
59 sequential    200  1158.012    32.1
60 inverter      135   324.900     9.0
61 logic        842  2123.136    58.9
62 physical_cells    0     0.000     0.0
63 -----
64 total        1177  3606.048   100.0
65

```

Figure 3: Area utilization report of mult_signed.sv

1	Instance: /mult_unsigned					
2	Power Unit: W					
3	PDB Frames: /stim#0/frame#0					
4	-----					
5	Category	Leakage	Internal	Switching	Total	Row%
6	-----					
7	memory	0.000000e+00	0.000000e+00	0.000000e+00	0.000000e+00	0.00%
8	register	2.08384e-08	7.69642e-05	5.83476e-06	8.28198e-05	6.18%
9	latch	0.000000e+00	0.000000e+00	0.000000e+00	0.000000e+00	0.00%
10	logic	6.65846e-08	6.30892e-05	1.18948e-03	1.25264e-03	93.46%
11	bbox	0.000000e+00	0.000000e+00	0.000000e+00	0.000000e+00	0.00%
12	clock	0.000000e+00	0.000000e+00	4.85998e-06	4.85998e-06	0.36%
13	pad	0.000000e+00	0.000000e+00	0.000000e+00	0.000000e+00	0.00%
14	pm	0.000000e+00	0.000000e+00	0.000000e+00	0.000000e+00	0.00%
15	-----					
16	Subtotal	8.74231e-08	1.40053e-04	1.20018e-03	1.34032e-03	100.00%
17	Percentage	0.01%	10.45%	89.54%	100.00%	100.00%
18	-----					

Figure 4: Power report of mult_signed.sv

```

1 =====
2 Generated by:      Genus(TM) Synthesis Solution 21.17-s066_1
3 Generated on:     Nov 06 2025 03:07:32 pm
4 Module:          mult_unsigned
5 Operating conditions: PVT_0P9V_125C (balanced_tree)
6 Wireload mode:   enclosed
7 Area mode:       timing library
8 =====
9
10
11 Path 1: MET (1262 ps) Setup Check with Pin M_reg_0__39_/CK->D
12   Startpoint: (R) rA_reg_1_/CK
13   Clock: (R) clk
14   Endpoint: (R) M_reg_0__39_/D
15   Clock: (R) clk
16
17           Capture      Launch
18   Clock Edge:+ 6667      0
19   Src Latency:+ 0        0
20   Net Latency:+ 0 (I)    0 (I)
21   Arrival:= 6667        0
22
23   Setup:- 117
24   Required Time:= 6550
25   Launch Clock:- 0
26   Data Path:- 5288
27   Slack:= 1262
28
29 #-----
30 # Timing Point      Flags      Arc      Edge      Cell      Fanout Load Trans Delay Arrival Instance
31 #                  (fF)      (ps)      (ps)      (ps)      (ps)      (ps)      Location
32 #-----
33 rA_reg_1_/CK      -      -      R      (arrival) 200      -      0      0      0      (-,-)
34 rA_reg_1_/0      -      CK->Q F      DFFX1    27 9.8 255 329 329      (-,-)
35 mul_26_12_g10615_5526/Y -      B->Y R      XNOR2X1 25 10.0 224 362 691      (-,-)
36 mul_26_12_g10512/Y -      A->Y F      INVX1    3 0.9 72 156 847      (-,-)
37 mul_26_12_g10503_1881/Y -      B->Y F      OR2X1    24 9.5 251 243 1090      (-,-)
38 mul_26_12_g10426_6260/Y -      A1->Y R      OAI22X1 1 0.8 121 201 1291      (-,-)
39 mul_26_12_g10171_6783/S -      B->S R      ADDFX1   1 0.8 46 312 1603      (-,-)
40 mul_26_12_g10108_5477/C0 -      B->C0 R      ADDFX1   1 0.6 39 203 1806      (-,-)
41 mul_26_12_g10087_6783/C0 -      CI->C0 R      ADDFX1   1 0.6 39 186 1992      (-,-)
42 mul_26_12_g10055_6260/C0 -      CI->C0 R      ADDFX1   1 0.6 39 186 2178      (-,-)
43 mul_26_12_g10030_5526/C0 -      CI->C0 R      ADDFX1   3 1.2 51 193 2371      (-,-)
44 mul_26_12_g10021_1666/Y -      B->Y F      NAND2BX1 2 0.5 66 73 2444      (-,-)
45 mul_26_12_g9983_5115/Y -      A1N->Y F      AOI2BB1XL 1 0.2 41 104 2548      (-,-)
46 mul_26_12_g9952_5115/Y -      A1->Y F      OA21X1   1 0.4 29 127 2675      (-,-)
47 mul_26_12_g9940_5526/Y -      A1->Y R      OAI21X1   3 1.2 93 80 2754      (-,-)
48 mul_26_12_g9937_6260/Y -      B->Y F      NAND2BX1 2 0.5 70 96 2850      (-,-)
49 mul_26_12_g9932_7410/Y -      A1N->Y F      AOI2BB1XL 1 0.2 41 106 2956      (-,-)
50 mul_26_12_g9927_9315/Y -      A1->Y F      OA21X1   1 0.4 29 127 3084      (-,-)
51 mul_26_12_g9925_4733/Y -      A1->Y R      OAI21X1   5 1.8 119 95 3179      (-,-)
52 mul_26_12_g9918_7098/Y -      A2->Y F      AOI31X1   2 0.7 145 178 3356      (-,-)
53 mul_26_12_g9917_8246/Y -      B->Y R      NOR2X1    3 1.0 83 124 3480      (-,-)
54 mul_26_12_g9912_3680/Y -      C->Y F      NAND3BXL 1 0.3 126 130 3609      (-,-)
55 mul_26_12_g9907_6260/Y -      C0->Y R      OAI211X1 2 0.8 92 95 3704      (-,-)
56 mul_26_12_g9900_2346/Y -      B->Y F      NAND2BX1 3 0.8 85 104 3808      (-,-)
57 mul_26_12_g9897_9315/Y -      D->Y R      NOR4X1    1 0.2 103 99 3908      (-,-)
58 mul_26_12_g9893_5115/Y -      C0->Y F      AOI211XL 3 1.2 194 113 4021      (-,-)
59 mul_26_12_g9889_8246/Y -      A1->Y R      OAI221X1 1 0.6 118 174 4196      (-,-)
60 mul_26_12_g9882_5526/C0 -      CI->C0 R      ADDFX1   1 0.6 39 226 4422      (-,-)
61 mul_26_12_g9881_8428/C0 -      CI->C0 R      ADDFX1   1 0.6 39 186 4608      (-,-)
62 mul_26_12_g9880_4319/C0 -      CI->C0 R      ADDFX1   1 0.6 39 186 4794      (-,-)
63 mul_26_12_g9879_6260/C0 -      CI->C0 R      ADDFX1   1 0.6 39 186 4980      (-,-)
64 mul_26_12_g9878_5107/C0 -      CI->C0 R      ADDFX1   1 0.4 35 184 5164      (-,-)
65 mul_26_12_g9877_2398/Y -      B->Y R      XNOR2X1 1 0.3 24 124 5288      (-,-)
66 M_reg_0__39_/D      <<<      -      R      DFFHQX1 1      -      -      0 5288      (-,-)
67 #-----

```

Figure 5: Timing report of mult_signed.sv

- Place and Route (PnR)

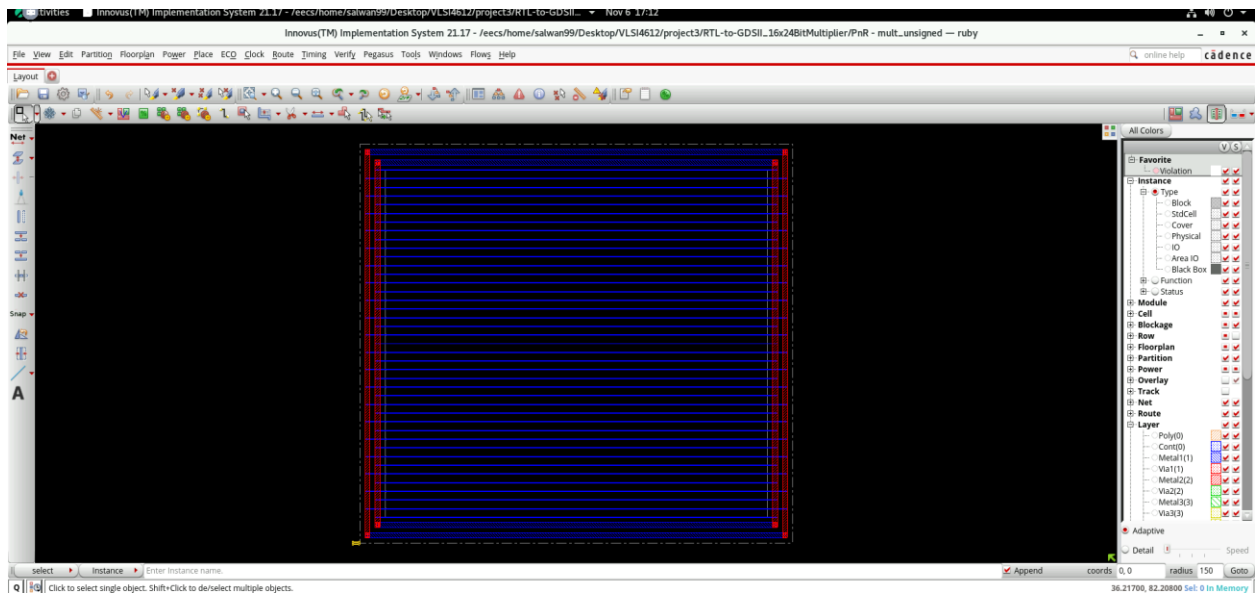


Figure 6: Power and ground routing of `mult_signed.sv`

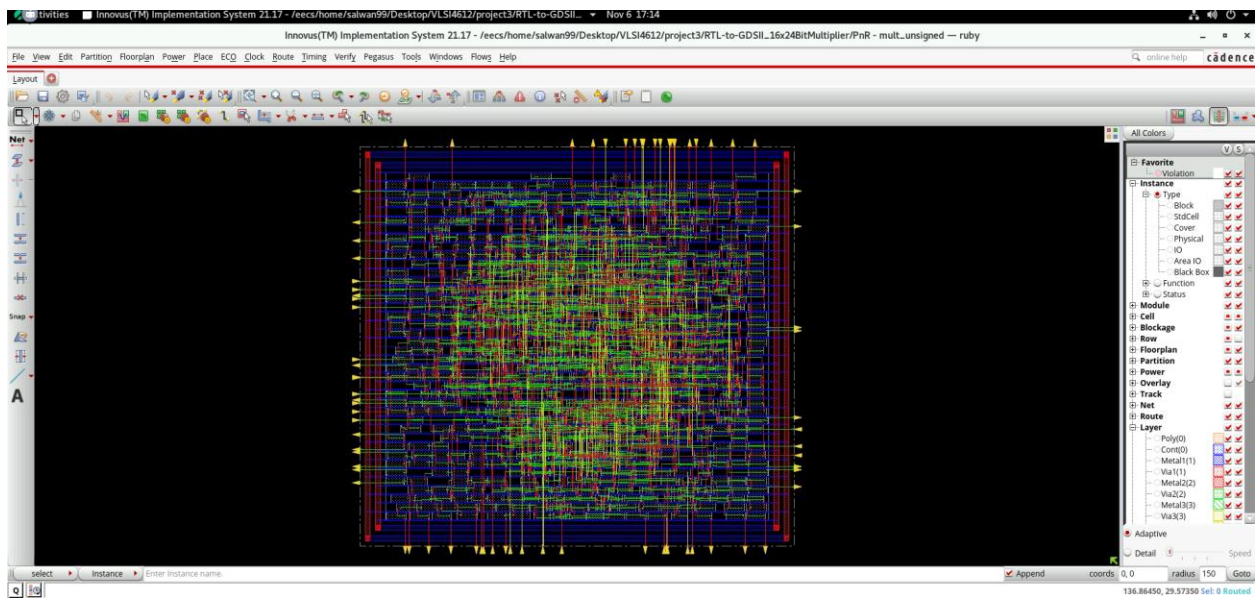


Figure 7: Placement of `mult_signed.sv`

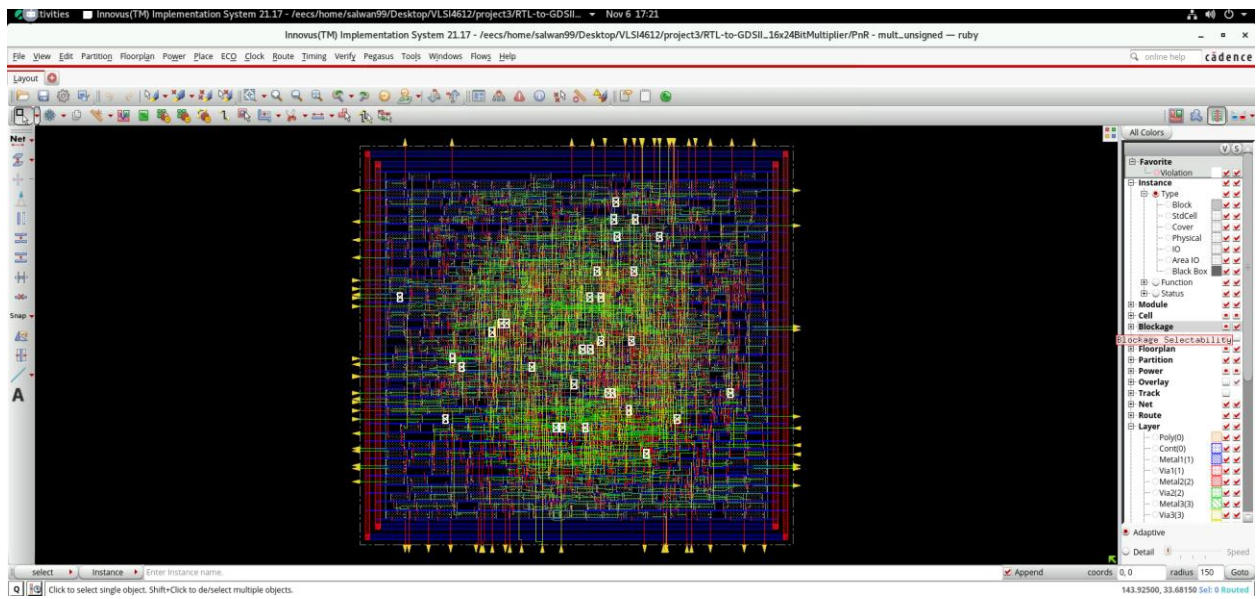


Figure 8: Final routing with NanoRoute for mult_signed.sv

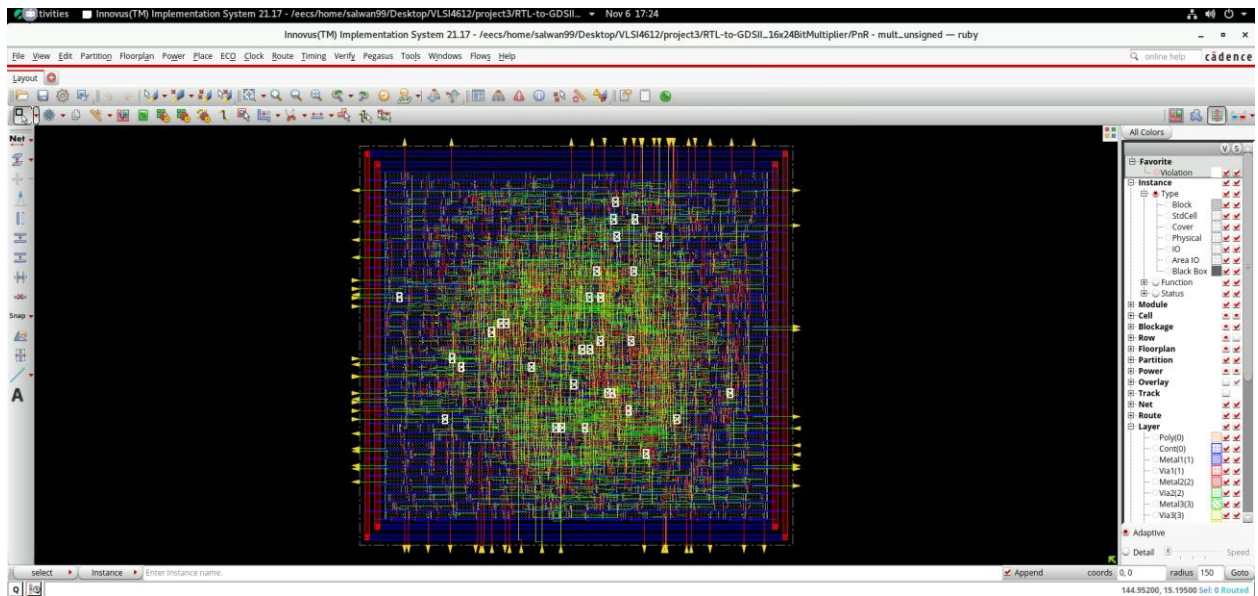


Figure 9: Filler placement for mult_signed.sv

```
ruby:/eecs/home/salwan99/Desktop/VLSI4612/project3/RTL-to-GDSII_16x24BitMultiplier/PnR _ □ x
File Edit View Search Terminal Help
*INFO: Added 218 filler insts (cell FILL4 / prefix FILLER).
*INFO: Added 361 filler insts (cell FILL2 / prefix FILLER).
*INFO: Added 430 filler insts (cell FILL1 / prefix FILLER).
*INFO: Total 1171 filler insts added - prefix FILLER (CPU: 0:00:00.1).
For 1171 new insts, innovus 5> #-check_ndr_spacing auto # enums={
true false auto}, default=auto, user setting
#-check_same_via_cell true # bool, default=false, user setting
#-exclude_pg_net true # bool, default=false, user setting
#-report mult_unsigned.drc.rpt # string, default="", user setting
*** Starting Verify DRC (MEM: 2737.5) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.0000 0.0000 85.4000 78.6600} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.2 ELAPSED TIME: 0.00 MEM: 256.1M) ***
innovus 5> 
```

Figure 10: DRC verification results for mult_signed.sv

```
ruby:/eecs/home/salwan99/Desktop/VLSI4612/project3/RTL-to-GDSII_16x24BitMultiplier/PnR _ □ x
File Edit View Search Terminal Help

innovus 5> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Thu Nov 6 17:28:27 2025

Design Name: mult_unsigned
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (85.4000, 78.6600)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
Found no problems or warnings.
End Summary

End Time: Thu Nov 6 17:28:27 2025
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)

innovus 5> 
```

Figure 11: Connectivity verification results for mult_signed.sv

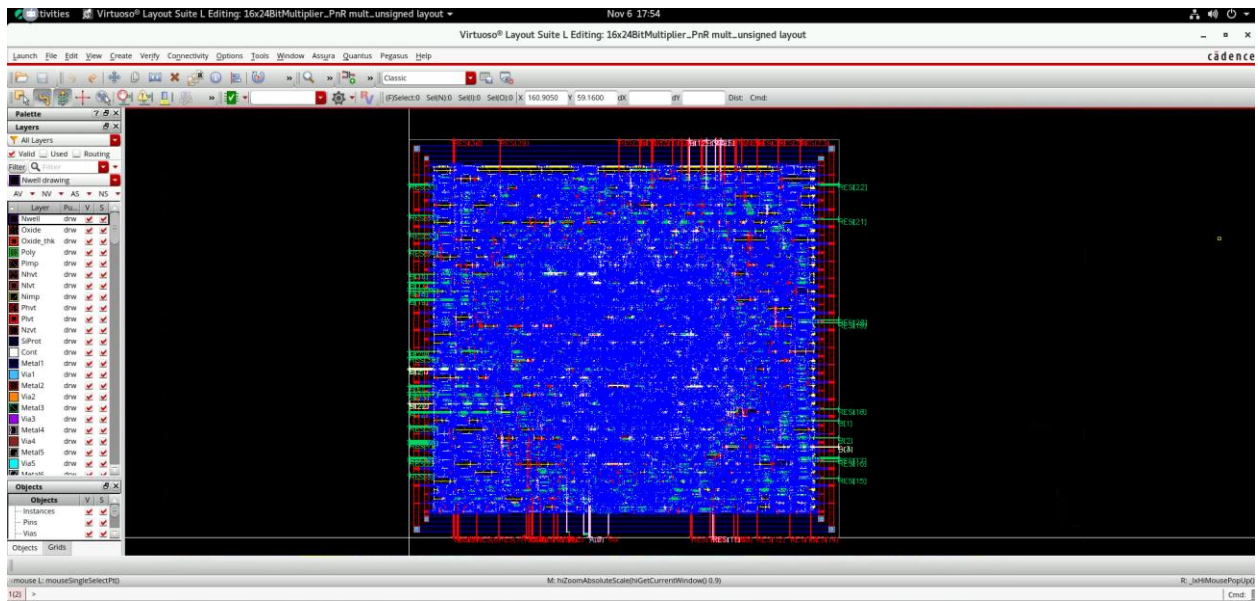


Figure 12: Layout of mult_signed.sv in Virtuoso